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*Original*

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This version is available <http://hdl.handle.net/11390/1064835> since 2021-03-23T11:44:48Z

*Publisher:*

*Published*

DOI:10.1109/JEDS.2015.2390643

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# Two-dimensional Heterojunction Interlayer Tunneling Field Effect Transistors (Thin-TFETs)

Mingda (Oscar) Li, David Esseni, Joseph J. Nahas, Debdeep Jena, and Huili Grace Xing

**Abstract**—The 2D crystals embrace the unique features of the atomically thin bodies, the dangling bond free interfaces, and step-like 2D density of states. To exploit these features for the design of a steep slope transistor, we propose a Two-dimensional Heterojunction Interlayer Tunneling Field Effect Transistor (Thin-TFET) to reach a steep subthreshold swing (SS) of  $\sim 14$  mV/dec and a high on-current of  $\sim 300 \mu\text{A}/\mu\text{m}$ . The SS is ultimately limited by the density of states broadening at the band edges and the on-current density is estimated on the basis of the interlayer charge transfer time measured in recent experimental studies. A potential material system of monolayer  $\text{WSe}_2/\text{SnSe}_2$  heterojunction can be used to build both  $n$ -type and  $p$ -type Thin-TFETs. Non-ideality effects such as the non-uniform van der Waals gap thickness between two 2D semiconductors and the finite access resistances are also studied. Finally, the benchmarking for digital applications shows the Thin-TFETs may outperform MOSFETs in term of both performance and energy consumption at low supply voltages..

**Index Terms**—Tunnel FET, 2D crystals, transport model, benchmarking

## I. INTRODUCTION

**T**UNNEL Field Effect Transistors (FETs) are perceived as promising transistors that may enable scaling supply voltage  $V_{DD}$  down to 0.5 V or lower by reducing the subthreshold swing (SS) below 60 mV/dec at room temperature. To date, numerous Tunnel FETs have been demonstrated, among which the heterostructures with near broken gap band alignment are favored in order to achieve sub-60 mV/dec SS and high on currents simultaneously [1]. Tunnel FETs also require a very strong gate control over the channel region to obtain sub-60 mV/dec SS values, which in turn demands ultra-thin body or narrow nanowire structures, where size induced quantization enlarges the bandgap and impedes the realization of near broken gap alignment [2]–[4]. 2D layered crystals, such as monolayers of transition metal dichalcogenides (TMD)  $\text{MX}_2$  (e.g.  $\text{M} = \text{Mo}, \text{W}, \text{Sn}$ ;  $\text{X} = \text{S}, \text{Se}, \text{Te}$ ), offer a native thickness of about 0.6 nm with a variety of bandgaps and band-alignments [4], [5], as well as a sharp turn on of density of states at the band edges and the absence of interface dangling bonds, which are highly desired for achieving a sharp SS [6]. Recent experimental results show that the monolayer 2D crystals heterojunction band alignment can be directly controlled by applying perpendicular electric field [7] and the charge transfer

in monolayer 2D crystals heterojunction is reasonably fast [8]. In such a contest, a Two-dimensional Heterojunction Interlayer Tunneling FET (Thin-TFET) based on a vertical arrangement of 2D layered materials is proposed. In particular, we discuss both  $n$ -type and  $p$ -type Thin-TFETs employing the potential material system of  $2\text{H-WSe}_2$  and  $1\text{T-SnSe}_2$ . Our simulations suggest that the Thin-TFETs can achieve very competitive SS values and a high on-current. Along with the low gate-to-drain and gate-to-source capacitance, the Thin-TFETs enable fast switching and low energy consumption. The effect of non-uniform van der Waals gap thickness and the external source and drain total access resistance are also discussed. Experimental efforts have been carried out to demonstrate the Thin-TFET based on  $\text{WSe}_2/\text{SnSe}_2$  heterojunction. Some experimental insights are shared at the end of the paper.

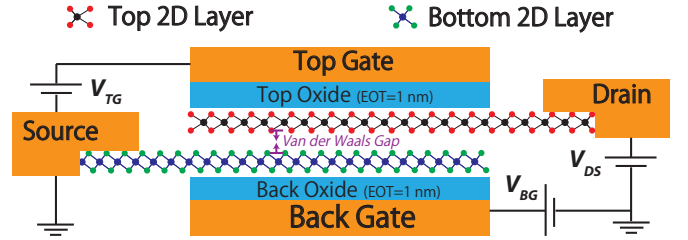


Fig. 1. The schematic device layer structure of the Thin-TFET

## II. DEVICE STRUCTURE AND MODELING APPROACH

The Thin-TFET device structure is shown in Fig.1, where the bottom and top 2D semiconductors act as the source and the drain respectively. The van der Waals gap separates top and bottom 2D semiconductors and the thickness of the van der Waals gap is defined as the distance from the center of the chalcogenide atom in the top 2D layer to the center of the nearest chalcogenide atom in the bottom 2D layer (see Fig.1). The device working principle can be explained as follows: take the  $p$ -type Thin-TFET as the example, when  $E_{CB}$  is higher than  $E_{VT}$  (see Fig.2), tunneling from the bottom layer is inhibited and the device is nominally off. When a negative top gate voltage pulls  $E_{VT}$  above  $E_{CB}$  (see Fig.3[a]), a tunneling window is opened and a current can flow.

To calculate the band alignment between  $E_{CB}$  and  $E_{VT}$  along the direction perpendicular to the 2D semiconductors we first use Gauss's law and write [9]

$$\begin{aligned} C_{TOX}V_{TOX} - C_{vdW}V_{vdW} &= e(p_T - n_T + N_T) \\ C_{BOX}V_{BOX} + C_{vdW}V_{vdW} &= e(p_B - n_B + N_B) \end{aligned} \quad (1)$$

where  $e$  is the magnitude of electron charge,  $C_{T(B)OX}$  is the capacitance per unit area of top (back) oxide, and  $C_{vdW}$

This work was supported in part by the Center for Low Energy Systems Technology (LEAST), and by a Fulbright Fellowship for D. Esseni.

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is the capacitance per unit area of the van der Waals gap.  $V_{T(B)OX}$  and  $V_{vdW}$  are the corresponding potential drops.  $n(p)_{T(B)}$  is the electron (hole) densities in the top (bottom) 2D semiconductor layer, and  $N_T$ ,  $N_B$  are the net chemical doping concentrations (donor minus acceptor) in the layers, which are set to zero in this work. The potential drops can be written in terms of the top gate  $V_{TG}$ , back gate  $V_{BG}$ , and drain-source voltage  $V_{DS}$  (which sets the split of the quasi-Fermi levels in the top and bottom semiconductor layers), and of the material properties as

$$\begin{aligned} eV_{vdW} &= eV_{DS} - e\phi_{p,B} - e\phi_{n,T} + E_{GB} + \chi_{2D,B} - \chi_{2D,T} \\ eV_{TOX} &= eV_{TG} + e\phi_{n,T} - eV_{DS} + \chi_{2D,T} - e\Phi_{M,T} \\ eV_{BOX} &= eV_{BG} - e\phi_{p,B} + E_{GB} + \chi_{2D,B} + e\Phi_{M,B} \end{aligned} \quad (2)$$

where we define  $e\phi_{n,T(B)} = E_{CT(B)} - E_{FT(B)}$  and  $e\phi_{p,T(B)} = E_{FT(B)} - E_{VT(B)}$ ,  $E_{GB}$  is the energy gap in the bottom 2D semiconductor and  $V_{T(B)OX}$  is the potential drop across the top (back) gate dielectric,  $V_{vdW}$  is the potential drop across the van der Waals gap,  $\chi_{2D,T(B)}$  is the electron affinity of the top (bottom) 2D semiconductor, and  $\Phi_{M,T(B)}$  is the metal workfunction of the top (back) gate (see Fig.2).

By using effective mass approximation and assuming that the majority carriers of the two 2D semiconductors are at thermodynamic equilibrium with their Fermi levels [10], the carrier densities can be written as

$$n(p) = \frac{g_v m_c^* (m_v^*) k_B T}{\pi \hbar^2} \ln \left[ \exp \left( -\frac{q\phi_{n,T}(\phi_{p,B})}{k_B T} \right) + 1 \right] \quad (3)$$

where  $g_v$  is the valley degeneracy and  $m_c^* (m_v^*)$  is the conduction (valence) band effective mass.

By inserting Eqs.2 and 3 in Eq.1 we obtain two equations determining  $\phi_{n,T}$ ,  $\phi_{p,T}$  and thus the band alignment.

We calculate the tunneling current by using the transfer-Hamiltonian method [11], as recently revisited for resonant tunneling graphene transistors [12], [13]. We here summarize the basic equations; a more thorough discussion can be found in [9]. The tunneling current density,  $J_T$ , is expressed as [9]:

$$J_T = \frac{g_v e |M_{B0}|^2 A}{4\pi^3 \hbar} e^{-2\kappa T_{vdW}} \times \int_{\mathbf{k}_T} \int_{\mathbf{k}_B} d\mathbf{k}_T d\mathbf{k}_B S_F(q) S_E(E_B - E_T) (f_B - f_T) \quad (4)$$

where  $\kappa$  is the decay constant of the wave-function in the van der Waals gap [12], [13],  $T_{vdW}$  is the thickness of the van der Waals gap,  $\mathbf{k}_{T(B)}$ ,  $E_{T(B)}$  and  $f_{T(B)}$  are the wave-vector, the energy and Fermi occupation function in the top (bottom) 2D semiconductor and  $M_{B0}$  is the tunneling matrix element [9], which is a property of the material system and is further discussed in Sec.III. Eq.4 assumes that in the tunneling process electrons interact with a random scattering potential, whose spectrum is taken as  $S_F(q) = \pi L_C^2 / (1 + \mathbf{q}^2 L_C^2 / 2)^{3/2}$ , where  $q = |\mathbf{k}_T - \mathbf{k}_B|$  and  $L_C$  is the correlation length. The scattering relaxes the momentum conservation, i.e. allowing tunneling for  $\mathbf{k}_B \neq \mathbf{k}_T$ . A similar  $S_F(q)$  has been used to analyze the resonance linewidth in graphene tunneling transistors [13]. The  $S_F(q)$  may be representative of different

scattering mechanisms that are discussed in [9], [13]. Finally  $S_E(E) = \exp(-E^2/\sigma^2)/(\sqrt{\pi}\sigma^2)$  describes the energy broadening in the 2D semiconductors, where  $\sigma$  is the energy broadening parameter [9]. The contact resistance is included by self-consistently calculating the tunnel current density and the voltage drop on the total access resistance in our model.

### III. SIMULATION RESULTS AND DISCUSSIONS

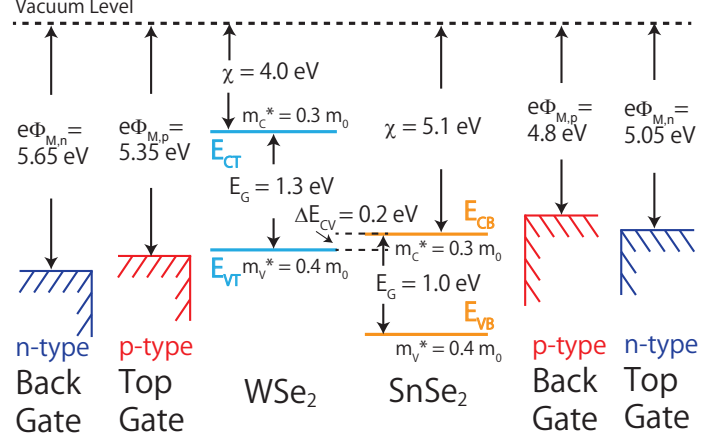


Fig. 2. For the *n*-type Thin-TFET, SnSe<sub>2</sub> is the top 2D layer and WSe<sub>2</sub> is the bottom 2D layer, along with the top and back gate labeled as *n*-type in blue. While for the *p*-type Thin-TFET, WSe<sub>2</sub> is the top 2D layer and SnSe<sub>2</sub> is the bottom 2D layer, along with the top and back gate labeled as *p*-type in red; Band gaps, electron affinities, effective masses are shown for WSe<sub>2</sub> and SnSe<sub>2</sub>. The *n*-type and *p*-type metal work functions are tuned to give symmetric threshold voltages for the *n*-type and *p*-type Thin-TFETs.

#### A. Material system and *n*-type & *p*-type Thin-TFETs

$C_{G,avg}$  Out of various 2D semiconductors studied by density function theory calculations [5] and various experimental efforts, we chose the trigonal prismatic coordination monolayer WSe<sub>2</sub> and the octahedral coordination (CdI<sub>2</sub> crystal structure) monolayer SnSe<sub>2</sub> (see Fig.2). Since there is no experimental band structure reported for *monolayer* WSe<sub>2</sub> and SnSe<sub>2</sub>, the potential band alignment of the WSe<sub>2</sub>/SnSe<sub>2</sub> system used in this work are based on the existing experimental results of *multilayer* WSe<sub>2</sub> and SnSe<sub>2</sub> [14]–[16] and their approximated effective masses are based on the DFT results [5] (see Fig.2). WSe<sub>2</sub>/SnSe<sub>2</sub> heterojunction can potentially form a staggered or near broken band alignment, which reduces the voltage drop in the van der Waals gap in the on-state condition [1] and also help to suppress the thermionic leakage current. Also, SnSe<sub>2</sub> tends to be an *n*-type semiconductor [17], [18] and WSe<sub>2</sub> can be electrostatically doped to be *p*-type [19]. Therefore, if one considers the *p*-type Thin-TFET as an example, by applying negative top gate voltage  $V_{TG}$ , the top layer WSe<sub>2</sub> can be electrostatically tuned to be more *p*-type (see Fig.3[e]) in order to open the tunnel window, while the bottom layer SnSe<sub>2</sub> stays *n*-type (see Fig.3[e]) and screens most electrical field from the top layer so as to maximize the potential drop across the WSe<sub>2</sub>/SnSe<sub>2</sub> heterojunction induced by the gate voltage. It is also worth noting that there may be dipoles on the WSe<sub>2</sub>/SnSe<sub>2</sub> interface [15], so that the electron

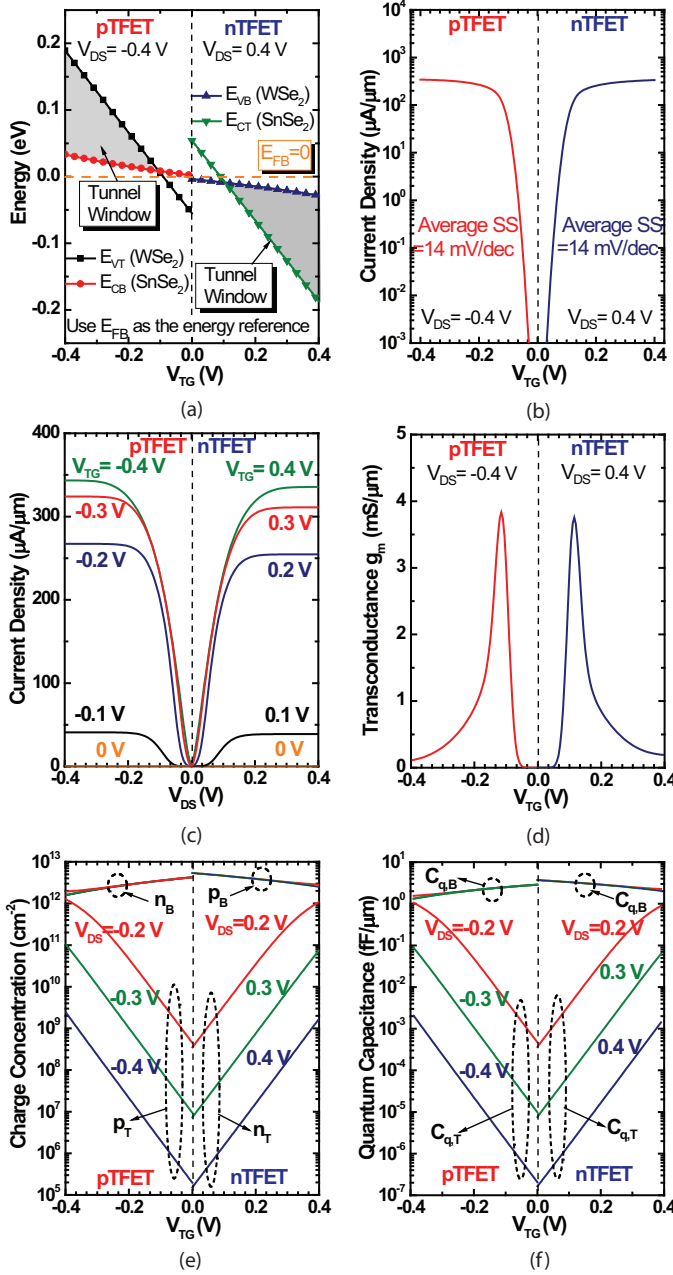


Fig. 3. For both the  $n$ -type Thin-TFET and the  $p$ -type Thin-TFET (a) the band alignment versus  $V_{TG}$ ; (b) Current density versus  $V_{TG}$ , the average SS is calculated from  $10^{-3}$   $\mu A/\mu m$  to  $10$   $\mu A/\mu m$ ; (c) the current density versus  $V_{DS}$  at various  $V_{TG}$ ; (d) the transconductance versus  $V_{TG}$ ; (e) the carrier concentration in the top and bottom 2D layers versus  $V_{TG}$  at various  $V_{DS}$ ; (f) the quantum capacitances of the top and bottom 2D layers versus  $V_{TG}$  at various  $V_{DS}$ ;

affinity rule requires some modifications, although interfacial dipoles are not considered in this work.

Following the complex band method [20], we assume the effective barrier height  $E_B$  of the van der Waals gap is 1 eV and the electron mass in the van der Waals gap is the free electron mass  $m_0$ , thus the decay constant is  $\kappa = \sqrt{2m_0E_B}/\hbar = 5.12 \text{ nm}^{-1}$ . In the model, the scattering correlation length  $L_C$  in  $S_F(q)$  was set to  $L_C=10 \text{ nm}$ , which is also consistent with the value employed in [13]; the energy broadening  $\sigma$  is set to 10 meV.  $M_{B0}$  in Eq.4 is directly related to the interlayer

charge transfer time  $\tau_{b(t)}$  across the van der Waals gap of the carrier in bottom (top) 2D semiconductor, which can be written as [21]

$$\tau_{b(t)}^{-1} = \frac{2\pi}{\hbar} \rho_{t(b)} |M_{B0}|^2 e^{-2\kappa T_{vdW}} S_F(q) \quad (5)$$

where  $\rho_{t(b)}(E)$  is the density of states (DOS) of the top (bottom) 2D semiconductors and  $\rho_{t(b)} = g_v m_{t(b)}^* / \pi \hbar^2$ . For the  $n$ -type Thin-TFET,  $\rho_{t(b)}(E)$  is the DOS of the conduction (valence) band of the top (bottom) 2D semiconductor, while for the  $p$ -type Thin-TFET,  $\rho_{t(b)}(E)$  is the DOS of the valence (conduction) band of the top (bottom) 2D semiconductor. As can be seen from Eq.5 and then the  $S_F(q)$  expression (given after Eq.4), due the scattering in our model the  $\tau$  increases with  $q$ , which is the magnitude of the wave-vector difference across the van der Waals gap defined as  $q = |\mathbf{k}_T - \mathbf{k}_B|$ . Recent experimental results [8] observed the charge transfer time across van der Waals gap between MoS<sub>2</sub> and WS<sub>2</sub> is  $\sim 25$  fs, which, according to Eq.5, gives us the  $M_{B0} \sim 0.02 \text{ eV}$  when  $q=0$ . We recognize that the charge transfer time might be different for different 2D heterojunctions, but it might be reasonable to assume they have similar values. Thus, we choose  $M_{B0}=0.02 \text{ eV}$  in all following simulations.

In all current calculations the top and back oxide have an effective oxide thickness (EOT) of 1 nm, which give the top and back oxide capacitance  $C_{TG}$  and  $C_{BG}$  of  $0.518 \text{ fF}/\mu m$ . The thickness of the van der Waals gap is set to be  $3.5 \text{ \AA}$ , unless specified otherwise. We assume the relative dielectric constant of the van der Waals gap is 1.0 therefore the van der Waals gap capacitance  $C_{vdW}$  is  $0.38 \text{ fF}/\mu m$ . Throughout this work, the gate length is 15 nm as well as the back gate and the source are grounded. The external total access resistances are neglected unless specified.

The material systems for both the  $p$ -type and the  $n$ -type Thin-TFET are shown in Fig.2. The  $n$ -type and  $p$ -type metal work functions are tuned to give symmetric threshold voltages for the  $n$ -type and the  $p$ -type Thin-TFET. Figure 3[a] shows the band alignment versus  $V_{TG}$  curves. As can be seen, the  $V_{TG}$  can effectively control the vertical band alignment in the device and, for the  $p$ -type Thin-TFET in particular, induce the crossing between  $E_{VT}$  and  $E_{CB}$ , with  $E_{CB}$  being relatively insensitive to  $V_{TG}$  compared to  $E_{VT}$ . Figure.3[b] shows  $I_D$  versus  $V_{TG}$  with very compelling average SS (from  $10^{-3}$   $\mu A/\mu m$  to  $10$   $\mu A/\mu m$ ) of  $\sim 14 \text{ mV/dec}$ . The  $I_D$  versus  $V_{DS}$  family curves are shown in Fig.3[c].  $I_D$  is well saturated with  $V_{DS}$  when  $V_{DS} > \sim 0.2 \text{ V}$ . The superlinear onset is also observed and the so called  $V_{DS}$  threshold voltage increases at lower  $V_{TG}$  [22]. The peak transconductances around  $4 \text{ mS}/\mu m$  are shown in Fig.3[d], which are much larger than reported peak transconductances of sub-22 nm MOSFET [23], [24]. In Fig.3[e], the top gate changes the carrier concentrations of the top 2D semiconductor much faster than of the bottom 2D semiconductor under different  $V_{DS}$ . The ability to efficiently change the hole (electron) concentration in the top 2D semiconductor while keeping the high electron (hole) concentration in the bottom 2D semiconductor is vital to achieve good electrostatics control of the  $p$ -type ( $n$ -type) Thin-TFET. The values of the so called quantum capacitances are written as



Eq.6:

$$C_{Q,T(B)} = - \left[ \frac{e \partial p_{T(B)}}{\partial \phi_{p,T(B)}} + \frac{e \partial n_{T(B)}}{\partial \phi_{n,T(B)}} \right] \quad (6)$$

Figure.3[f] illustrates the quantum capacitances under different bias conditions.

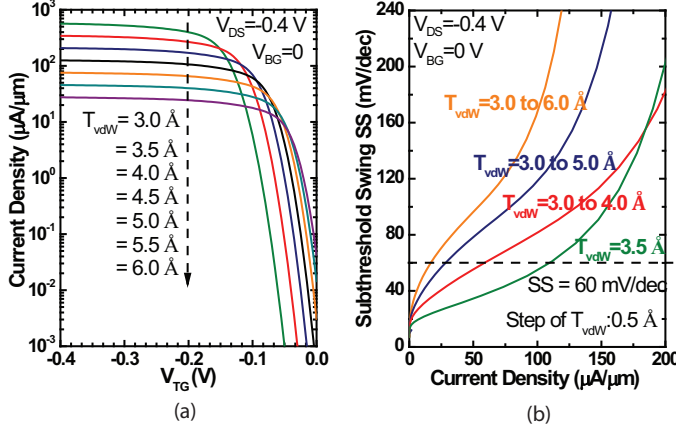


Fig. 4. For the *p*-type Thin-TFET: (a) tunnel current density versus  $V_{TG}$  for different van der Waals gap thicknesses  $T_{vdW}$ ; (b) SS versus  $V_{TG}$  when having equally distributed van der Waals gap thickness  $T_{vdW}$  variations;

### B. Effects of non-uniform van der Waals gap thicknesses and Total Access Resistances

Due to the nature of van der Waals bonds, the van der Waals gap thickness is subject the interlayer rotational alignment of the two 2D semiconductors [25]. Meanwhile, the tunneling probability is very sensitive to the tunneling distance, namely the van der Waals gap thickness, to investigate the effects of non uniform van der Waals thickness. In the instance of *p*-type Thin-TFET, we vary the van der Waals gap thickness  $T_{vdW}$  from 3.0 Å to 6.0 Å with the step of 0.5 Å. As shown in Fig.4[a], the on-current density decreases and the threshold voltage moves towards 0 when increasing the  $T_{vdW}$ . The impact on the sub-threshold swing is instead modest when  $T_{vdW}$  is still considered uniform. However, in Fig.4[b], we consider various  $T_{vdW}$  values across a heterojunction by assuming the  $T_{vdW}$  are equally distributed. For example, for a 2D heterojunction with equally distributed  $T_{vdW}$  from 3.0 Å to 5.0 Å with the step of 0.5 Å, we take the  $I_D$ - $V_{TG}$  curves for each  $T_{vdW}$  (i.e. 3.0 Å, 3.5 Å, 4.0 Å, 4.5 Å, and 5.0 Å) shown in Fig.4[a] and average them to obtain the overall  $I_D$ - $V_{TG}$  curve. The SS of the average  $I_D$ - $V_{TG}$  curves versus  $I_D$  are plotted in Fig.5[b] with difference  $T_{vdW}$  variation ranges. For the van der Waals gap with equally distributed deviations, the SS increases with increasing variation ranges. For a randomly distributed van der Waals gap thicknesses, this trend is also expected.

Since the total access resistances have become critical to ultra-scaled transistors and how to optimize the total access resistance on 2D crystals still remains as an open question, we included the total access resistance  $R_C$  in I-V curves calculations. Figure 5[a] shows the  $I_D$  versus  $V_{TG}$  at  $V_{DS} = -0.4$  V with different  $R_C$ : the current density remains almost the same with  $R_C$  up to 320  $\Omega\mu\text{m}$  and decreases with increasing

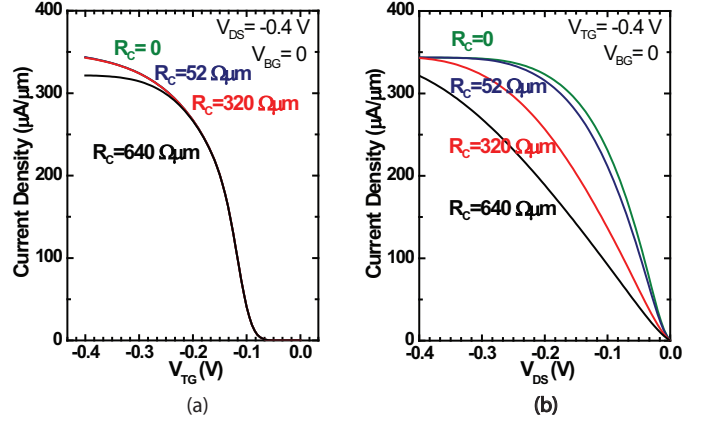


Fig. 5. For the *p*-type Thin-TFET: (a) the tunnel current density versus  $V_{DS}$  at different  $V_{TG}$  with total access resistances  $R_C$ ; (b) the tunnel current density versus  $V_{DS}$  with different total access resistances  $R_C$ .

$R_C$ . From Fig.5[b], the saturation region of  $I_D$  versus  $V_{DS}$  curve can be affected when  $|V_{DS}| < 0.4$  V if  $R_C > \sim 52 \Omega\mu\text{m}$ . In an ideal 2D conductor, the total access resistance is around  $\sim 52 \Omega\mu\text{m}$  for a degenerate 2D semiconductor and is around  $\sim 325 \Omega\mu\text{m}$  for a nondegenerate 2D semiconductor [26]. Thus the access region of 2D semiconductors must be degenerately doped to approach the optimal  $R_C$ .

### C. Capacitance Evaluation

The gate-to-drain and gate-to-source capacitances (i.e.  $C_{GD}$ ,  $C_{GS}$ ) can be readily calculated from the capacitance network shown in Fig.6. The quantum capacitances  $C_{Q,T(B)}$  of the top

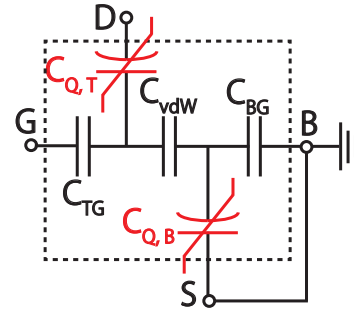


Fig. 6. Capacitance network model of the Thin-TFET

(bottom) 2D semiconductor are defined in Eq.6 and indicated as the red non-linear capacitances in Fig.6. First we define  $C_S$  and  $C_T$  as:

$$\begin{aligned} 1/C_S &\equiv 1/C_{vdW} + 1/(C_{Q,B} + C_{BG}) \\ C_T &\equiv C_{TG} + C_{Q,T} + C_S \end{aligned} \quad (7)$$

Then,  $C_{GD}$  and  $C_{GS}$  can be written as Eqs.8:

$$\begin{aligned} C_{GS} &= \frac{C_{TG} C_S}{C_T} \\ C_{GD} &= \frac{C_{TG} C_{Q,T}}{C_T} \end{aligned} \quad (8)$$

For the *p*-type Thin-TFET, the source is the bottom 2D semiconductor  $\text{SnSe}_2$  while the drain is the top 2D semiconductor layer  $\text{WSe}_2$  (see Fig.2). The capacitances calculated for the *p*-type Thin-TFET are shown in Fig.7. From Fig.7[a],  $C_{GD}$  is

only significant when the  $p$ -type Thin-TFET is in the linear region of the  $I_D$ - $V_{DS}$  curve, where the drain is coupled with the top gate to change the tunnel current. While  $|V_{DS}|$  further increases, the Thin-TFET enters the saturation region, where the  $C_{GD}$  becomes close to zero. On the other hand,  $C_{GS}$  remains significantly larger than  $C_{GD}$  in the saturation region, indicating the top gate and the source stay closely coupled as desired. But  $C_{GS}$  becomes smaller when entering linear region. From Fig.7[b],  $C_{GD}$  dramatically increases while  $C_{GS}$  decreases when  $|V_{TG}| > |V_{DS}|$ . In practice, when designing the Thin-TFET as a switch in a digital circuit, we should avoid to bias  $|V_{TG}| > |V_{DS}|$  because of losing gate control. The capacitance model will be useful for implementing the Thin-TFET into circuit simulations.

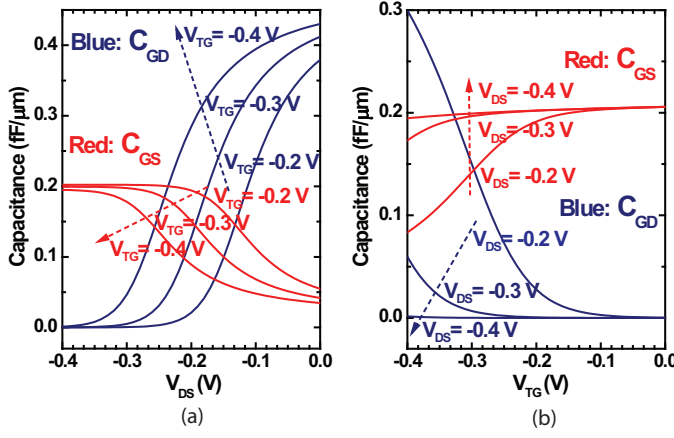


Fig. 7. For the  $p$ -type Thin-TFET, (a)  $C_{GD}$  and  $C_{GS}$  versus  $V_{DS}$  at  $V_{TG} = -0.2, -0.3, -0.4$  V; (b)  $C_{GD}$  and  $C_{GS}$  versus  $V_{TG}$  at  $V_{DS} = -0.2, -0.3, -0.4$  V.

#### D. Benchmarking

The Semiconductor Research Corporation (SRC) Nano-electronic Research Initiative (NRI) has supported research on beyond CMOS devices as reported by Bernstein, et al. [27]. As part of the initiative, a comparison of the projected performance of new devices with the projected performance of CMOS of the same generation (benchmarking) was performed. The benchmarking of beyond CMOS devices in SRC has continued and been standardized by Nikonov and Young [28] [29]. The Thin-TFET research, since it is partially supported by SRC under STARnet, participates in benchmarking using the Nikonov and Young (N&Y) methodology.

The N&Y methodology uses basic device performance parameters such as operating voltage ( $V_{DD} = |V_{DS}|$ ), saturation current ( $I_{Dsat}$ ), and average gate capacitance ( $C_{G,avg}$ ), to project logic switching energy and switching delay. The change of the net charge under the gate ( $\Delta Q$ ) when  $V_{TG}$  switching from 0 to  $V_{DD}$  is the sum of the change of the net charge in the top 2D semiconductor and the bottom 2D semiconductor. The average gate capacitance ( $C_{G,avg}$ ) is defined as  $\Delta Q/V_{DD}$ . Here we take the  $p$ -type Thin-TFET as an example,  $I_{Dsat}$  and  $C_{G,avg}$  are provided in Tab.I for the supply voltages  $V_{DD}$  equal to 0.2, 0.3, and 0.4 V and total access resistances  $R_C$  equal to 52 and 320  $\Omega\mu\text{m}$ , projected values

for intrinsic switching energies and intrinsic switching delays are generated using the N&Y methodology and are plotted as shown in Fig. 8. The device parameters for High Performance (HP) CMOS and Low Power (LP) CMOS are taken from Ref. [29] and we use the same geometrical parameters for both the CMOS and Thin-TFET are shown in Tab.I. Also, we ignore the contact capacitance [29] in this benchmarking.

TABLE I  
BENCHMARKING PARAMETERS FOR THIN-TFETs WITH DIFFERENT  $V_{DD}$  AND  $R_C$ , DEVICE PARAMETERS FOR HP CMOS AND LP CMOS, AND GEOMETRICAL PARAMETERS FOR BOTH THE CMOS AND THE THIN-TFET

Parameters for Thin-TFETs with Different $V_{DD}$ and $R_C$						
$V_{DD}$ (V)	0.2		0.3		0.4	
$R_C$ ( $\Omega\mu\text{m}$ )	52	320	52	320	52	320
$I_{\text{Dsat}}$ ( $\mu\text{A}/\mu\text{m}$ )	263	233	325	317	349	348
$\Delta Q$ ( $\text{mC}/\text{m}^{-2}$ )	2.34	2.80	3.33	3.72	4.30	4.47
$C_{\text{G, avg}}$ (fF/ $\mu\text{m}$ )	0.175	0.210	0.167	0.186	0.161	0.168
Parameters for HP and LP CMOS [29]						
	$V_{\text{DD}}$ (V)		$I_{\text{Dsat}}$ ( $\mu\text{A}/\mu\text{m}$ )		$C_{\text{G}}$ (fF/ $\mu\text{m}$ )	
HP CMOS	0.73		1805		1.29	
LP CMOS	0.3		2		1.29	
Geometrical Parameters for Benchmarking						
Half-pitch (nm)	EOT (nm)		Gate Length (nm)		Gate Width (nm)	
15	1		15		60	

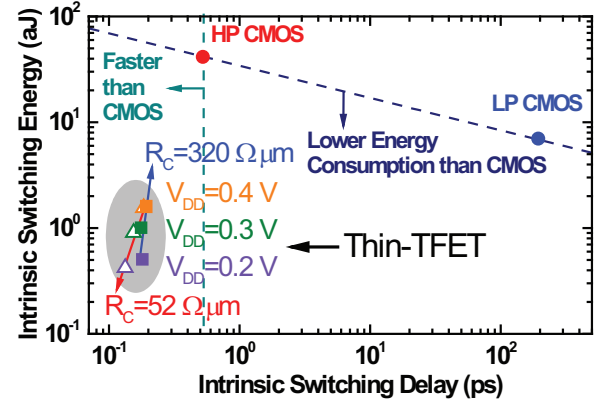


Fig. 8. The intrinsic switching energy and intrinsic switching delay for HP CMOS, LP CMOS, and Thin-TFET with  $V_{DD} = 0.2, 0.3, 0.4$  V and  $R_C = 52, 320 \Omega\mu\text{m}$ .

Note that the Thin-TFET is projected to be able to operate down to a supply voltage of 0.2 V which provides a distinct energy consumption and performance advantage.

#### E. Experimental Insights

While trying to demonstrate Thin-TFET experimentally, some key challenges have been identified. First, the current Dry Transfer is not suitable for integrated circuit processes [30]. The Molecular Beam Epitaxy 2D crystal heterojunctions have been grown but the grain size is in the order of several nanometers [31]. Second, efficient top gate control requires a high quality and interfacial state free dielectrics. Atomic layer deposition has been improved over years to achieve good quality gate dielectrics on 2D crystals [32]. Using 2D dielectrics such as hexagonal boron nitride as the gate dielectrics has also been pursued [33]. Third, low resistance ohmic contacts to 2D crystal are vital to device performance.

Various techniques such as external chemical doping [34], internal chemical doping [35], electrostatic doping such as ion doping [36] and phase-engineering from the semiconductor phase to the metallic phase of a 2D crystal [37], have been implemented to reduce the contact resistances. Last but not least, with the material properties remain unclear for most 2D crystals, a lot of initial effort will be put into understanding the materials characteristics.

#### IV. CONCLUSION

A new tunnel transistor, Thin-TFET, has been proposed and possible material systems are identified. Simulations based on the transfer Hamiltonian method suggest that the Thin-TFETs can achieve very good sub-threshold swing (SS) and high on-current, and are thus promising devices for ultra-low energy digital systems.

**Acknowledgments:** This work was supported by the Center for Low Energy Systems Technology (LEAST), one of six SRC STARnet Centers, sponsored by MARCO and DARPA, by the Air Force Office of Scientific Research (FA9550-12-1-0257), and by a Fulbright Fellowship for D. Esseni. The authors are also grateful for the helpful discussions with Profs. K. J. Cho, R. Feenstra, S. Datta and A. Seabaugh.

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