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Universal analytic model for tunnel FET circuit simulation

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Hao Lu[a], David Esseni[b], and Alan Seabaugh[a]

[a]Department of Electrical Engineering, University of Notre Dame, Notre Dame, IN 46556, United States. Email: {hlu1, seabaugh.1@nd.edu}.
[b]Dipartimento di Ingegneria Elettrica Gestionale e Meccanica, University of Udine, Udine 33100, Italy. Email: esseni@uniud.it.

Abstract

A simple analytic model based on the Kane-Sze formula is used to describe the current-voltage characteristics of tunnel field-effect transistors (TFETs). This model captures the unique features of the TFET including the decrease in subthreshold swing with drain current and the superlinear onset of the output characteristic. The model also captures the ambipolar current characteristic at negative gate-source bias and the negative differential resistance for negative drain-source biases. A simple empirical capacitance model is also included to enable circuit simulation. The model has fairly general validity and is not specific to a particular TFET geometry. Good agreement is shown with published atomistic simulations of an InAs double-gate TFET with gate perpendicular to the tunnel junction and with numerical simulations of a broken-gap AlGaSb/InAs TFET with gate in parallel with the tunnel junction.

I. INTRODUCTION

Tunnel field-effect transistors (TFETs) are candidates to compete with complementary metal-oxide-semiconductor (CMOS) FETs at low voltages because of their capability to achieve a subthreshold swing of less than 60 mV/decade at room temperature [1-3]. To build TFET circuits and make performance projections, it is of interest to develop simple, closed-form expressions for the drain current that contain the basic physics of the tunneling process and can be implemented in circuit simulators, e.g. SPICE.

Quite a few compact analytic models for the TFET have been developed [4-14]. References [4-9] employ a semianalytical solution of Poisson's equation in the channel region to model the channel charge [4] or to obtain the current-voltage characteristics [5-9]. These reports focus on particular TFET gate configurations, single-gate [5-7], double-gate [4, 8, 9, 11], or gate-all-around [10], or on specific aspects of the transport, such as the output characteristic at small drain biases [12, 13]. In most cases, the resulting expressions for the drain current are complex because the aim is to be predictive. The closest approach to our paper is that of Hong *et al.* [14] where the motivation is to develop an analytic model for use in circuit modeling. The resulting model gives good representation of the TFET characteristics, but is discontinuous and lacks an intuitive connection to the device physics.

Our intent has been to provide a simple and continuous equation set to describe the TFET current-voltage (*I-V*) characteristics [15]. In this paper our model is extended into all operating regions and a capacitance model is added. The resulting model produces the *I-V* characteristics of the TFET at the level of an elementary MOSFET SPICE model. This model is shown to capture the essential features of the TFET predicted by more comprehensive numerical simulators. The generalized formulation does not rely on a specific TFET embodiment, e.g. lateral, vertical, single-gate, double-gate, gate-all-around, inversion-mode, enhancement-mode, gate-field aligned to the tunnel junction, or gate-field perpendicular to the tunnel junction, hence the model is widely configurable. The purpose is to provide a

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model which has the core physics, like in the level 1 MOSFET SPICE model, which can be easily implemented and fitted to experimental data, and allow elementary circuit design.

The paper is organized as follows. Section II describes the development of the model in the normal operating region, including the physics of the subthreshold and above threshold regions and how these regions are connected. In this section, the model is applied to the representation of a homojunction InAs double gate *p-i-n* TFET and a broken-gap AlGaSb/InAs vertical TFET. Section III extends the model into other operating regions by incorporating the ambipolar current and negative differential resistance (NDR). Section IV introduces a simple empirical capacitance model that is shown to capture the behavior of capacitances in TFETs. Section V demonstrates the use of the model in HSPICE and provides a simple charge pump circuit example.

II.   MODEL DEVELOPMENT

Tunnel FETs utilize an MOS-gate to control the band-to-band tunneling across a degenerate *p-n* junction. The schematic cross-section and energy band diagrams of an *n*-channel TFET in OFF and ON states are shown in Fig. 1. The device is normally off. When zero bias is applied to the gate, the conduction band minimum of the channel is located above the valence band maximum of the source, so band-to-band tunneling is suppressed. A tunneling window, qV_{TW}, opens up as the conduction band of the channel is shifted below the valence band of the source. Electrons in the valence band with energy in this tunneling window tunnel into empty states in the channel and the transistor is ON.

The central expression in the TFET model is an experimentally well-established equation for band-to-band, Zener tunneling in *p-n* junctions [16, 17], the primary transport mechanism in tunnel transistors [1, 18]. The two-terminal Zener tunneling behavior is then generalized to three terminals by introducing physics-based expressions for the bias-dependent tunneling window and a dimensionless factor which accounts for the superlinear current onset in the output characteristic.
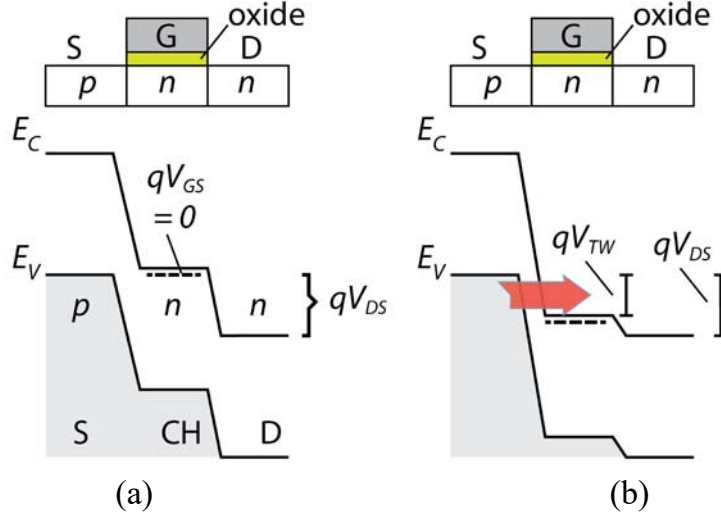
Fig. 1. Schematic cross-section and energy band diagram of an *n*-channel TFET when the device is biased in (a) OFF and (b) ON-state where the symbols are defined as follows: E_C, conduction band, E_V, valence band, V_{GS}, gate-source voltage, V_{DS}, drain-source voltage, and V_{TW}, tunneling window.

The signature feature of the TFET is the decrease in subthreshold swing with decreasing drain current, which is well established in both simulations [17, 19] and experiments [20, 21]. The model assumes that this behavior is caused by the exponential band tails that arise from imperfections and lattice disorder due to impurities, dopants, and phonons [22, 23] and extends into the band gap. This band tail, also known as the Urbach tail, represents a fundamental limit to the steepness that can be practically achieved [24] and thus becomes an adjustable element in the model. The subthreshold swing can be degraded by interface states and defects [25, 26]. While the physics of these effects are not included in the model, they presumably could be added as experiments reveal the generic aspects of these mechanisms.

A.   *Kane-Sze Model*

The TFET model is built on the expression for the current in a *p+n+* tunnel junction described by the Kane-Sze tunneling formula, which is evaluated by integrating the product of charge flux and the

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tunneling probability in the tunneling window, where the tunneling probability is calculated by applying the Wentzel-Kramers-Brillouin (WKB) approximation [27]

$$J_D = aV_R\xi\exp\left(-\frac{b}{\xi}\right),$$ (1)

where V_R is the reverse bias on the tunnel junction and physically accounts for the energy range, qV_R, over which the tunneling occurs, ξ is the maximum electric field in the reverse biased junction, and a and b are coefficients determined by the material properties of the junction, given by [1]:

$$a = \frac{q^3}{8\pi^2\hbar^2}\sqrt{\frac{2m_R^*}{E_G}}$$
$$b = \frac{4\sqrt{2m_R^*}E_G^{3/2}}{3q\hbar}$$ (2)

where $m_R^* = (1/m_E^* + 1/m_H^*)^{-1}$ is the reduced effective mass, which is the average of the electron, m_E^*, and hole, m_H^*, effective masses, E_G is the semiconductor band gap, and $\hbar$ is the reduced Planck's constant. The cross-sectional area of the junction, A, is the product of the channel thickness, t_{CH}, and the width of the channel, W.

The Kane-Sze expression, (1) is adapted to the following form,

$$J_D = afV_{TW}\xi\exp\left(-\frac{b}{\xi}\right),$$ (3)

where the term V_R is split into two bias-dependent terms, f and V_{TW}. The first term, f, is a dimensionless factor controlling both the current onset and saturation versus V_{DS}, which is based on the Fermi occupancy probability of filled states in the valence band and unfilled states in the conduction band. The second term, V_{TW}, is the tunneling window, in volts, related to the crossing and uncrossing of the energy bands. Because of the smearing of the band edge caused by the exponential decay of the band-tails in the band gap as $\sim e^{-|E-E_{C,V}|/E_0}$, with E_0 being the Urbach parameter [28], the tunneling window is assumed to

increase exponentially with gate bias before the bands cross and then linearly after the bands have crossed.

The maximum electric field, ξ, is assumed to be linearly dependent on the gate-source bias and drain-source bias. In deriving (1), the tunneling process is approximated by a particle tunneling through a triangular barrier, with a slope given by the electron charge times the electric field $q\xi$. It has been shown by Hurks [26] that the maximum electric field can be used effectively here without taking the actual electric field distribution near the tunnel junction into account. Mathematically speaking, the detailed dependence of maximum electric field on V_{GS} and V_{DS} can always be approximated with a polynomial of certain degree. To make the model widely applicable to devices with different architectures, the maximum electric field is taken to be linearly dependent on V_{GS} and V_{DS} by dropping the second and higher order terms.

B. *Electric Field*

The maximum electric field in (3) is taken to be linearly dependent on gate-source bias, V_{GS}, and drain-source bias, V_{DS},

$$\xi = \xi_O \left(1 + \gamma_1 V_{DS} + \gamma_2 V_{GS}\right). \tag{4}$$

The electric field, ξ_O, is the built-in electric field at the source-channel tunnel junction when zero bias is applied to both gate and drain terminals. Parameters, γ_1 and γ_2, are linear coefficients with units of inverse volts. Increasing gate bias enhances the electric field at the source-channel junction by both enlarging the voltage drop (compared to the built-in voltage) and narrowing the tunneling barrier region. Increasing the drain bias has the same effect, but to a lesser degree because the drain field is screened by the gate electrode.

It is worth noting that the use of (4) remains physically meaningful even for broken-gap heterojunctions, where the concept of tunneling path and corresponding electric field can still be phenomenologically applied. Consideration of [29] shows that quantization effects along the transport

direction produce a forbidden gap in the local density-of-states in the broken gap junction. Also note that there exists an electron energy barrier for tunneling in the AlGaSb/InAs heterojunction that approaches a rectangular barrier with nanometer-scale thickness in the ON-state. As a result, a current relation of the same form of (4) can be expected.

C. Subthreshold Region

In the subthreshold region, the drain current of a tunnel FET depends exponentially on the gate bias, which is dominated by the exponential decrease of the tunneling window with V_{GS} below the threshold voltage. Accordingly, the tunneling window in the subthreshold region can be expressed by

$$V_{TW} \approx U \exp\left(\frac{V_{GS} - V_{TH}}{U}\right). \tag{5}$$

Here, the factor, U, called the Urbach factor, is given by

$$U = \gamma_0 U_0 + \left(1 - \gamma_0\right) U_0 \left(\frac{V_{GS} - V_{OFF}}{V_{TH} - V_{OFF}}\right), \tag{6}$$

$$U_0 = n k_B T / q$$

where γ_O is a parameter that controls how quickly the tunneling window closes with gate bias, n is the subthreshold ideality factor, V_{OFF} is the minimum V_{GS} voltage for which (6) is valid. The threshold voltage V_{TH} is defined as the gate-source bias at which the source valence-band-maximum equals the channel conduction-band-minimum (for an n-channel TFET). The expression (6) causes the subthreshold swing to decrease linearly with gate bias. When V_{GS} equals V_{OFF}, U is $\gamma_O U_O$ and γ_O is a factor less than or equal to 1. When the gate bias is equal to the threshold voltage then U equals U_O.
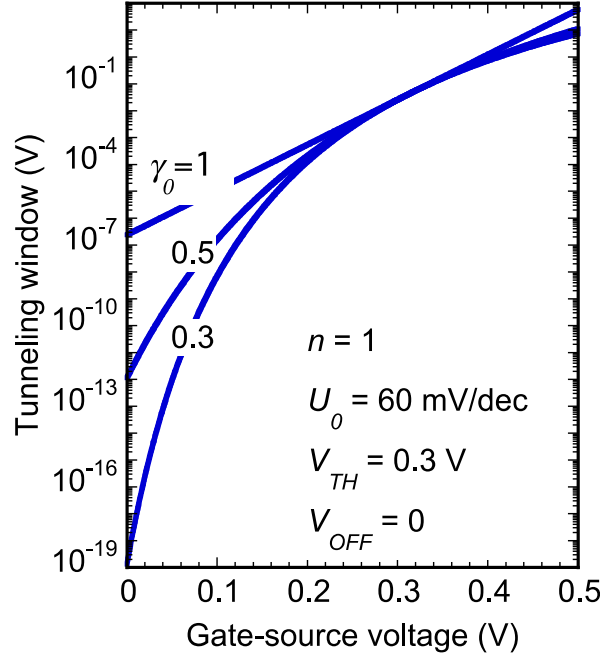
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Fig. 2. Tunneling window, V_{TW}, plotted as a function of gate-source voltage at room temperature in the subthreshold region.

The dependence of the tunneling window on gate-source bias is plotted in Fig. 2 for different γ_O values. When the parameters γ_O and n equal one, U reduces to U_O and the tunneling window is represented by a straight line in a semilog plot, corresponding to an exponentially closing tunneling window of 60 mV/decade. If γ_O is reduced below 1, the subthreshold swing decreases as the gate-source voltage decreases as can be observed in Fig. 2.

D.   *Above-Threshold Region*

According to (3), the drain current in the above-threshold region should be directly controlled by the tunneling window. Above-threshold the tunneling window should be given by

$$V_{TW} \approx V_{GS} - V_{TH},\tag{7}$$

which can be called the overdrive voltage.

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E.   *Bridging the Subthreshold and Above-Threshold Regions*

A function is needed to connect the subthreshold and above-threshold regions smoothly. Borrowing from Khakifirooz [30] and Wright [31] for MOSFETs, the following expression allows a continuous transition between the subthreshold and above-threshold regions,

$$V_{TW} = U \ln\left[1 + \exp\left(\frac{V_{GS} - V_{TH}}{U}\right)\right]. \tag{8}$$

Fig. 3 shows the tunneling window as a function of gate-source voltage. When in the subthreshold region, the tunneling window grows exponentially with gate bias, but in the above-threshold region, it tends to a linear dependence on the gate bias. Whereas the mathematical expression in (8) is able to describe both exponential and linear regions in a single equation, there is no physical basis to justify its accuracy in the transition region, $\sim 3nkT$. This is also true in the MOSFET where this function has been effectively utilized to link subthreshold and linear regions [30, 31].
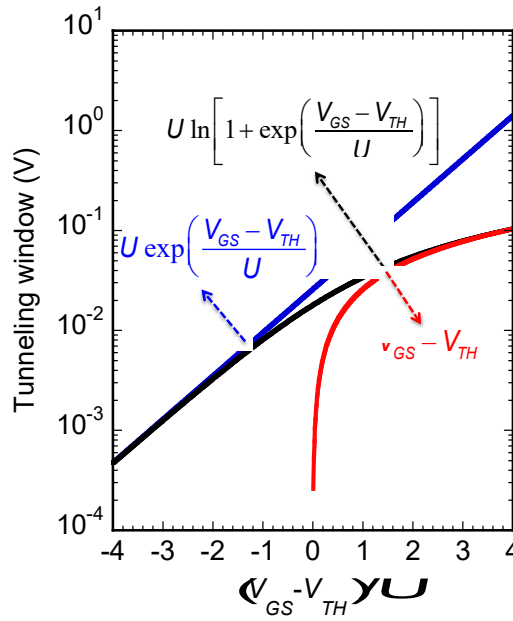

Fig. 3. Tunneling window, V_{TW}, plotted as a function of $(V_{GS} - V_{TH})/U$. When $(V_{GS} - V_{TH})/U$ is larger than about 3, V_{TW} reduces to a linear function; when $(V_{GS} - V_{TH})/U$ is smaller than about -3, V_{TW} reduces to an exponential function.

F. *Superlinear Current Onset*

The superlinear onset of the output characteristic is another signature behavior of the TFETs. De Michielis [13] showed that this characteristic arises from the Fermi occupancy of filled states in the source and unoccupied states in the channel. However, their expression for the drain current was not devised to account for the saturation of the drain current. This can be readily added as shown below. Initially the following simple function f, was used to describe both the superlinear onset and the saturation of drain current with drain-source bias,

$$f = \frac{1 - \exp\left(-\dfrac{V_{DS}}{\Gamma}\right)}{1 + \exp\left(\dfrac{V_{THDS} - V_{DS}}{\Gamma}\right)}, \tag{9}$$

where Γ is a constant and V_{THDS} is the drain threshold voltage which corresponds to the minimum drain voltage needed to initiate the tunneling current [32]. When V_{DS} equals zero, then (9) and the tunneling current are zero. When V_{DS} becomes large, the function f tends to one.
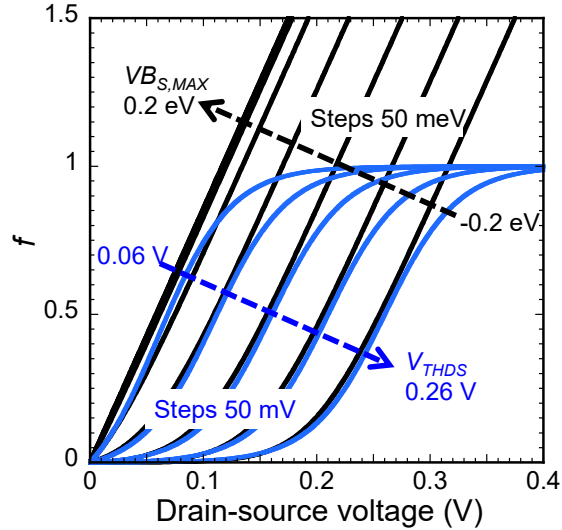

Fig. 4. Output characteristics for different source degeneracies based on occupation probability. The black lines are reproduced from [13]. The blue lines are based on (9), where Γ equals 32 mV.

In Fig. 4, (9) is plotted together with the expression from De Michielis [13]. In the low V_{DS} region the nonlinear turn-on of the drain current is well captured by (9). The superlinear onset degrades drastically as V_{THDS} becomes bigger than 0.1 V. At large V_{DS}, the function f saturates to 1, as desired.

In utilizing (9) to fit TFET simulations, it became apparent that the drain threshold voltage, V_{THDS}, should be made sensitive to gate bias. The drain threshold voltage has been found to increase linearly with gate voltage and then saturate at large V_{GS} [32]. To account for this dependence, the drain threshold voltage was modified to

$$V_{THDS} = \lambda \tanh\left(V_{GS} - V_{OFF}\right), \tag{10}$$

where λ is a constant with the unit of volts and the voltage inside the *tanh* function is normalized to 1 V. The hyperbolic tangent function is chosen because when $V_{GS} - V_{OFF}$ is small,

$$\tanh\left(V_{GS} - V_{OFF}\right) \approx V_{GS} - V_{OFF}, \tag{11}$$

and when $V_{GS} - V_{OFF}$ is large,

$$\tanh\left(V_{GS} - V_{OFF}\right) \approx 1. \tag{12}$$

The function f in (9) then becomes

$$f = \frac{1 - \exp\left(-\dfrac{V_{DS}}{\Gamma}\right)}{1 + \exp\left(\dfrac{\lambda \tanh\left(V_{GS} - V_{OFF}\right) - V_{DS}}{\Gamma}\right)}. \tag{13}$$
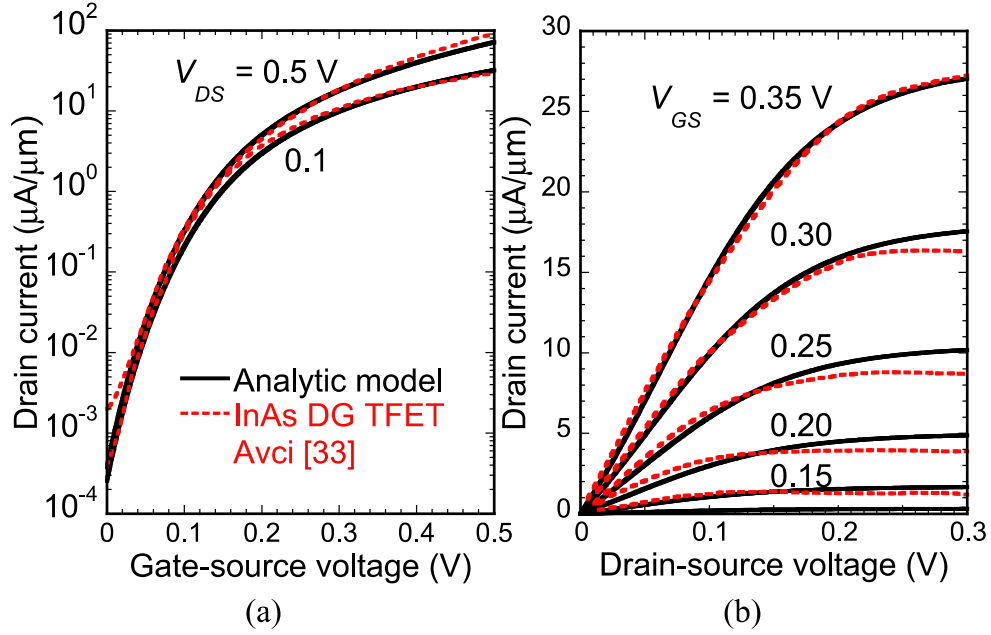
Fig. 5. Modeled and simulated transfer and output characteristics of a 20 nm InAs double-gate TFET. Atomistic simulation data are from [33].

In order to test the ability of the model to represent TFET physics, we have fitted the model to two very different TFET embodiments. The first is a double-gate (DG) *p-i-n* InAs TFET [33] with characteristics predicted by an atomistic quantum-mechanical device simulator, and the second is an in-line broken-gap AlGaSb/InAs TFET [34] as predicted by Synopsis technology computer-aided design (TCAD). The results are shown in Figs. 5 and 6. The channel length and width are 20 nm and 1 μm, respectively. The device model parameters for both devices are shown in Table I. The model shows good agreement to the simulations. Excellent representation of the superlinear current onset is shown in Figs. 5(b) and 6(b). Close inspection of the bias dependence of the transconductances and conductances obtained by the model shows that the terminal dependences are not matched precisely owing to the generic nature of the tunneling description.
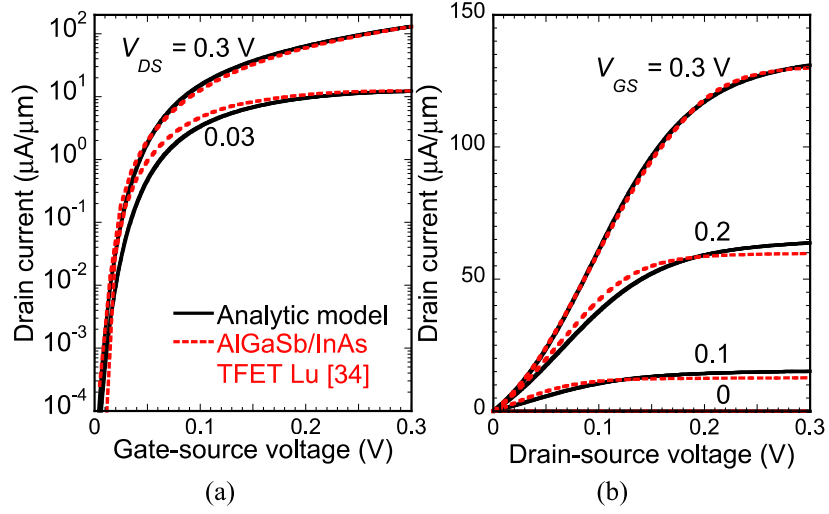
Fig. 6. Modeled and simulated transfer and output characteristics of a 20 nm broken-gap AlGaSb/InAs TFET. Numerical simulation data are from [34].

TABLE I

SUMMARY AND RANGE OF PARAMETERS IN THE MODEL

	Range	InAs DG TFET	AlGaSb/InAs TFET
E_G (eV)	–	0.35	0.35
m_R^*	–	0.012	0.012
t_{CH} (nm)	–	5	5
Γ (V)	$0-1$	0.06	0.046
γ_0	$0-1$	0.5	0.2
γ_1 (m^{-1})	$0-1$	0.01	0.1
γ_2 (m^{-1})	$0-2$	1.3	0.9
ξ_0 (MV/cm)	$0.5-5$	0.527	1
λ (V)	$0-1$	0.19	0.32
n	>1	1.8	1.2
V_{OFF} (V)	$0-V_{DD}$	0.01	0
V_{TH} (V)	$0-V_{DD}$	0.17	0.08

III.   COMPLETE DC MODEL OF TFETs

The model discussed thus far is valid for positive V_{DS} and V_{GS}. Often in RF or transient simulations all four quadrants of the I_D-V_{GS} characteristic may be needed. A tunnel FET is essentially a gated *p-i-n* tunnel diode. The asymmetrical source/drain junction causes tunnel FETs to have asymmetrical

characteristics when the drain-source bias is reversed. When forwardly biased ($V_{DS} < 0$), the band-to-band tunneling current gradually gives way to the diffusion current as V_{DS} is decreased, resulting in NDR in the I_D-V_{DS}. Also due to the asymmetrical doping, the tunnel junction shifts from the source-channel junction to drain-channel junction when the gate bias reverses, resulting in ambipolar conduction.

To fully make use of these features in circuit design, our model is extended into all four quadrants of operation: (1) I_D [$V_{GS} > V_{OFF}$, $V_{DS} > 0$], (2) I_D [$V_{GS} < V_{OFF}$, $V_{DS} > 0$], (3) I_D [$V_{GS} < V_{OFF}$, $V_{DS} < 0$], and (4) I_D [$V_{GS} > V_{OFF}$, $V_{DS} < 0$]. The equation set outlined in section II describes a model that operates in the first quadrant only. In this section, currents in the other three quadrants are defined.

A.   *Second quadrant – the ambipolar current: I_D [$V_{GS} < V_{OFF}$, $V_{DS} > 0$]*

In the conventional mode of operation, the TFET tunnel current is suppressed when V_{GS} is low and then the tunnel window at the source junction is opened with positive V_{GS}. However the TFET can also turn on when gate bias is sufficiently negative. As shown in Fig. 7(a), when the gate bias is negative, the valence band maximum of the channel can be shifted above the conduction band minimum of the drain. Meanwhile, the drain-channel junction narrows as a result of the large voltage drop on the junction, leading to electrons tunneling from the channel into the empty states in the drain. Therefore, the tunneling window opens up gain, with the tunnel junction shifted from the source-channel junction to the drain-channel junction. When this happens the channel conduction changes from one carry type to another and the current is said to be ambipolar.

The ambipolar current is added to the model by copying the current for $V_{GS} > V_{OFF}$ to $V_{GS} < V_{OFF}$ and multiplying the current by a smoothing function, f_S. The term V_{GS} is replaced with $V_{GS} - V_{OFF}$ in (4). To preserve the current continuity at $V_{GS} = V_{OFF}$, f_S decreases from 1 when $V_{GS} = V_{OFF}$ to an attenuation factor s when $V_{GS} << V_{OFF}$. As $V_{GS} - V_{OFF}$ decreases from 0, as shown in Fig. 7b. The ambipolar drain current is given by

$$I_D\left(V_{GS} < V_{OFF}\right) = I_D\left(V_{GS} > V_{OFF}\right) f_S$$

$$f_S = \left(1 - (1-s)\tanh\left(-\frac{V_{GS} - V_{OFF}}{s}\right)\right) \tag{14}$$

where s is an attenuation factor that sets the ratio of I_D ($V_{GS} < V_{OFF}$) to I_D ($V_{GS} > V_{OFF}$). In cases where the ambipolar current is suppressed, s can be set to a small number. The scaling factor, s, is taken to be dimensionless, because $V_{GS} - V_{OFF}$ in the argument of the *tanh* function is considered to be normalized to 1 V. Fig. 8 shows the drain current plotted as a function of gate-source bias from -0.5 V to 0.5 V with s set to 1 and 0.1, respectively.
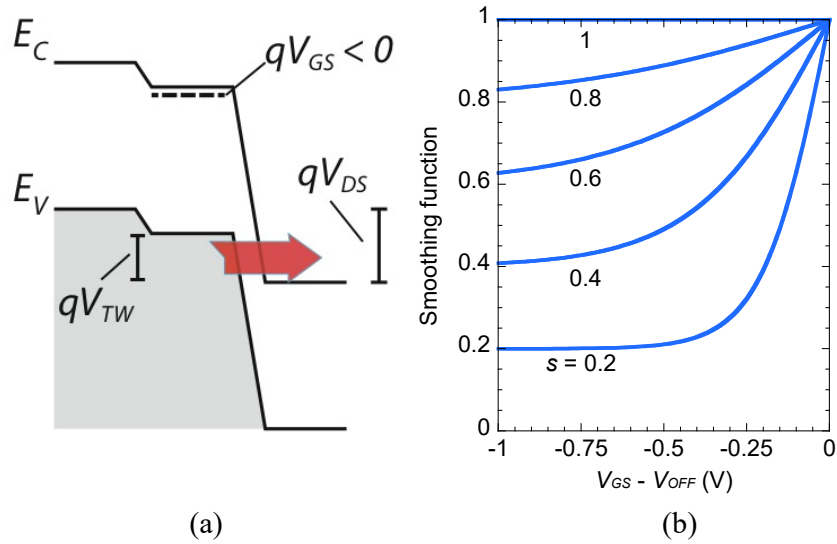

(a)   (b)

Fig. 7. (a) Band diagram showing ambipolar conduction of tunnel FETs. (b) Smoothing function plotted as a function of $V_{GS} - V_{OFF}$ with s increasing from 0.2 to 1 in steps of 0.2.
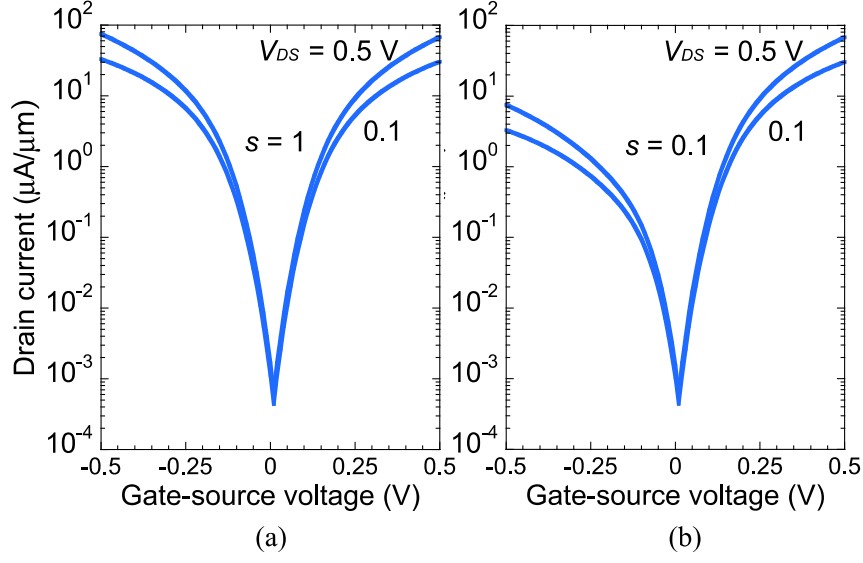
Fig. 8. Transfer characteristics of 20 nm InAs DG TFET showing ambipolar current for $s = 1$ (a) and $s = 0.1$ (b).

B.   *Third quadrant: $I_D [V_{GS} < V_{OFF}, V_{DS} < 0]$*

The third quadrant is the least used region. In this region, the current is defined using the universal diode current equation.

$$J_D = -J_0 \left[\exp\left(-\frac{V_{DS}}{nkT/q} \right) - 1 \right]. \tag{15}$$

C.   *Fourth quadrant – the negative differential resistance region: $I_D [V_{GS} > V_{OFF}, V_{DS} < 0]$*

When the drain-source bias, V_{DS}, is negative, the source-channel junction is forward biased and behaves like a forward-biased tunnel diode. The NDR is included by modifying a model for the tunnel diode from Sze and Ng [35]

$$J = J_P \frac{V}{V_P} e^{1-\frac{V}{V_P}} + J_0 \left(e^{\frac{V}{nkT/q}} - 1 \right). \tag{16}$$

Adapted to the notation of our model, this formula becomes

$$J_D = -\left(-J_P \frac{V_{DS}}{V_P} K(V_{GS} - V_{OFF}) \exp\left(1 + \frac{V_{DS} + \eta V_{GS}}{V_P} \right) + J_0 \left(\exp\left(-\frac{V_{DS}}{nkT/q} \right) - 1 \right) \right). \tag{17}$$
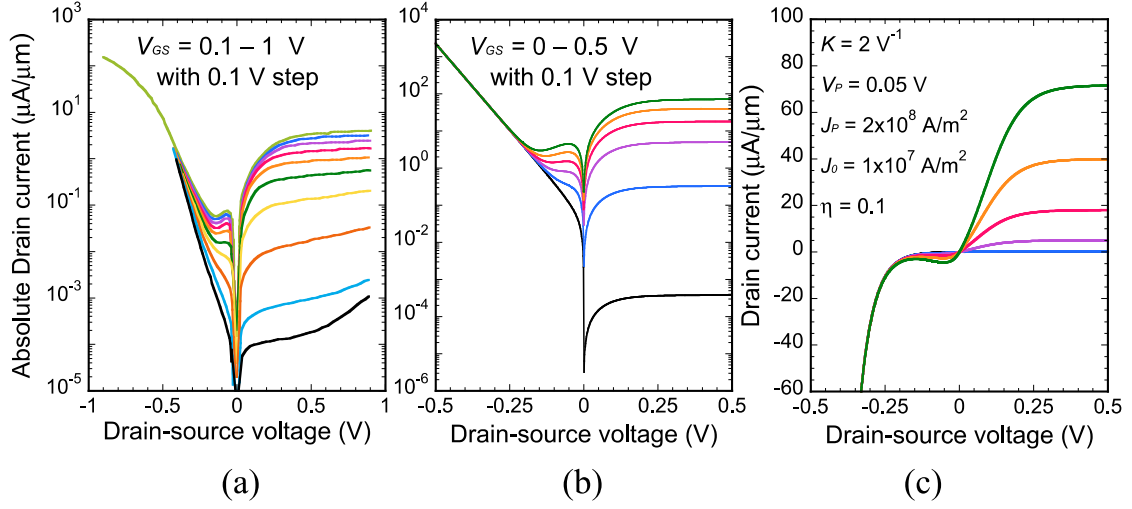
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Fig. 9. (a) Experimental forward and reverse bias drain current vs. drain-source voltage for InGaAs heterojunction TFET after Dewey [21], (b) logarithmic and (c) linear-scale, modeled forward and reverse-bias drain current vs. drain-source voltage for the 20 nm InAs DG TFET.

The five parameters J_P, J_0, V_P, K, and η, are fitting parameters. Parameter K has unit of V^{-1}. The last parameter η is dimensionless. Parameter n shares the same value as n in (6). As shown in Fig. 9, the experimental NDR behavior is well captured by this semi-empirical equation. Series drain and source resistance can always be added as subcircuit parameters to account for parasitic resistances.

IV. CAPACITANCE MODEL

The partitioning of gate capacitances between the source and drain in TFETs is significantly different from CMOS, primarily due to the difference in the distribution of inversion charge [36]. Because C_{GS} is much smaller compared to C_{GD}, it is set as a constant. Noticing the similarity between the f function (Fig. 4) and the behavior of C_{GD} with increasing V_{GS} and V_{DS} (Fig. 10), the f function is modified to model the behavior of C_{GD}

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$$C_{GD} = C_{GD,MIN} + \left(C_{GD,MAX} - C_{GD,MIN}\right) \frac{\left(1 + \beta V_{GS}^{m}\right) - \exp\left(-\dfrac{V_{GS} - V_{OFF}}{\Gamma'}\right)}{1 + \exp\left(\dfrac{\left(V_{TH} + \alpha V_{DS}\right) - \left(V_{GS} - V_{OFF}\right)}{\Gamma'}\right)}, \tag{18}$$

where $C_{GD,MIN}$ and $C_{GD,MAX}$ are the approximate minimum and maximum of C_{GD}. Parameters α, β, Γ', and m are fitting parameters, in which α and m are dimensionless, β has unit of $1/V^{m}$, and Γ' has unit of V. C_{GD} is set to $C_{GD,MIN}$ in the other three quadrants.
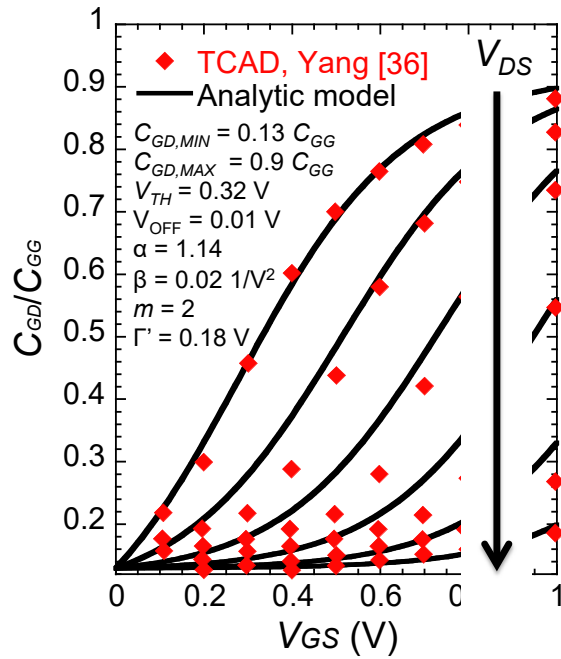

Fig. 10. Modeled gate drain capacitance, C_{GD}/C_{GG}, vs. V_{GS} plotted against TCAD simulation data from [36] with V_{DS} increasing from 0 to 1 V in steps of 0.2 V.
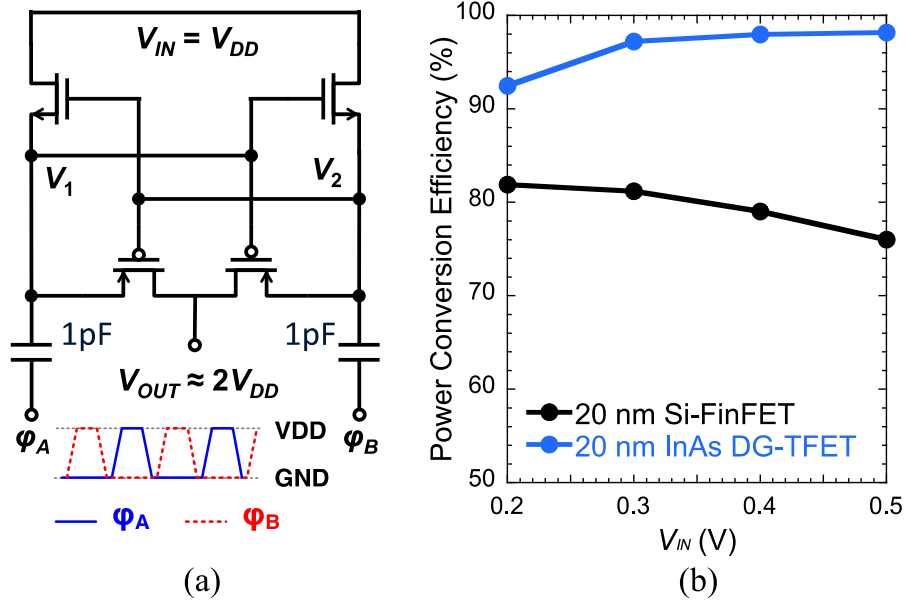
Fig. 11. (a) TFET charge pump circuit and (b) power conversion efficiency vs. input voltage for 20 nm HP Si FinFET [37] and InAs DG TFET.

The complete model is implemented as a subcircuit model in HSPICE 2013 and applied to a simple 4T charge pump circuit to demonstrate its use [38]. As shown in fig. 11(a), a charge pump circuit converts an input DC voltage to a higher output DC voltage. In this case, the output voltage is $2V_{IN}$. The circuit is simulated using modeled 20 nm InAs DG TFET as shown in Fig. 5 and Table I [33] and 20 nm HP Si FinFET PTM-MG model [37]. The power conversion efficiency, the ratio of output power to input power, for both devices is shown in Fig. 11(b). TFETs can achieve efficiency higher than 90% when V_{IN} is in the range of 0.2-0.5 V, whereas CMOS can only achieve efficiency higher than 70% when V_{IN} is 0.5 V.

VI.   CONCLUSION

An analytic n-channel TFET model for circuit simulation is shown to capture the current-voltage characteristics of the TFET in all operation regions. The model can be readily adapted to describe the p-channel TFET. The model accounts for bias dependent subthreshold swing, saturation, the superlinear

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current onset, ambipolar conduction, and negative differential resistance. A simple behavioral capacitance model is also included. To justify the versatility of the model, the model is applied to two TFETs with distinctly different geometries, a planar double-gate InAs TFET and a vertical broken-gap AlGaSb/InAs TFET, and good agreement is demonstrated between the model and both simulations. The model is implemented in HSPICE and a simple charge pump circuit is simulated to prove the functionality of the model. The equation set enables the implementation of an entry-level TFET model for exploration of steep transistor circuits.

Acknowledgement

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