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Understanding the Potential and Limitations of Tunnel-FETs for Low-Voltage Analog/Mixed-Signal Circuits

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***Abstract*—In this paper, the analog/mixed-signal performance is evaluated at device and circuit levels for a III-V nanowire Tunnel FETs technology platform and compared against the predictive model for FinFETs at the 10 nm technology node. The advantages and limits of Tunnel FETs over their FinFET counterparts are discussed in detail considering the main analog figures-of-merits, as well as the implementation of low-voltage track-and-hold and comparator circuits. It is found that the higher output resistance offered by TFET-based designs allows achieving significantly higher intrinsic voltage gain and higher maximum-oscillation frequency at low current levels. TFET based track-and-hold circuits have better accuracy and better hold performance by using the dummy switch solution for the mitigation of the charge injection. Among the comparator circuits, the TFET-based conventional dynamic architecture exhibits the best performance while keeping lower area occupation with respect to the more complex double-tail circuits. Moreover, it outperforms all the FinFET counterparts over a wide range of supply voltage when considering low values of the common mode voltage.**

***Index Terms*—Tunnel FET, analog circuits, analog figures-of-merit, track-and-hold, comparators.**

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I. Introduction

The Tunnel Field Effect Transistor (TFET) is considered a promising option for future low energy electronic circuits [1], [2]. The TFET operating principle is the energy filtering of high energy electrons obtained by injecting carriers by band to band tunneling (BTBT) from the valence band of the source (for an *n*-type device) rather than thermionic emission from the conduction band, as in conventional MOSFETs. The energy of source electrons is thus upper limited by the edge of the valence band, hence thermionic emission is not involved and the 60 mV/dec limit for the subthreshold swing SS (at room temperature) can be overcome.

However, the TFETs fabricated so far [3]-[5] are not competitive with conventional MOSFETs, the main limitations being the low on-current (one of the highest reported is 180 μA/μm at $V_{DS} = V_{GS} = 0.5\ V$ [6]) and the too narrow and too low current range where sub-60 mV/dec operation is observed (1-10 nA/μm [7]). By contrast, many simulation-based studies predicted TFETs with superior performance at device level (in terms of figures of merit such as transconductance efficiency, intrinsic gain, cut-off frequency) and at circuit level (delay and dynamic power) in the ultra-low voltage regime (a few hundreds of millivolts) compared to conventional MOSFETs [8]-[19].

The use of full-quantum simulations [8], [9] or calibrated TCAD models [13], [14] allows capturing the effect of size- and bias-induced quantization on the BTBT rate more accurately than in commercial TCAD tools. In particular, according to simulations, III–V hetero-structure TFETs have the potential to maintain sub-60 mV/dec operation at suitable current levels (up to 1-10 μA/μm) [20], [21], whereas experiments still report unattractive SS values [7] with the exception of a recent publication [22]. Other aspects which are often neglected in simulations include the band tails of the density of states in the energy gap [23], [24], and the effects of defects and interface states on the device characteristics and on device variability [24], [25].

Encouraged by the promising simulation predictions,

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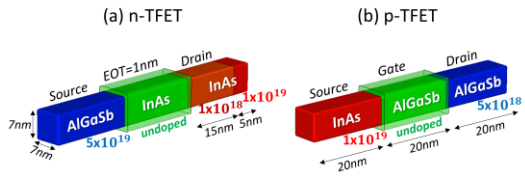

(c) TCAD parameters

	$Al_{0.05}Ga_{0.95}Sb$	$InAs$
$E_G\ (eV)$	1.04	0.59
$\chi\ (eV)$	4.01	4.9
$A_{path}\ (cm^{-3}s^{-1})$	1.51×10^{20}	1.44×10^{20}
$B_{path}\ (V/cm)$	9.54×10^{6}	2.94×10^{6}
$N_C\ (cm^{-3})$	1.26×10^{18}	5.22×10^{17}
$N_V\ (cm^{-3})$	1.8×10^{19}	6.6×10^{18}

Fig. 1. Structure of *n*-type (*a*), *p*-type (*b*) InAs/AlGaSb TFETs and calibrated parameters (*c*) as used in the TCAD simulations (see [13], [14]) to reproduce the full-quantum results in [8], [9]. The metal gate electrode runs all around the nanowire and lies exactly on top of the gate dielectric, resulting aligned to the source/drain-channel abrupt junctions. Reported dimensions, materials and doping levels are the same as in [9].

several research groups have performed an early assessment of TFET technology for low voltage electronics. Such investigations have used mixed-mode device-circuit simulations as available in TCAD tools, and/or look-up-table (LUT) based simulations in the Verilog-A environment [10]-[14]. Most of these studies focused on digital circuits, while only a few of them are devoted to analog and mixed-signal circuits [17]-[19]. These works consider virtual technologies and assume *p*-type and *n*-type devices having similar electrical characteristics.

Recently, B.Sedighi *et al*. reported an extensive analysis of TFET-based analog circuits and a systematic comparison with their MOSFET counterparts [10]. The results of [10] highlighted that several analog circuit topologies have to be revised for a TFET implementation, due to the peculiar characteristics of the devices, such as the unidirectional conduction, the ambipolar leakage, the large output resistance, the large gate-to-drain capacitance, and the negative differential resistance. The study by B.Sedighi *et al*., however, embraced the optimistic assumption of a perfect symmetry between *p*-type and *n*-type TFETs: in fact *p*-TFET electrical characteristics were obtained by mirroring the *n*-TFET curves. Unfortunately, both experimental data and simulations have highlighted that a quite strong asymmetry between the *n*- and *p*-type TFETs is expected and hard to circumvent [7].

The aim of this study is to improve our understanding of the potential and the limits of TFETs for low-voltage analog/mixed-signal circuits. To this purpose, we consider well-calibrated TCAD models, in order to reproduce the III-V TFET virtual technology platform reported in [8], [9], which consists on *n*- and *p*-type TFET templates designed by means of full-quantum simulations, thus removing the *a priori* assumption of a symmetric behavior for *n*- and *p*-type devices. The main analog figures of merit at device and circuit levels are compared against the predictive models for FinFETs at the 10 nm technology node [28]. Basic analog/mixed-signal

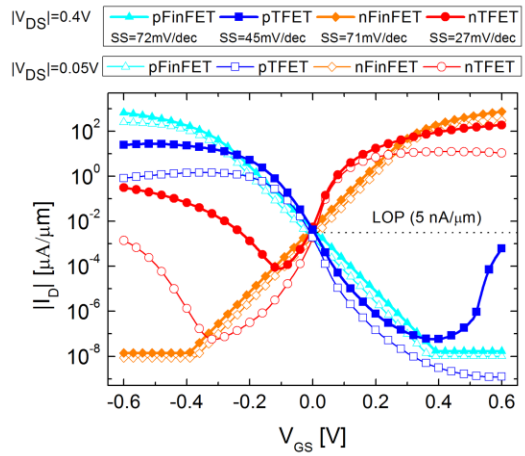

Fig. 2. Simulated I_D as a function of V_{GS} at $|V_{DS}| = 0.05\ V$ and $|V_{DS}| = 0.4\ V$ for the *p*- and *n*-type TFETs of Fig.1 compared to their FinFET counterparts. $I_D - V_{GS}$ characteristics are normalized by the device perimeter and the I_{OFF} is about 5 nA/μm (LOP) for all transistors at $|V_{DS}| = 0.4\ V$.

building blocks, such as track-and-hold and comparators, have been selected as benchmarks.

II. Device Description and Simulation Approach

Fig.1 shows the TCAD structures of the complementary TFET technology platform designed and optimized in [8], consisting of squared cross-section InAs/AlGaSb nanowires (NWs), with 20 nm gate length, squared cross-section with side $L_{side} = 7nm$ and Al_2O_3 gate dielectric with an equivalent oxide thickness, EOT of 1 nm. In particular, a non-uniform drain side doping with abrupt profile yields a sort of gate underlap which reduces the ambipolar behavior of the n-type device.

Simulations are performed using the Synopsys-Sentaurus TCAD environment. The physical models are somewhat simplified in several respects, one prominent example being neglecting the effects of quantum confinement; to cope with this limitation, the simulation deck has been carefully calibrated against the full-quantum simulation results of [8]. In particular, the band-gap parameters for the InAs/AlGaSb hetero-structure (energy gap, E_G and the electron affinity, χ) have been adjusted and the dynamic nonlocal-path BTBT model parameters (${A_{path}}^{dir}$ and ${B_{path}}^{dir}$ [26]) have been recalibrated according to the effective masses of bulk InAs and GaSb [27]. Also, the effective valence/conduction band density of states (N_V and N_C) have been considered as fitting parameters to improve the match with full-quantum simulations, as reported in [13]. The calibrated parameters are summarized in Fig.1(c).

As regards the CMOS counterpart, 10 nm technology node FinFETs are simulated via the SPICE predictive technology models (PTM) described in [28] and available in [29]. It is worth noting that these models are calibrated against experimental data. The FinFETs have 14 nm gate length, 21 nm fin height (H_{fin}), 9 nm fin width (W_{fin}) and EOT of 0.88 nm.

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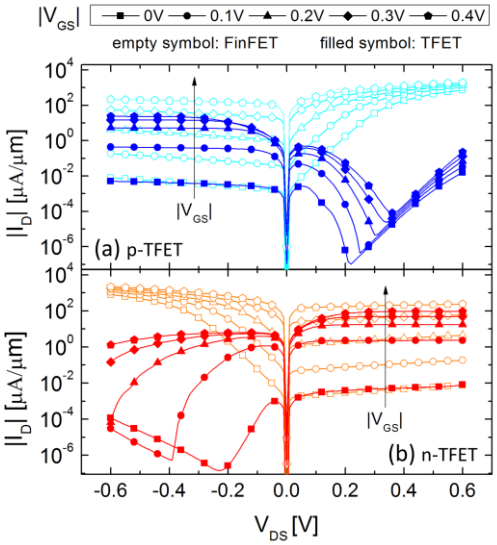

Fig. 3. Simulated I_D as a function of V_{DS} at various $|V_{GS}|$ from $0\,V$ to $0.4\,V$ for the *p*- and *n*-type TFETs of Fig.1 compared to their FinFET counterparts.

Circuit level simulations are carried out within the Cadence design environment by implementing for the TFETs a Verilog-A model based on the LUTs generated from TCAD simulations for the drain current I_D, the gate-to-source (C_{GS}) and the gate-to-drain (C_{GD}) capacitances, as a function of the biasing voltages (i.e. V_{GS} and V_{DS}) [13].

III. TFETs vs FinFETs: Analog Performance Comparison at Device Level

As can be seen in Fig.2, the $I_D - V_{GS}$ characteristic of the devices have been aligned at the same $I_{OFF}/W_{perimeter} = 5\,nA/\mu m$ (for $|V_{DS}| = 0.4\,V$), consistently with the low operating power (LOP) target of the ITRS [30]. In particular, we have $W_{perimeter} = 2H_{fin} + W_{fin} = 51\,nm$ for FinFETs and $W_{perimeter} = 4L_{side} = 28\,nm$ for TFETs. The *I-V* characteristics of *n*- and *p*-type FinFETs are essentially symmetric in subthreshold, due to the very similar electrostatics [31], while they feature slight differences above threshold. On the other hand the *p*-TFET exhibits significantly lower values of current (about 1/4) and, as shown in Fig.4(*a-b*), transconductance (about 1/9) at $|V_{GS}| = |V_{DS}| = 0.4\,V$ compared to the corresponding *n*-TFET. Note that, these I-V characteristics are quite far from the experimental data in [32] for similar hetero-structure. In fact, as discussed in the introduction, due to the limited maturity of the TFET fabrication process, significant amount of defects or interface traps (not included here) can deteriorate SS values. Also, we assume abrupt doping profiles and aggressive EOT scaling.

Fig.3 reports the $I_D - V_{DS}$ curves of the considered devices. Negative differential resistance (NDR) is exhibited by both the p-TFET ($V_{DS} > 0$) and the n-TFET ($V_{DS} < 0$). Furthermore, beyond the peak of NDR, the current of the p-TFET/n-TFET will increase for higher positive/negative V_{DS} values irrespective of the gate voltage due to the forward biased p-i-n junction. Both *p*- and *n*-type TFETs exhibit an excellent

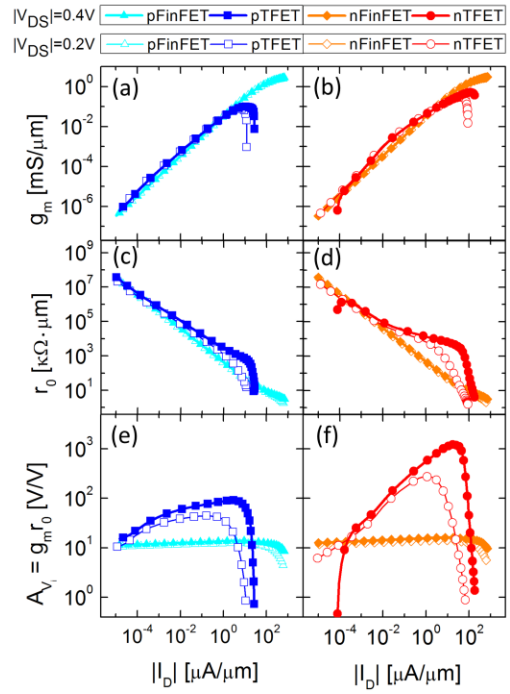

Fig. 4. Simulated transconductance (g_m), output resistance (r_0) and intrinsic gain ($A_{V_i} = g_m r_o$) as a function of I_D at $|V_{DS}| = 0.2\,V$ and $|V_{DS}| = 0.4\,V$ for the *p*/*n*-type devices described in section II.

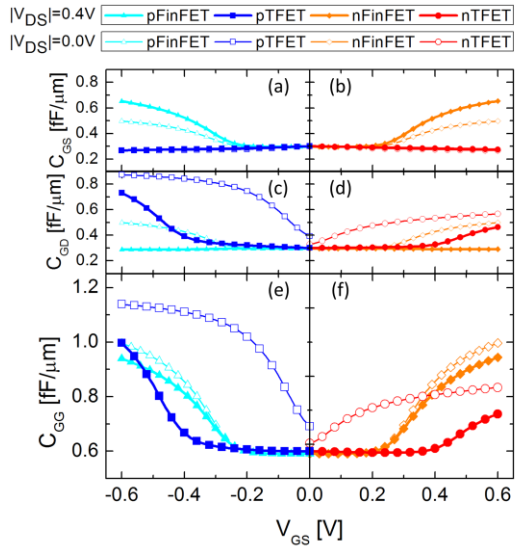

Fig. 5. Simulated capacitances (normalized by the device perimeter) C_{GS},C_{GD},C_{GG} as a function of V_{GS}, at $|V_{DS}| = 0.0\,V$ and $|V_{DS}| = 0.4\,V$ for the *p*- and *n*-type devices described in section II. All devices have been aligned at the same normalized extrinsic capacitances of about 0.6 fF/μm, equally split between gate-source and gate-drain contributions.

saturation, but for *p*-TFET the onset of saturation occurs at a larger $|V_{DS}|$ compared to the *n*-TFET and the output resistance, r_0, is somewhat smaller for a given drain current, as shown in Fig.4(*c-d*).

The combined effect of g_m and r_0 can be observed in Fig.4(*e-f*), where the intrinsic small-signal voltage gain ($A_{Vi} = g_m r_0$) is reported as a function of the I_D, showing that, beside the larger r_0 of TFETs, *the better* g_m *at given* I_D *(due to the*

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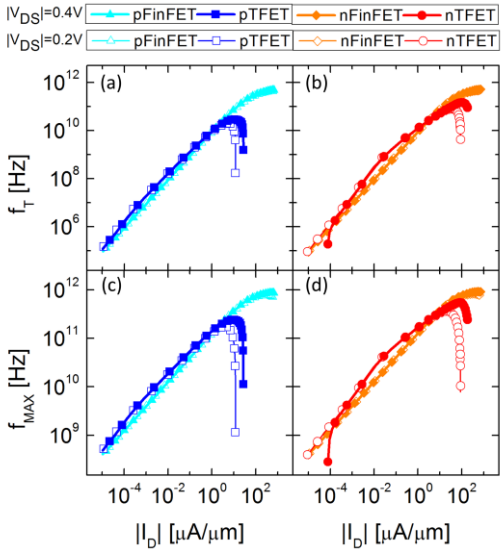

Fig. 6. Simulated cut-off frequency (f_T) and maximum oscillation frequency (f_{max}) as a function of I_D at $|V_{DS}| = 0.2\ V$ and $0.4\ V$ for the TFET and FinFET devices considered in this work.

better subthreshold slope, SS) makes TFETs advantageous over FinFETs at low current levels. In particular, at $|V_{DS}| = 0.4\ V$ the intrinsic gain of the n-TFET can be 100 times larger than for the n-FinFET, while the p-TFET reaches 10 times larger A_{Vi} compared to the p-FinFET. Comparing the experimental silicon p-type TFET NW data presented in [33] with the III-V p-TFET simulated here, it can be observed essentially the same trend of A_{Vi} as a function of the gate-source bias. In particular, both devices show A_{Vi} values up to 100 V^{-1} (but at different current levels), basically because of the good output current saturation.

Fig.5 shows the gate-source capacitance, C_{GS} and the gate-drain capacitance, C_{GD} for both FinFET and TFET devices (including both extrinsic and intrinsic contributions) as well as the total gate capacitance, C_{GG} as a function of V_{GS}. These trend are in line with the expected shape of these curves as already described in several comparative papers [17], [34].

Realistic layout rules and parameters will be required for a more accurate benchmarking of this III-V TFET technology platform against CMOS. However, these aspects are difficult to evaluate in a virtual technology also because, most likely, TFETs would be implemented as vertical nanowires. Physical design and layout parasitics are thus expected to be significantly different in the TFET and FinFET technologies. To reduce the number of additional parameters and ease the comparison, we employ the same parasitics for FinFETs and TFETs. In particular, here an extrinsic gate-source and gate-drain capacitances is included in the TFET models in order to align the devices at the same normalized capacitances at $|V_{GS}| = 0.0\ V$ (for $|V_{DS}| = 0.4\ V$), since the predictive FinFET models includes about 0.6 fF/μm extrinsic capacitance equally split between the gate-source and gate-drain contributions. It can be seen that the p-type and n-type TFET exhibit a lower C_{GS} than the FinFET counterparts, while have higher C_{GD} than

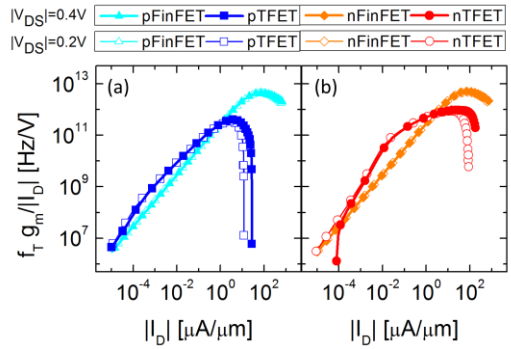

Fig. 7. Simulated $f_T\, g_m/I_D$ product [36] as a function of I_D at $|V_{DS}| = 0.2\ V$ and $|V_{DS}| = 0.4\ V$ for the considered TFET and FinFET devices.

the FinFET when $|V_{GS}|$ is larger than $|V_{DS}|$. We also note that p-TFET exhibits higher capacitance values compared to the n-TFETs, mainly due to the much larger valence band effective density of states ($N_V = 1.8 \times 10^{19}\ cm^{-3}$), for the AlGaSb channel region of the p-TFET, compared to the conduction band effective density of states ($N_C = 5.22 \times 10^{17} cm^{-3}$) for the InAs channel region of the n-TFET. These values have been adjusted in TCAD simulations in order to match full-quantum simulations [13], [14]. The intrinsic gate oxide capacitance for the TFETs is about 0.8 fF/μm (equivalent to about 40 fF/μm^2 when normalized to the device area).

Fig.6 reports the cut-off frequency (f_T) and the maximum oscillation frequency (f_{MAX}), which are evaluated in the simulation environment by using the Y parameters as described in [35]. In particular, in order to obtain a fair estimation of f_{MAX}, the source and drain resistance of FinFETs (65 Ω×μm included in the Spice model) has been added also to the Verilog-A model for the TFETs. It is worth noting that the assumed source and drain resistances (about 2.3 kΩ for one TFET) don't impact significantly the TFET and FinFET performances in the considered operating conditions, due to the small I_{ON} in the ultra-low voltage regime ($< 300\ mV$) which causes small voltage drop across each resistance.

The main difference between n-type and p-type TFET is in the current at which we observe the peak of the cut-off frequency, whereas at low current the f_T value is almost the same, slightly better than for FinFET thanks to the larger g_m of TFETs at low current. This is also reflected in the maximum frequency, where the better output resistance of TFETs slightly amplifies their advantage at low currents. At high current, the g_m of the FinFETs is much better resulting in higher f_T and f_{MAX}.

The $f_T \frac{g_m}{I_d}$ figure-of-merit proposed in [36] is reported in Fig.7 as a function of the normalized I_D. This figure of merit summarizes the combined effect of the main analog parameters in terms of cut-off frequency f_T (which is a measure of the speed of the device) and transconductance efficiency g_m/I_D (which is a measure for the power efficiency of the device). Note that the optimum occurs at lower current levels for TFETs compared to FinFETs. Furthermore, as

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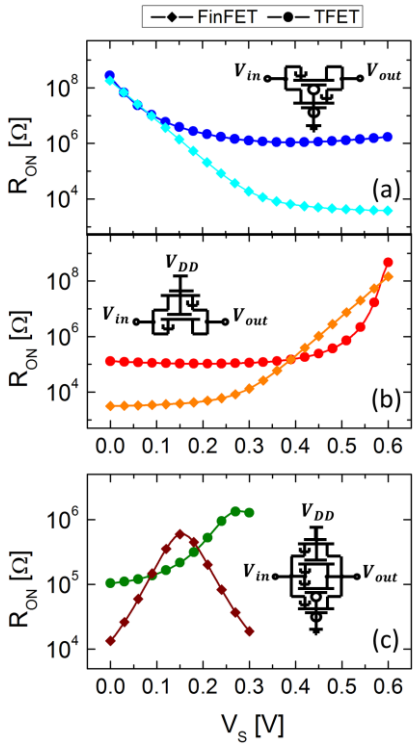

Fig. 8. Simulated ON resistance (considering $V_{in} = V_{out} = V_S$) of (*a*) p-type pass-transistor and (*b*) n-type pass-transistor both at $V_{DD} = 0.6\,V$, and (*c*) transmission-gate (considering $V_{DD} = 0.3\,V$) when used as track-and-hold circuit.

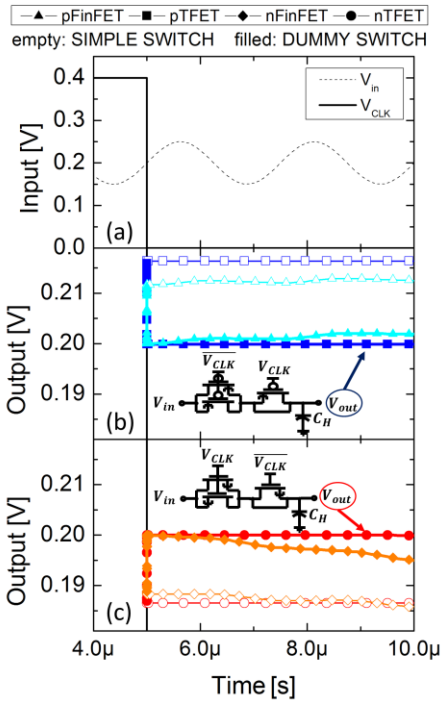

Fig. 9. Simulated time evolution of a Track and Hold circuits in "hold" mode with (see schematics in the insets) and without (circuits sketched in Fig.8) the dummy switch, considering: (*a*) $V_{CLK} = 400\ mV$ and a sinusoidal signal with $V_{in(pp)} = 100\ m$ and a dc magnitude of 200 mV. (*b*) *p*-type devices and (*c*) *n*-type devices. TFET switches are compared against the predictive model of FinFETs at the 10 nm technology node.

expected from the trends of g_m and f_T seen in Fig.4(*a*-*b*) and Fig.6(*a*-*b*), *n-TFETs perform significantly better (up to 10X) than n-FinFETs at low current, whereas p-TFETs present a smaller advantage (up to 3X) with respect to p-FinFETs in the same current range (0.01–1 μA/μm*). However, for currents larger than approximately 1 μA/μm, FinFETs always perform better than TFETs thanks to the higher g_m at such current levels.

IV. TFETs vs FinFETs: Performance Comparison at Circuit Level

Circuit simulations are performed by comparing FinFETs and TFETs at almost the same $W_{perimeter}$, which implies nearly the same I_{OFF}, as the I_{OFF} per unit perimeter has been set to 5 nA/μm for all devices (see section II and Fig.2). Thus, two TFET nanowires (overall $W_{perimeter} = 2 \times 28\ nm = 56\ nm$) are parallel-connected to have about the same I_{OFF} as a single FinFET ($W_{perimeter} = 51\ nm$). We have also compared (not shown in the following) the same number of devices (i.e. one TFET and one FinFET) with the purpose to make a one-by-one device comparison by realigning their characteristics for the same absolute value of the off current. In such a case, TFETs maintain almost the same current range over which they outperform FinFETs, while showing improved advantages in terms of dynamic energy mainly due to the higher capacitance of a FinFET device compared with a single TFET.

A. Track-and-hold circuits

Pass transistors and transmission gates are important building blocks of analog/mixed-signal circuits. To assess their performance as analog track-and-hold (T/H) circuits, we need to analyze their small-signal behavior. We have thus computed the equivalent differential on-resistance (R_{ON}), that is plotted in Fig.8 as a function of the voltage ($V_{in} = V_{out} = V_S$) applied to source and drain terminals, when the gate terminal of *n*-type and *p*-type switches is connected respectively to V_{DD} and ground. Note that TFET-based pass transistors use two transistors of the same type (i.e. two *n*-type or two *p*-type FETs) but with an opposite connection of source and drain in order to obtain a bi-directional device. FinFETs based pass-transistors, instead, consist of a single transistor, because individual FinFETs are bi-directional due to the symmetry of the source and drain regions.

As it can be seen, *n*-type TFET (plot *b*) has lower R_{ON} with respect to *n*-FinFET for V_S higher than $V_{DD} - 250\,mV = 350\,mV$, but recover again the FinFET value when V_S approaches V_{DD}. Simulations also show that the V_S range of potential advantage remains about 250 mV below V_{DD} in the entire V_{DD} range analyzed in this work (not shown), while for the *p*-type option there is no significant advantage over the whole V_S range (plot *a*).

The transmission gate consisting of both *n*- and *p*-type TFETs, instead, offers advantages with respect to the FinFET implementation (in a small V_S range) only at V_{DD} below 300

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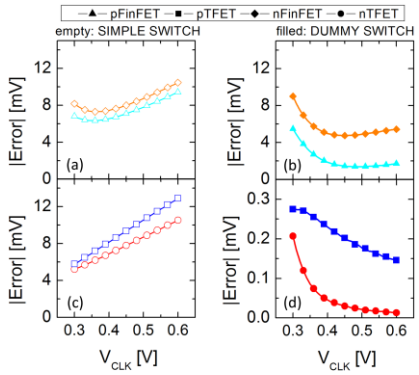

Fig. 10. Simulated absolute value of the output voltage error after 5µs from the beginning of the hold phase with $V_{CLK} = 0$ (corresponding to the time 10 µs in Fig.9) as a function of V_{CLK}, considering a sinusoidal signal with $V_{in(pp)} = 100\ mV$ and a dc magnitude of $V_{CLK}/2$ for the *p*- and *n*-type TFETs switches compared to their FinFET counterparts. Note that the TFET dummy switch solution (*d*) has a different Y-axes range due to the significantly lower values of the absolute error.

mV (plot *c*). Note that transmission gate configuration works well even for TFETs (with a conventional source and drain connection for *n*- and *p*-type), because the asymmetry of complementary TFETs takes place for opposite current directions. Simulations with higher V_{DD} (not shown here) do not display advantages of TFETs over FinFETs implementation. In particular, the asymmetry in complementary TFET results in higher on-resistance for V_S approaching V_{DD}. $W_{perimeter,p}/W_{perimeter,n}$ higher than one can be used in order to achieve symmetric complementary TFET, however this results in increased area occupation and higher capacitance, thus a trade-off should be considered in order to keep the advantage of TFETs over FinFETs.

The resistance R_{ON} is an indication of the performance of the T/H circuit during the 'track' phase. One of the major issues that has to be addressed in T/H circuits is the charge injection, resulting in considerable error during the 'hold' phase, because of the voltage change at the high impedance node. This is particularly problematic for high resolution data converters, where the accuracy required is below the so called 'quantization step': $V_{ref}/2^N$ [37]. As an example, for $V_{ref} = 0.4\ V$ and N=12 bit resolution, the quantization step is less than 0.1 mV.

Fig.9 shows the effect on the output voltage of using a direct compensation technique by injecting an equal and opposite amount of charge through a transistor with shorted source and drain (dummy switch) connected to the hold capacitor. The area of the dummy switch is assumed to be half of the actual switch because the hold capacitor receives only a fraction of the charge in the channel. As expected, the dummy switch greatly improves the disturb related to charge injection taking place at the beginning of the hold phase. However, it can be seen that for increasing time in the 'hold' phase ($V_{CLK} = 0$) the *p*-type FinFET pass-transistor shows increasing voltage at the output node, while *n*-type counterpart shows an output voltage lowering.

This disturb is influenced by the different behavior of *p*-type and *n*-type TFETs and FinFETs during the "hold" mode

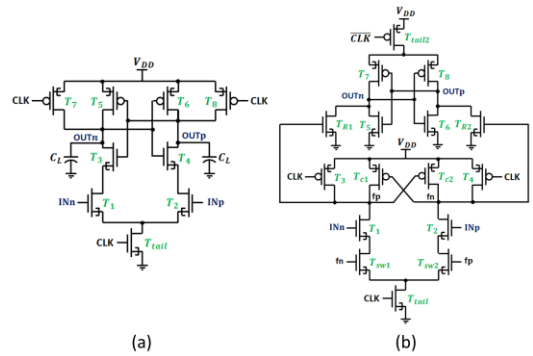

Fig. 11. Architectures of the conventional dynamic comparator (*a*) and the double tail comparator [38] (*b*) simulated in this work.

(i.e. $V_{GS} < 0$ for *n*-TFETs/FinFETs and viceversa for *p*-TFETs/FinFETs). Furthermore, *n*- and *p*-type devices experience both negative and positive V_{DS} values, depending on the peak of the sinusoidal input. In the case of a few hundred mV of sinusoidal input signal as in Fig.10, we have to compare the current of *n*-TFETs and *n*-FinFETs at slightly negative V_{GS}, and the current of *p*-TFETs and *p*-FinFETs at slightly positive V_{GS} for small V_{DS} values. As it can be seen in Fig.2, in this range of V_{GS} the current is lower for the TFETs compared to the FinFETs. This results in a *reduced drift of the sampled voltage over time for TFETs compared to their FinFET counterparts*. Thus, the ambipolar conduction of n-TFET is a limiting factor on the maximum applicable input signal swing (i.e. a large input signal swing will result in higher V_{DS} and V_{GS} experienced by the device thus in higher leakage current with respect to FinFETs).

In Fig.10 the absolute value of the output voltage error is reported as a function of the voltage applied at the gate of the switches, where the error is defined and evaluated as the difference between the input value sampled at the transition of V_{CLK} to zero, and the value observed 5µs after the beginning of the 'hold' phase. Notice that this drift over time of the sampled value is produced by two different effects: a) charge injection (largely mitigated by the dummy switch); b) leakage current of nominally switched-off pass-transistors. It can be seen that only *n*- and *p*-type TFET switches using dummy solution allow to mitigate the error from few mV down to only a few hundred µV. In particular, the absolute error of TFETs without the dummy switch increases as V_{CLK} increases, because of the charge injection contribution, while the error obtained with the dummy switch solution decreases as V_{CLK} increases, because of the reduced leakage current. In the FinFETs, instead, the compensation helps, but the leakage remains an important limiting factor.

B. Comparators

The use of the dynamic regenerative comparators is required for high speed and energy efficient analog-to-digital converters. Hence we have compared TFET- and FinFET-based implementations for both the conventional dynamic comparator shown in Fig.11(*a*) and the double tail structure proposed in [38], and here illustrated in Fig.11(*b*).

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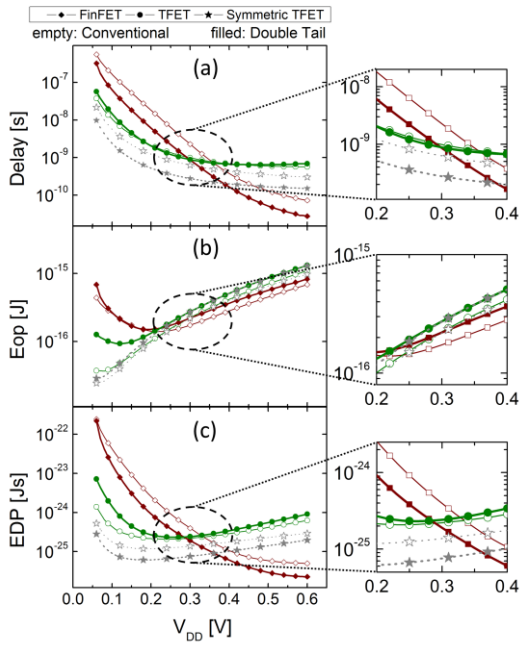

Fig. 12. Simulated Delay (*a*), Energy/Operation (*b*), Energy-Delay product (*c*) and associated zoom for the conventional and double tail comparators, considering $\Delta V_{in} = 5\,mV$, $V_{cm} = 0.7\,V_{DD}$, $C_L = 1\,fF$ and employing a progressive sizing for TFET and FinFET designs. The label "symmetric" indicates a special case where the I-V and C-V characteristics of the p-TFETs are assumed to be a mirrored version of the n-TFET ones.

Simulations are performed considering a differential input signal $\Delta V_{in} = INp - INn = 5\,mV$ and an input common-mode voltage $V_{cm} = 0.7V_{DD}$ for different V_{DD}values, while the load capacitances ($C_L = 1\,fF$) have been chosen equal to 10 times the input capacitances of a minimum size inverter. The two comparator topologies are designed considering the progressive sizing methodology for the stacked transistors, keeping a multiplicative sizing factor of 2 between two subsequent series-connected devices. In the double tail topology, $I_{tail1} > I_{tail2}$ is maintained for proper design as indicated in [38]. We verified that the delay is improved by about 20% for the progressive sizing compared to the corresponding minimum size designs (not shown).

As shown in Fig.12(*a*-*b*), the double tail topology is rewarding in a FinFET implementation because it allows to significantly boost the speed. For TFETs, instead, the conventional dynamic comparator shows similar speed as the double tail scheme, and yields a modest advantage in terms of energy/operation (Eop). Fig.12(*c*) shows that, thanks to the lower delay and Eop, TFETs allow for a better energy-delay product (EDP) for the conventional comparator at low V_{DD} (up to 300 mV) compared to both FinFET implementations. Furthermore, the ambipolarity of TFETs (stronger for n-TFETs in our models) does not significantly affect the performance of comparator circuits because the transistors in stack do not operate at negative V_{GS} bias. Note that, when a mirrored version of the n-type is considered as p-type TFET (see *symmetric TFET* in Fig.12) the upper voltage limit where TFET based comparators exhibit delay advantages over FinFET design is extended up to 400 mV. This can be

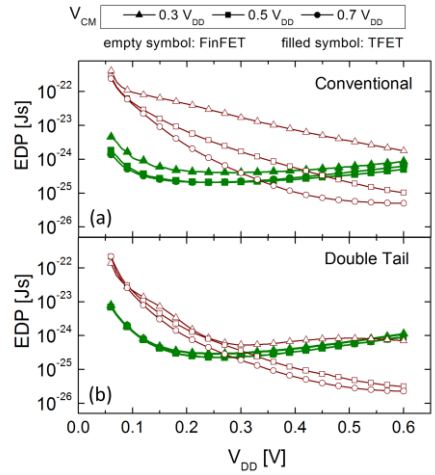

Fig. 13. Impact of the common mode voltage (V_{cm}) for conventional and double tail comparators.

reasonably ascribed to the *presence of stacked transistors which cause the lowering of the voltage drop across each device, thus emphasizing the speed advantages of TFETs due to the better SS at lower voltages.*

Moreover, *the TFET based conventional comparator outperforms even the TFET based double tail topology because of the asymmetric characteristics of p- and n-type TFET devices* (when compared to the *symmetric case*, the delay of the double tail circuit worsens of about 3.2X at $V_{DD} = 300\,mV$, while for the conventional topology there is only a factor of 1.6X). The stronger impact of asymmetric TFETs on the double tail architecture is mainly due to the lower performance of *p*-type TFET (discussed in section II) which is used as one of the tail transistors. Thus, the conventional TFET comparator is the best solution also due to the potential area saving coming from the reduced number of transistors.

The impact of the V_{CM} on the EDP of the circuits at study is analysed in Fig.13. While $V_{CM} = 0.7\,V_{DD}$ is needed for optimum performance in FinFET implementations, the corresponding TFET based circuits can reach optimum performance also at $V_{CM} = 0.5\,V_{DD}$ in the conventional architecture (keeping good performance also for lower V_{CM}), and even at $V_{CM} = 0.3\,V_{DD}$ in the double tail structure. It is worth noting that reducing the V_{CM} value allows for an extended range of V_{DD} where TFET based comparators outperform the FinFET based circuits.

All these considerations remain valid if the sizing ratio $W_{perimeter,p}/W_{perimeter,n}$ is changed to a value of 2 (not shown here). In particular, it has been found that the EDP of TFET circuits improves by less than 10% when the $W_{perimeter,p}/W_{perimeter,n}$ is set to 2, whereas the EDP becomes even worse if higher values of the sizing ratio are used, essentially because of additional capacitances.

V. Conclusions

We have presented a study of low-voltage analog/mixed-signal circuit designs exploiting heterojunction III-V Tunnel-FETs (designed and optimized for digital applications [8], [9]), with asymmetric *p*- versus *n*-type transistors, as actually

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reported in most of the experimental reports. TFET-based circuit characteristics were systematically compared to their FinFET counterparts (PTM [28], [29]).

Our analysis started with the figures of merit at device level, and was then extended to consider the performance of some important blocks, such as track-and-hold and comparator circuits.

The comparative analysis at device level points out that:

- TFETs exhibit a significantly higher A_{Vi} (up to two decades for n-type and one decade for p-type) than FinFETs, mainly due to their higher output resistance in the ultra-low voltage regime ($V_{DD} < 300\ mV$);
- the f_T of TFETs is slightly higher than that of FinFETs at low current levels (a higher advantage is observed for the n-type device), while it is significantly lower at high current levels, mainly due to the correspondent transconductance behavior;
- the f_{MAX} holds the same behavior of the f_T for both TFETs and FinFETs, but the observed improvement of TFETs at low current levels is slightly amplified by the effect of the higher output resistance.

Our analysis at circuit level points out that:

- TFET-based T/H circuits exhibit significant advantage in keeping a stable voltage in the 'hold' mode (lower drift over time). This is due to the fact that, once the charge injection problem has been mitigated by using the dummy switch solution, the error on the sampled voltage is mainly affected by the leakage current, which is lower for TFETs compared to FinFETs. However, ambipolar conduction of TFETs (mainly for n-TFET in our case) limits the input voltage swing which has to be small in order to reduce the V_{DS} and V_{GS} experienced by the device;
- TFET-based comparators (both conventional and double tail architectures) allow for a better EDP in the ultra-low voltage regime ($V_{DD} < 300\ mV$) compared to their FinFET counterpart. In particular, the conventional TFET comparator is the best choice in terms of area occupation and it outperforms the double tail topology because of the lower sensitivity on the asymmetry between p- and n-type TFETs.

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