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PHD THESIS

Pushing the Boundary of the 48 V Data Center Power Conversion in the AI and IoT Era

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Abstract

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The increasing interest in cloud-based services, the Internet-of-Things and the take-over of artificial intelligence computing require constant improvement of the power distribution network. Electricity consumption of data centers, which drains a consistent slice of modern world energy production, is projected to increase tremendously during the next decade. Data centers are the backbone of modern economy; as a consequence, energy-aware resource allocation heuristics are constantly researched, leading the major IT services providers to develop new power conversion architectures to increase the overall *webfarm* distribution efficiency, together reducing the resulting carbon footprint and maximizing their investments.

As higher voltage distribution yields lower conduction losses, vendors are moving from the 12 V rack bus to 48 V solutions together with research centers and especially data center developers. As mentioned, efficiency is crucial to address in this scenario and the whole conversion chain, i.e. from the 48 V bus to the CPU/GPU/ASIC voltage, must be optimized to decrease wasted energy inside the server rack. Power density for this converters family is also paramount to consider, as the overall system must occupy as less area and volume as possible.

LLC resonant converters are commonly used as IBCs (intermediate bus converters), together with their GaN implementations because of their multiple advantages in efficiency and size, while multiphase-buck-derived topologies are the most common solution to step-down-to and regulate the final processor voltage as they're well-know, easy to scale and design.

This dissertation proposes a family of non-isolated, innovative converters capable of increasing the power density and the efficiency of the state-of-the-art 48 V to 1.8/0.9 V conversion. In this work three solutions are proposed, which can be combined or used as

stand-alone converters: an ASIC on-chip switched-capacitor resonant voltage divider, two unregulated Google-STC-derived topologies for the IBC stage (48 V to 12 V and 48 V to 4.8 V + 10.6 V dual-output) and a complete 48 V to 1.8 V ultra-dense PoL converter.

Each block has been thoroughly tested and researched, therefore mathematical and experimental results are provided for each solution, together with state-of-the-art comparisons and contextualization.

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Chapter 1

Introduction

This chapter outlines the context of this research, its motivations, objectives and a brief overview of the treated topics. The *state-of-the-art* solutions involved in modern data center power conversion are investigated and explained, focusing on the reasons behind the shift to the 48 V distribution architecture and the underlying challenges that were here researched.

1.1 The Data Center role in the IT development

The increasing interest in cloud-based services, the Internet-of-Things and the take-over of artificial intelligence computing, together with the telecommunication infrastructure expansion, require constant improvement of the power distribution network. Electricity consumption of data centers has grown tremendously in the last decade, and it is projected to increase of 70% from 2013 to 2020 in the U.S. alone [2]. This infrastructure is the backbone of modern economy and uses about 3% of the world's total energy consumption [3]; as a consequence, energy-aware resource allocation heuristics are constantly researched [4] and leading companies such as Amazon, Facebook and Google are developing new power conversion architectures to increase the overall *webfarm* distribution efficiency, together reducing the resulting carbon footprint and maximizing their investments.

The SMARTer 2020 report shows that, globally, data center emissions will reach a 7%-increase per year by 2020 [5]. Although the pace of growth is reducing with respect to previous estimations, IT industry size is relentlessly expanding together with its energy requirement. Considering that, in 2010, this machine was consuming the equivalent of a country similar to Spain or Italy [6], it's clear that this is bound to significantly contribute to overall future carbon emissions. This phenomena has pushed member-based organizations like the Green Grid and the Uptime Institute, together with federal agencies like the U.S. Department of Energy and the Environmental Protection Agency to develop new standards

and policies to improve data center energy efficiency. At first the data center cooling infrastructure was improved, as it typically consumes one to two times the energy required by the actual IT equipment [2].

Adapting to increased environmental concerns, pushed by cost reduction, publicity and environmental organization pressures, the largest IT providers such as Google, Facebook, eBay, Microsoft, and Apple have addressed this problems reorganizing their facilities. Although their impact on the overall picture remains limited, as they represent only a 5 to 7% of the worldwide operating webfarms [7], efforts made by these companies can hopefully expand from corporate-owned (enterprise) data center to small server rooms.

It is clear that data center software and/or hardware re-fitting could require huge investments, especially when dealing with the power distribution network; nonetheless, the ideas hereby researched yield easily implementable architectures complying with the expanding 48 V rack distribution grid, which could become one of the leading choice during the next rack generation. During the 2019 OCP Global Summit, in fact, Google has proposed one of the hereby presented solutions, which was developed together with their power electronics division [8].

In the upcoming years, IoT (Internet of Things) and AI (Artificial Intelligence) will supposedly pervade our daily routine, as it is already massively happening with the introduction of a brand-new service class. Amazon, for example, is proposing a wide range of artificial intelligence-driven products, ranging from media automatic subtitling to data forecasting, image-based identity verification and document indexing. Portable devices are seeing the integration of new *online* features such as image classification and real-time object recognition. The internet of things, which embodies a growing number of interconnected devices dealing with any kind of data, intrinsically rely on decentralized computational power to operate, as usually its devices and sensors don't embed the required hardware, or simply it is not suitable for their batteries. This extreme decentralization is not only pushed by the inconvenient power and hardware embedding, but especially by the *big data* pool that these services require in order to operate. For example, the mobile image recognition and classification cannot be rapidly completed with the mobile phone's hardware, nor can it be consistent without others' millions remotely-stored images that are constantly being analyzed in the cloud by power-hungry parallel architectures. These mechanisms are constantly growing in our daily lives and enable a wide spectrum of possibilities, pushing service providers to participate in the forging of brand new products. This has an unique rebound on the data center context: an exponentially increasing processing power request to be dealt with specific software power analysis and tailored policies, such as in [4], together with intelligent power distribution networks that minimize losses and cooling energy waste inside the *webfarm*, at

the same time pushing power densities to free-up computing equipment space on the server board.

1.2 Server board power share

As briefly introduced, the effective amount of energy delivered to the computational hardware is about on half of the total input power, which is dissipated in power conversion and cooling. In the general case, the main source of inefficiency is related to ineffective software resources allocations [4]; i.e., although the power conversion hardware is designed to operate at its peak efficiency when almost fully-loaded, this scenario rarely occurs as many machines or logical subsystems are *idle*. IT-resources optimization requires complex modifications, as it implies the collaborations of many different systems such as power conversion hardware, power analysis software and dynamic reallocation algorithms, and can be in contrast with company security policies.

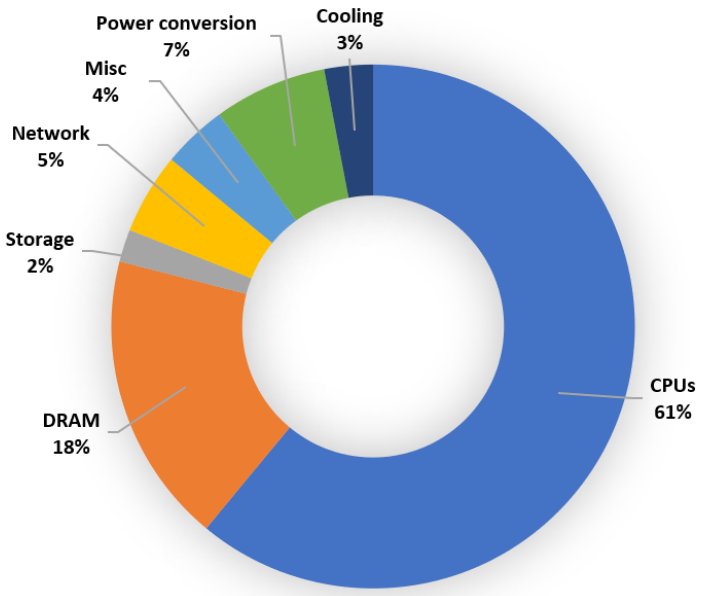


Fig. 1.1 Approximate distribution of peak power usage by hardware subsystem in a modern data center using late 2017 generation servers. The figure assumes two-socket x86 servers and 12 DIMMs per server, and an average utilization of 80% [1].

In order to understand the motivation behind this dissertation, it is important to understand that the converters hereby proposed are designed to be efficient when the attached loads (CPUs, ASICs, DRAM, peripherals) are operating at medium/full load, and the digital system power increased is dealt with a modular approach, i.e. enabling the proposed converters

to be *parallelizable*. This assumption is related to the overall system power density, as a performance-dense system is desirable when the space is constrained, or anyway when occupation cost is taken into account. Fig 1.1 depicts the typical power usage for a server/data center board operating at full load [1], i.e. it is supposed that a consistent software-level resource allocation is achieved and the overall system is efficient[1].

Although the power share depicted in Fig 1.1 can vary consistently with different configurations, the graph shows an important slice of power delivered to the CPU, which is the most energy demanding component on the board. Different editions of [1] show that CPU/DRAM peak powers, which were almost equal in 2007, decreased to 42 %/11.7 % of 2012 to the most recent 61 %/18 % of 2017. In fact, improved cooling technology has enabled the CPU to run close to its peak power and DRAM has shifted from power-demanding FBDIMMs to more recent implementations such as DDR4, together lowering supply voltage from 1.8 V to 1.2 V.

1.3 Typical Data Center distribution architecture

To understand the motivations supporting this research, the power distribution network structure of the typical data center and its main sources of energy inefficiencies must be outlined. As discussed earlier, energy management in data center is now one of the key issue for this business. The reduction of all energy-related costs and environmental impact is paramount. Different energy saving techniques have been developed in the last few decades to improve each conversion step.

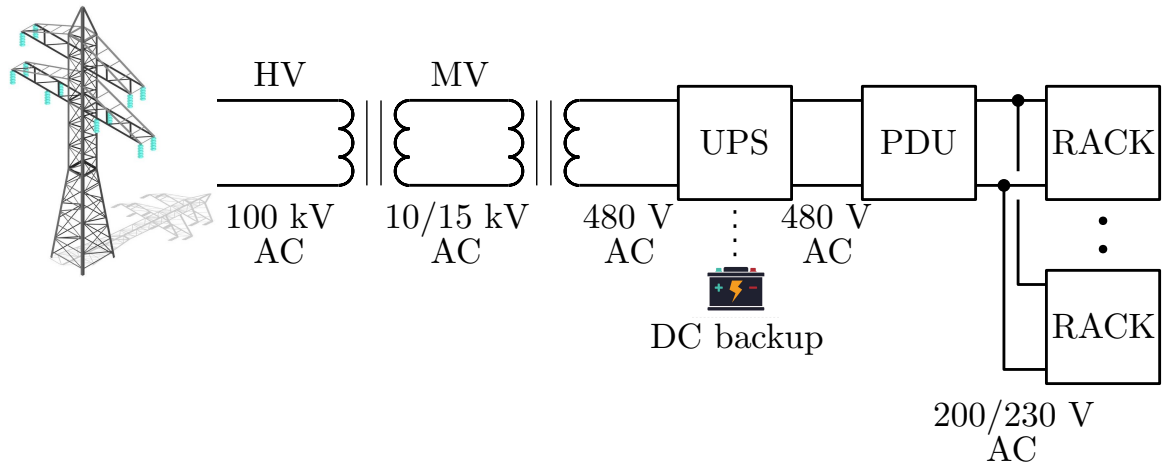


Fig. 1.2 Conventional 480 V AC distribution architecture.

[1]Power converters' light load conditions are also an important figure of merit in this context, but are not the main subject of research.

Existing power architectures may be divided into three categories, ordered *grid-to-rack*: AC, facility-level DC and rack-level DC [9], as shown in Fig. 1.2. At first, grid high-voltage is stepped down typically from 100 kV to 10-15 kV and then down to a 480 V bus. These conversions are usually very efficient, degrading overall efficiency by around 0.5 %. Inside the building the Uninterruptible Power Supply (UPS) causes most of the electrical losses (around 88 % of efficiency), due to the double AC/DC and DC/AC conversions. This device is usually connected to a backup system composed of diesel generators. From the UPS the lines reach different Power Distribution Units (PDUs), which are typically the last layer before the facility-level distribution system [1]. PDUs deliver energy to the racks with a very long cable (more than 100 m).

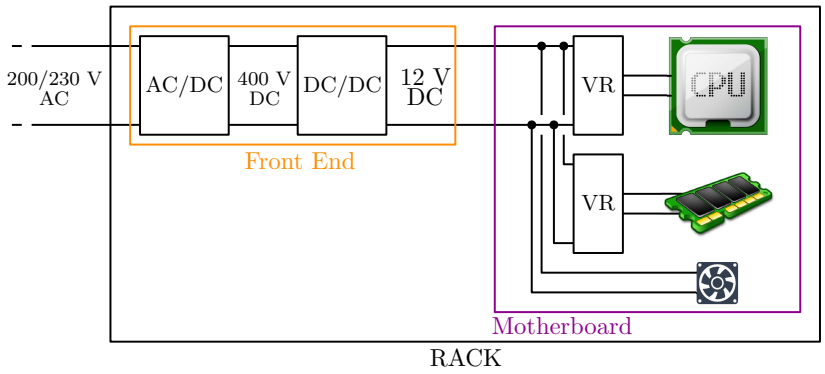


Fig. 1.3 Conventional 12 V DC bus rack-level distribution architecture.

In this scenario, power distribution losses drain the 50 % of the overall input energy, with a 25 % coming from the cooling system, which is historically marginally considered in the data center design [10]. Improving the power distribution network means to decrease wasted copper losses and together reducing the cooling energy overhead.

In Fig. 1.3 a typical power distribution architecture with a 12 V DC bus is shown. This conversion chain is burdened by many stages: inside the UPS of Fig. 1.2 the AC input is converted to an intermediate DC required by the backup system, i.e. a battery or generators, and then reconverted to AC. This output enters the rack and its Power Supply Unit (PSU) and is initially transformed to a 400 V DC bus with a Power Factor Corrector (PFC) stage. This DC voltage is stepped down to the 12 V rail, which supplies the server equipment through Voltage Regulation modules (abbreviated with VR or VRM). These last devices are characterized by a high current and low voltage output, and must finely regulate the semiconductor input voltage supply.

1.4 Shifting to the 48 V bus

Nowadays, challenges related to the 12 V power delivery are becoming critical. In the past, a typical rack was designed for 4 to 5 kW energy consumption, but nowadays it can consume up to 10 kW and it is predicted to reach 30 kW in the near future [11]: if the 12 V current is now around 833 A, in the future it would reach 2500 A with this design. Therefore, since power losses increase with the current squared (i.e. $P_{loss} = R \cdot I^2$), a higher voltage is mandatory to enable next generation's power requirements, and/or to lower nowadays increasing distribution losses. The 48 V bus has been proposed by *VICOR* [12] and *STMicroelectronics* (ST) [13], and enables higher overall efficiency and power supply volume reduction [14, 15].

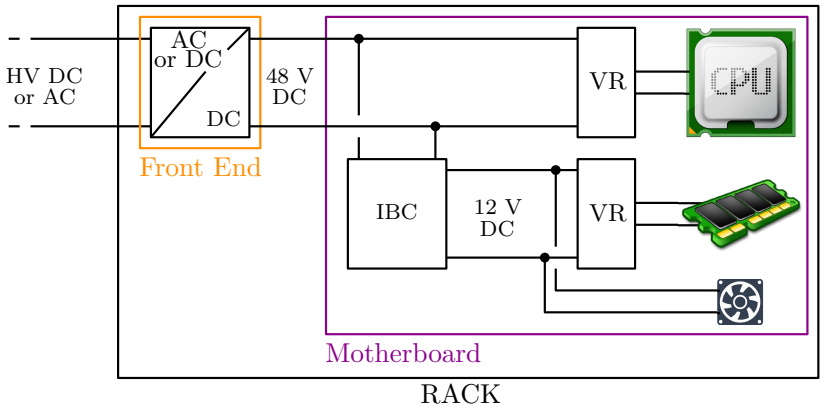


Fig. 1.4 New 48 V DC bus rack-level distribution architecture.

Fig. 1.4 shows the Google data center *Open Rack Standard* [16]. In this scenario the front-end hardware supplies the motherboard with a higher voltage, while core voltages and other rails are obtained through single-stage VRMs or Intermediate Bus Converters (IBCs). The rack-level transition from 12 V DC to 48 V DC provides several benefits: an overall reduction of power losses due to higher bus voltage, fewer conversion steps and better deployment flexibility. Moreover, the UPS is replaced by a battery pack placed new the rack itself, leading to an optimized use of space and conversion volume reduction.

Due to the large conversion ratio from 48 V to Point-of-Load (PoL), the most common approach is a two-stage conversion system, in which an intermediate 12 V DC bus is used (which is represented with the IBC of Fig. 1.4). The first stage is usually implemented using LLC resonant converters [17, 18], with their GaN implementations [19] or with Switched-capacitor DC-DC resonant converters [20, 21]. The second stage uses a multi-phase buck voltage regulation module (VRM) topology which is fed from the 12 V DC bus [22, 23].

1.5 Dissertation outline

In the 48 V DC bus scenario a whole new converter family is emerging, requiring modular and compact architectures able to increase power density and/or efficiency when the 48 V bus is stepped down towards core voltages or intermediate rails.

This dissertation proposes a family of non-isolated, innovative converters capable of increasing the power density and the efficiency of the state-of-the-art 48 V to 1.8/0.9 V converters present in literature. In this work three solutions are proposed, which can be combined or used as stand-alone converters.

This research is outlined starting from the high current/low voltage of the CPU/ASIC domain: Chapter 2, in fact, describes an ASIC on-chip switched-capacitor resonant voltage divider used for a 1.8 V-0.9 V, 300 A conversion. This architecture is developed to halve the overall digital load input current, or equivalently to halve the input pin count of a generic digital power package. As the CPU/ASIC load is characterized by fast current transients and strict voltage stability requirements, the Power Distribution Network (PDN) between the converter and the *socket* has been thoroughly analyzed with a novel dynamic-system-based approach.

The dissertation continues with the two examples of Google-STC-derived unregulated IBCs of Chapter 3: these novel architectures exploit the combination of switched-capacitors and coupled magnetics to achieve high power densities and resonant operation. The first converter, developed for Google LLC, implements a 48 V to 12 V unregulated conversion and has recently been proposed inside the *Google 48V Rack Adaptation and Onboard Power Technology Update* of the 2019 OCP Global Summit [8]. The second converter, which belongs to the same family, achieves a double-conversion with a single magnetic component, i.e. yielding 4.8 V + 10.6 V rails from the 48 V bus.

The last proposed converter, operating inside the 48 V context, is reported in Chapter 4, and implements different technologies to achieve a full 48 V-V_{core} regulated conversion.

Chapter 2

High Current Switching Capacitor Converter for On-Package VR

As a first step in the 54 V-to-V_{core} conversion chain optimization, the digital semiconductor core package is chosen. The following analysis, which is developed for a specific digital ASIC, can be extended for a generic CPU/GPU device.

In this chapter the lowest-voltage, highest-current domain of this research is addressed. A switched-capacitor on-package resonant voltage divider is presented considering the case of a digital ASIC requiring 300 A at 0.8 V, where the conversion is constrained to an area of 10 cm^2. A novel resonant driver is also presented, which enables the recycling of power devices gate charge. Output impedance is paramount to consider for this kind of converters, therefore this parameter is analyzed with a new technique, involving the analysis of a periodically time-varying system.

2.1 Introduction

Today digital ASICs, implemented in short channel technology, require low voltage and high current power supply with a critical PDN design and a huge number of supply voltage pins. Modern Intel processors integrate voltage regulators in order to overcome these limitations, improving also the system efficiency and increasing the available peak power. Unfortunately, fully integrated voltage regulator modules (FIVR) require a considerable design effort, therefore conversion implemented directly on the package can be a good compromise for ASIC applications. Switched capacitor (SC) DC-DC converters have become increasingly convenient for high-density conversion [24–32] because of the relatively high energy-density of capacitors compared to inductors [24, 33]. Moreover, they can be potentially integrated

in scaled CMOS technologies [34–40]. The on-package conversion system proposed here is based on a fixed-ratio switched capacitor structure, as reported in Fig 2.1. The resonant converter is composed of two phases connected in parallel operating with a 180° phase shift, where each phase is composed of 20 elementary cells.

The area required for the conversion system is about 20 mm × 50 mm and can supply up to 300 A. With a 2:1 switched capacitor conversion the input supply voltage of the ASIC is doubled and the input pin quantity is potentially halved. In order to improve the system efficiency and, at the same time, to reduce the output impedance of the converter, the switched capacitor circuits are driven at the resonant frequency of the flying capacitor structure, operating as a resonant switching converter. To minimize the output impedance many switches are connected in parallel, making driving losses a crucial issue, especially at light load. In order to overcome this limitation, a new driving technique is presented and tested, where a single resonant structure is used to commutate groups of paralleled cells, allowing to recycle gate charge energy.

Besides the design of the high-performance 2:1 SC converter, the development of a full-spectrum description of a generic periodic switched-structure is presented. In fact, for this type of converters, one of the most important performance indicator is the Power Distribution Network (PDN). The PDN describes the electrical behaviour of the power supply/load interconnection, therefore depends on the power supply itself, the physical interconnections such as VIAs, copper traces and especially on passive components such as decoupling capacitors or stray inductors on the power path. In this context, it is common to describe this quantity with the impedance seen by the socket, i.e. the complex $V_{socket}(j\omega)/I_{socket}(j\omega)$ ratio in the frequency range of interest. In this case the power supply is composed of the resonant voltage divider, and the PDN depends on its switching behaviour; therefore, a fundamental contribution of this part is the mathematical description of this dependency.

This is paramount to consider as digital loads (such as ASICs) require extremely fast current transients. Current frequency spectrum therefore comprises high-frequency harmonics, which must be taken into account with correct capacitor selection and layout simulations. In a periodic switched-structure, until now, layout simulation and lumped element models had never been completely included in the PDN description, as the only result present in literature can only give a rough estimation of the output impedance as a frequency-independent value [41]. It is important to notice that the lack of an accurate PDN description prevents the full-spectrum analysis of voltage transients; as a consequence, digital load voltage transient compliance could be difficult to estimate. The classical methods used to analyze inductor-based converters, such as state-space average models, hold validity in a reduced range of frequencies, which is a fraction of the switching frequency. Besides, with this techniques,

the use of lumped parameters for the description of the converter blocks is mandatory. To address this issues, the output impedance calculation for the SC converter is achieved with a novel technique, involving the analysis of an equivalent dynamic system. With the new proposed approach, every internal voltage and/or current can be simulated with high accuracy for any periodic switched-structure system. Each converter block can be described with an arbitrary input/output relation: lumped impedances (capacitors, inductors, resistors) can be described using the manufacturer's model, while the physical connections among them can be calculated via FEM, and the raw simulation results can be directly used. Therefore, this technique overcomes the limitations encountered during the estimation of a switched-capacitor converter performances, such as the overall efficiency, internal waveforms or input/output impedance. As a result, input and output transients can now be correctly predicted.

The chapter is organized as follows: in section 2.2 the switched capacitor structure characteristics, the operation principle and the total output impedance issue are discussed; in section 2.3 the resonant driving architecture is explained; in section 2.4 the novel analytic description of the open-loop output impedance is reported, while in section 2.5 and 2.6 experimental results and conclusions are presented.

2.2 Converter architecture

The implementation of the SC converter, which is constrained by the given package size specification, is based on the optimization of the PDN. For a SC resonant converter, the output impedance is proportional to the overall resistance [41]. This parameter depends on the capacitor ESR and FET $R_{ds,on}$, as it will be discussed in the next sections. In order to minimize the resistance for the given area, the best capacitors (with minimum $ESR \cdot area$) and FETs ($R_{ds,on} \cdot area$) were selected for this voltage rating. This figure of merit decreases proportionally with the device performance: in fact, a better device has a lower resistance and/or a smaller area. The area ratio is then chosen to minimize the sum of the two contributions; consequently, the number of devices is selected determining the structure of an optimized elementary cell.

The general approach to design the resonant tank can be therefore described as follows: first, the power conversion area constraint must be considered, together with the required voltage ratings. The power conversion area and shape restrict the device selection to a limited number of footprint combinations: the best-in-class devices must be consequently selected from this set. Usually, as ceramic capacitors have lower resistance for increasing capacitance values, high-capacitance components are often the best choice. Finally, the overall tank resistance can be minimized with the appropriate combination, as previously explained. This

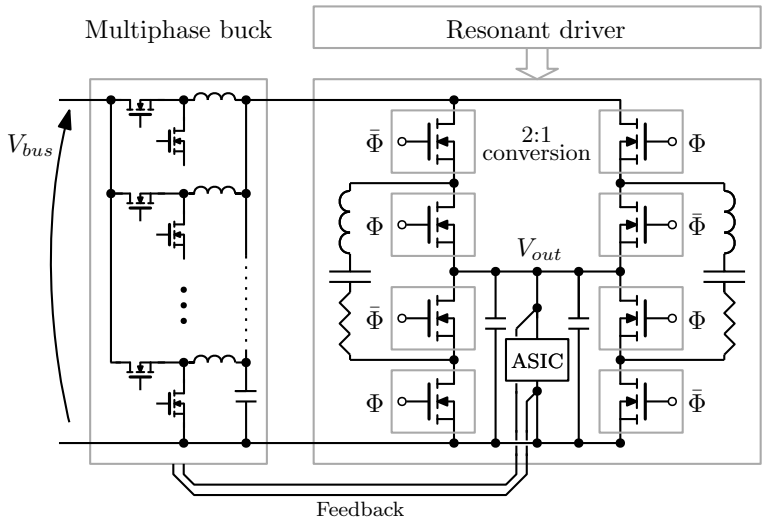


Fig. 2.1 Converter architecture (regulated multi-phase buck and 2:1 SC stage).

last step must take into account the whole power conversion area, therefore creating a cell which best-fits the available space. It is possible for some iterations to be required to achieve the best outcome. As the overall capacitance value is a result of this process, the resonant frequency must be selected considering the stray inductance of the structure. If the resonant frequency is also constrained, the stray inductance can be engineered with PCB design or with discrete components. For this prototype, the loop composed by input capacitors, FETs, resonant capacitors and output capacitors implements the stray inductance[1]. This loop is designed with a symmetric approach, filling the available area with copper as shown in Fig. 2.3; i.e., no particular PCB structures were used. The simulated and measured stray inductance were compatible with an intermediate switching frequency of 500 kHz, suitable for this application.

Therefore, the final stage of Fig. 2.1 is actually composed by the parallelization of many elementary cells to fill the available area. Each cell has the structure reported in Fig. 2.2 (a) and Fig. 2.3, where adjacent cells are 180° phase-shifted. In every elementary cell, a block of three capacitors (represented as C_p with its parasitcs) is switched at fixed frequency. Commutating the capacitor block near its resonant frequency ensures a sinusoidal current excitation, that is rectified to the output through the same cell structure. It is important to notice that the inductor represented in Fig. 2.2 (a) is not a physical device, but it is in fact given by capacitor package combined with the layout stray inductance. The whole converter is hence composed of 120 switched-capacitors and 160 MOSFETs. Charge balance among C_p terminals ensures $V_{out} = V_{in}/2$ in steady state, hence the SC stage operates as a

[1] Packages and VIAs additional inductance contributions must be considered.

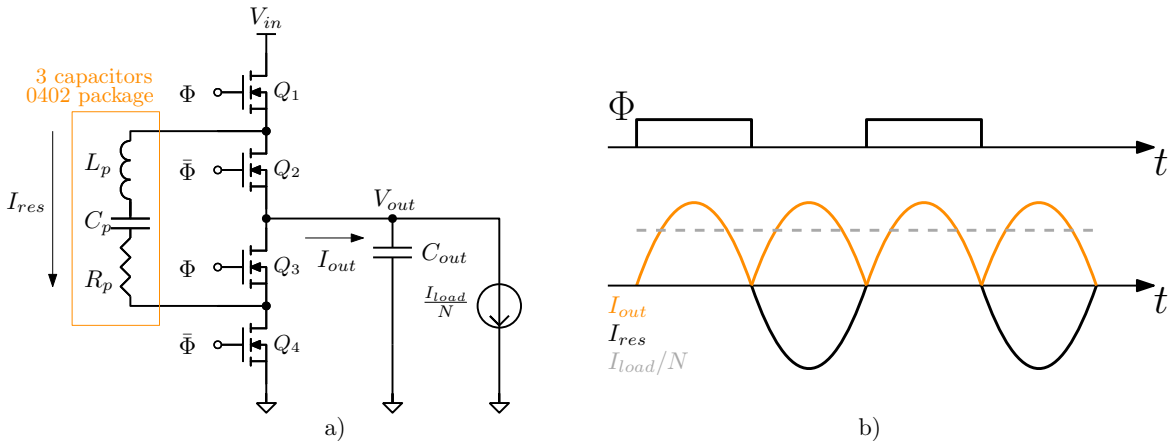


Fig. 2.2 Elementary switched-capacitor cell schematic supplying a fraction of load current (a) and operation principle (b).

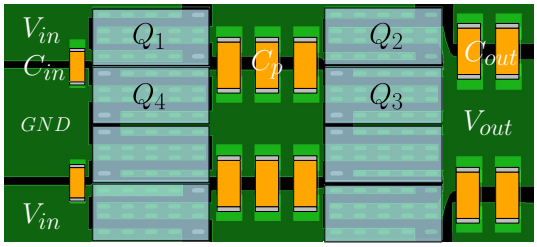


Fig. 2.3 Elementary switched-capacitor cell layout.

high-current voltage divider. The output voltage is filtered by capacitors placed at the output of every cell, as reported in Fig. 2.3. As the converter is operated at resonant frequency, every switch commutation is at zero-current. The switched-capacitor cell operation principle is shown in Fig. 2.2 (b).

Current-sharing could be achieved by connecting grouped SC cells to each buck phase, and connecting each SC group output together (which is in fact V_{out}): such configuration would ensure current balance for each cell group thanks to the first stage current-sharing loop. This connection strategy would require to isolate the buck phases outputs from each other and to connect the feedback at the end of the SC stage, which has no drawbacks as the regulated voltage is in fact the *core voltage*. For a 4-phase buck converter, as the SC stage here discussed is composed of 40 elementary cells, the connection would be 10 cells per buck phase. In this experiment the VRM board was externally connected and the cell-splitting was avoided; nevertheless, as reported in Fig 2.14 (b) of Section 2.5, the thermal analysis at I_{load} = 150 A reveals that the current distribution is inherently balanced by a passive current-sharing due to self-heating.

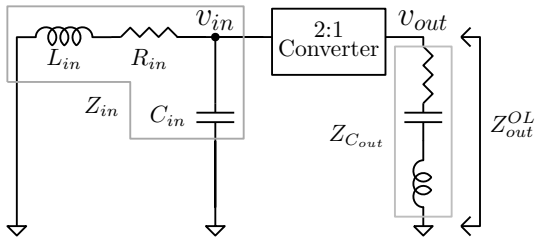


Fig. 2.4 Equivalent small signal model of the converter.

As mentioned, the converter's output impedance is a critical performance indicator and must be correctly designed. In the closed-loop architecture reported in Fig. 2.1, without load line regulation, it can be expressed as:

$$Z_{out}^{CL}(f) = \frac{Z_{out}^{OL}(f)}{1 + G_{loop}(f)} \tag{2.1}$$

where $Z_{out}^{OL}(f)$ is the open-loop impedance and $G_{loop}(f)$ is the loop transfer function of the full regulated system of Fig. 2.1, that includes the series of the buck converter together with the SC and the controller. Equation (2.2) is found in literature [41] as an estimator for this parameter:

$$Z_{out}^{OL}(0) = \frac{\pi^2 R_{cell}}{8} \tag{2.2}$$

where R_{cell} is the total resistance due to the series of the MOS on-resistance and the total ESR of the structure. While equation (2.2) is compact and yields, under certain conditions, a fast estimation of the open-loop value of the impedance at low frequencies, the behavior of $Z_{out}^{OL}(f)$ is far more complex and its calculation was proven to require the study of a periodically time-varying system. In particular, circuit-level simulation shows that (2.2) loses validity when Z_{in} and $Z_{C_{out}}$ impedances are considered. As Z_{in} depends, in this application, on the multi-phase buck, $Z_{out}^{OL}(f)$ must be precisely evaluated to achieve the correct selection of the regulator parameters. As shown in Fig. 2.4, the converter structure is composed of the input impedance Z_{in}, the 2:1 conversion cells and the output capacitance $Z_{C_{out}}$. Circuit-level simulation (Fig. 2.5) shows three main frequency intervals where $Z_{out}^{OL}(f)$ changes accordingly to the small signal model. The simulated model of Fig. 2.5 is based on the real converter parameters as, in this case, the three different behaviors for $Z_{out}^{OL}(f)$ are clearly visible. The measured output impedance, compared with simulation results, will be further discussed in Section 2.5. Impedance at low frequencies is dominated by $R_{in}/4$, that is the total resistance

between the first stage and the output, divided by the squared converter transformation ratio. After the resonance between the input inductance L_{in} and the input capacitance C_{in}, the output impedance becomes dominated by the SC-converter cell impedance, approaching the value of (2.2). Regulated-system's closed-loop crossover frequency is usually set inside this interval. At high frequency the converter influence decreases and C_{out} is the only contributor to Z_{out}.

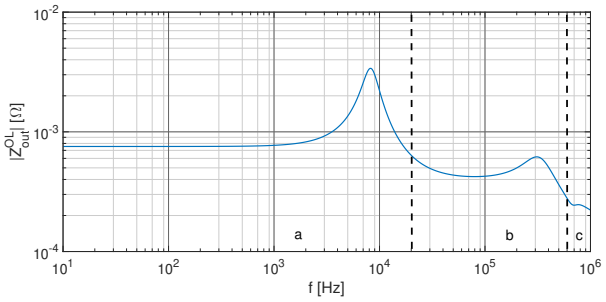


Fig. 2.5 Open-loop output impedance simulation based on the real prototype converter. $Z_{out}^{OL}(f) \simeq Z_{in}/4$ (a); $Z_{out}^{OL}(f) \simeq \frac{\pi^2 R_{cell}}{8}$ (b); $Z_{out}^{OL}(f) \simeq Z_{C_{out}}$ (c).

As mentioned, the analytic expression of Z_{out} is not simple and, without the results of Section 2.4, it has to be computed through circuit-level simulation (as in Fig. 2.5). Moreover, with the provided results, transfer functions' high-frequency effects can be included, such as eddy-currents resistance variations, as the complete description of the converter can now be obtained by using arbitrary transfer functions.

2.3 Driver architecture

The most noticeable drawback of the proposed solution is the driving power loss, caused by the large number of devices connected in parallel. The top-level view of the driver architecture is reported in Fig 2.6, where each group of paralleled switches $Q_{x,y}$ is driven by a dedicated driver with a floating supply, obtained with a multilevel bootstrap capacitor system. In order to increase the system efficiency, the resonant driver topology of Fig. 2.7 is adopted. The architecture is based on a multilevel half bridge with a clamping capacitor C_c. As shown in Fig. 2.8, the central node V_a commutates into three different levels: 0, $V_{dd}/2$ and V_{dd} with a fixed timing sequence. Each FET of the driver is activated with a commercial IC with independent high side and low side input. Obviously, a suitable form for this driving architecture is a fully integrated driver with only an external capacitor C_c.

The structure exploits the calibrated strip inductance from the drivers to the parallel connection of the transistor as resonance inductor, and the total C_{iss} of the paralleled switches

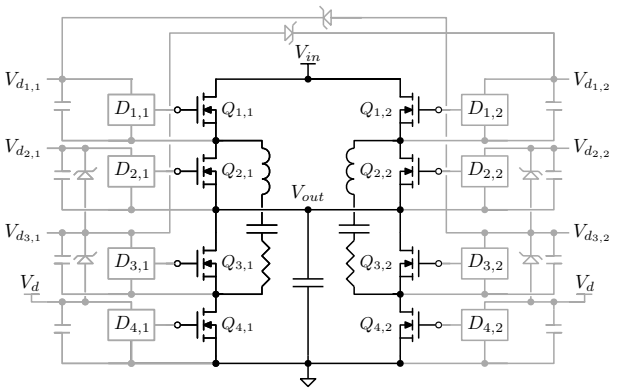


Fig. 2.6 Power converter (black) and driver architecture with multilevel bootstrap system (gray).

as resonance capacitor. At t_0 the V_a node commutates to $V_{dd}/2$, starting a resonant voltage transient between the L_{str} and the total C_{iss} capacitance. During this interval, V_{gs} can be expressed as

$$V_{GS}(t) = V_{dd}(1 - \cos(2\pi f_{cc}(t - t_0))) \tag{2.3}$$

where f_{cc} is the resonance frequency of the network during the phase from $(t_0 - t_1)$

$$2\pi f_{cc} = \sqrt{\frac{1}{L_{str} N C_{iss}}} \tag{2.4}$$

and N in (2.4) is the number of devices connected in parallel.

The duration of this phase is fixed to one half of the resonance period, allowing the zero-current commutation of the drivers' switches and reaching the voltage supply of the driver V_{dd} at the end of the phase. Considering $V_{gs}(t_1) = V_{dd}$, during the interval $(t_1 - t_2)$, V_{gs} remains stable and equal to V_{dd}. To turn off the switch, the driver commutates the output to $V_{dd}/2$ at t_2 by using the same switching configuration of phase $(t_0 - t_1)$. In this interval, the voltage V_{gs} has an opposite commutation with respect to the $(t_0 - t_1)$ interval; as before, this interval lasts half of the resonance period. During the intervals $(t_0 - t_1)$ and $(t_2 - t_3)$ the current I_{Lres} has a sinusoidal shape with opposite signs as reported in Fig. 2.8. Using the same switch configuration in the two intervals, the gate charge extracted form the driver supply during $(t_0 - t_1)$ is restored in $(t_2 - t_3)$.

Thanks to the resonant operation, power losses of this driver are limited to the conduction losses associated with the gate current pulses. The total resistance on the driver path is

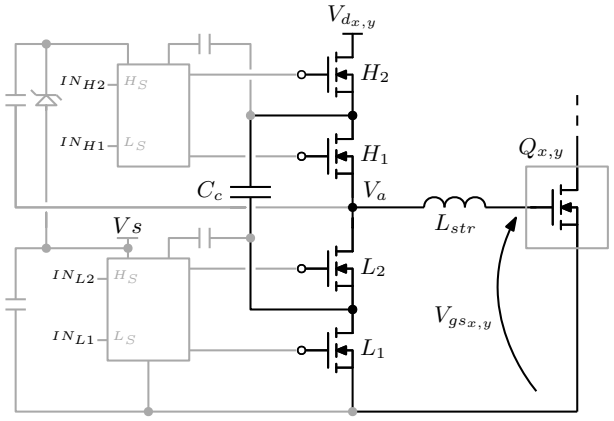


Fig. 2.7 Single driver circuit. $Q_{x,y}$ represents a power FET array.

composed of the parasitic resistance of C_C, the R_{dsON} of the FETs $H_{1,2}$ and $L_{1,2}$ of Fig. 2.7, the gate resistance of the power FETs and finally the strip resistance.

$$R_{driving} = ESR_{C_c} + 2R_{dsON} + R_{strip} \tag{2.5}$$

Considering the waveforms reported in Fig. 2.8, the inductor peak current can be approximated as

$$\max|I_L| = \frac{Q_g}{T_{cc}}\pi N \tag{2.6}$$

where Q_g represents the gate charge of a single FET, N is the number of FETs connected in parallel and T_{cc} is the resonance period of the driving structure. The total losses of the driver can be derived easily from (2.5) and (2.6).

$$P_{loss} = \left(\frac{Q_g}{T_{cc}}\pi N\right)^2 \frac{R_{driving}}{2}\frac{T_{cc}}{T_{sw}} = \frac{R_{driving}}{2}\frac{f_{cc}}{T_{sw}} {Q_g}^2\ \pi^2\ N^2 \tag{2.7}$$

The actual duration of the resonance and the value of the trace inductance L_{str} will be further discussed in Section 2.5.

It is clear that, in order for this driving technique to be effective, some criteria must be satisfied. First of all, the resonance path composed by the total gate capacitance and the stray inductance must have a high quality factor, which means that this solution is not feasible for integrated inductors, which are intrinsically characterized by *low-Qs*. In addition, turn-on/off

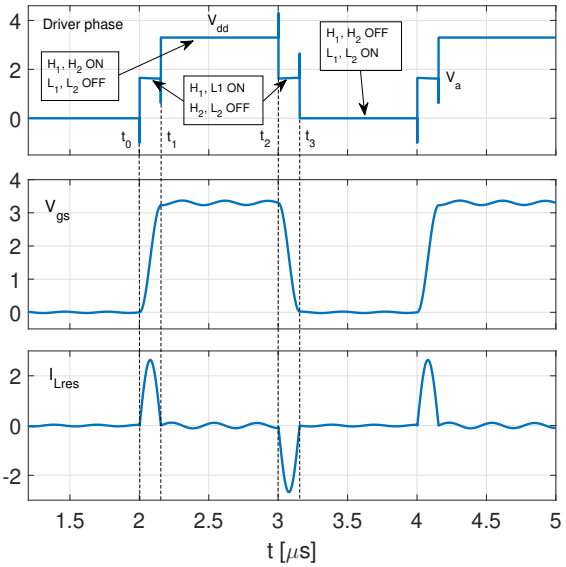


Fig. 2.8 Circuit-level simulation of the driver operation.

intervals are increased with respect to classical drivers, as a bigger series inductance is required and engineered to enable *high-Q* resonance: this means that ZVS/ZCD topologies are more suited for this applications, as hard-switched devices would experience unacceptable switching losses.

2.4 Impedance model

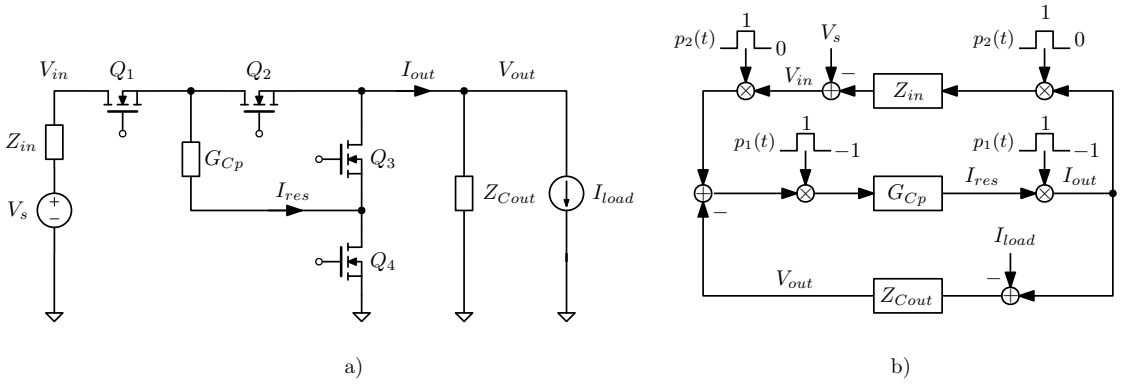


Fig. 2.9 Equivalent SC converter schematic (a) and block diagram with modulation signals (b).

A generic switched-capacitor block, such as the cell of Fig. 2.2 (a), can be described with a block scheme, as reported in Fig. 2.9 (a). Z_{in} represents the input impedance seen by the SC structure, G_{Cp} is the admittance of the SC structure (composed of the capacitor and the other parasitic components) and Z_{Cout} is the impedance of the output capacitor. $I_{load}(t)$ denotes the load current, while $V_S(t)$ is the input voltage[2]. Load current is considered the input signal of the model, while $V_{out}(t)$ and $I_{res}(t)$ (current in the switched capacitor) are considered system outputs. $I_{out}(t)$ is the SC rectified output current, that is divided between the load current and the output capacitors. In Fig. 2.9 (b) the equivalent block diagram of the SC converter is reported, where multipliers are used with square-wave signals in order to model the switching behavior of the architecture. Transfer functions can be determined through the injection of a sinusoidal input and measuring the harmonic contribution detected at the output of a generic path, at the same input frequency.

Mathematically, the relation mappping an input ($I_{load}(t)$) to an output signal (e.g., $V_{out}(t)$, $I_{res}(t)$, etc.) for this kind of dynamic system can be described as a Linear Time Periodic (LTP) map with *switching* frequency F_{sw} [42, 43]. In fact, all the signal transformations in the scheme are linear, including the square-wave modulators, and a time shift of an input by an amount kT_{sw}, $T_{sw} = 1/F_{sw}$ will determine an equal shift of the output, due to the period T_{sw} of the square-waves and to the time-invariance of blocks Z_{in}, G_{cp}, Z_{Cout}. In general, it is possible to show [42, 43] that the output $y(t)$ of an LTP system, with frequency F_{sw}, excited with an input signal in the form

$$x(t) = \sum_k x_k \, e^{j2\pi(f_0 + kF_{sw})t}$$

has indeed the same form:

$$y(t) = \sum_k y_k \, e^{j2\pi(f_0 + kF_{sw})t} \tag{2.8}$$

It can be seen that, in general, there is a *one-to-many* map between complex exponentials at the input and harmonics at the output. In particular, even if $x(t)$ is a single harmonic $x(t) = x_0 \, e^{j2\pi f_0 t}$, we expect the output $y(t)$ to have the form of (2.8), potentially with an infinite number of harmonics.

In the general case, calculating the transfer functions of the scheme of Fig. 2.9 (b) is a complex problem, even considering a single frequency of evaluation. The feedback connection and the presence of two groups of square-wave modulators (one interacting with G_{cp} and the other with Z_{in}) create a strong relationship between the high frequency signals in the loop and the evaluated output harmonic amplitude and phase.

[2] In this particular case, $V_S(t)$ corresponds to the time-averaged PWM voltage of the buck converter. In the following analysis it is considered stable, so its small-signal voltage is not considered.

In order to better understand the system behavior, we can at first consider $V_{out}(t)$ and $V_{in}(t)$ to be dominated by the harmonic component at the input signal frequency f_0, thus considering negligible Z_{Cout} and Z_{in} impedances at high frequency.

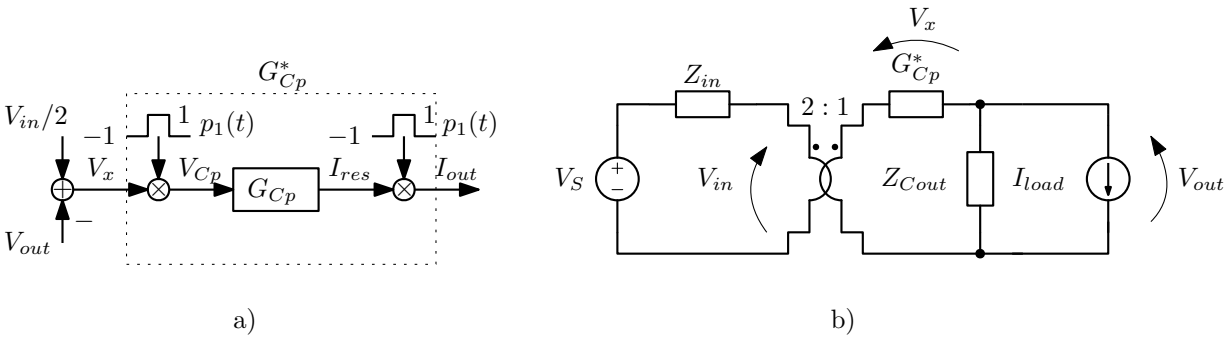


Fig. 2.10 Block diagram of the approximated impedance model.

2.4.1 Approximate model

Given the previous assumption, the transfer function within the modulators involving the admittance G_{C_p} can be analyzed separately with a pure sinusoidal input signal, as reported in Fig. 2.10 (a). The aim of this session is calculate the equivalent transfer function $G^*_{C_p}$ in order to describe the converter's dynamic with the linearized model reported in Fig. 2.10 (b).

We assume therefore a purely sinusoidal input $V_x(t) = V_0\, e^{j2\pi f_0 t}$, with generalized Fourier transform $V_x(f) = V_0\, \delta(f - f_0)$. The square wave $p_1(t)$ of Fig. 2.10 (a) can be expressed as[3]

$$p_1(t) = 2\sum_k \text{rect}\left(\frac{2(t - T_{sw}k)}{T_{sw}}\right) - 1. \tag{2.9}$$

The Fourier transform of the periodic signal $p_1(t)$ is the sum of an infinite number of harmonics, namely

$$P_1(f) = \sum_k p_{1,k}\, \delta(f - kF_{sw}), \tag{2.10}$$

where $F_{sw} = 1/T_{sw}$ and[4]

$$p_{1,k} = \begin{cases} 0, & k = 0, \\ \text{sinc}(k/2), & k \neq 0. \end{cases} \tag{2.11}$$

[3] $\text{rect}(t) = 1$ for $|t| < 0.5$ and 0 elsewhere.

[4] $\text{sinc}(t) = \sin(\pi t)/(\pi t)$, $\text{sinc}(0) \triangleq 1$.

Multiplication of $V_x(t)$ by $p_1(t)$, namely $V_{C_p}(t) = V_x(t)p_1(t)$, corresponds to a convolution in the frequency domain, so that

$$V_{C_p}(f) = V_0 \sum_k p_{1,k}\, \delta(f - f_0 - kF_{sw}). \tag{2.12}$$

After the $G_{C_p}(f)$ block a current signal is obtained, with Fourier transform

$$I_{res}(f) = V_{C_p}(f)G_{C_p}(f) = V_0 \sum_k p_{1,k} G_{C_p}(f_0 + kF_{sw})\, \delta(f - f_0 - kF_{sw}).$$

Finally another multiplication with $p_1(t)$ generates, in the frequency domain, the convolution result

$$\begin{aligned} I_{out}(f) &= \sum_h p_{1,h} I_{res}(f - hF_{sw}) \\ &= V_0 \sum_h \sum_k p_{1,h}\, p_{1,k} G_{C_p}(f_0 + kF_{sw})\, \delta(f - f_0 - hF_{sw} - kF_{sw}) \\ &= V_0 \sum_h \tilde{p}_{1,h}\, \delta(f - f_0 - hF_{sw}), \end{aligned} \tag{2.13}$$

where

$$\tilde{p}_{1,h} = \sum_k p_{1,h-k} p_{1,k} G_{C_p}(f_0 + kF_{sw}).$$

As expected, there is a one-to-many correspondance between the single harmonic input and the infinite number of harmonics at the output, due to the fact that the input-output relation is described by an LPT system with frequency F_{sw}.

In particular, we are interested in the harmonic at the same frequency f_0 of the input, in order to evaluate the equivalent admittance (note that $p_{1,k} = p_{1,-k}$)

$$G^*_{C_p} = \tilde{p}_{1,0} = \sum_k p^2_{1,k}\, G_{C_p}(f_0 + kF_{sw}). \tag{2.14}$$

Special case 1. Suppose $f_0 = 0$ (DC analysis) and that $G_{C_p}(kF_{sw})$ in (2.14) is negligible for $|k| > 1$, i.e., at high frequencies. Moreover, suppose[5] $G_{C_p}(\pm F_{sw}) = 1/R_{cell}$. From (2.14) we obtain

$$G^*_{C_p} = 2\, p^2_{1,1}/R_{cell} = \frac{8}{\pi^2 R_{cell}},$$

which is consistent with (2.2).

[5]This assumption holds if the converter is operated at the correct resonant frequency of the SC structure.

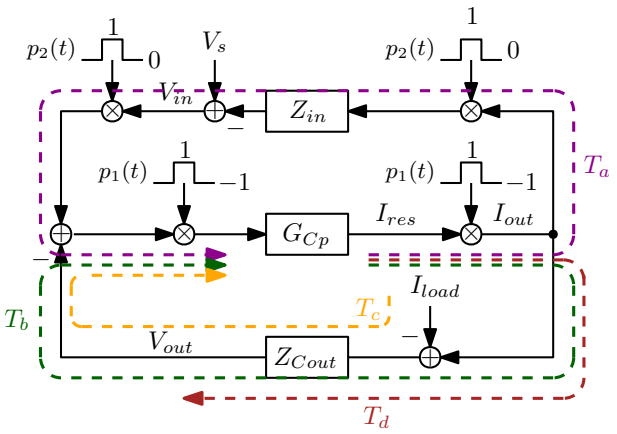


Fig. 2.11 Block diagram with modulation signals and operator paths.

Special case 2. Suppose again $f_0 = 0$, and that $G_{C_p}(f)$ corresponds to a real capacitor with capacitance C_p and resistance R, i.e.,

$$G_{C_p}(f) = \frac{j2\pi f C_p}{1 + j2\pi f R C_p}.$$

From (2.14) we can write (recall $p_{1,k}^2 = \text{sinc}^2(k/2) = 4/(k^2\pi^2)$ for k odd, and 0 elsewhere)

$$\begin{aligned} G_{C_p}^* &= \sum_k p_{1,k}^2 \frac{j2\pi k F_{sw} C_p}{1 + j2\pi k F_{sw} R C_p} \\ &= 2Re\left[\sum_{k=1}^{+\infty} p_{1,k}^2 \frac{j2\pi k F_{sw} C_p}{1 + j2\pi k F_{sw} R C_p}\right] \\ &= 4F_{sw}C_p \sum_{k=0}^{+\infty} \frac{8F_{sw}RC_p}{1 + 4\pi^2(2k+1)^2 F_{sw}^2 R^2 C_p^2}. \end{aligned} \tag{2.15}$$

Placing $\Delta x = 4F_{sw}RC_p$, for $F_{sw}RC_p \ll 1$, we can approximate the summation in (2.15) as an integral[6]

$$2\sum_{k=0}^{+\infty} \frac{\Delta x}{1 + \pi^2(\Delta x/2 + k\Delta x)^2} \simeq 2\int_0^{+\infty} \frac{1}{1 + \pi^2 x^2} dx = 1.$$

Thus,

$$G_{C_p}^* \simeq 4F_{sw}C_p.$$

2.4.2 Detailed model

The aim of this section is to characterize the output $V_{out}(t)$ when a sinusoidal signal $I_{load}(t) = I_0 e^{j2\pi f_0 t}$ is fed to the system, which is precisely the shape of the output impedance. Analysis will be developed following the references of Fig. 2.11.

As discussed above, there is in general a one-to-many map between input and output harmonics of a generic system block. For this reason, the injection of $I_{load}(f) = I_0 \delta(f - f_0)$ generates internal signals composed of an infinite number of harmonics. In particular:

$$I_{res}(f) = \sum_k i_k \delta(f - f_0 - kF_{sw}), \tag{2.16}$$

$$V_{out}(f) = \sum_k v_k \delta(f - f_0 - kF_{sw}). \tag{2.17}$$

The system can be described by the following relationships in the frequency domain:

$$\begin{cases} I_{res}(f) = G_{Cp}(f)(T_a[I_{res}(f)] + T_b[I_{res}(f)] + T_c[I_{load}(f)]) \\ V_{out}(f) = T_d[I_{res}(f)] - Z_{Cout}(f) I_{load}(f) \end{cases} \tag{2.18}$$

In (2.18), operators $T_n[X(f)]$ denote the frequency-domain relation between an input signal $X(f)$ with a spectrum

$$X(f) = \sum_k x_k \delta(f - f_0 - kF_{sw})$$

and the generated harmonics at the end of the corresponding path, as reported in Fig. 2.11.

In the following analysis, the first equation in (2.18) will be used to write an (infinite) linear system of equations for the unknown complex gains i_k of (2.16), while the second one will allow to evaluate the complex gains v_k of (2.17), and eventually the output impedance $Z_{out}(f_0) = v_0/I_0$.

Analysis of $T_a[I_{res}(f)]$

$I_{res}(f)$ crosses, on the path T_a, multiplicators p_1 and p_2 (twice). As $p_2 = 0$ when $p_1 = -1$, this last one is transparent and the modulator considered is p_2 alone: the square wave

$$p_2(t) = \sum_k \text{rect} \frac{2(t - kT_{sw})}{T_{sw}}$$

[6] This result can be derived considering the integral as a summation limit, with the Riemann approach, which states that $\int_a^b f(x)dx = \lim_{n\to+\infty} \sum_{i=0}^{n-1} f(x_i)\Delta x$, where $\Delta x = (b-a)/n$, $x_i = a + \Delta x/2 + i\Delta x$.

has Fourier transform

$$P_2(f) = \sum_k p_{2,k}\,\delta(f - kF_{sw}),$$

where $p_{2,k} = 0.5\,\mathrm{sinc}(k/2)$. Multiplication of $I_{res}(t)$ by $p_2(t)$, namely $I_a(t) = I_{res}(t)p_2(t)$, corresponds to a convolution in the frequency domain. As $I_{res}(f) = \sum_k i_k\,\delta(f - f_0 - kF_{sw})$, we obtain

$$\begin{aligned} I_a(f) &= \sum_h p_{2,h} \sum_k i_k\,\delta(f - f_0 - hF_{sw} - kF_{sw}) \\ &= \sum_k i_k \sum_h p_{2,h-k}\,\delta(f - f_0 - hF_{sw}). \end{aligned} \tag{2.19}$$

At the output of the $Z_{in}(f)$ block a voltage signal is obtained, with the following Fourier transform:

$$V_a(f) = \sum_k i_k \sum_h p_{2,h-k}\,Z_{in}(f_0 + hF_{sw})\,\delta(f - f_0 - hF_{sw}).$$

Finally, the second multiplication with $p_2(t)$ and the *minus sign* yields the output

$$\begin{aligned} T_a[I_{res}(f)] &= -\sum_k i_k \sum_m \sum_h p_{2,m}\,p_{2,h-k} Z_{in}(f_0 + hF_{sw})\,\delta(f - f_0 - hF_{sw} - mF_{sw}) \\ &= -\sum_k i_k \sum_h \tilde{p}_{2,h,k}\,\delta(f - f_0 - hF_{sw}), \end{aligned} \tag{2.20}$$

where

$$\tilde{p}_{2,h,k} = \sum_m p_{2,m} p_{2,h-m-k} Z_{in}(f_0 + hF_{sw} - mF_{sw}).$$

Analysis of $T_b[I_{res}(f)]$

The square wave $p_1(t)$ was already analyzed in Section 2.4.1, its Fourier transform is

$$P_1(f) = \sum_k p_{1,k}\,\delta(f - kF_{sw}),$$

where $p_{1,k}$ was defined in (2.11) and $F_{sw} = 1/T_{sw}$. According to the scheme of Fig. 2.11, the analysis of $T_b[I_{res}(f)]$ is formally identical to the one of $T_a[I_{res}(f)]$, once we replace Z_{in} with Z_{Cout} and $p_{2,k}$ with $p_{1,k}$. We can write therefore

$$T_b[I_{res}(f)] = -\sum_k i_k \sum_h \tilde{p}_{1,h,k}\,\delta(f - f_0 - hF_{sw}), \tag{2.21}$$

where

$$\tilde{p}_{1,h,k} = \sum_m p_{1,m} p_{1,h-m-k} Z_{Cout}(f_0 + hF_{sw} - mF_{sw}).$$

Analysis of $T_c[I_{load}(f)]$

With $I_{load}(f) = I_0\,\delta(f - f_0)$, the output of the impedance block $Z_{Cout}(f)$ is the complex exponential $-I_0 Z_{Cout}(f_0)\delta(f - f_0)$, and after the multiplication with $p_1(t)$ and by -1, we obtain:

$$T_c[I_{load}(f)] = I_0 Z_{Cout}(f_0) \sum_h p_{1,h}\delta(f - f_0 - hF_{sw}).$$

Analysis of $T_d[I_{res}(f)]$ and V(out)

With $I_{res}(f) = \sum_k i_k \delta(f - f_0 - kF_{sw})$, after the multiplication with $p_1(t)$, we obtain current $I_d(t)$ with Fourier Transform

$$\begin{aligned} I_d(f) &= \sum_h p_{1,h} \sum_k i_k\,\delta(f - f_0 - hF_{sw} - kF_{sw}) \\ &= \sum_k i_k \sum_h p_{1,h-k}\,\delta(f - f_0 - hF_{sw}). \end{aligned} \tag{2.22}$$

At the output of $Z_{Cout}(f)$, we obtain

$$T_d[I_{res}(f)] = \sum_k i_k \sum_h p_{1,h-k} Z_{Cout}(f_0 + hF_{sw})\,\delta(f - f_0 - hF_{sw}) \tag{2.23}$$

Moreover, according to the second equation in (2.18), the output voltage is

$$\begin{aligned} V_{out}(f) &= \sum_k i_k \sum_h p_{1,h-k} Z_{Cout}(f_0 + hF_{sw})\,\delta(f - f_0 - hF_{sw}) - I_0 Z_{Cout}(f_0)\,\delta(f - f_0) \\ &= \sum_h v_h\,\delta(f - f_0 - hF_{sw}). \end{aligned} \tag{2.24}$$

In particular, as $p_{1,k} = p_{1,-k}$,

$$v_0 = Z_{Cout}(f_0)\left(\sum_k i_k p_{1,k} - I_0\right). \tag{2.25}$$

Determining the complex gains i_k

In order to compute (2.24), (2.25), complex gains i_k must be explicitly calculated. Harmonic components on the left and right side of the first equation of system (2.18) can be equated,

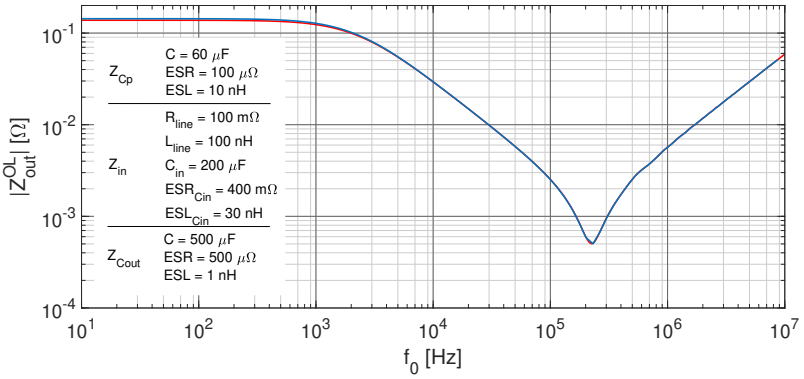


Fig. 2.12 Output impedance $|Z_{out}(f_0)| = |v_0/I_0|$ of a generic SC converter (characterized by the reported parameters) obtained by solving (2.26) with $h,k \in [-20,20]$, $\tilde{p}_{1,h,k}$ and $\tilde{p}_{2,h,k}$ truncated with sum index $m \in [-1000,1000]$ (blue) and with AC circuit-level simulation (red). $F_{sw} = 320$ kHz.

obtaining an infinite set of equations:

$$i_h = G_{Cp}(f_0 + hF_{sw}) \left(-\sum_k i_k \left(\tilde{p}_{1,h,k} + \tilde{p}_{2,h,k}\right) + I_0 Z_{Cout}(f_0)\, p_{1,h} \right). \tag{2.26}$$

To numerically solve system (2.26), it must be truncated to a finite number of unknowns i_k. Moreover, coefficients $\tilde{p}_{i,h,k}$ must also be computed by approximating the summations to a finite range.

The estimated output impedance $|Z_{out}(f_0)| = |v_0/I_0|$ for a random SC converter is reported in Fig. 2.12, where system (2.26) was evaluated at different load-current frequencies f_0. Note that the parameters reported in Fig. 2.12 are not the ones of the real prototype: this choice was made to demonstrate the efficacy of this modeling approach in a generic and different case; the same calculation is repeated for the real prototype in Section 2.5. The circuit-level AC analysis is also reported for comparison.

2.4.3 Multi-phase generalization

Results derived in this section can be extended to a multi-phase switched-capacitor architecture. As input/output current is split among N phase-shifted structures, the equivalent dynamic system becomes the one of Fig 2.13.

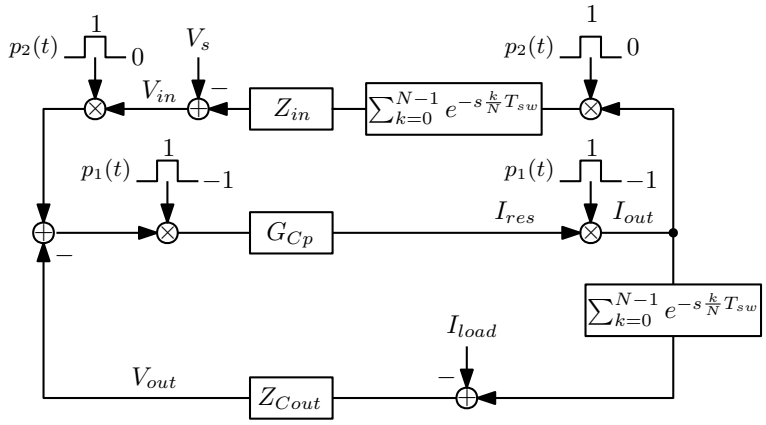


Fig. 2.13 Equivalent multi-phase SC converter block diagram with modulation signals and time-delay blocks.

2.5 Experimental Results

A 10-layers prototype PCB was built in order to demonstrate the effectiveness of the solution. Table 2.1 summarizes the main specifications of the prototype. The first stage was implemented through a multi-phase VRM buck.

Table 2.1 Converter and PCB specifications.

$V_{in,nom}$	1.6 V
$V_{out,nom}$	0.8 V
$I_{out,max}$	300 A
f_{sw}	500 kHz
PCB power area	2×50 mm $\times 10$ mm
PCB layer count	10
PCB copper weight	70 μm
MOSFETs (power + driving)	Intersil KGF20N05D (160 + 32)
Switched capacitors C_p	120×22 μF, 0402 (GRM155Z80E226M)
Input capacitors C_{in}	22×330 μF, 1210 (AMK325ABJ337MM)
	40×1 μF, 0201 (GRM033D70E105ME15)
Output capacitors C_{out}	80×22 μF, 0402 (GRM155Z80E226M)
	48×0.47 μF, 0204 (LLL153C70G474ME17)

Prototype efficiency was measured with precision current shunt resistors and is reported in Fig. 2.15. The power converter, neglecting driving losses, has a 98.8% measured peak efficiency. With an overall driving current of only 150 mA at 3.3 V (0.495 W), the measured total peak efficiency is 97%.

As this converter is characterized by high efficiency and high output current, efficiency calculation can be affected by considerable uncertainty: this is usually caused by errors on

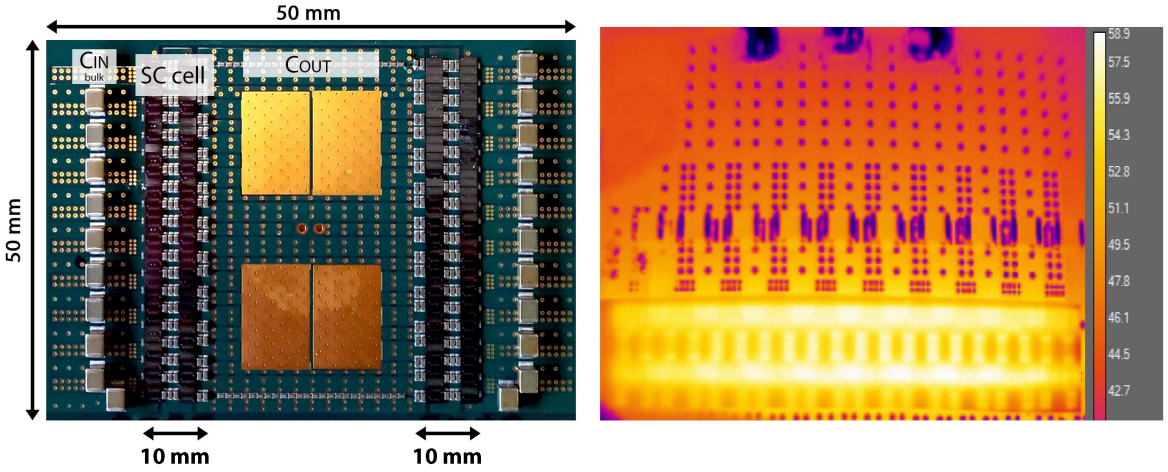


Fig. 2.14 Power stage on the PCB prototype (a) and thermal image at I_{load} = 150 A (b).

current measurements, especially when shunt resistors are used. For this reason, a custom setup was built to decrease current measurement uncertainty, which is composed of two copper shunt resistors (one for the input, one for the output) submerged in a common distilled water bath. At first, shunt resistors are connected in series and a test current is injected, then the resistance ratio is calculated by diving the two measured voltages. During converter operation, as the water bath ensures equal temperature for both resistors, the efficiency can be directly calculated by measuring the ratio between the two shunt voltages, and together measuring the converter input and output voltage, which can be done with great accuracy.

Without the resonant driver, driving losses would be as high as:

$$P_{driving}^{standard} = Q_{gate} V_{drive} f_{sw} N_{mos,tot} \simeq 1.56\,W \tag{2.27}$$

as Q_{gate} for KGF20N05D is 5.91 nC (V_{gs} = 3.3 V, ZVS commutation), V_{drive} = 3.3 V and $N_{mos,tot}$ = 160.

Driving waveforms can be observed in Fig. 2.16, where gate-source voltages are reported for phase 1. The resonant driving interval is set to 160 ns, which is needed to drive a total gate capacitance of 36.8 nF (each driver is in fact connected to 20 power FETs, each one with a C_{iss} = 1.84 nF) with a layout inductance of about about 70 nH. This value is justified by the long gate/source traces that connect the FET arrays to the driver output, which have a minimal length of 50 mm. The layout inductance was predicted in SIwave and used to calculate the resonance duration. As the long traces could lead to radiated and/or conducted noise, layout must be appropriately designed. In order to ensure proper operation, the driving traces were enclosed among power-ground planes. Besides, gate and source traces were

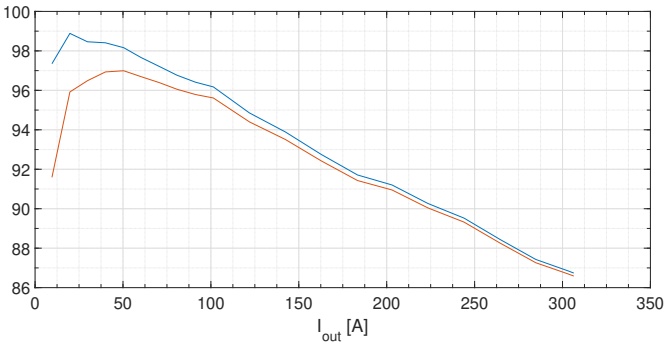


Fig. 2.15 Measured converter efficiency with driving losses (red) and without driving losses (blue) for the SC stage. V_{out} = 0.8 V.

designed on adjacent layers; therefore, EM fields are confined in the space among them as in a micro-strip transmission line. Nearby net coupling and radiated energy, which is mainly addressed by this two techniques, is also minimized by the low-frequency content of the gate current shape. In fact, as the driving technique is resonant, current spectrum does not contain high-frequency harmonics that would appear in a classic square-wave driving approach, especially when low gate resistance is required.

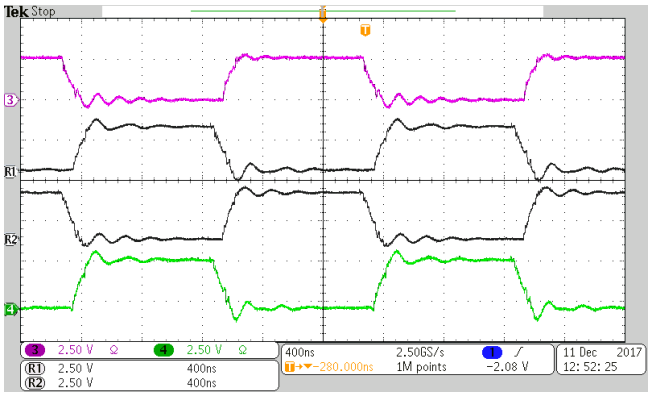


Fig. 2.16 Measured V_{gs} voltages of MOSFET columns for a single phase. Considering Fig. 2.6, signals corresponds to $Q_{1,1} \rightarrow Q_{4,1}$ in descending order.

Voltage waveforms measured on a single switched-capacitor cell are shown in Fig. 2.19 with 100 A output current, where the resonant operation of the SC converter is demonstrated: observing the voltage ripple V_{cp} on the switched capacitors it is noticeable that the commutations happen on the peak of the sinusoidal curve, i.e., when the tank current I_{res} is zero. This behavior can also be observed probing the V_{out} ripple, which shows that the commutations appear when the voltage is zero and evolves at $2 \cdot f_{sw}$: this is compatible with a rectified purely sinusoidal current (I_{out} in Fig. 2.19) entering the output capacitors. Also in Fig. 2.19,

the V'_{in} measurement shows the effects of the impedance between the SC stage and the VRM board.

The active-load tool (DLT100AGEVB, ON Semiconductor) allowed to directly measure the output open-loop impedance in a wide frequency range, validating the theoretical model discussed in Section 2.2. The measurement setup is shown in Fig. 2.17, where the output impedance is directly calculated as a transfer function through the active-load tool. The resulting measured output impedance is reported in Fig. 2.18. Z_{out} depends on the converter's SC impedance, a minimum value of $|Z_{out,min}| \simeq 411\ \mu\Omega$ is measured, coherently with (2.2) and the circuit-level simulation. It is important to notice that the low-frequency mismatch between the two curves is due to the selection of a higher tank parasitic resistance for this simulation, which better approximates high-frequency proximity effects in the range of interest. In this experiment the prototype was powered through a high-current buck-type VRM board: input impedance Z_{in} used in the calculations is therefore composed of the output impedance of the VRM board, the physical connection to the prototype and the input capacitors on the prototype. This quantity was previously measured with the same load tool. Z_{Cin}, Z_{Cp} and Z_{Cout} were extracted from the SPICE models of the mounted components and combined with RF layout analysis. As a consequence, these impedances are actually expressed as functions of the frequency and can only be approximated with lumped models, which is why the lumped parameters associated to the real converter are not reported.

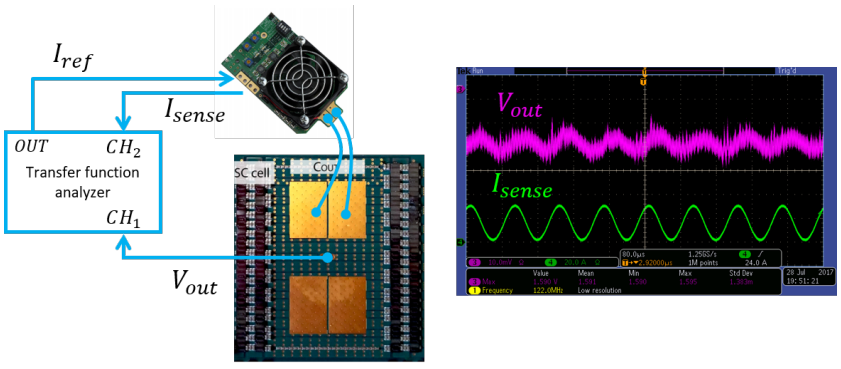


Fig. 2.17 Output impedance measurement setup and input signals waveforms.

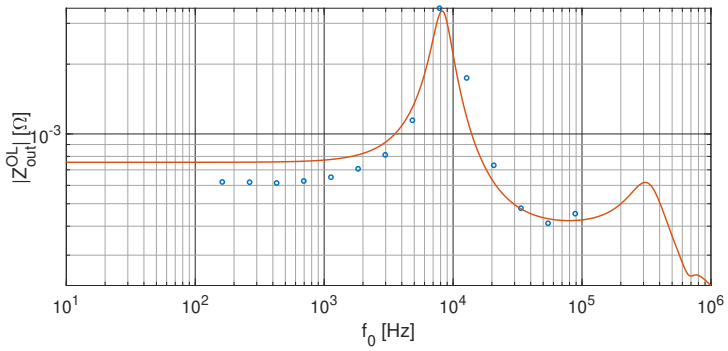


Fig. 2.18 Open-loop output impedance $|Z_{out}^{open}(f_0)| = |v_0/I_0|$ calculated with (2.25) (2.26) (red line) and measured with active load tool (blue dots).

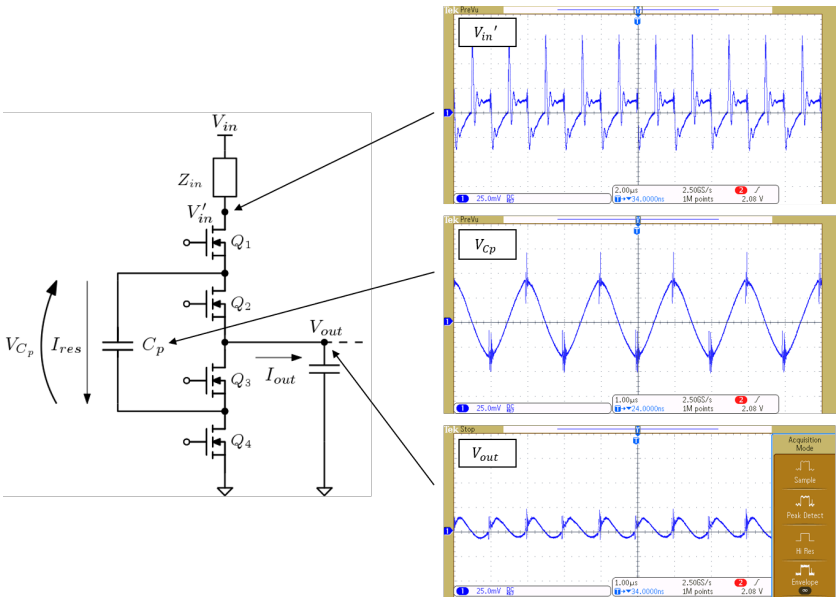


Fig. 2.19 Converter waveforms measured with differential probe, AC coupled. This image demonstrates the resonant operation of the converter and the effects of the input impedance Z_{in} on the SC cell input voltage. I_{load} = 100 A.

2.6 Conclusions

In this chapter the core-voltage-domain conversion issues were analyzed and an on-package conversion system based on resonant switched capacitors for high current (up to 300 A) low voltage (0.8 V) digital ASICs, in an area of 10 cm^2. Experimental results confirm the effectiveness of the solution with a 98.8 % peak efficiency and a very small driving current (150 mA at 3.3 V) that makes the new proposed resonant driver a reasonable choice for this type of converter. A novel mathematical approach for the study of the state variables of a generic SC converter was proposed, adding the input/output impedances to the overall Z_{out} calculation. The researched algorithm enables the usage of *arbitrary transfer functions* to model the complete system and can be used to compute important figures of merit, such as the detailed shape of the output impedance. This result is of paramount importance as, until now, there was no method to merge the various contributions of the SC converter blocks to the output impedance, therefore a wide-spectrum calculation could not be performed. The proposed algorithm not only enables this, but can also be used with layout-simulation-outputs, i.e., complex values defined for each frequency point. The direct measurement of Z_{out} confirmed the predictions of the theoretical model for this prototype. In conclusion, this approach allows a consistent selection of the control loop and a deep knowledge of the system performances. As the output impedance can now be calculated for an arbitrary frequency range, load transient responses are now fully predictable.

It's important to notice that this analysis is feasible for an arbitrary switched-structure architecture.

This solution has been presented at APEC 2018, while the mathematical model has ben published on *IEEE Journal of Emerging and Selected Topics in Power Electronics* [44, 45].

Chapter 3

Unregulated Resonant non-isolated IBCs from the 48 V bus

The intermediate voltage conversion from the 48 V to lower bus voltages of 5 V ÷ 12 V is presented in this chapter with two different unregulated converters. These solutions are derived from the Google Switched Tank Converters family [20]: the first converter achieves the 48 V to 12 V conversion, i.e. $V_{in}/4$, while the second one yields two separated output rails of 4.8 V and 9.6 V, i.e. $V_{in}/10$ and $V_{in}/5$, always from a 48 V input. The provided results prove the effectiveness and adaptability of the STC converters used in conjunction with a transformer to achieve different conversion ratios with very high efficiency.

3.1 Introduction

LLC resonant converters are widely used as IBCs (intermediate bus converters), this topology achieves ZVS in the whole operating range, have low turn-off current for primary side switches and ZCS for the synchronous rectifier devices [46, 47]. For increased efficiency, GaN devices can be used in the same structure. If the isolation is not required, a conversion based on resonant STC (switched tank converters) can be effectively adopted as already reported in [20]. These topologies are based on the composition of switched capacitors cells and resonant tanks built with off-the-Shelf devices without requiring custom magnetic components. In fact, magnetic component design and integration is the greatest challenge for system optimization and often defines the system efficiency and power density. Moreover, a huge customization effort can increase cost and reduces the time to market. On the other hand, switched capacitor topologies obtain the best performance by adopting matched resonant tanks, with the R_{ac} of the inductor representing the only bottleneck for high frequency opera-

tion. This problem doesn't occur with traditional topologies like LLC resonant converters, which can operate at high frequencies without losing efficiency, as transformers with a high coupling allow for a better current density distribution at high frequency, i.e. lower R_{ac}.

In this chapter a different approach is proposed for high density fixed-ratio conversion topologies, which successfully combines the advantages of the STC capacitor cells and the LLC resonant converters. These topologies still use transformers but reduce the design constraints for their development by adopting STC cells. As this new kind of converters combine these two elements, the *STC-TX* name was chosen.

The converter family here described can be derived from hybrid switched-capacitor step-down topologies operating with a soft charging mechanism by transforming them into unregulated, resonant converters capable of ZVS and/or ZCD commutations. There are many hybrid converter types in which capacitors are charged/discharged by the inductor current, as this behaviour improves conversion efficiency by reducing capacitor RMS current. The simpler converter characterized by soft-switching operation is the *Series Capacitor Buck converter* [48], but many others can be obtained by stacking soft-switched capacitors [49, 50]. The *Series Capacitor Buck converter* can be simply transformed into its ZVS/ZCD-enabled counterpart by coupling the phase inductors and fixing the duty-cycle at 50 %, obtaining the converter reported in Fig. 3.1.

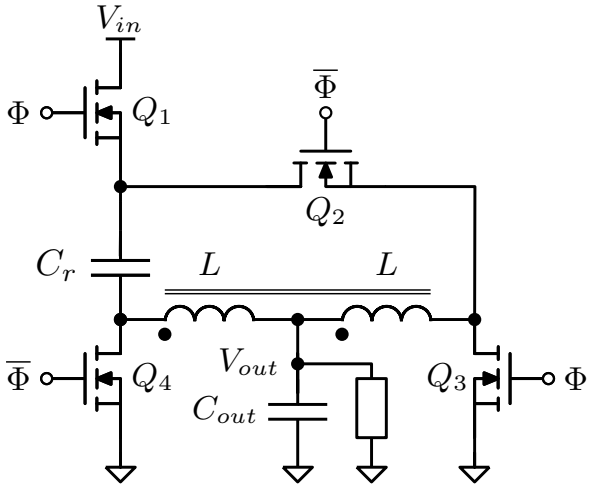


Fig. 3.1 Series capacitor buck converter configured as a fixed ratio non isolated DC-DC converter.

By using a high-coupling factor, the converter loses the regulation capability but its power density can be improved. In fact, with a duty cycle lower than 50 %, the RMS current in each phase increases, thus the converter can not work at different duty cycles without having a large power dissipation. Considering the magnetic core, the DC flux density associated

with the output current is cancelled, hence the equivalent area of the magnetic core A_e does not depend on the maximum output current but only on the output voltage and the switching frequency. Hence, only the winding area of the transformer A_w is bound to the maximum acceptable conduction losses, which depend on the output current I_{out}. This reasonably reduces the total A_eA_w product for a given output power. As it will be discussed in the next section, this converter can be operated at the resonant frequency between the leakage inductor L_k and the capacitor C_r. Moreover, at this frequency the magnetizing inductance of the transformer L_m can guarantee ZVS conditions for all the switches.

Compared to the traditional LLC solutions, this converter can guarantee a better usage of the transformer winding area A_w. In fact, the windings required for this solution are the same of an equivalent center-tapped secondary LLC converter transformer. On the other hand, the LLC converter is an isolated converter and power flows into the transformer from the input port to the outputs ports, thus the remaining space available for the output windings potentially allows lower conduction losses for a given core. Compared to Switching Tanks Converters, this solution can be developed with less driving complexity and less R_{ac}, due to the better current distribution in the transformer with respect to the resonant inductor currents, but requiring a custom magnetic component. Similar approaches were described in some topologies [18], with the substantial difference that the resonance took place with the output capacitance C_{out}. In the proposed non-isolated topology the output capacitance is designed solely considering output impedance constraints, and its contribution to the resonance is negligible.

3.2 Dual-phase 4:1 STC-TX Converter

The topology described in this chapter, on which the prototype and experimental results are based on, is reported in Fig. 3.2. This is a double-phase switched capacitor buck converter that can adopt uncoupled (or with a low coupling factor) inductors as a double-phase buck converter. [1] Thanks to the double-phase operation, the capacitors C_{f_x} operate without hard-charging for duty-cycles less than 50% even if they close a mesh with the input voltage V_{in} during the phases in which $Q_{1,3}$ and $Q_{6,8}$ are turned on (or $Q_{2,4}$ and $Q_{5,7}$ are turned on). In these conditions the sum of the two capacitors voltages is always equal to the input voltage V_{in} and the RMS current that is flowing in the two flying capacitors depends only on the inductor currents. By using high-coupling inductors, as in the previous example, a fixed ratio DC-DC converter can be obtained with ZVS condition on all switches. Moreover, the

[1] This topology can also work in a single-phase configuration and it can regulate the output with a duty-cycle higher than 50%.

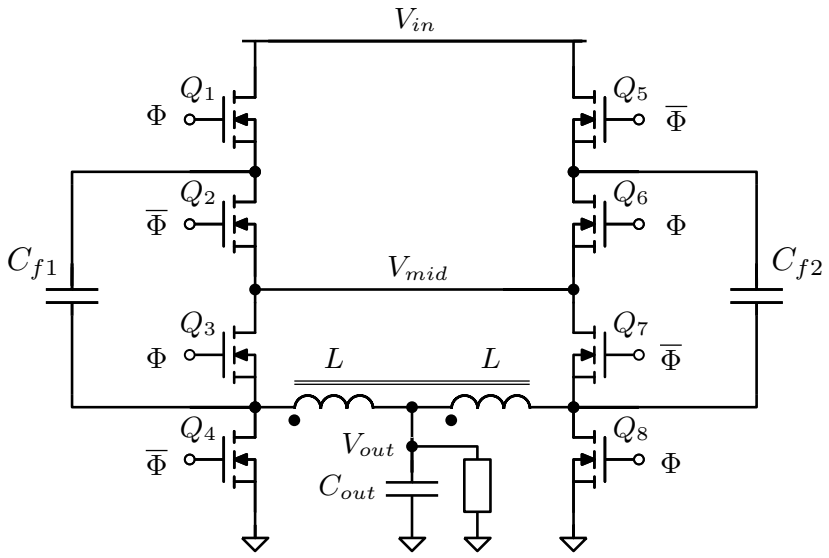


Fig. 3.2 Two-phases switched capacitor buck converter topology.

transformer operates with the same currents and voltages of the previous solution, and the total amount of capacitors required is the same because the second solution works with the parallel of the two flying capacitors. The main difference between the two topologies is the number and the voltage ratings of the switches. The first solution requires the Q_2 switch to be input-voltage-rated, instead the second solution works with all switches rated at $\frac{V_{in}}{2}$. Finally, the second solution has a very symmetric operation with respect to the second solution. In fact, considering the high coupling factor, the leakage inductor of the transformer L_k is very low, and it is comparable with the other layout parasitic inductors on the PCB. Moreover, the area of the converter is dominated by the transformer, hence the use of the second solution does not affect the power density.

3.2.1 Converter operation

The results of this section are related to the topology of Fig. 3.2; obviously equal results and methods can be applied to the converter of Fig. 3.1.

This converter is driven by two complementary signals with a fixed frequency and 50% duty-cycle, interrupted by a fixed dead-time T_d. Timings are shown in Fig. 3.5, while the two semi-periods switches configuration are reported in Fig. 3.4, where the dead-time phase is omitted.

From t_0 to t_1, the equivalent circuit is reported in Fig. 3.6; it consists of a resonant circuit constituted by the parallel of the two capacitors C_{f_1} and C_{f_2} and the leakage inductor L_k.

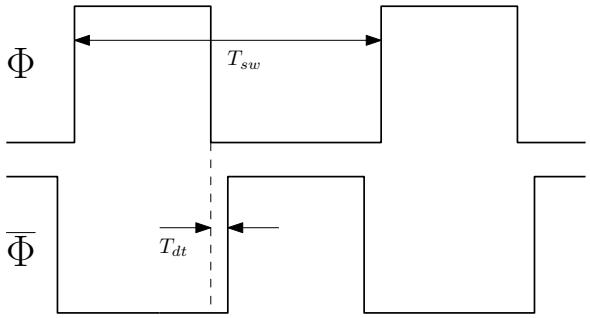


Fig. 3.3 Two-phases SC-buck converter control signals.

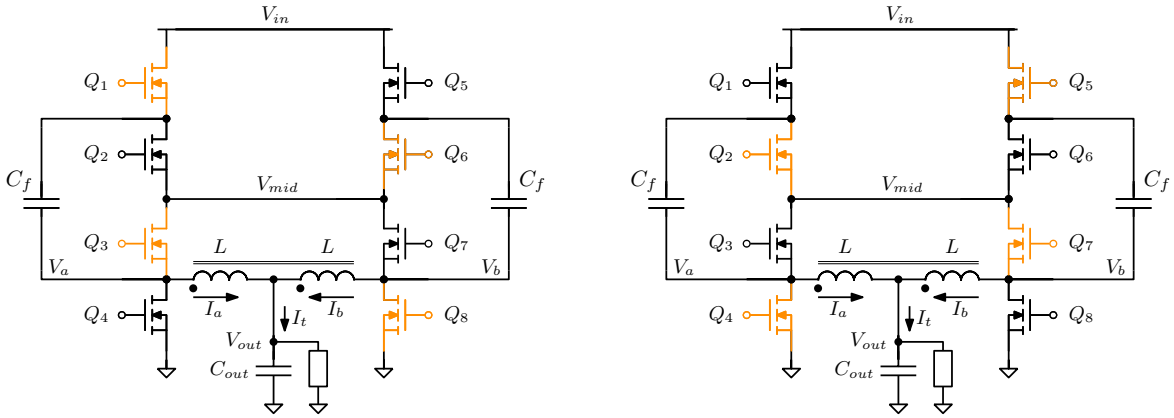


Fig. 3.4 Operation phases (t_0-t_1 and t_2-t_3) of the two-phases SC-buck converter.

Similarly, from t_2 to t_3 the equivalent circuit will be the same with I_a replaced by I_b and C_{f_1} replaced by C_{f_2}.

The current in the transformer winding I_a from t_0 to t_1 can be expressed as the sum of the resonant current I_r and the magnetizing current I_m:

$$I_a(t) = I_r(t) + I_m(t) = \frac{V_{C_r}(t_0) - 2V_{out}}{\sqrt{L_k/C_r}} \sin(\omega_r(t - t_0)) + I_m(t) \tag{3.1}$$

where $V_{C_r}(t_0)$ is the initial value of the capacitor voltage at the starting point of the commutation t_0 and $C_r = 2C_f$. Note that C_{out} does not contribute to the resonance as $C_{out} \gg C_r$, i.e. the output is considered to be an ideal voltage source. A similar result is obtained for the total current on the other terminal of the transformer:

$$I_b(t) = I_r(t) - I_m(t) = \frac{V_{C_r}(t_0) - 2V_{out}}{\sqrt{L_k/C_r}} \sin(\omega_r(t - t_0)) - I_m(t) \tag{3.2}$$

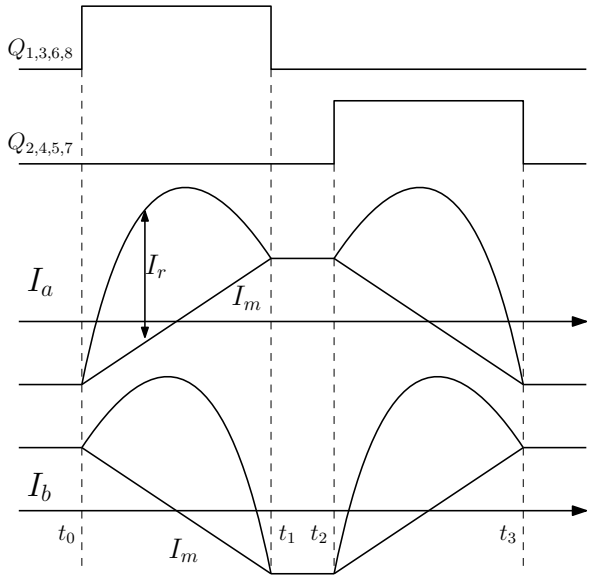


Fig. 3.5 Ideal waveforms of the two-phases SC-buck converter.

Hence the expression of the total current from t_0 to t_1 is

$$I_t(t) = I_a(t) + I_b(t) = 2\frac{V_{C_r}(t_0) - 2V_{out}}{\sqrt{L_k/C_r}} \sin(\omega_r(t - t_0)) \tag{3.3}$$

and the voltage $V_{C_r}(t)$ on the capacitor can be expressed as

$$V_C(t) = (V_C(t_0) - 2V_{out}) \cos(\omega_r(t - t_0)) + 2V_{out} \tag{3.4}$$

After the resonance transition, from equation (3.3) we can derive the value of the capacitor voltage

$$V_{C_r}(t_1) = -V_{C_r}(t_0) + 4V_{out} \tag{3.5}$$

During the dead time T_d from t_1 to t_2, capacitors $C_{f_{1,2}}$ hold the charge. In the next phase (t_2 to t_3) the capacitors C_{f_1} and C_{f_2} exchange. By considering the symmetry of operation for the two phases t_0 to t_1 and t_2 to t_3 we can conclude that, in steady state:

$$V_{C_r}(t_3) = V_{in} - V_{C_r}(t_1) = V_{C_r}(t_0) \tag{3.6}$$

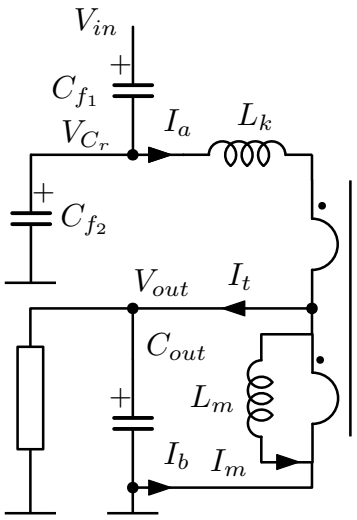


Fig. 3.6 Equivalent circuit of the converter during t_0 to t_1.

by substituting (3.6) into (3.5) we can conclude that

$$V_{in} = 4V_{out} \tag{3.7}$$

In this analysis an ideal resonant behaviour is considered during the phases from t_0 to t_1 and from t_2 to t_3. Considering the small values of the resonant inductor, that is dominated by the leakage inductor L_k in the real application, the total result is a dumped resonant current waveform as reported in the Fig. 3.7. As calculated in the previous analysis, the output current of the transformer I_t does not include the magnetizing current I_m used to obtain a ZVS condition on the switches. In fact, the resonant inductor L_k is too small to guarantee ZVS on the switches at light load.

Similar results can be obtained for the converter of Fig. 3.1, as there are no substantial differences in the resonant operation.

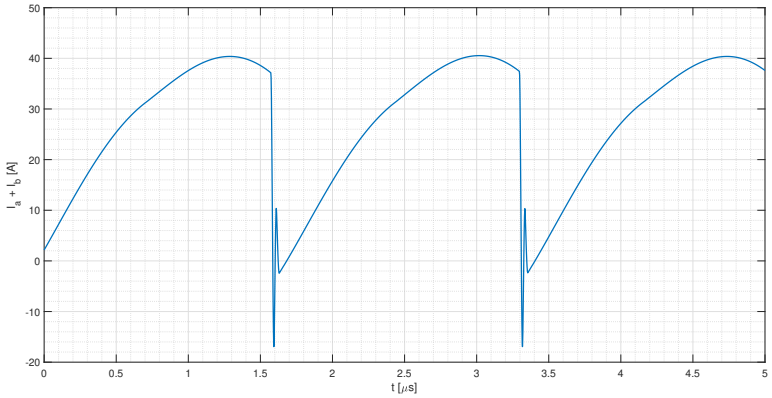


Fig. 3.7 Simulated transformer output current I_t at medium load condition (Simetrix).

3.2.2 Comparison with the LLC topology

In order to understand the proposed topology advantages, a comparison with an equivalent full-bridge LLC converter is proposed. The converter of Fig. 3.2 is therefore compared with the LLC of Fig. 3.8, the two implementing a 4:1 conversion with a given output voltage V_{out} and switching period T_{sw}.

This analysis also holds for the *Series capacitor buck converter* of Fig. 3.1, as transformer waveforms don't change. A similar approach can demonstrate the achievable volume reduction of the increased-conversion ratio solutions shown in Section 3.2.3.

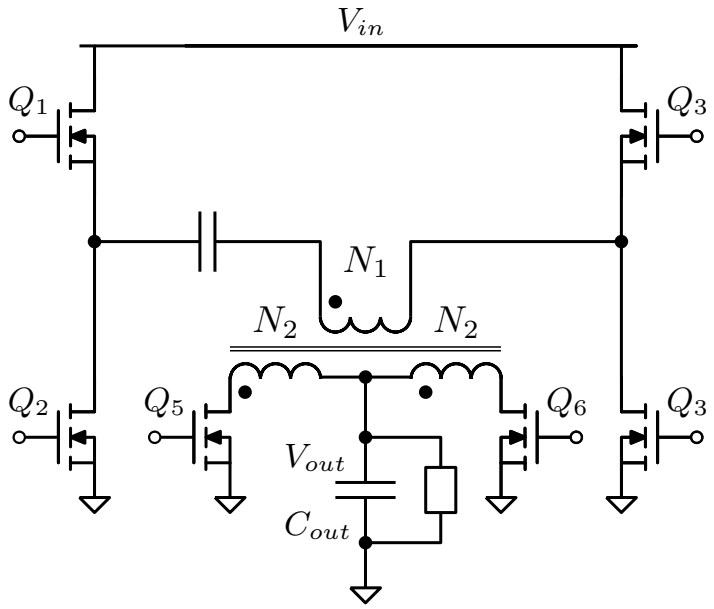


Fig. 3.8 Full-bridge LLC topology.

The objective of this section is to obtain the transformer area product, for a given magnetic field $B_{ac,max}$ and winding RMS current I_{rms}, for the two architectures. The area product, which yields an estimation for the core selection, is defined as the product of the winding area and the magnetic area:

$$A_p = A_e \cdot A_w \tag{3.8}$$

LLC analysis

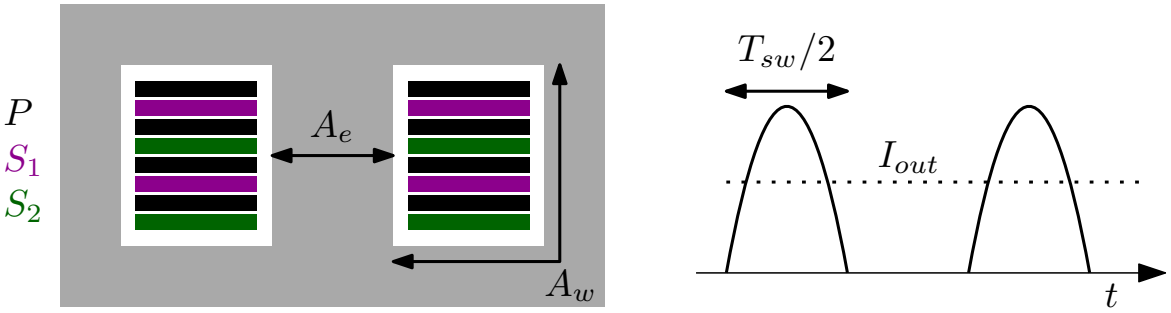


Fig. 3.9 Core stack-up for the LLC converter (left) and secondary winding current I_2 shape for a given output current I_{out}.

Fig. 3.9 (left) depicts the LLC core winding arrangement, where the area A_w is split to equalize primary/secondary copper losses. Under this assumption, primary and secondary sides occupy half of the winding area each, therefore a single secondary winding is given 1/4 of the full A_w, and for a given fill-factor k_r[2] and a given RMS current J_{rms} the following relation holds:

$$\frac{A_{w,LLC}}{4} = \frac{I_{2,rms} N_2}{J_{rms} k_r} \tag{3.9}$$

As the secondary winding current is composed of rectified sinusoidal half-waves, as reported in Fig. 3.9 (right), the required winding area can be written as a function of the output current:

$$A_{w,LLC} = k_w \pi I_{out} N_2 \tag{3.10}$$

[2]The fill-factor here mentioned is the ratio between the copper area and the total winding area A_w. It describes the loss of copper density for a given ferrite core and winding technique; in fact, the winding are cannot be completely filled with copper due to the manufacturing process (wire roundness, insulations, dielectric between copper traces), and k_r is the correction factor that yields an equivalent, reduced $A_{w,eq} = k_r \cdot A_w$.

where $k_w = \frac{4}{k_r J_{rms}}$.

For a given maximum field B_{ac}, the magnetic flux density is:

$$A_{e,LLC} B_{ac} = V_{out} \frac{T_{sw}}{2N_2} \tag{3.11}$$

and the required core cross section is

$$A_{e,LLC} = \frac{k_e V_{out} T_{sw}}{2N_2} \tag{3.12}$$

where $k_e = 1/B_{ac}$. Finally, the required area product can be calculated:

$$A_{p,LLC} = A_{e,LLC} \cdot A_{w,LLC} = k_e k_w \frac{\pi P_{out}}{2 f_{sw}} \tag{3.13}$$

STC-TX analysis

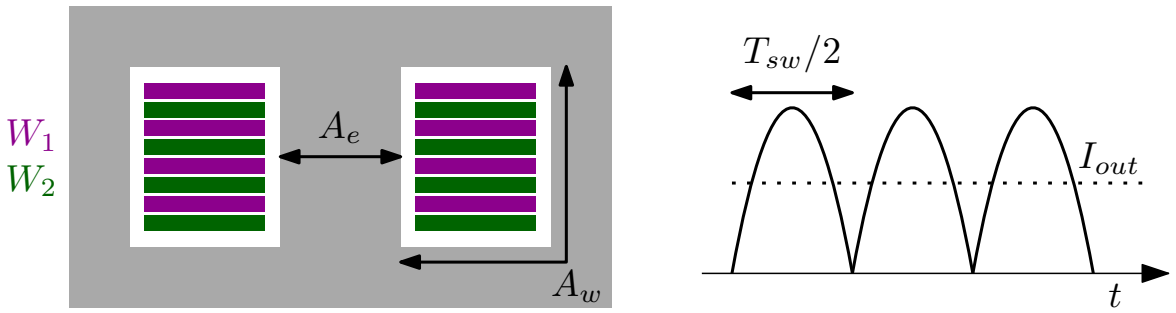


Fig. 3.10 Core stack-up for the STC-TX converter (left) and secondary winding current I_2 shape for a given output current I_{out}.

Fig. 3.10 (left) depicts the STC-TX core winding arrangement, where the area A_w is now split to equalize the two windings' copper losses. In this case each winding takes half of the full A_w, and for the same k_r and J_{rms} of (3.9), the relation becomes:

$$\frac{A_{w,stctx}}{2} = \frac{I_{2,rms} N_2}{J_{rms} k_r} \tag{3.14}$$

The secondary winding current is now composed of rectified sinusoidal full-waves, as reported in Fig. 3.10 (right). The required winding area is written as a function of the output current:

$$A_{w,stctx} = k_w \frac{\pi I_{out}}{2\sqrt{2}} N_2 \tag{3.15}$$

where k_w is the same of the LLC case.

For a given maximum field B_{ac}, the magnetic flux density is:

$$A_{e,LLC} B_{ac} = V_{out} \frac{T_{sw}}{2N_2} \tag{3.16}$$

and the required core cross section is

$$A_{e,LLC} = \frac{k_e V_{out} T_{sw}}{2N_2} \tag{3.17}$$

where $k_e = 1/B_{ac}$: as anticipated, the required core cross-section is the same of (3.12) and doesn't vary for the two topologies. Finally, the required area product can be calculated:

$$A_{p,sctx} = A_{e,sctx} \cdot A_{w,sctx} = k_e k_w \frac{\pi P_{out}}{4\sqrt{2} f_{sw}} \tag{3.18}$$

The STC-TX area-product, which is related to the core volume, is reduced by a factor of $2 \cdot \sqrt{2} \simeq 2.82$. It is clear that, in absence of isolation requirements, the converter family hereby proposed can be desirable to increase system power density. As the magnetic cross sections (3.12) and (3.17) are equal, the core volume reduction must be performed acting on the A_w/A_e ratio; i.e., when designing a transformer to have equal copper and core losses, the A_w/A_e of the STC-TX will be greater than the LLC one. In other words, for a given converter specifications set (V_{in}, V_{out}, P_{out}, f_{sw}), the proposed solution will require less area for the winding pack.

3.2.3 Increasing conversion ratio

If a higher conversion ratio is required, the two topologies can be transformed into the ones reported in Fig. 3.11 and in Fig. 3.12, derived respectively from the converter of Fig. 3.1 and of Fig. 3.2.

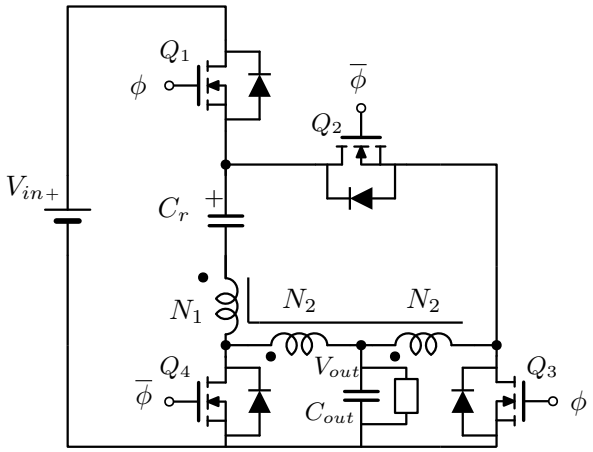


Fig. 3.11 Single-phase converter with increased conversion ration derived from the converter of Fig. 3.1.

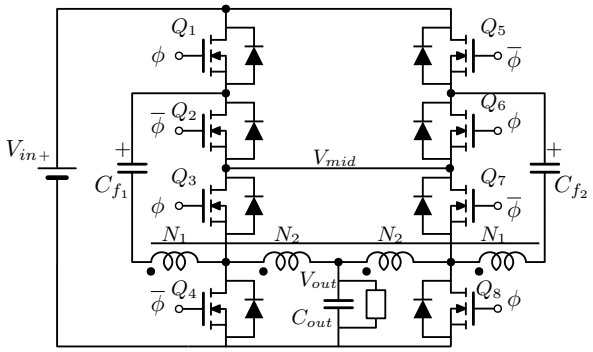


Fig. 3.12 Two-phases converter with increased conversion ration derived from the converter of Fig. 3.2.

In this case, the conversion is increased and corresponds to:

$$V_{in} = V_{out}\left(4+2\frac{N_1}{N_2}\right) \tag{3.19}$$

3.2.4 Experimental results

To confirm the validity of the proposed method, a 750 W quarter-brick prototype of the DC-DC server power supply has been built as shown in Fig. 3.13, with the specifications of Table. 3.1.

The transformer (which is in fact coupled inductors) is a fully-interleaved 2:2 structure made with two Ferroxcube 3C95 - E22/6/16 halves[3]. The core was gapped on the three legs in order to minimize fringing flux and to obtain a magnetizing inductance of $L_m = 4\ \mu$H.

[3]Efficiency has also been evaluated with an E/I combination.

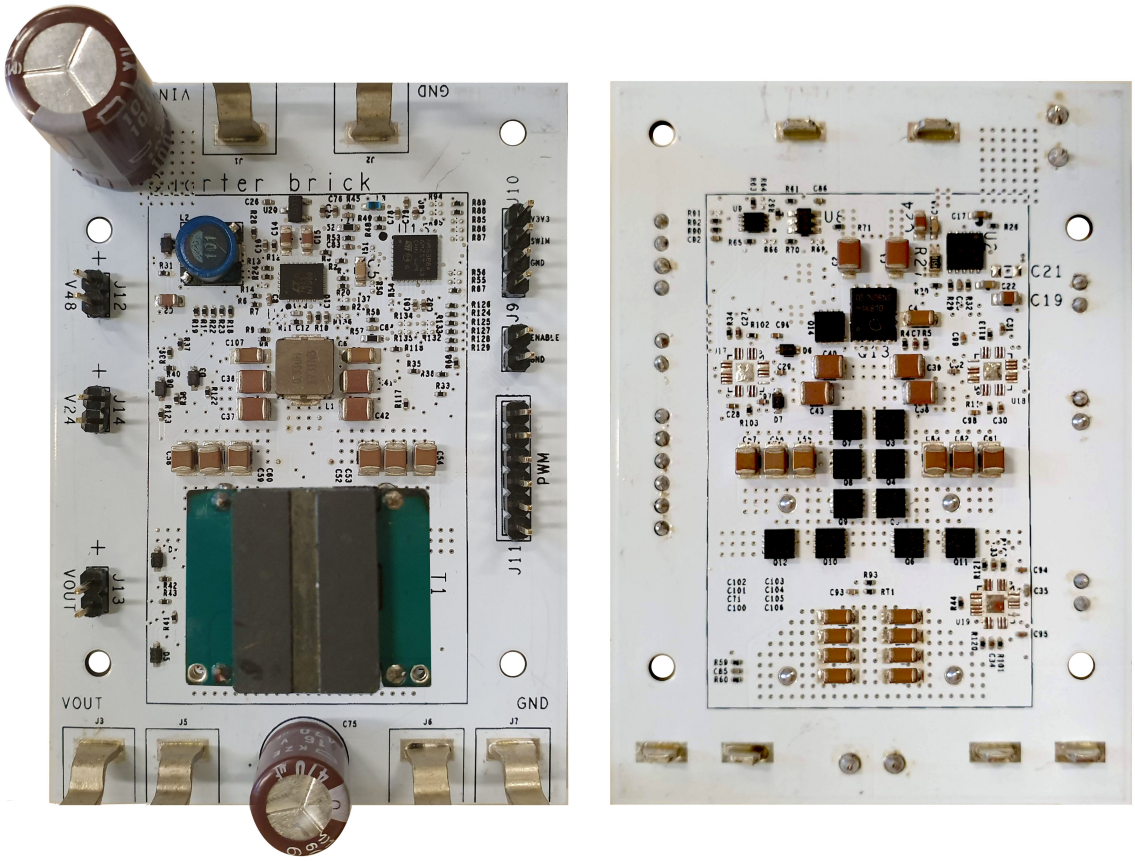


Fig. 3.13 Prototype of the proposed converter. The quarter-brick area, i.e. the black rectangle, includes the hot-swap controller and the control logic, besides the converter itself.

The winding structure is obtained by stacking 6 PCBs of 4 layer each (4 oz outer layers / 3 oz inner layers) as shown in Fig. 3.18. The parallelization of the structure is obtained by using pins. The total leakage inductance is measured to be $L_k = 16$ nH. Experimental peak efficiency (considering converter, driving and control losses) is around 99% as shown in Fig. 3.17, with a switching frequency of about 290 kHz and without forced air cooling[4]. Note that this curve was obtained in thermal steady state, therefore it was not measured during a load transient.

The transformer input terminal voltages V_a and V_b are shown in Fig. 3.14 (the corresponding schematic nodes are reported in Fig. 3.4). A detail of the same node voltages is reported in Fig. 3.15, where ZVS achievement can be observed. In this condition it is possible to notice the contribution of the L_k resonant current and the magnetizing inductance L_m. As previously discussed, the shape of the resonant current is dumped for the small value of inductance L_k. The energy present is inductance at full load is sufficient to discharge switches

[4]This measurement was performed with the same approach described in 2.5.

Table 3.1 Converter and PCB specifications

$V_{in,nom}$	48 V / 54 V
$V_{out,nom}$	12 V / 13.5 V
$I_{out,max,continuous}$	62.5 A
$P_{out,max,thermal}$	800 W
$f_{sw,nom}$	290 kHz
PCB power area	Quarter-brick (36.8 mm $\times$ 58.4 mm)
PCB layer count	14
PCB copper weight	70 μm outer layers
	35 μm inner layers
MOSFETs	BSZ025N04LS
Switched capacitors C_r	(6 + 6) $\times$ 4.7 μF, 1210 (GRM32ER71K475ME14L)
Input capacitors C_{in}	4 $\times$ 4.7 μF, 1210 (GRM32DC72A475ME01L)
Output capacitors C_{out}	8 $\times$ 22 μF, 1206 (GRM32ER71E226KE15L)

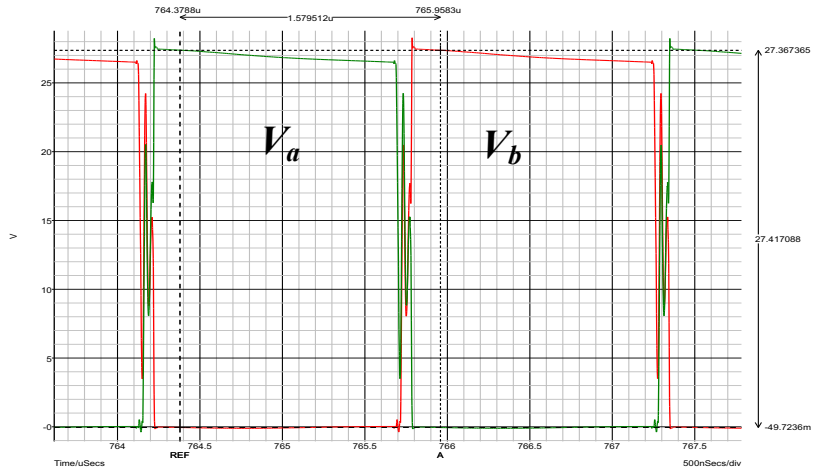
output capacitances C_{oss} but not to hold the condition for all the duration of the dead time T_d. Thanks to the contribution of the magnetizing inductor L_m the nodes reach approximately the ZVS condition anyway.

In Fig. 3.16 the output voltage ripple at full-load is reported. Ripple shape is compatible with an operating condition close to the resonance: this behaviour is also confirmed observing the simulation of Fig. 3.7, as output voltage ripple is the integral of this curve[5].

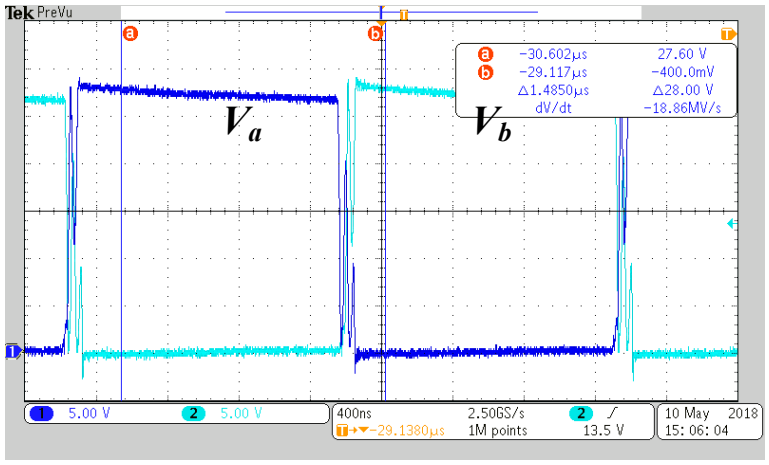
The converter includes a hot-swap input stage, which allows to power up the module without interfering with the input bus[6]. This function is implemented through an input buck converter configured to soft-start V_{out} and designed to occupy the smallest area. To achieve this performance the hot-swap buck inductor has a small value, as the only requirement is to avoid saturation at full load and to withstand the peak current during start-up. The high-side switch, which is driven by a charge-pump included in the auxiliary controller, is kept constantly ON during normal operation. The low-side switch of this block can be shrunk in order to save space, as its dissipation manifests only during the start-up interval.

[5]Fig. 3.7 shows the output transformer current, which is feeding the load and the output capacitor C_{out}. As simulations and measurements were performed with a constant load current, the voltage ripple of Fig. 3.16 corresponds to the integral of Fig. 3.7 when the DC load current is subtracted.

[6]I.e. without having to soft-start the input bus, which is impractical in a server application, and together avoiding inrush currents or output voltage overshooting.



a)



b)

Fig. 3.14 Transformer input terminal voltages a) simulated and b) measured on the prototype with $V_{in} = 54$ V, $I_{out} = 47$ A, $f_{sw} = 250$ kHz.

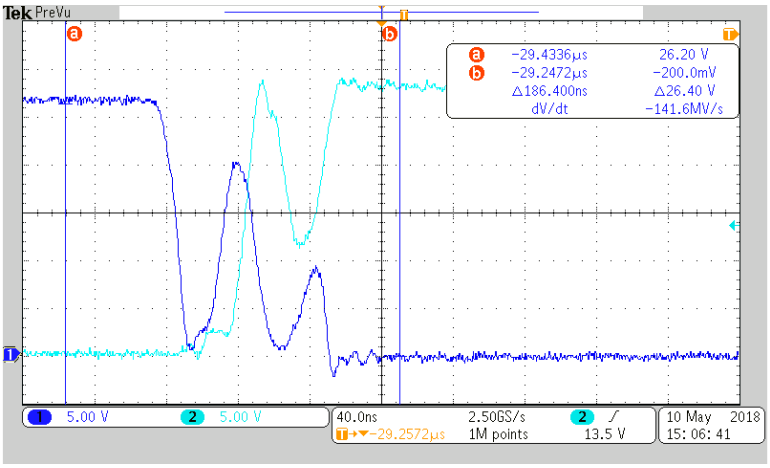


Fig. 3.15 Detail of the transformer input terminal voltages of Fig. 3.14 that shows the ZVS operation at full load.

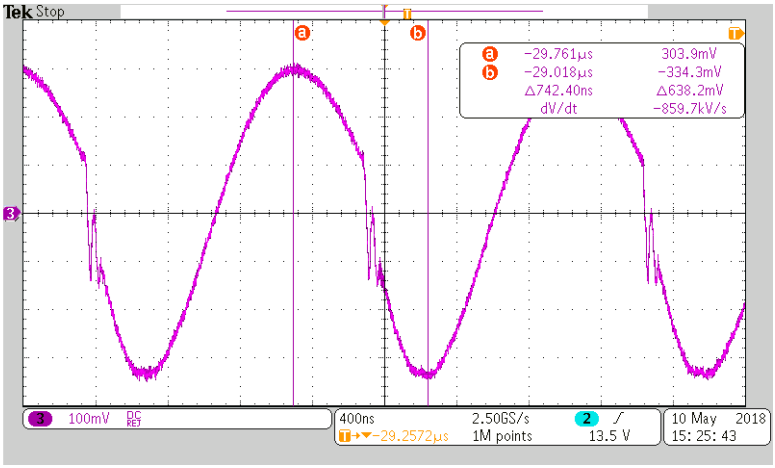


Fig. 3.16 Output voltage ripple with $V_{in} = 54$ V, $I_{out} = 47$ A, $f_{sw} = 290$ kHz.

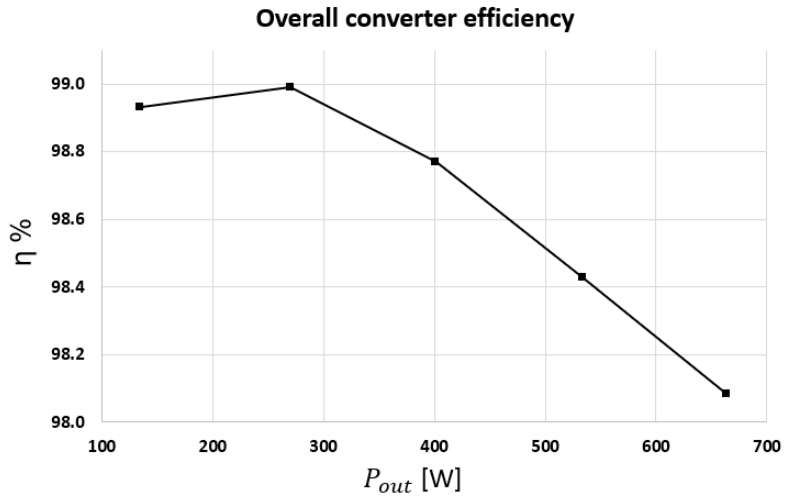


Fig. 3.17 Prototype efficiency with $f_{sw} = 290$ kHz, $V_{in} = 54$ V and without forced air cooling. Thermal steady state.

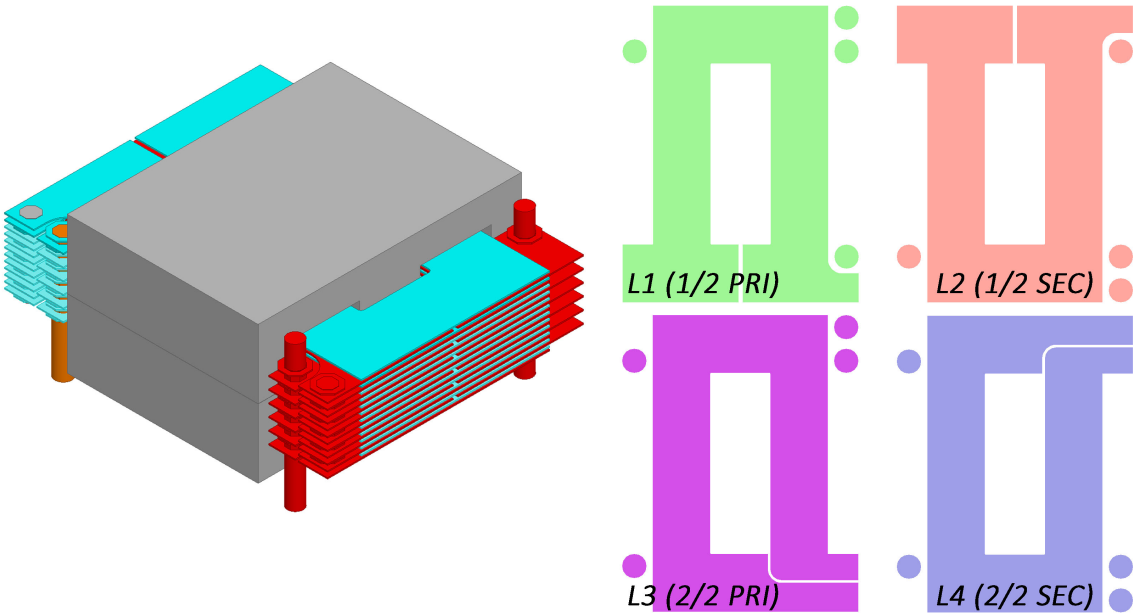


Fig. 3.18 Transformer layout. One PCB is made of 4 layers and it's paralleled to fill the winding area. The 2:2 winding arrangement is fully interleaved.

Fig. 3.18 shows the transformer/coupled inductors structure with the corresponding stackup. The 2:2 winding arrangement is implemented on a 4-layers fully-interleaved PCB. FEM simulation has shown that an E/I combination can also be used with a total of 3 PCBs without excessive impact on total efficiency. As the AC winding current component is strong, the bottom-feeding approach shown in Fig. 3.18 causes an uneven utilization of the windings, where the furthest ones are less used. This problem can be reduced with a central winding connection, for example embedding the transformer inside the main PCB. Resulting measured efficiency is shown in Fig. 3.19, where parallelized transformer PCBs were progressively removed.

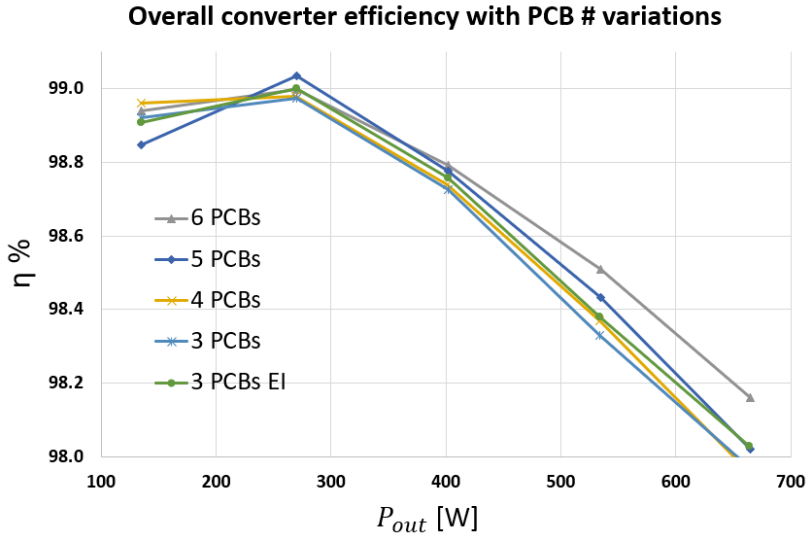


Fig. 3.19 Overall converter efficiency with different transformer PCB winding packs. $f_{sw} =$ 310 kHz. Thermal steady state.

3.2.5 *Droop* function and current sharing

Fig. 3.20 shows the *droop curve* of this converter. This behaviour is important to observe as it expresses the output impedance in steady state, i.e. the output resistance defined as

$$R_{droop} = \frac{\Delta V_{out}}{\Delta I_{out}} = Z_{out}(f = 0) \tag{3.20}$$

The frequency-dependent behaviour of this parameter has already been discussed in Chapter 2, and a rough estimation in steady-state was found in literature [41]. In this case the high-frequency shape of (3.20) is not paramount to consider as the overall conversion chain output

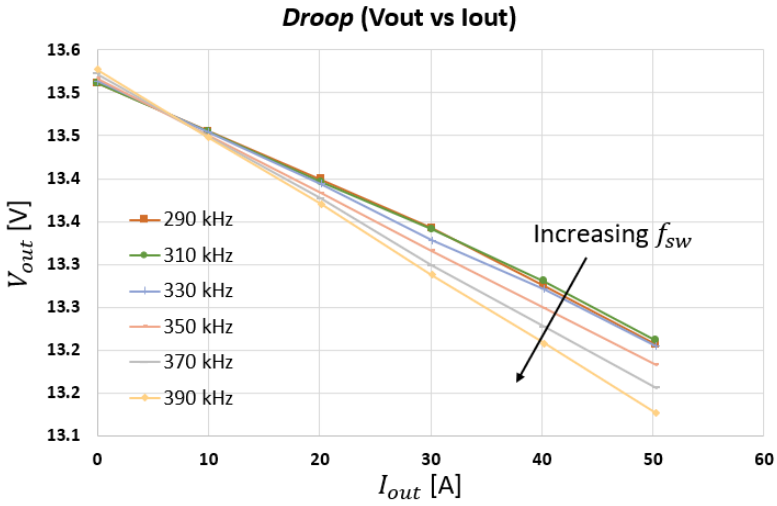


Fig. 3.20 $V_{out}(I_{out})$ for different switching frequencies.

impedance will depend on the last VRM; on the other hand the *droop* function is useful to understand the intrinsic current-sharing capabilities of the system. In fact, the duty-cycle is fixed and the conversion ration is almost independent from it, therefore the parallelization of multiple modules must rely on a different technique. Fig. 3.20 shows that the output resistance is also weakly dependent on the switching frequency, as a consequence the only remaining method to balance output currents is to rely on the *droop* itself, which acts as an automatic current-sharing loop with only a proportional gain. The steady-state performance of this equivalent regulation can be directly understood from the reported figure. The average measured value of the output resistance is:

$$R_{droop} = \frac{\Delta V_{out}}{\Delta I_{out}} = 5.5 \text{ m}\Omega \tag{3.21}$$

As the transformer is implemented in a planar architecture, its variability is supposed to be small with respect to the switched capacitors, both in resistance and leakage inductance. The transformer gap is related to the magnetizing inductance and is the most uncertain parameter of the magnetic part manufacturing, but does not participate to the resonance transient and therefore has no impact on output current. To show the effectiveness of the passive current-sharing loop, a simulation has bee performed with the parallelization of two phases. For one phase branch, a switched capacitor block is decreased by a 20% value, which

is actually an uncommon situation[7]. Output average currents for the two unmatched phases, at full load, are:

$$I_{out,ph1} = 27.15 \text{ A}$$
$$I_{out,ph2} = 28.71 \text{ A} \tag{3.22}$$

Fig. 3.21 shows the effects of this mismatch in the transformer currents I_a, I_b when two phase-shifted converters are connected in parallel.

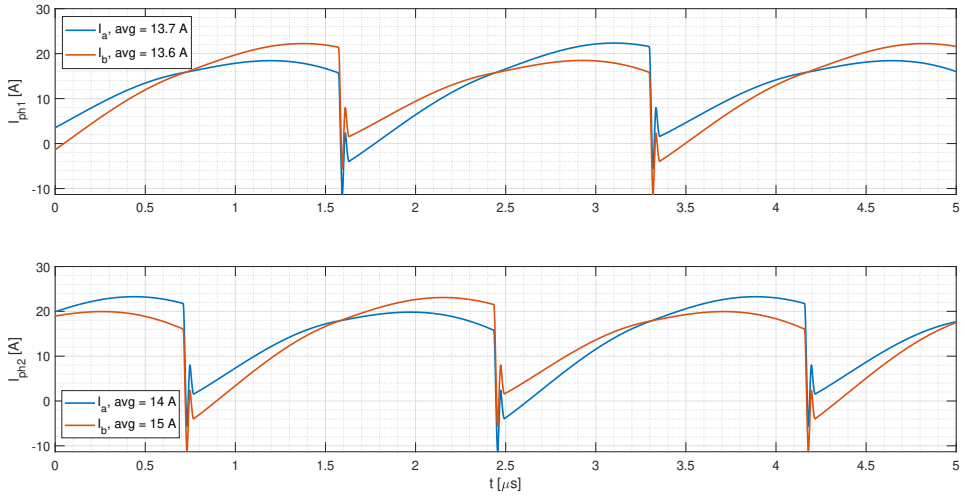


Fig. 3.21 Transformer currents I_a, I_b with a -20% switched capacitor block mismatch for phase 2 on the I_b side. Reported average values show an increased value for the mismatched phase 2.

3.3 Dual-Output, Multiresonant 5:1 + 10:1 STC-TX Converter

This chapter is concluded with another converter that features a switched-tank capacitor block and a transformer, which can be actually considered as three coupled inductors. This topology aims to be an example of the extreme configurability of this kind of architecture, which relies on the transformer connections and winding arrangement to achieve a wide range of unregulated conversions with high efficiency and power density.

[7]The reader must consider that a similar mismatch is rare with 6 capacitors per branch, as every capacitor should be equally mismatched. Better estimations can be made with a Monte Carlo approach.

In a server board it is common to require many low-voltage rails in order to power various peripherals, or to implement an intermediate conversion towards the VRM step. Besides, in some data-center architectures, battery-backup mode can lead to decreased distribution bus voltages, requiring specific solutions [51] to maintain the conversion chain inside a safe and efficient operating range. To address these issues, a configurable, dual-output DC-DC converter is researched, enabling a wide range of equivalent transformation ratios. First, the generic/configurable topology is presented, while in the following sections the specific case of the 5:1 + 10:1 prototype is presented.

3.3.1 Converter operation

The generic, configurable architecture is reported in Fig. 3.22. This converter operates at the resonant frequency of the tank composed of C_r and the leakage inductance of the transformer, as for the converter of Section 3.2. Switches S1 and S2, which can also be direct connections to the desired net, determine the V_{in}/V_{out1} and V_{in}/V_{out2} ratios reported in Table 3.2. In this converter, the resonance shape is determined by the leakage inductance associated with the two different outputs, but remains almost-sinusoidal as it will be shown in Section 3.3.2.

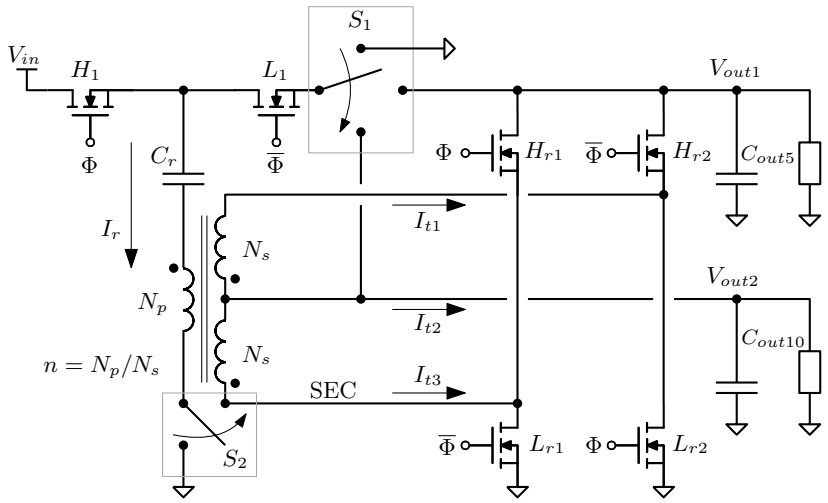


Fig. 3.22 Dual-Output, Multiresonant STC-TX Converter configurable topology.

Converter timings are composed of two complementary square waves at constant frequency, as in the previous case and as reported in Fig 3.23. The resonant current I_r is reflected by currents I_{tx}, which are rectified to the outputs by switches H_{rx}, L_{rx}. For S1, S2 = GND this topology is similar to a classic LLC converter and the isolation can be restored. For other configurations, it becomes similar to the converter of Section 3.2 and to the new researched family.

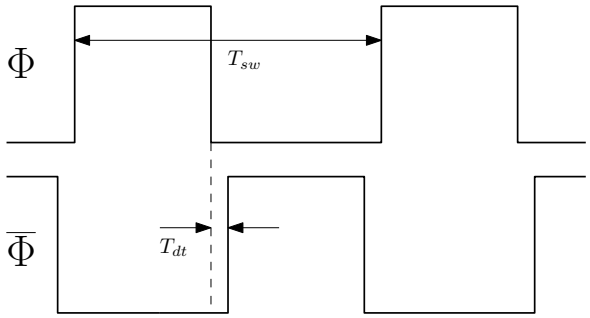


Fig. 3.23 Two-phases SC-buck converter control signals.

Table 3.2 Transformation ratios V_{in}/V_{out1} (left) and V_{in}/V_{out2} (right) for different S_1, S_2 configurations.

$\frac{S_1}{S_2}$	V_{out1}	V_{out2}	GND
SEC	$\frac{1}{n+2}$	$\frac{1}{n+3/2}$	$\frac{1}{n+1}$
GND	$\frac{1}{n+1}$	$\frac{1}{n+1/2}$	$\frac{1}{n}$

$\frac{S_1}{S_2}$	V_{out1}	V_{out2}	GND
SEC	$\frac{1}{2n+4}$	$\frac{1}{2n+3}$	$\frac{1}{2n+2}$
GND	$\frac{1}{2n+2}$	$\frac{1}{2n+1}$	$\frac{1}{2n}$

As the converter transformation ratio not only depends on the winding ratio $n = N_p/N_s$ but also on the S1, S2 connection, this degree of freedom can be used to overcome input voltage temporary transitions such as battery backup modes[8]. It is clear that S1 and S2 cannot be used to regulate intermediate voltages apart from the ones of Table 3.2; nonetheless, this solution might be useful when the following converters implement the voltage regulation and the objective of the re-configuration is to maintain the overall system at maximum efficiency and/or to supply the VRMs with a sufficient input voltage. Transitions of S1 and S2 is currently being researched, and an example for the 54 V to 48 V transition is reported in Section 3.3.2.

The proposed converter family ensures ZVS on all switches through the magnetizing current and enables the use of small ferrite cores, as the volt·second product is extremely small for this kind of topologies when compared to a classical LLC converter, as explained

[8]The most common case in the 48 V architecture is the transition between the 54 V nominal input voltage to the 48 V battery backup.

in Section 3.1. As only two FETs are input-voltage rated, this solution is desirable when high-efficiency and high power-density is required, together with conversion flexibility.

3.3.2 Experimental results

To demonstrate the performances of this topology, the dual-output architecture of Fig. 3.24 was selected, i.e. n = 3, S1 = V_{out1} and S2 = OUT. Converter parameters are reported in Table 3.3.

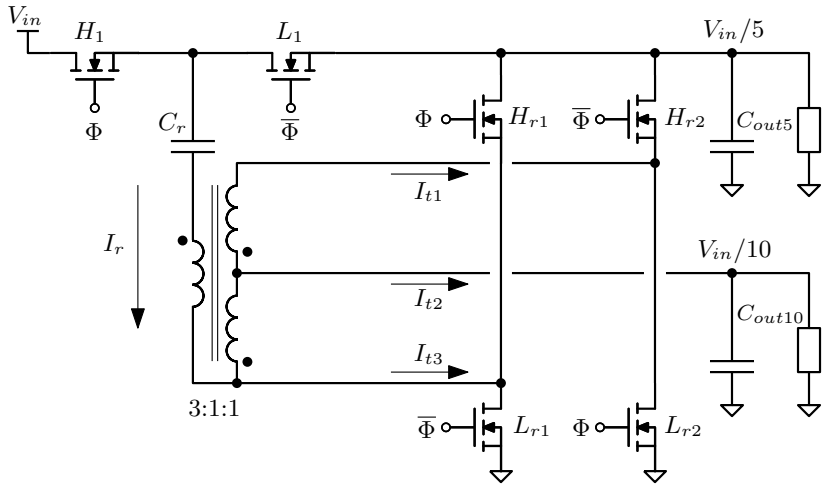


Fig. 3.24 Dual-Output, Multiresonant 5:1 + 10:1 STC-TX Converter topology.

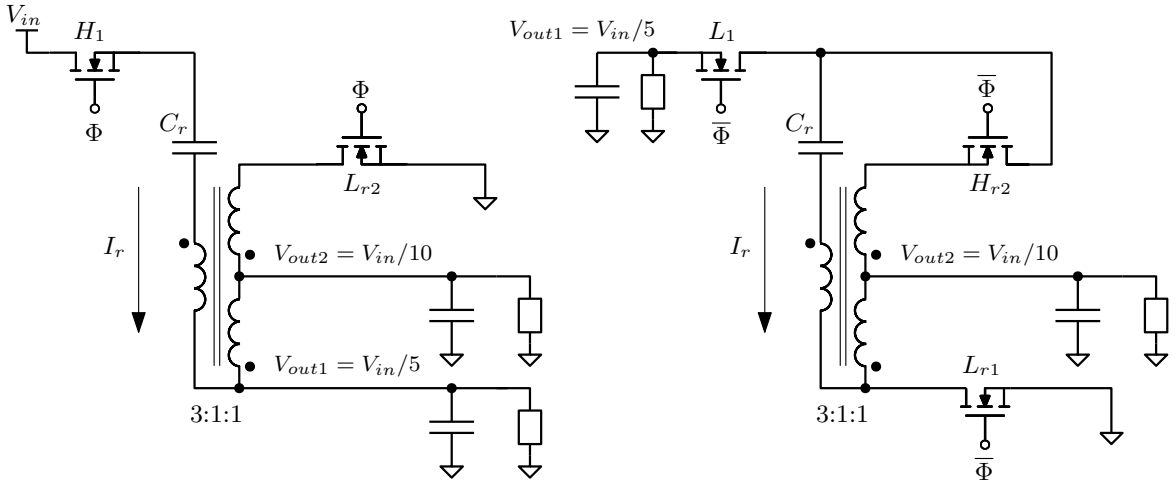


Fig. 3.25 Equivalent sub-topologies during Φ and $\overline{\Phi}$.

For this prototype the main target was to obtain a modular, flexible, low-profile module. To meet the profile specifications, an E18/4/10 + plate 3F36 core was embedded in the PCB

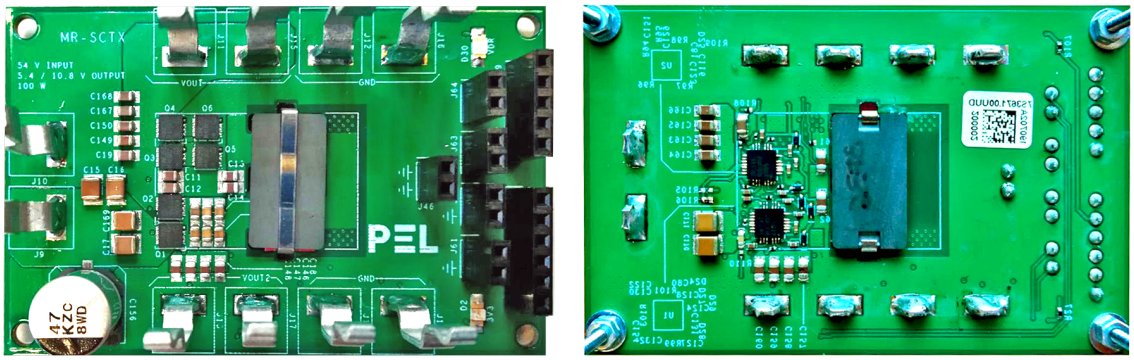


Fig. 3.26 PCB prototype of the 200 W converter.

board and the transformer was implemented on the main PCB. The selected all-legs gap is about 60 μm. Power-area maximum thickness corresponds to the core itself and measures 6 mm.

Table 3.3 Converter and PCB specifications

$V_{in,nom}$	48 V / 54 V
$V_{out1,nom}$	9.6 V / 10.8 V
$V_{out2,nom}$	4.8 V / 5.4 V
$I_{out1,max,continuous}$	21 A
$I_{out2,max,continuous}$	42 A
$P_{max,thermal,combined}$	200 W
$f_{sw,nom}$	500 kHz
PCB layer count	10
PCB power area (w transformer)	27.8 mm × 18.5 mm
Power area max height	6 mm
PCB copper weight	35 μm (1 oz) all layers
H_1, L_1 MOSFETs	BSZ040N06LS5
H_{rx} MOSFETs	BSZ013NE2LS5I
Switched capacitors C_r	6 × 1 μF, 0805 (GRM21BC72A105KE01L)
Input capacitors C_{in}	3 × 4.7 μF, 1210 (GCM32DC72A475ME02L)
	1 × 100 nF, 0603 (CL10B104KC8NNNC)
	1 × 47 μF, Radial (EEH-ZC1K470P)
Output capacitors C_{out}	(12 + 12) × 22 μF, 0805 (GRT21BR61E226ME13L)

Transformer winding arrangement is reported in Fig 3.27, together with a rendered model for FEM simulation. As this converter operates at high frequency, interleaving is paramount to implement, therefore the 3 primary turns are split among 4 layers, with different partial turns to obtain a manufacturable board. Secondary windings are replicated on alternate layers to fill the whole winding area. For this prototype a 1-oz copper weight was chosen in order to meet components density requirements, but an improved weight could be desirable to increase output power. Efficiency is shown in Fig. 3.28 for the two outputs when the converter is in thermal steady state: it is clear that the low-voltage rail becomes rapidly affected by copper losses, limiting the output power capability[9]. This effect can be mitigated by implementing the converter with thicker copper weight.

Converter waveforms at nominal conditions f_{sw} = 500 kHz, V_{in} = 54 V are reported in Fig. 3.29, 3.30, 3.31 and 3.32. Fig. 3.33 shows a thermal image at high load and natural convection. Observing L_1 drain voltage of Fig. 3.29 and the output rectifier central nodes shown in Fig. 3.30 it is clear that the ZVS transient is almost perfectly matched. To observe the body diode conduction and completely discharge these switching nodes, the transformer gap can be increased.

[9]This measurement was performed with the same approach described in 2.5.

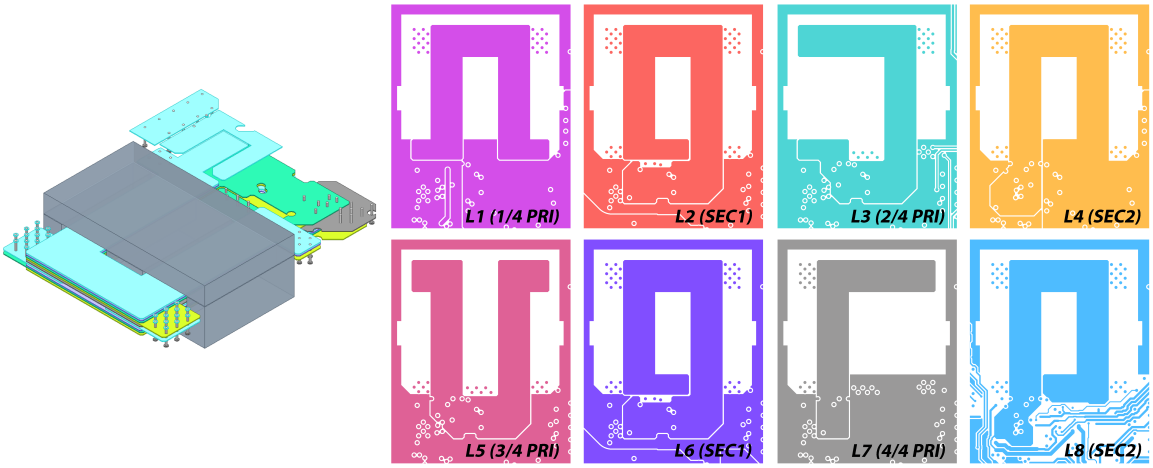


Fig. 3.27 Transformer layout of the 200 W converter.

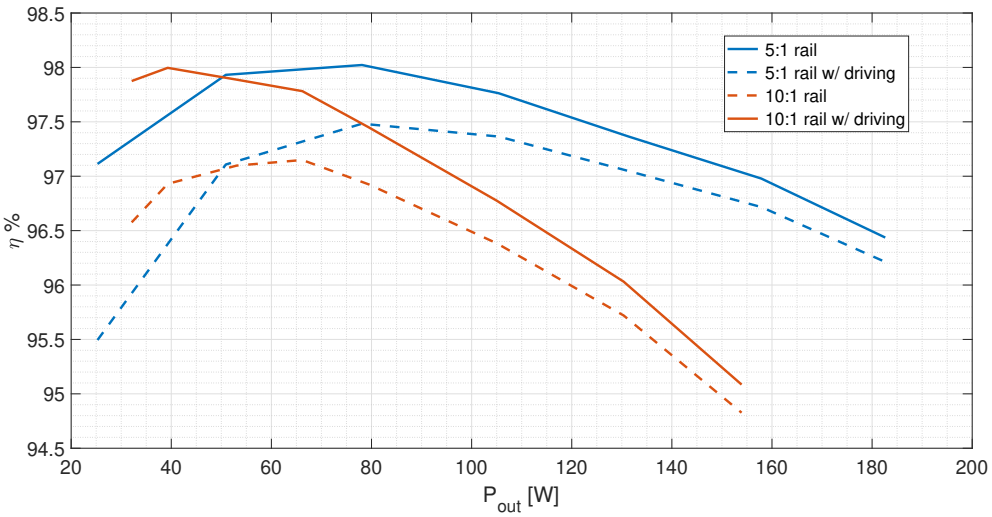


Fig. 3.28 Efficiency of the 200 W converter at $f_{sw} = 500$ kHz, $V_{in} = 54$ V.

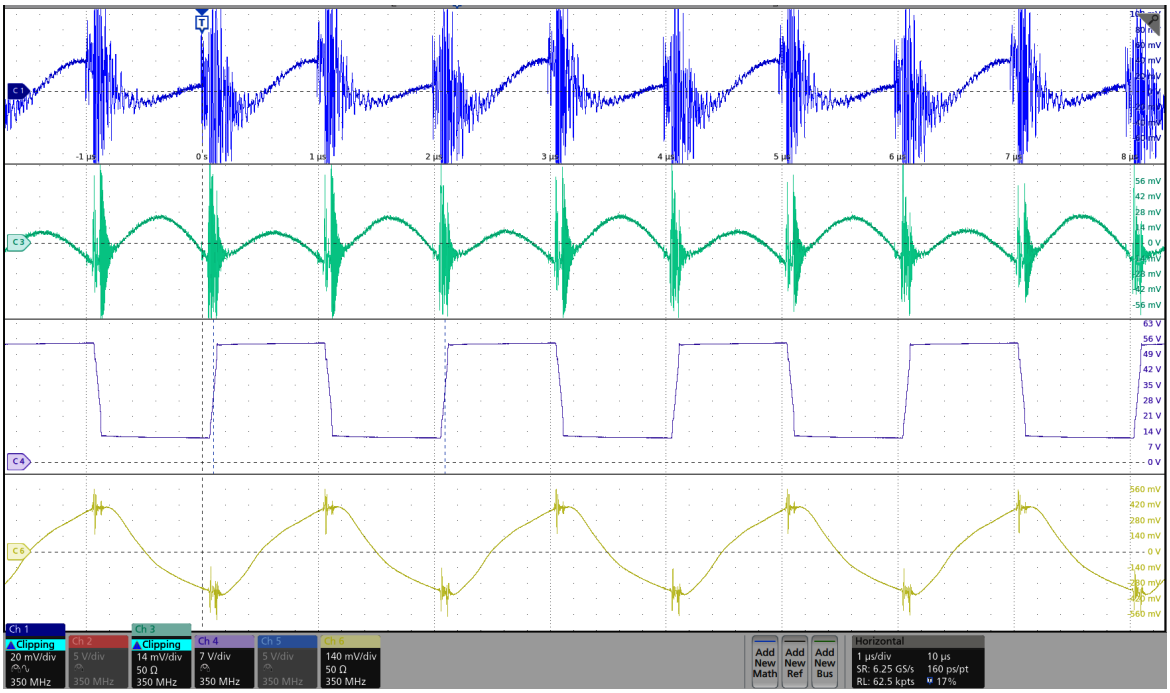


Fig. 3.29 Converter waveforms at f_{sw} = 500 kHz, V_{in} = 54 V, 50 W load on V_{out2}. From top to bottom: V_{out1} AC-coupled; V_{out2} AC-coupled; L_1 drain voltage; C_r differential voltage.

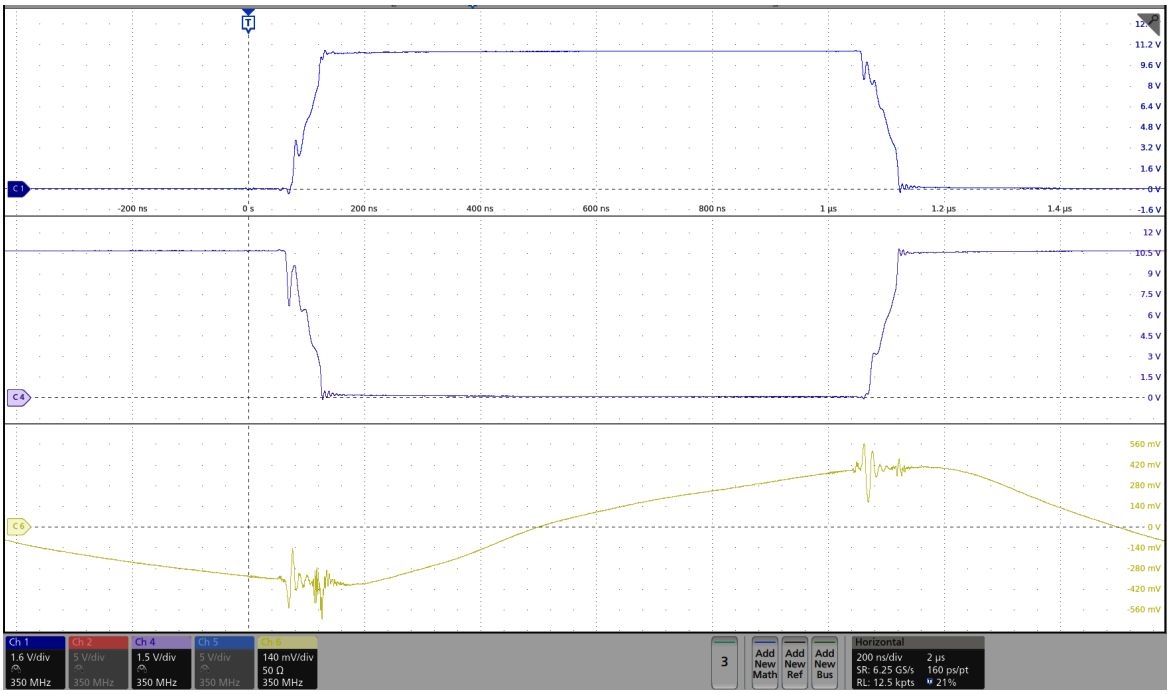


Fig. 3.30 Converter waveforms at f_{sw} = 500 kHz, V_{in} = 54 V, 50 W load on V_{out2}. From top to bottom: V_{ds} of L_{r1}; V_{ds} of L_{r2}; C_r differential voltage.

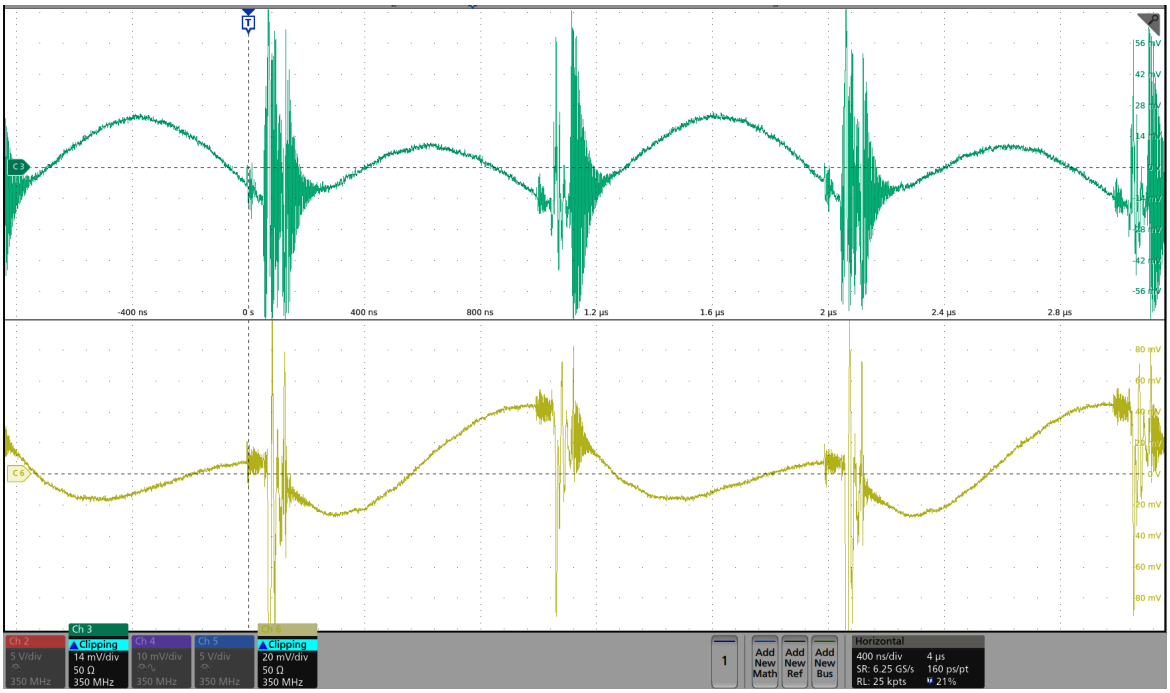


Fig. 3.31 V_{out2} voltage ripple (top) and V_{out1} voltage ripple (bottom) at f_{sw} = 500 kHz, V_{in} = 54 V, 50 W load on V_{out2}.

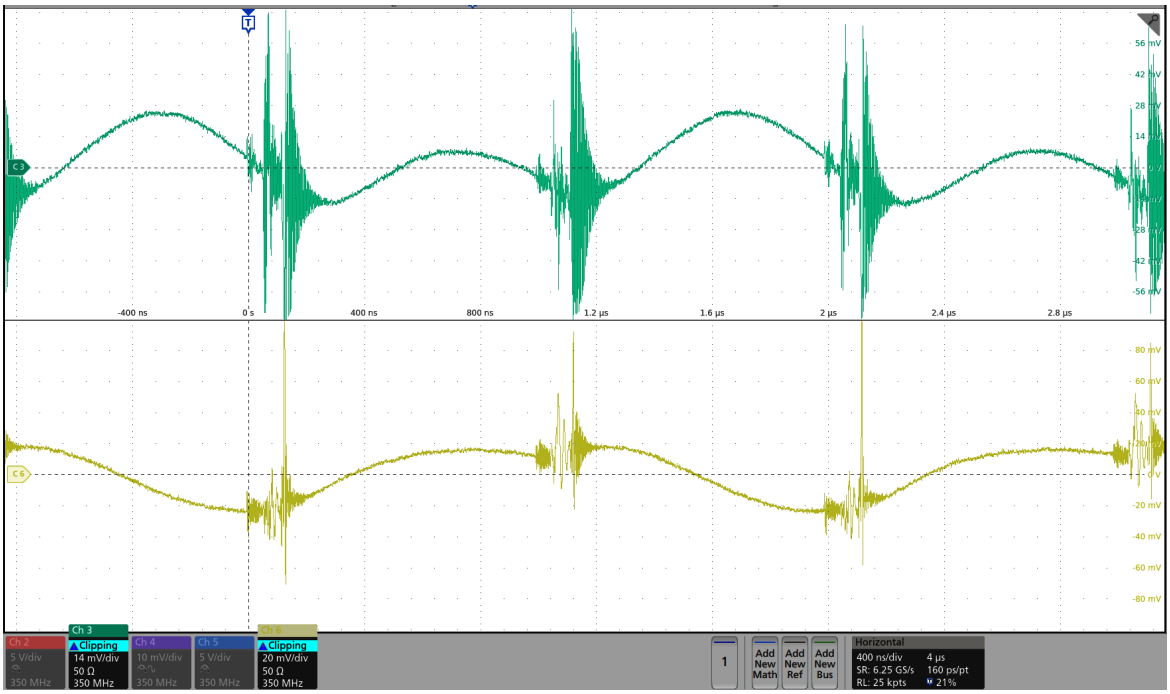


Fig. 3.32 V_{out2} voltage ripple (top) and V_{out1} voltage ripple (bottom) at f_{sw} = 500 kHz, V_{in} = 54 V, 50 W load on V_{out1}.

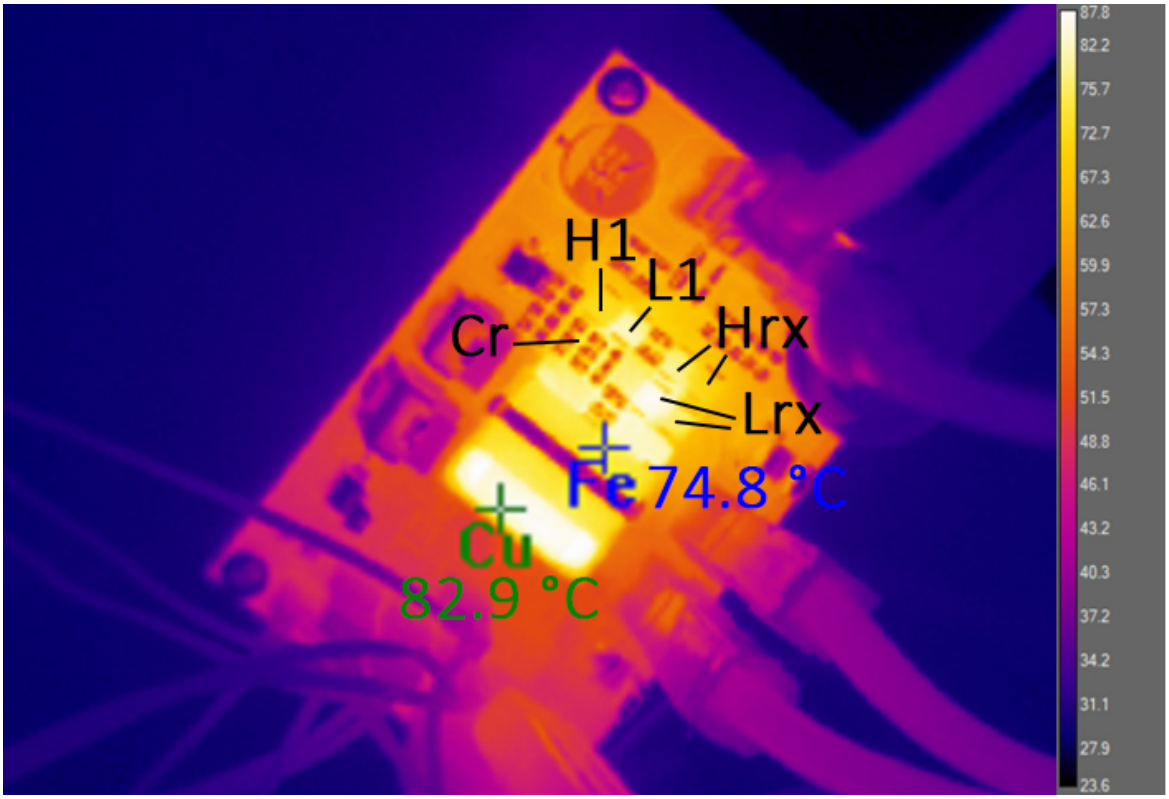


Fig. 3.33 Thermal image after 5 minutes of natural convection, 182 W load on V_{out1}. f_{sw} = 500 kHz, V_{in} = 54 V.

3.3.3 *Droop* function and current sharing

As for the converter of Section 3.2, also in this case the modularity of the solution depends on the output equivalent resistance, or droop function, defined in (3.20). This value was evaluated with both the output rails in parallel and it is reported in Fig 3.34. For the two output rails, the average measured values are

$$\begin{aligned} R_{droop_1} &= \frac{\Delta V_{out_1}}{\Delta I_{out_1}} = 21\ \text{m}\Omega \\ R_{droop_2} &= \frac{\Delta V_{out_2}}{\Delta I_{out_2}} = 10\ \text{m}\Omega \end{aligned} \tag{3.23}$$

These values can be directly used to estimate the intrinsic, passive current sharing performance.

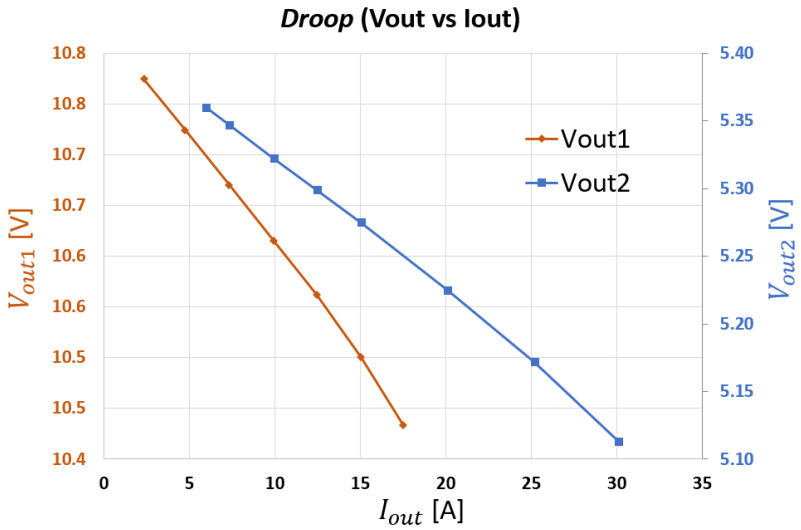


Fig. 3.34 $V_{out1}(I_{out1})$ (orange) and $V_{out2}(I_{out2})$ (blue).

3.3.4 *Online* topology reconfiguration

As anticipated in Section 3.3.1, the topology here examined is prone to an *online* reconfiguration, i.e. an S1 and/or S2 position change when the converter is loaded. The implementation of these auxiliary switches and the transitioning method depend on the specific case; nonetheless, in this context it's interesting to analyse the behaviour of the 54 V bus transitioning to the 48 V battery-backup mode when S1 and/or S2 commutate instantly, for example when these

devices are MOSFETs driven by a common gate driver[10]. This event is depicted in Fig. 3.35, where S1 is toggled to GND to maintain the output rails over the 10 V/5 V thresholds. Fig. 3.36 shows the resonant current evolution during the commutation, where the current *overshoot* is tied to the output capacitors recharge transient. A *soft* S1/S2 commutation mechanism could be implemented with a linear gate driving approach, i.e. transitioning in a resistive manner between the two states. This method must be tailored to the particular application and carefully shaped to maintain the devices insider their SOAs, given the high instantaneous power involved when the converter is loaded.

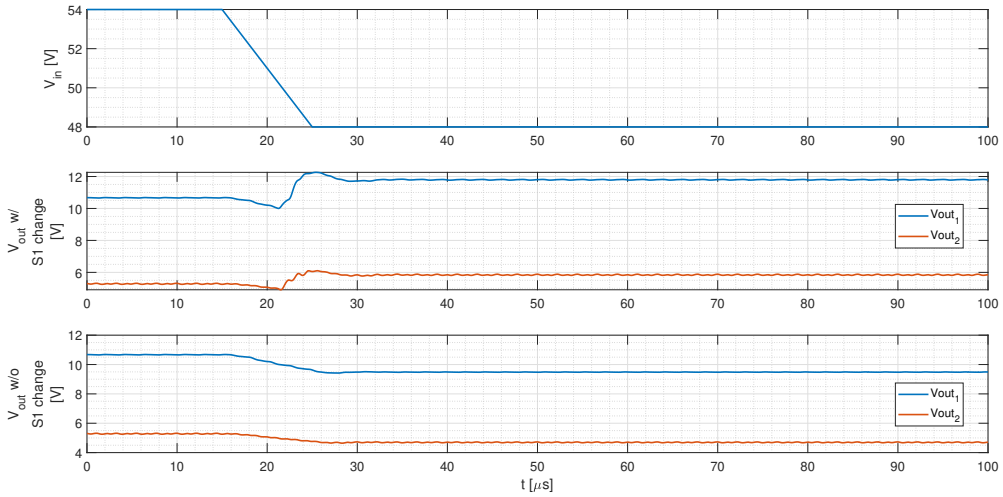


Fig. 3.35 Converter waveforms during a V_{in} transition from 54 V to 48 V. S1 is disconnected from V_{out1} and connected to GND when V_{in} drops below 51 V.

[10] A driver with an integrated charge pump could be mandatory, as S1/S2 must remain active after the commutation.

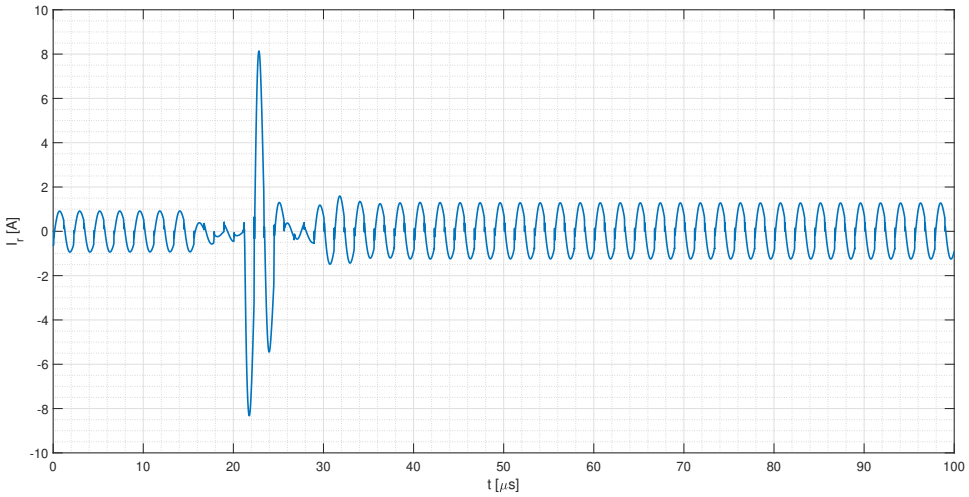


Fig. 3.36 Resonant current I_r during V_{in} transition from 54 V to 48 V. S1 is disconnected from $V_{out}1$ and connected to GND when V_{in} drops below 51 V.

3.4 Conclusions

In this chapter a different kind of non-isolated unregulated step-down converters is presented. This family combines the structures of traditional isolated LLC converters with the SC architectures. These topologies use transformers as coupled inductors, reducing the design constraints for their development, i.e. enabling the reduction of the magnetic window A_e. Two examples were presented to prove this concept, reaching high efficiencies up to 99% for the 750 W, 4:1 conversion and up to 98% for the dual-output converter. A passive current sharing allows to easily parallel multiple phases, which is a common requirement when dealing with IBCs as it enables the solution to scale with load requirements.

The 4:1, dual-phase converter has been presented at APEC 2019 [52], while the dual-output one has been accepted to be presented at APEC 2020.

Chapter 4

Regulated 48 V to 1.8 V Switched-Capacitor converter with Fully-coupled Buck PoL

In this chapter a the whole conversion chain from the 48 V bus to the regulated V_{core} is implemented in a single converter with high power density and efficiency, featuring the combination of two novel architectures. The proposed system is an example of efficiency/density maximization through the use of stacked, current-fed switched capacitor stages and a new unregulated VRM based on a fully-coupled buck converter. This chapter includes the two stages' architecture description and analysis in two different subsection. Output impedance and experimental results are included in the final section.

4.1 Introduction

Switched-capacitors used with soft-charge mechanisms (i.e. without charge redistribution issues) have become a widespread solution for high-density step-down conversions for their increased energy density with respect to inductors, as explained in Chapter 1. Soft-charging techniques are often achieved through resonant operation, as seen in Chapters 2 and 3, possibly allowing to obtain ZVS and/or ZCS. This technique relies on a series inductor to obtain a resonant current inside an equivalent LC tank: current shape is therefore almost-sinusoidal as seen for the previous converters.

Soft-charging is inherently achieved when the switched-capacitors are current-fed, therefore resonant operation is not mandatory. Of course, depending on the considered topology, ZVS/ZCS can be lost on some switches: this could lead to increased switching losses es-

pecially when devices are operated at high voltages. Voltage step-up/down can be easily obtained by stacking different capacitors in series, ensuring the soft-charge through an inductive loop. A simple example of this technique, as mentioned in Chapter 3, is the *Series Capacitor Buck converter*, where only a single switched-capacitor is used. Recently, more complex architectures have been proposed [53], [54], [55]: the main advantage of this approach is that inductive component(s) and semiconductors withstand only a fraction of the input voltage, therefore current ripple is decreased and/or inductor value(s) can be reduced for a given operating frequency.

This switched capacitor stage is used in conjunction with a novel PoL module which we call *fully-coupled buck converter*. The proposed architecture solves one of the most common trade-offs encountered during the design of the VRM module, which is the constraint given by inductor size, bandwidth and efficiency. The classical VRM is usually implemented through a multi-phase buck converter, which was widely researched in literature and industry. It is common to increase the VRM performance with the use of coupled inductors in order to decrease inductor RMS current magnitude and improve transient response [56–58]; nonetheless, inductor volume remains tied to the required phase current and transient response performance. The intrinsic limitations of the multi-phase buck converter, which can be potentially coupled, was already researched in [59] where the concept of *critical inductance* was outlined.

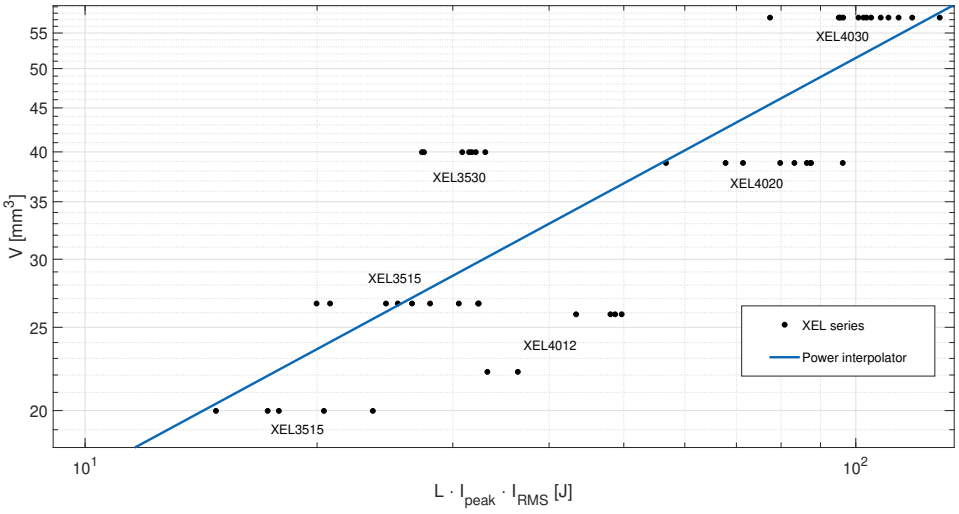


Fig. 4.1 Inductor volume vs energy-related product $L \cdot I_{peak} \cdot I_{RMS}$ for the *Coilcraft*^{TM} XEL series.

It is important to understand that, with the classical multi-phase approach, one must scale up magnetic volumes to achieve high efficiency or bandwidth. For a given transient

response and phase number, in fact, efficiency can be increased with inductor volume (which can be considered proportional to the $A_w \cdot A_e$ product, where A_w and A_e are the core cross-section and winding area, respectively). This constraint depends on the DC magnetic flux saturation boundary, which must be respected inside the A_e area and which limits output current capability. On the other hand, fast output transients can only be achieved by reducing inductance value, as the maximum phase current slew rate is inversely proportional to it [59]. This problems can be summarised observing Fig. 4.1, where inductor volume is plotted against the $L \cdot I_{peak} \cdot I_{RMS}$ product for the *Coilcraft*^{TM} XEL series. It is well known that, even with coupling, this relation cannot be overcome and the DC current constraints the magnetic cross section.

To remove the DC magnetic flux saturation problem, and as a consequence the phase current limitation, the *fully coupled buck converter* is proposed, where each phase inductor becomes part of common magnetic path. Besides, to maximize transient response capability, a well-coupled winding pack is designed in order to obtain a small leakage inductance, which relaxes the control loop strength.

In this chapter a new two-stage solution is proposed, combining the advantages of the two different conversion steps: the first one is composed by the chain of a switched-capacitor voltage divider which feeds two counter-phased three-level buck converters, that enable regulation. The last stage, which yields V_{core}, is the novel high-density, fully-coupled, four-phases buck that behaves like a 4:1 transformer and enables DC flux cancellation.

4.2 Converter architecture

The whole converter is represented in Fig. 4.2. Input voltage V_{in} is first stepped-down through switched-capacitor blocks (*SC divider*, abbreviated with SC, and *Regulated 2-phases 3-level buck*, abbreviated with 3LB), yielding $V_{mid} = \frac{1}{2}V_{in}$ and $V_{IBx} = \frac{1}{4}V_{in}$ at nominal duty-cycle. The 2:1 DC divider and the following 3-level buck are synchronized, ensuring C_{SC}, C_{B1} and C_{B2} to be always soft-charged through the output inductors L_{out_1} and L_{out_2}: in fact, V_{mid} is not capacitive, as this would cause hard-charging for the first stage and high RMS currents for FETs SC_{Mx}[1].

The first stage is controlled with a commercial Constant-On-Time digital VMR controller (COT) which senses the V_{core} voltage and generates PWM signals Φ_α/Φ_β for the 3LB stage. These signals are used by the *synchronized square wave generator* to generate the

[1] In the real prototype a small capacitance was added to prevent excessive voltage drop of V_{mid} during certain conditions (discussed in Subsection 4.2.1): its value must remain small in order to maintain C_{SC} current-fed.

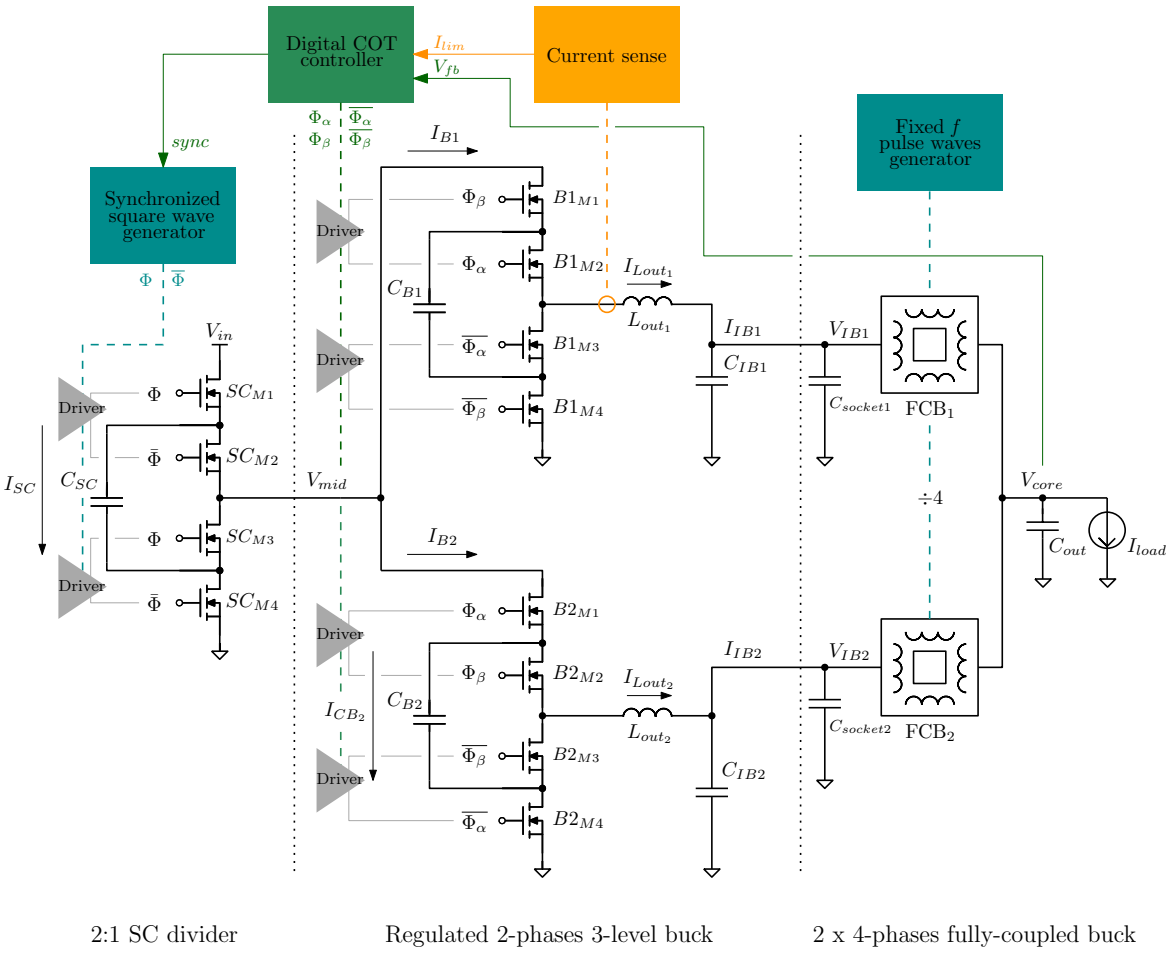


Fig. 4.2 Hybrid Regulated 48 V to 1.8 V Switched-Capacitor converter with Fully-coupled Buck PoL top-level schematic.

first switched capacitor stage square wave drive signal Φ, while the FCBs are independently controlled with a fixed-frequency, fixed-DC signal generator.

Of course, in order to maintain voltage balance in the input switched capacitor bank C_{SC}, phase shedding is not possible at this level; i.e. the two 3LB phases are always operating. Fig. 4.2 shows that the *digital COT controller* also uses the inductor current I_{lim}, which is only used to implement an over-current protection and not in the voltage regulation loop. Current sharing is intrinsically achieved as capacitor C_{SC} acts as an integrator on the phases current difference. In other words, in the case of a 3LB-FCB current path mismatch, C_{SC} drifts from $V_{in}/2$ restoring current balance: this behaviour is achieved separating the two 3LB outputs and merging them ant the FCB outputs. This C_{SC} unbalance manifests with node V_{mid} offsetting above $V_{in}/2$ during the less-conductive mismatched phase, and below $V_{in}/2$ during the other half switching cycle.

Capacitor banks C_{IB_x} and C_{socket_x}, which where separated to underline their different layout positions, decouple the first stage from the output fully-coupled buck converters (FCB): they are the output capacitors of the 3LB and the input capacitors of the FCB. This stage, composed of two paralleled blocks, implements a 4:1 DC transformer placed below the CPU/ASIC socket built with a custom ultra-thin ferrite core.

4.2.1 SC and Three-Level Buck stage

The first stage of Fig. 4.3 is composed by the 2:1 SC divider and the regulated 2-phases 3-level buck. These converters are synchronized: the SC divider operates at a fixed duty-cycle (DC) of 50 %, while the 3LB phases are driven by a COT controller with reference target frequency[2].

[2]The digital controller is *STmicroelectronics* and uses the STVCOT^{TM} algorithm. The controller operates with a classical COT loop that slowly changes the on-time to reach the target frequency.

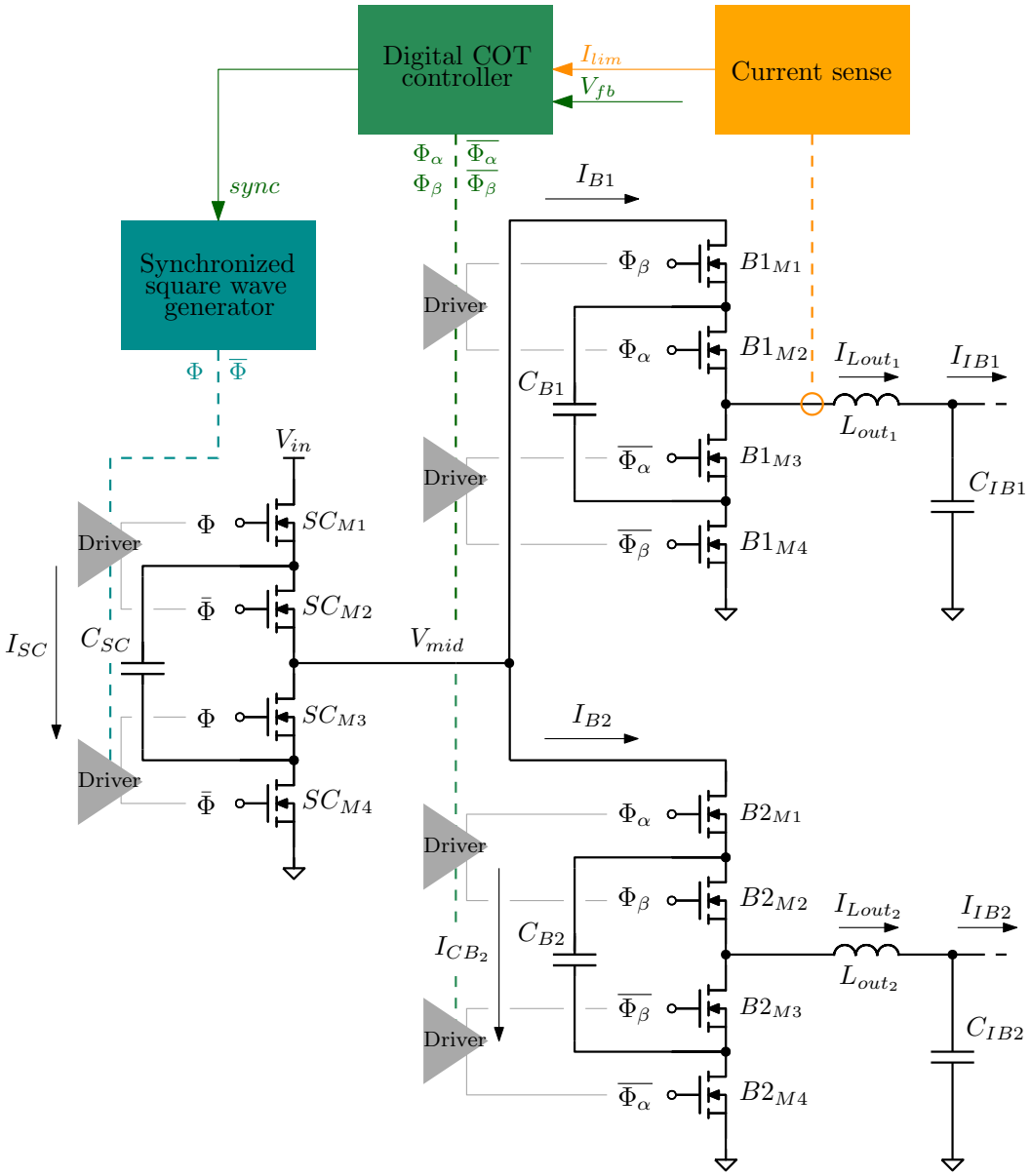


Fig. 4.3 First stage schematic.

To understand the converter steady-state operation, the resulting duty-cycle is considered. For the sake of simplicity, intermediate voltages are supposed to be equal, i.e. there is no FCB modules mismatch and the following relations hold:

$$V_{IB1} = V_{IB2} = V_{IB} \tag{4.1}$$

$$\mathrm{DC}_1 = \mathrm{DC}_2 = \mathrm{DC} \tag{4.2}$$

where DC_x is the duty-cycle of 3LB phase x. For the 48 V/54 V to 1.8 V conversion, as the FCB behaves like a 4:1 transformer, the intermediate bus voltage must be regulated to

$$V_{IB_{nom}} = 7.2 \text{ V} \tag{4.3}$$

The steady-state operating voltage for the switched capacitors C_{SC} and C_{Bx} can be derived applying the charge-balance, and corresponds to

$$V_{C_{SC}} = \frac{V_{in}}{2} = V_{mid} \tag{4.4}$$

$$V_{C_{Bx}} = \frac{V_{mid}}{2}$$

The steady-state 3LB gain is the same of the standard buck converter; in fact, observing the waveforms of Fig. 4.5, 4.7 and 4.9 the output voltage is the same as the input when DC = 100 % and it is zero when DC = 0 %. Therefore, its conversion ratio and the steady-state duty-cycle for this application can be calculated from (4.4):

$$V_{IB} = \mathrm{DC} \cdot V_{mid} \tag{4.5}$$

$$\mathrm{DC}_{nom} = 2 \cdot \frac{V_{IB_{nom}}}{V_{in}} = 0.3 \tag{4.6}$$

It is interesting to analyse the 3LB waveforms for different duty-cycles, in particular on the 50 % boundary. Fig. 4.4 shows the converter switches configurations when DC = 50 %, while Fig. 4.5 reports the corresponding waveforms. In this operation mode the output current ripple is almost zero, as V_{ph_x} is alternatively V_{CB_x} or $V_{mid} - V_{CB_x}$, both equal to $V_{in}/4$.

Fig. 4.6 shows the converter switches configurations when DC < 50 %, with the corresponding waveforms of Fig. 4.7. In this case, phase nodes V_{ph_x} see a 0 V period with switches

B_{xM3} and B_{xM4} active at the same time. Current ripple increases as the voltage excitation is not constant any more.

The situation with DC > 50 % is shown in Fig. 4.8 and Fig. 4.9. Now, phase nodes V_{ph_x} have a V_{mid} period with switches B_{xM1} and B_{xM2} active at the same time. In this case the first stage loses the ZCD condition, as the 3LB phases don't turn off before its commutation and C_{SC} must withstand both the buck phases currents during the overlap.

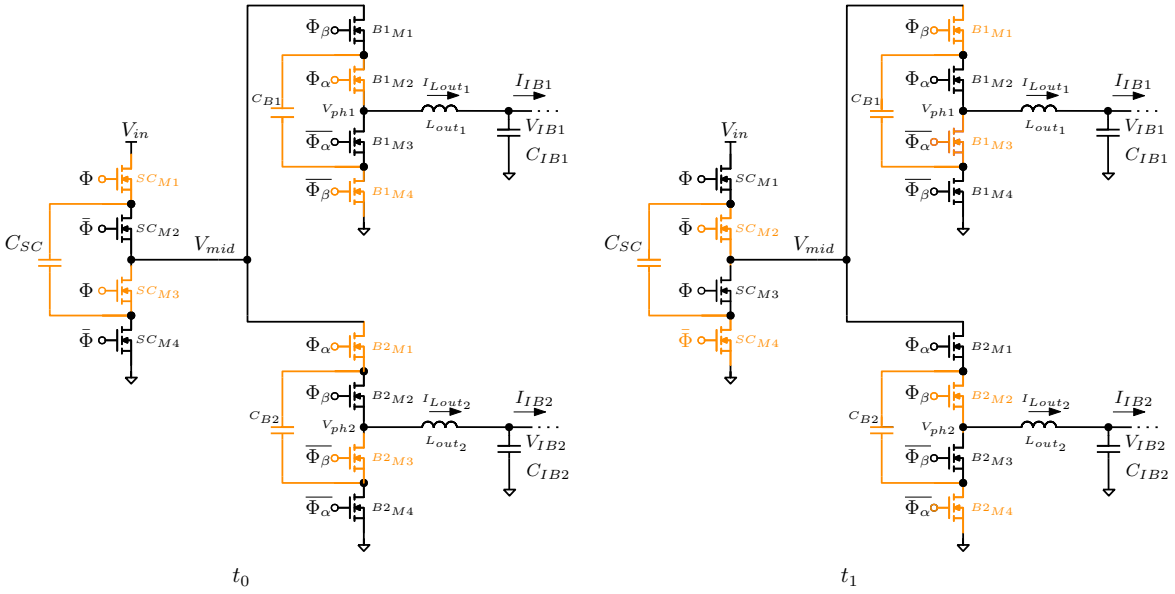


Fig. 4.4 First stage operating pattern at DC = 50 % with the waveforms of Fig. 4.5.

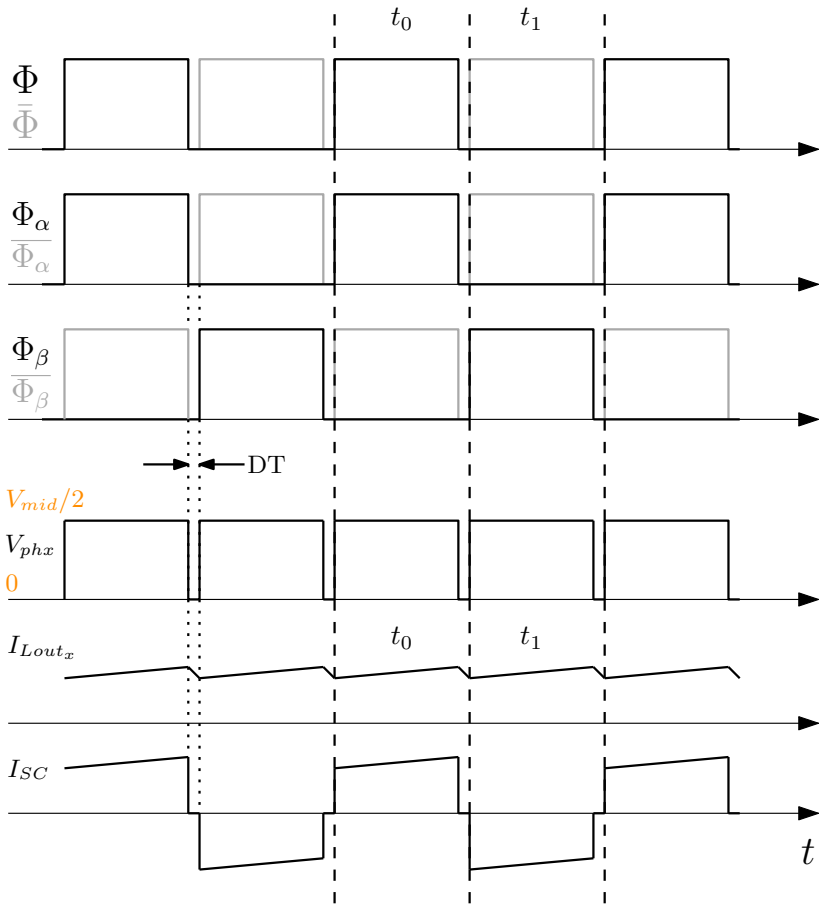


Fig. 4.5 First stage waveforms at DC = 50 %. The dead-time effects on the $V_{ph,x}$ and on the inductor current I_{Lout_x} were exaggerated.

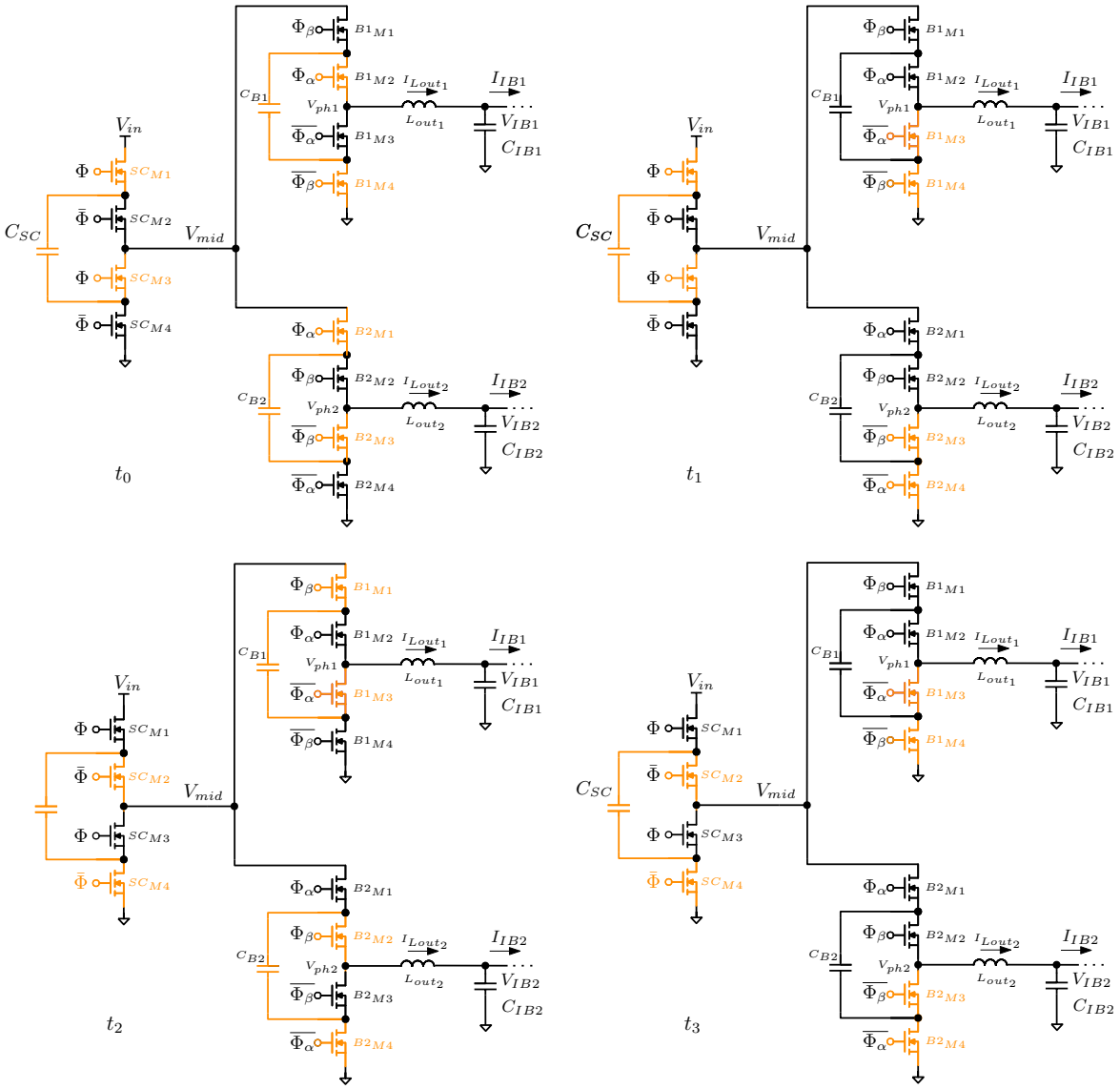


Fig. 4.6 First stage operating pattern at DC < 50 % with the waveforms of Fig. 4.7.

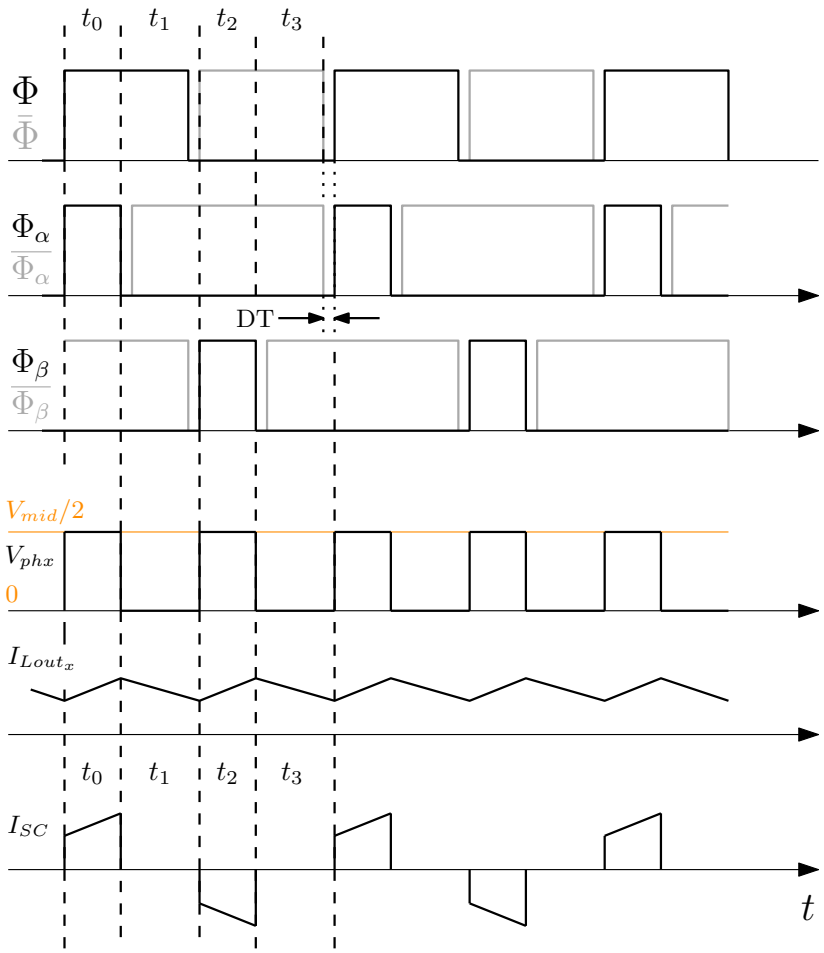


Fig. 4.7 First stage waveforms at DC < 50 %.

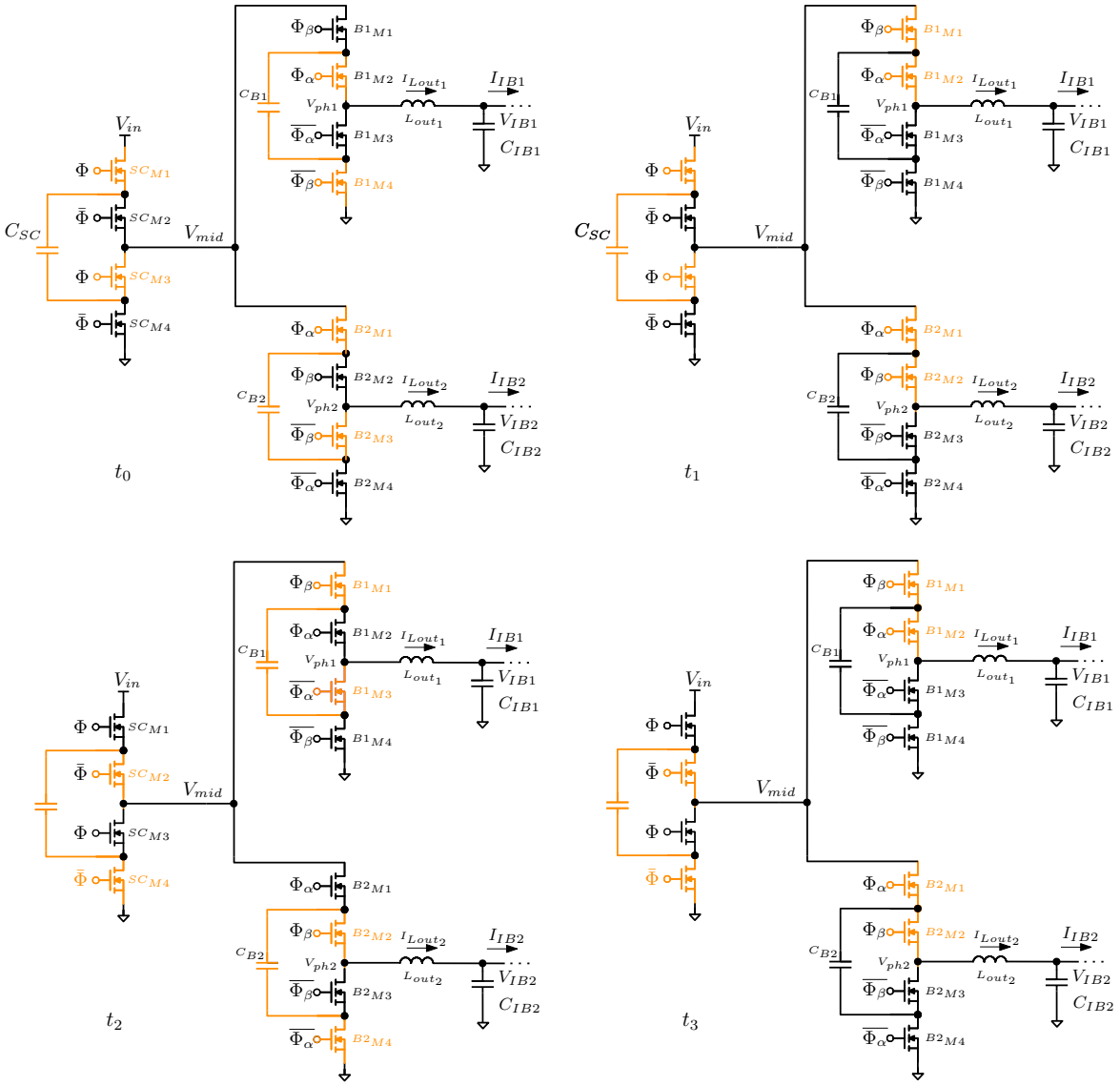


Fig. 4.8 First stage operating pattern at DC > 50 % with the waveforms of Fig. 4.9.

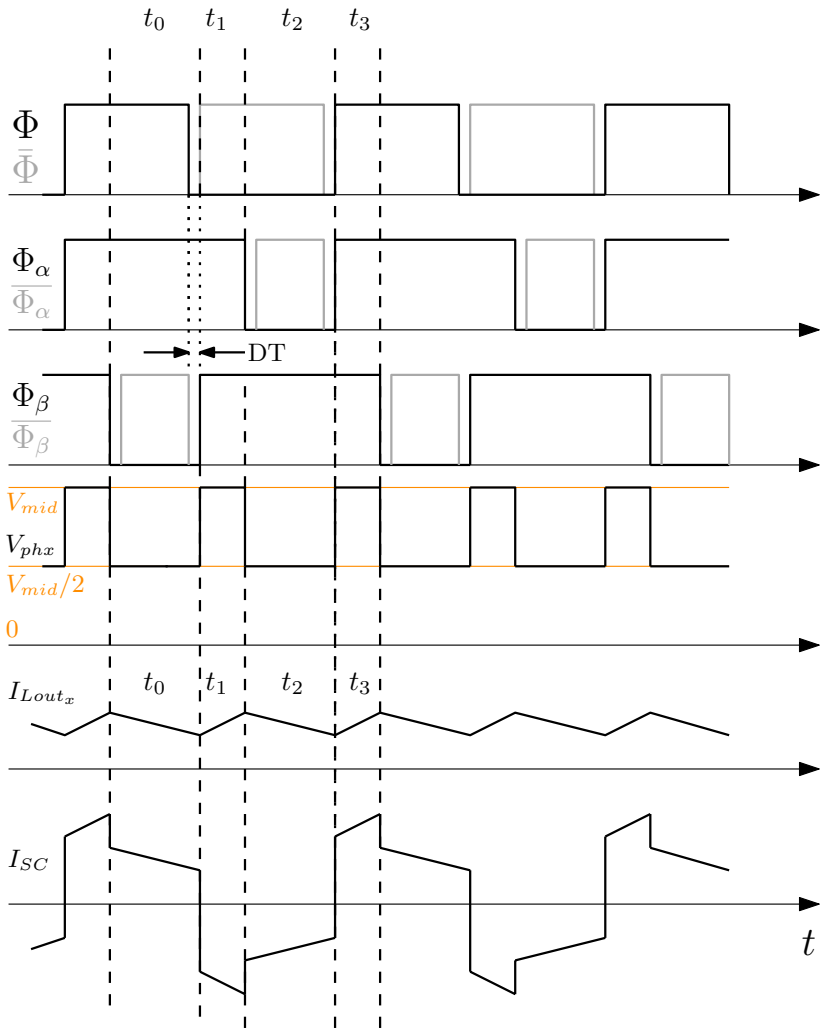


Fig. 4.9 First stage waveforms at DC > 50 %.

4.2.2 Fully-coupled Buck 4:1 PoL

The last stage of the conversion chain is the fully-coupled buck, operating a 4:1 fixed voltage conversion. This converter is placed below the CPU/ASIC socket and determines the point-of-load performances of the whole converter, as its output capacitors, connection layout and intrinsic impedance (together forming the power distribution network, already discussed for the converter of Section 2) weight on the impedance seen by the socket.

This stage carries the full digital load current and must have a low impedance, as the digital controller acting on the 3LB has to regulate V_{core} transients with wide bandwidth. Besides, equivalent series-resistance must be low in order to achieve high efficiency.

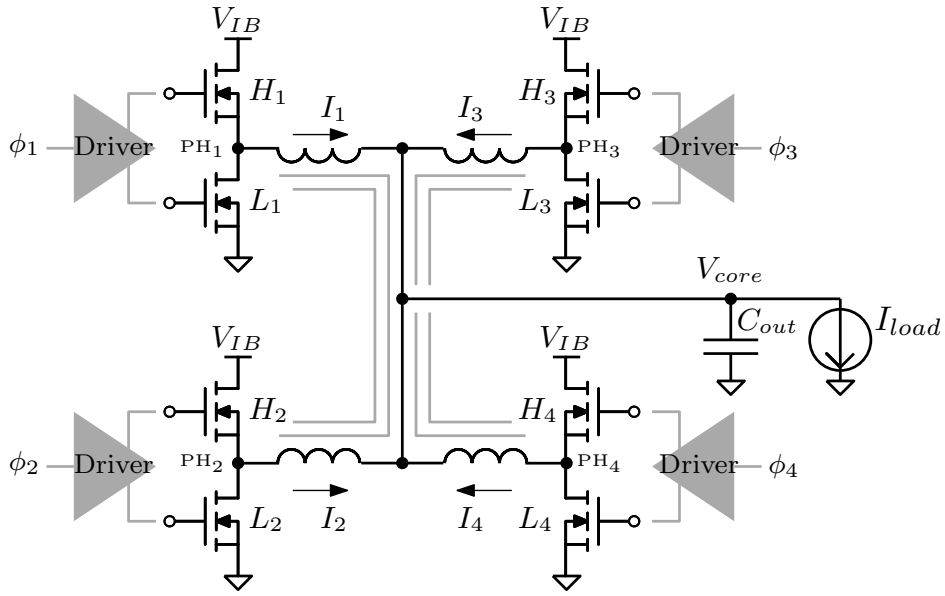


Fig. 4.10 Fully-coupled buck converter equivalent schematic. The grey lines indicate a fully coupled, symmetric structure. ϕ_x indicate the drivers input PWMs signals.

The equivalent schematic of the proposed converter is reported in Fig. 4.10, where the grey lines indicate a fully-coupled magnetic structure. This device, which is one of the *squares* represented in Fig. 4.2, is composed of four half-bridges driven with a fixed pulse wave at fixed frequency and fixed 25 % duty-cycle. Each phase is powered for exactly $T_{sw}/4$; i.e. there is no dead-time between a phase change but only during an half-bridge (H_x/L_x) commutation. In other words, the half-bridges dead times are compensated with an anticipated turn-on of the next phase as, otherwise, the core would be *shorted*.

The proposed solution is a novel approach to solve the inductor volume/phase current correlation limit. Delegating regulation to the previous stage and minimizing series impedance enables DC magnetic flux complete cancelling. As a consequence, core dimension is now designed as a function of copper losses and AC magnetizing flux.

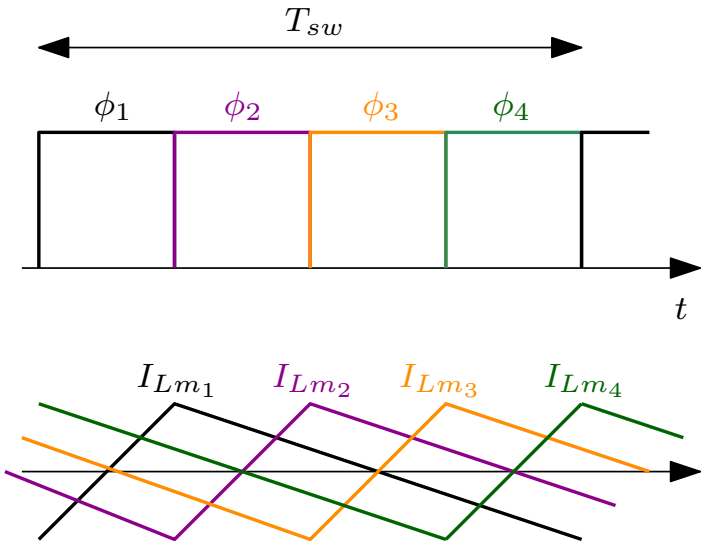


Fig. 4.11 Fully-coupled buck converter timings and magnetizing currents.

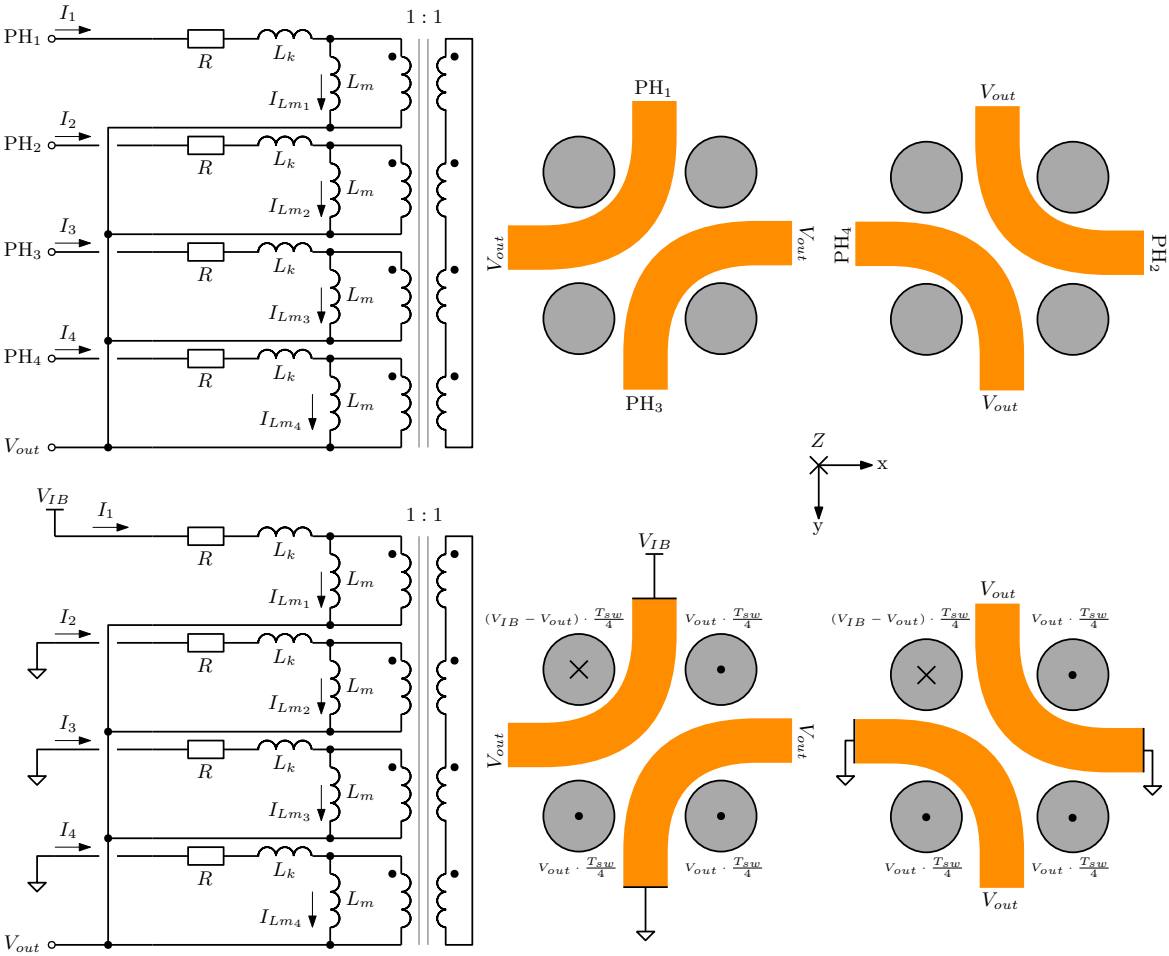


Fig. 4.12 Fully-coupled buck converter equivalent magnetic circuit (left) and planar winding implementation (right) with PH1-ON operation (bottom).

The fully-coupled magnetic structure is composed of planar windings developed around a custom 4-legged ferrite core. To understand its shape and operation logic, it's important to observe the driving signals and corresponding phase currents of Fig. 4.11, the equivalent magnetic circuit (Fig. 4.12, left) and the planar winding topology of(Fig. 4.12, right). The rendered view of the entire device, with the clamped ferrite core, is shown in Fig. 4.14.

The DC magnetic flux cancellation, which is the main advantage given by this solution, is achieved by mean of the common ferrite core. Fig. 4.12 (bottom) shows the *volt · second* flux configuration when phase 1 in active, i.e. its winding is connected to the input voltage V_{IB} and the others are connected to 0 V. During this ϕ_1 period, winding 1 voltage is clamped to $V_{IB} - V_{out}$. As each winding has a single turn, magnetic flux increases of $(V_{IB} - V_{out}) \cdot \frac{T_{sw}}{4}$ during ϕ_1 in this leg. This flux spreads inside the *ferrite plates* shown in Fig. 4.13 and the splits among the other three legs, whose windings are connected to V_{out} (note that flux direction is opposed to leg 1). Leg fluxes, represented by the magnetizing currents of Fig. 4.11 (bottom), complete their cycle in a T_{sw}. With this operation, DC magnetic flux is cancelled and the leg cross-section depends only on T_{sw} and $V_{IB} - V_{out}$, enabling an extreme magnetic volume reduction.

As phase currents I_x are virtually constant, high-frequency operation can be reached without incurring in *eddy-current* losses, which can affect efficiency in the classic inductor. As this topology has no soft-switching, frequency is still bound to switching losses.

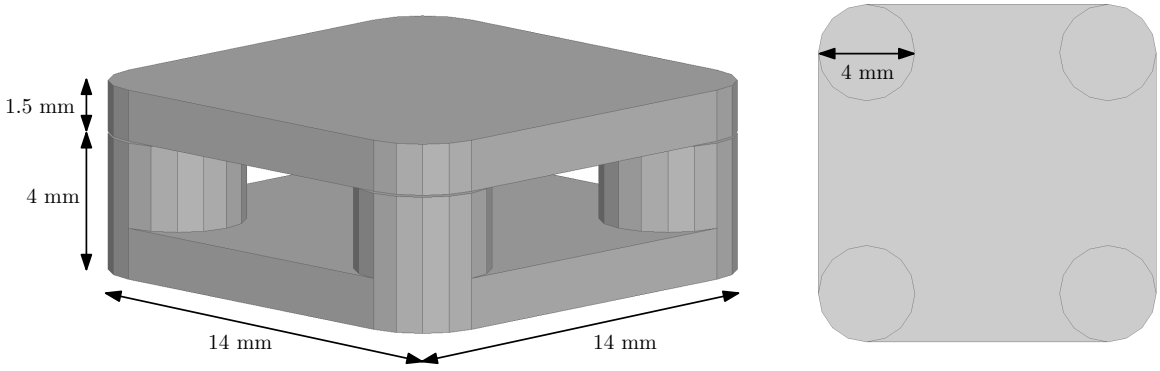


Fig. 4.13 Ferrite core used to fully-couple the converter winding swith dimensions. Isometric view (left) and top view (right).

As this converter's series impedance must be minimal in order to allow high bandwidth, the winding physical structure must be highly-coupled; i.e. leakage flux must be low. This specification is addressed by designing couples of interleaved windings, as reported in Fig. 4.12 (right).

Phase current sharing can be achieved inside a single module with duty-cycle regulation. As the magnetic flux among the legs must always be balanced, when a phase is *boosted*

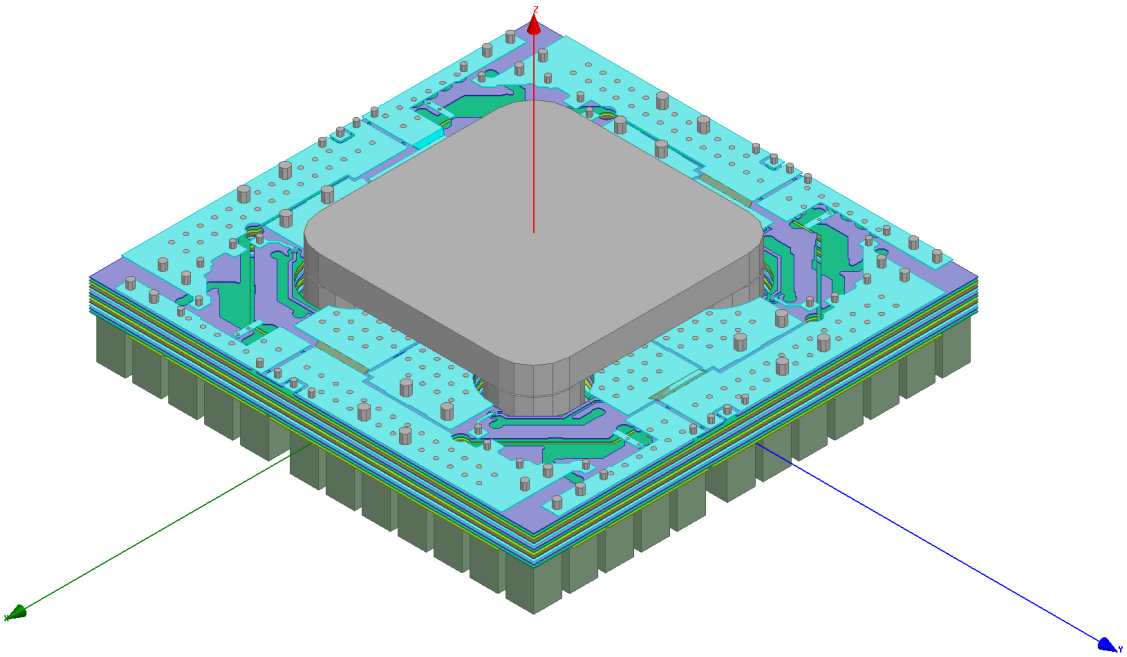


Fig. 4.14 Entire fully-coupled buck converter render. The bottom cubes are used to connect this device to the main board. At the center the 4-legged core is closed through 4 PCB holes. Windings develop on internal layers while semiconductors are placed on the top.

through duty-cycle stretching the others must be reduced of $1/3$ of the same amount. In other words, there must always be one active-high phase and three active-low ones with no ϕ_x overlapping. Current sharing has proven to be easily achieved with this technique, which is explained in Fig. 4.15.

It is straightforward to scale this architecture to different transformation ratios and/or different power capabilities. Steady-state transformation ratio is simply given by the inverse of the phase count N:

$$\frac{V_{out}}{V_{in}} = \frac{1}{N} \tag{4.7}$$

as the converter can be interpreted as a classical multi-phase buck where each phase is shifted by an amount T_{SW}/N and driven with a duty-cycle of $1/N$. The core must maintain a full coupling among the phases, i.e. each winding must develop along the same direction and must embrace only one leg, possibly with a Z symmetry.

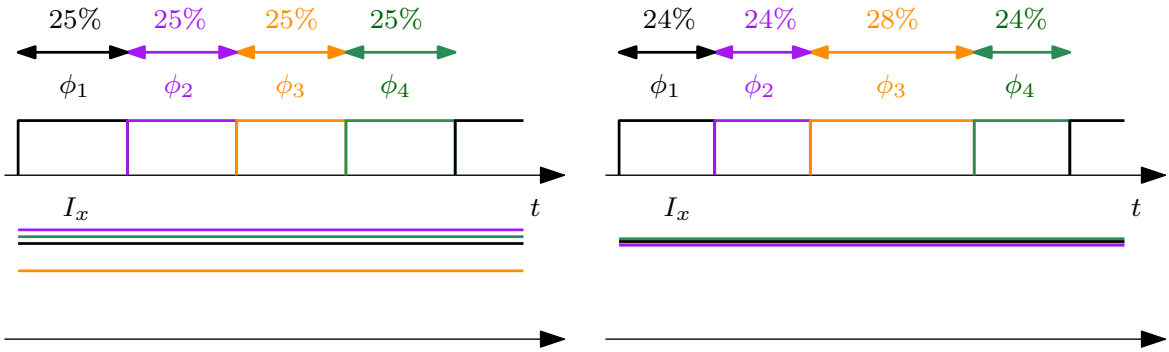


Fig. 4.15 Module phases current sharing regulation achieved through duty-cycle repartitioning. Current unbalance (left) is resolved by boosting ϕ_3 of +3 % and decreasing $\phi_{1,2,4}$ by -1 %. Reported waveforms and duty-cycle corrections are extremized, as in the real case much smaller corrections are sufficient.

4.3 Experimental results

A 360 W experimental prototype has been built for the 48 V to 1.8 V regulated conversion, able to reach 600 W when operating as a 4:1 unregulated divider. The switched capacitor stage, which is composed by the SC divider and the 3LB regulated block, occupies an *eight-brick* area, comprising digital regulator, pre-bias logic and drivers. The PoL stage is a composed of two PCB modules, with the clamped ferrite core, connected below the CPU socket by mean of brass *power pins* together with two arrays of ceramic capacitors. Converters' specifications are summarized in Table 4.1 for the SC stage and in Table 4.2 for the FCB. The prototype board is shown in Fig 4.16.

Experimental results are split into two sections for the two stages, where more detailed pictures are included.

Table 4.1 Converter and PCB specifications for the SC-3LB stage.

$V_{in,nom}$	48 V / 54 V
$V_{out,nom}$	7.2 V
$I_{out,max,continuous}$	50 A
$P_{out,max,thermal}$	360 W
f_{sw}	205 kHz
PCB power area	*Eight-brick* (58 mm × 23 mm)
Maximum height	7 mm
PCB layer count	14
PCB copper weight	35 μm
SC stage MOSFETs	4 × BSZ025N04LS
SC stage switched capacitors	6 × 10 μF, 1210 (GRM32ER71J106KA12)
3LB stage MOSFETs	8 × BSZ013NE2LS5I
3LB stage switched capacitors	14 × 10 μF, 0603 (GRM188R6YA106MA73)
3LB inductors	2 × Coilcraft XAL7070-1μH
Input capacitors	4 × 4.7 μF, 1210 (GRM32ER71K475ME14)
3LB output capacitors C_{IB}	10 × 22 μF, 1206 (GRM31CC81E226ME11)
Socket FCB input capacitors C_{socket}	*not mounted*
Socket V_{core} capacitors C_{out}	180 × 22 μF, 0402 (GRM155C80E226M)

Table 4.2 Converter and PCB specifications for the FCB stage (single module).

$V_{in,nom}$	7.2 V
$V_{out,nom}$	1.8 V
$I_{out,max,continuous}$	100 A
$P_{out,max,thermal}$	180 W
f_{sw}	520 kHz
PCB power area	25 mm × 25 mm
Total module height (comprising *power pins*)	6.4 mm
PCB layer count	14
PCB copper weight	35 μm
Half bridge ICs	Integrated, w/ drivers PN not disclosed (3.2 mm × 7 mm)
Input capacitors	12 × 4.7 nF, 0402, PN not disclosed 4 × 1 μF, 0603, PN not disclosed 4 × 10 μF, 0603 (GRM188R61C106MA73D)
Output capacitors	32 × 100 μF, 0805 (GRM21BC80G107ME15)
Brass *power pins*	80 × (1.6 mm × 1.6 mm × 2.8 mm)

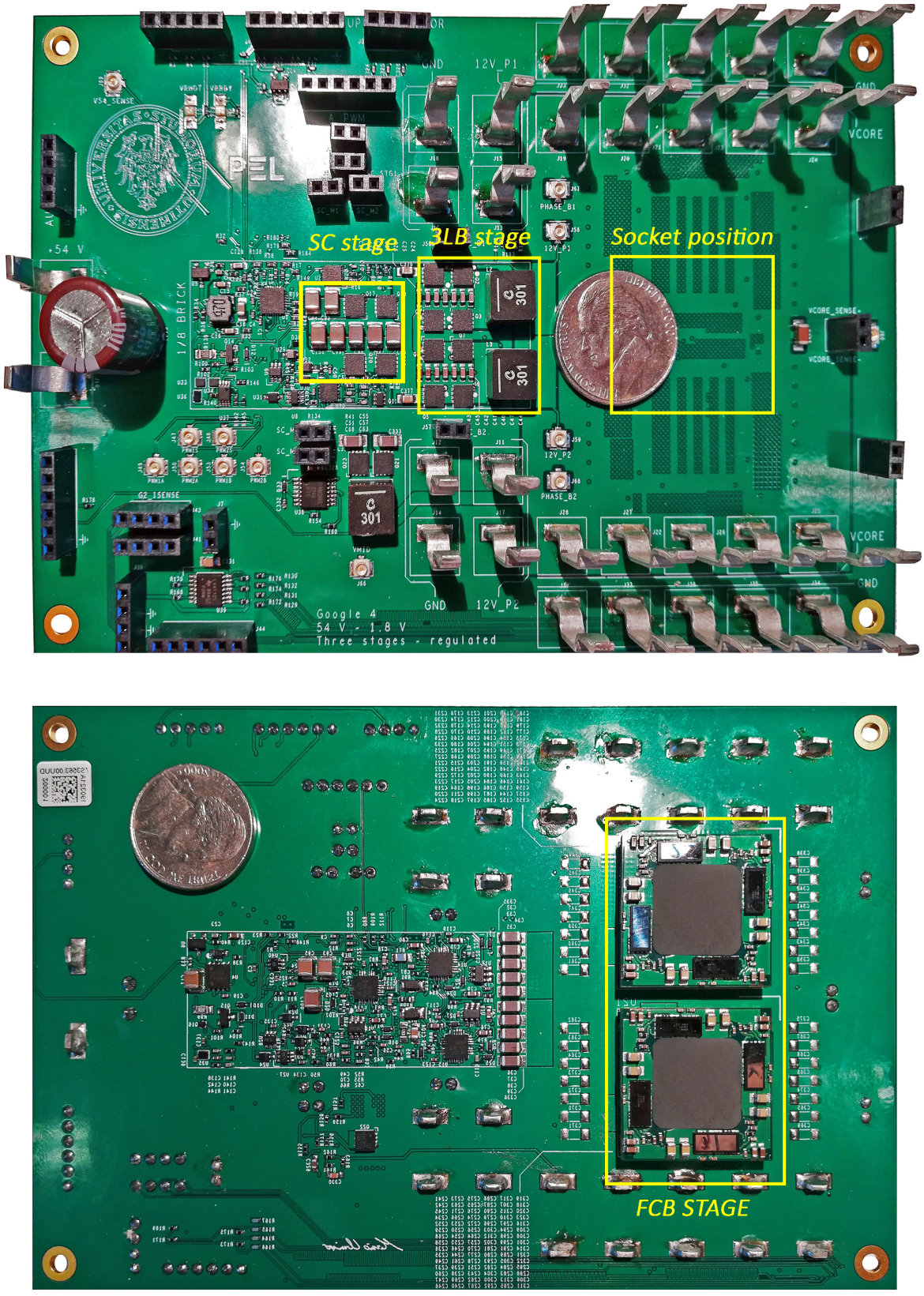


Fig. 4.16 Regulated 48 V to 1.8 V switched capacitor converter with fully-coupled buck PoL 360 W prototype. Top and bottom views of the *motherboard*.

4.3.1 Switched capacitor and three-level buck stage

The SC-3LB regulated stage is reported in Fig 4.17, with the naming convention of Fig 4.3 (only M_x labels are reported, as the SC/3LB positions have already been noted).

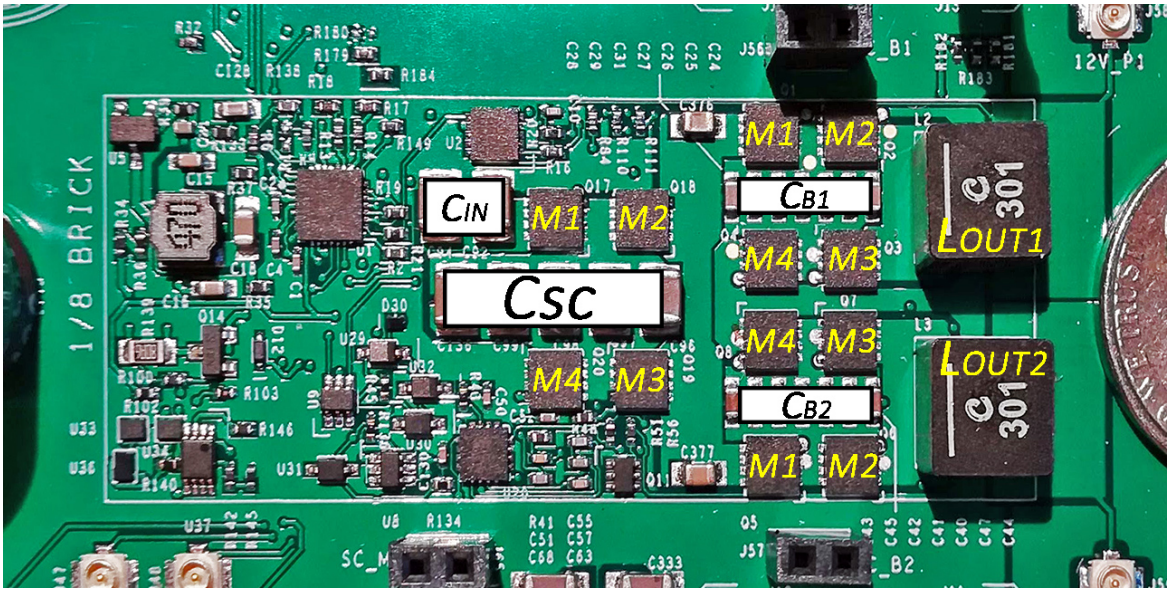


Fig. 4.17 Switched capacitor stage (SC) and three-level buck (3LB) on the PCB prototype (top view) with corresponding MOSFET naming as in Fig 4.3.

This stage is evaluated at the nominal 30 % duty-cycle of (4.5), and when it's used as an unregulated 4:1 voltage divider achieving a 54 V to 13.5 V, i.e. at 50 % duty-cycle. The latter case is interesting as this stage becomes the series of a two-stage switched-capacitor voltage divider, where inductor current ripple is virtually cancelled achieving high efficiency.

Fig 4.18 shows main converter waveforms when operating at 30 % duty-cycle. This picture clearly shows the current-driver charge and discharge of 3LB switched capacitors C_{Bx} (blue and yellow). Phase 1 voltage is reported in purple, together with ϕ_α and ϕ_β control signals. This image is the same of the ideal waveforms anticipated in Fig 4.7.

Fig 4.19 shows the equivalent case of Fig 4.5, i.e. when the converter is operating near the 50 % duty-cycle, and Fig 4.20 reports the first stage capacitor C_{SC} AC-coupled voltage at fixed 50 % duty-cycle.

Fig 4.21 shows converter efficiency for different conversion rations, inductors and frequencies. Please note that this curve was measured in thermal steady state, therefore this was not measured during a load transient. These efficiency families were measured to understand the converter performance in different contexts: when regulating (DC = 30 %), the efficiency maximum is found with the nominal 1 μH inductor and lower frequencies (intermediate curves). We this architecture operates close to the 4:1 ratio (DC = 50 %), L_{outx} current

ripple decreases and a smaller inductor value of 300 nH can be used with the same package, therefore reducing conduction losses (upper curves). The same small-valued inductor must be used at high frequency when regulating to avoid saturation, degrading efficiency due to the increased AC copper losses, switching losses and core losses. Finally, Fig 4.22 reports two thermal images in free air convection for two load conditions when the converter operates with DC = 30 %.

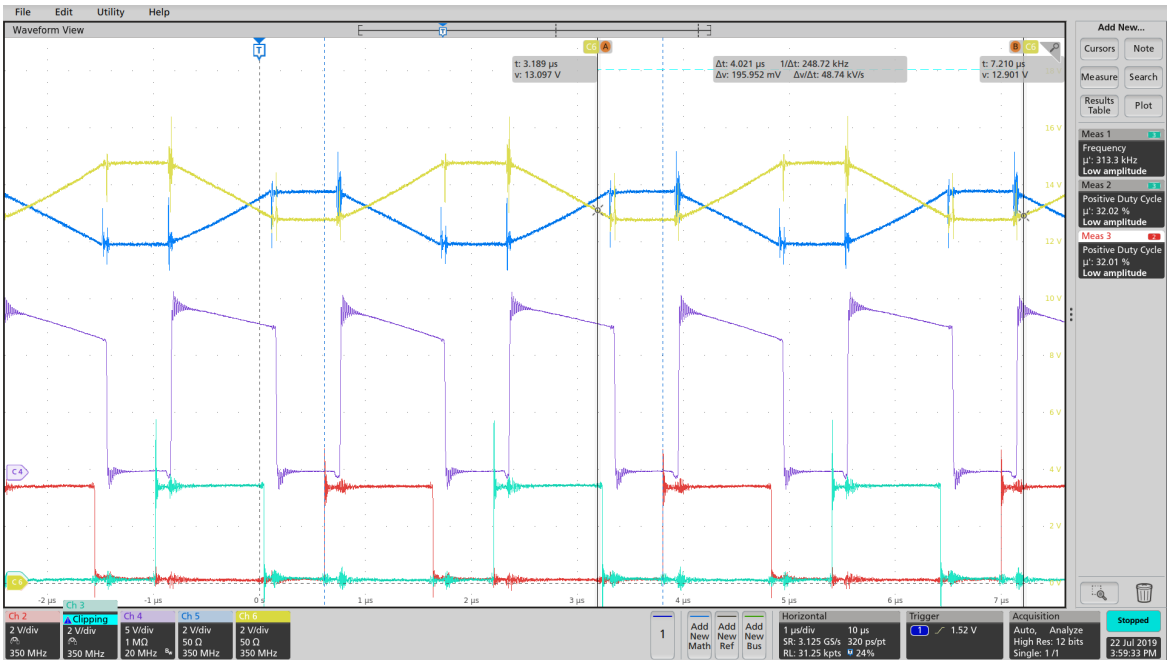


Fig. 4.18 Main converter waveforms. V_{CB1} and V_{CB2} (blue and yellow), buck phase 1 voltage (purple) and ϕ_α, ϕ_β control signals. V_{in} = 54 V, $V_{IB1} = V_{IB2}$ = 8 V, $I_{IB1} + I_{IB2}$ = 38 A. f_{sw} = 260 kHz.

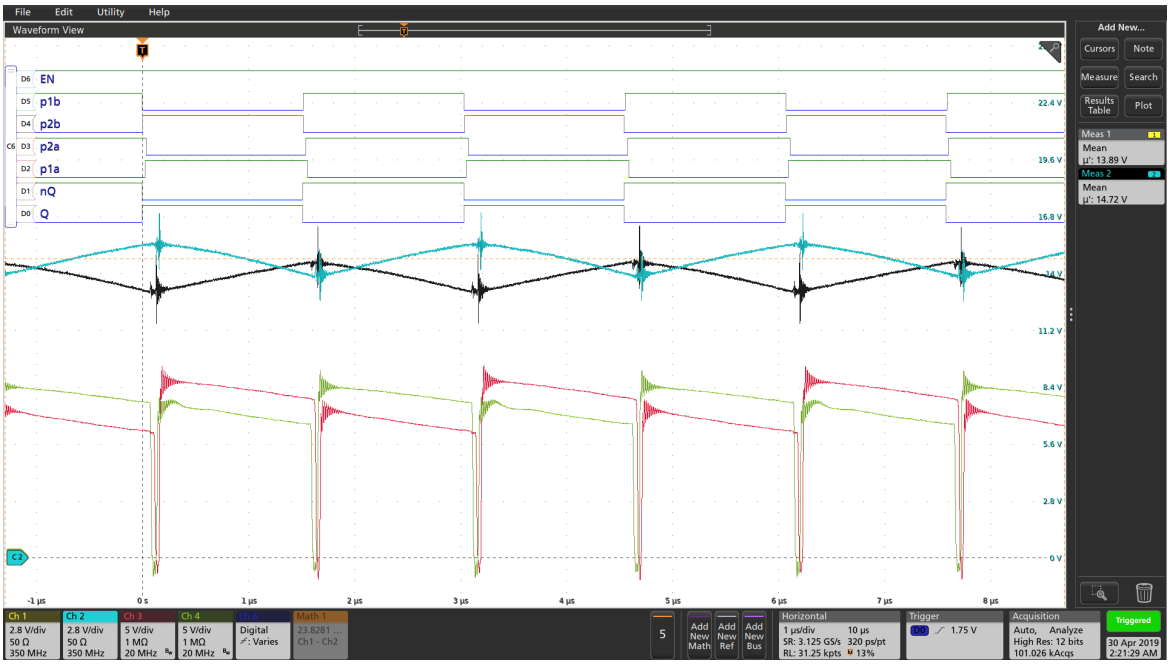


Fig. 4.19 Main converter waveforms at fixed DC = 50 %. Internal PWM signals (digital probe), V_{CB1} and V_{CB2} (light blue and black) and phase 1/2 voltages (green and red). V_{in} = 54 V, $V_{IB1} = V_{IB2}$ = 12.9 V, $I_{IB1} + I_{IB2}$ = 17 A. f_{sw} = 330 kHz.

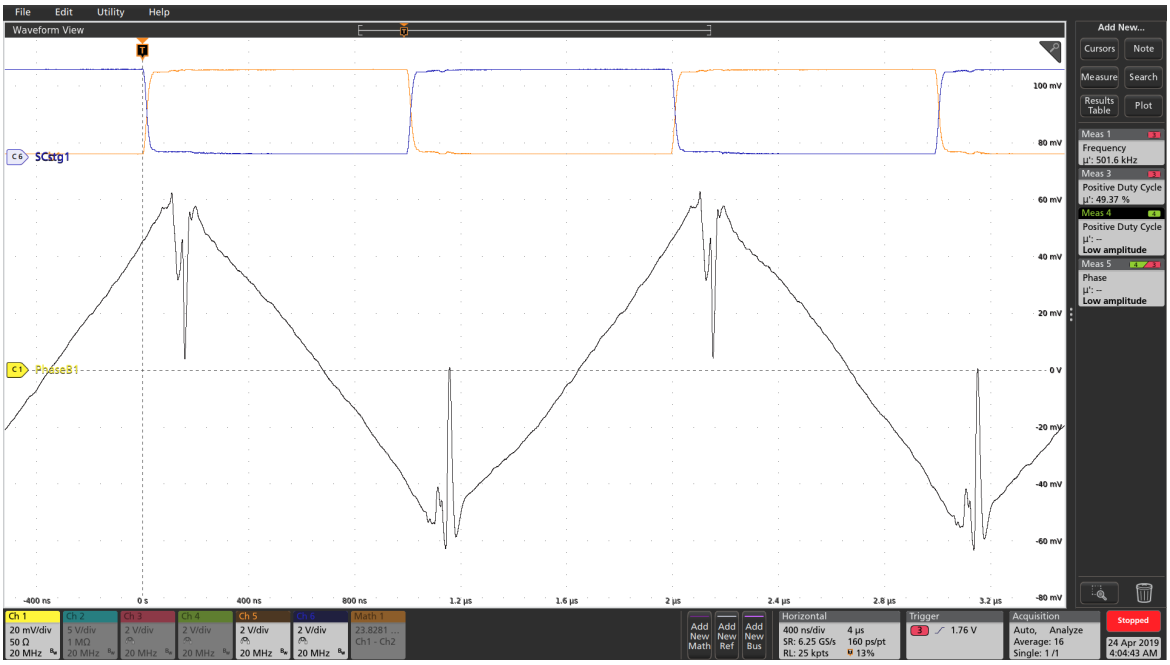


Fig. 4.20 First stage switched capacitor C_{SC} voltage (bottom) and first stage square wave driving signals at fixed DC = 50 %. V_{in} = 54 V, $V_{IB1} = V_{IB2}$ = 13.4 V, $I_{IB1} + I_{IB2}$ = 1 A. f_{sw} = 500 kHz.

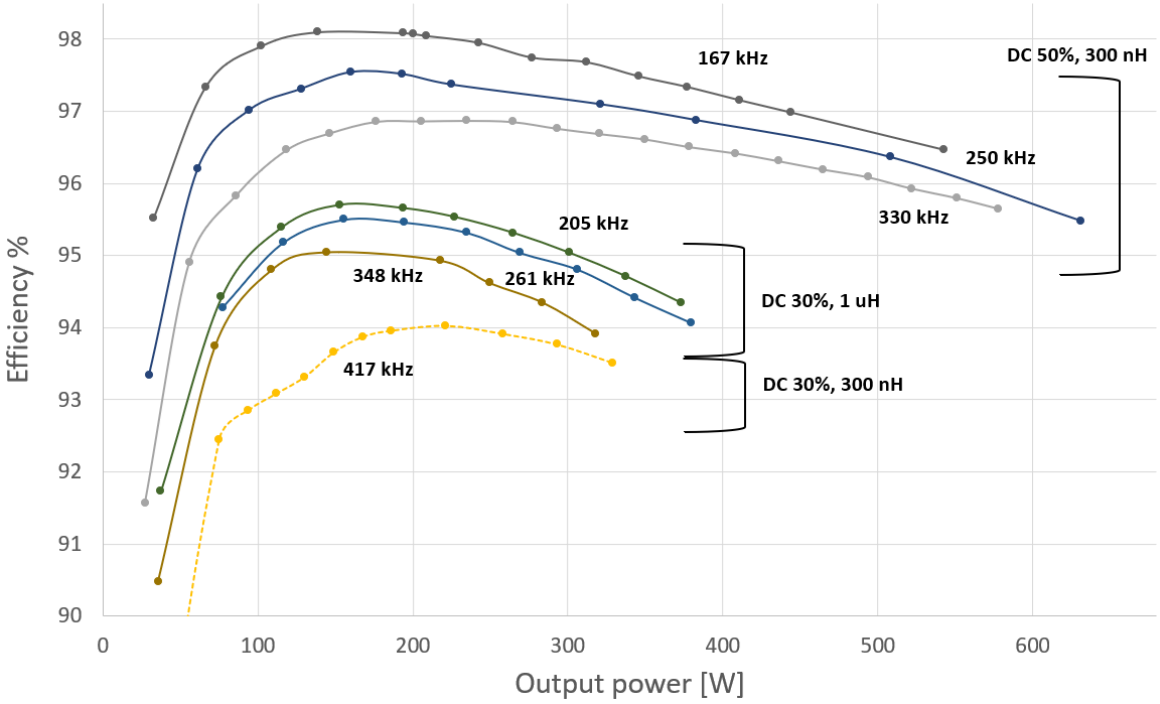


Fig. 4.21 First stage efficiency with different conversion rations, inductors and frequencies. V_{in} = 54 V. Thermal steady state.

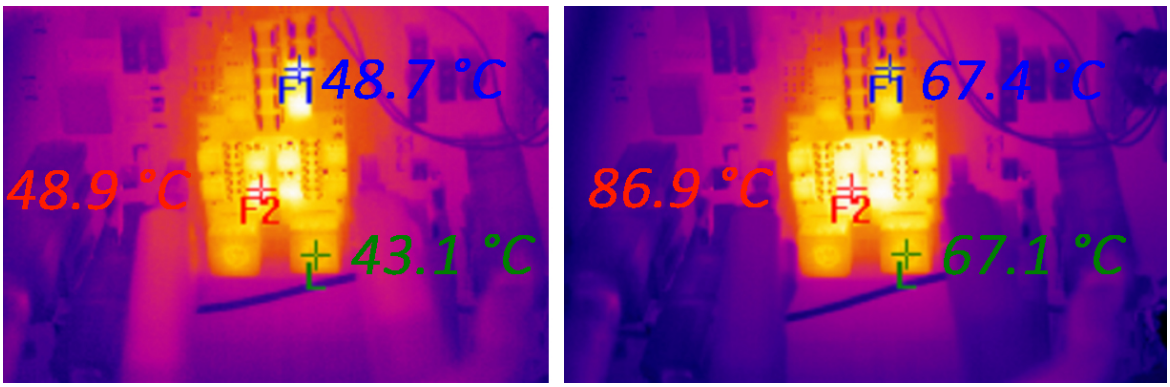


Fig. 4.22 Thermal images at $I_{IB1} + I_{IB2}$ = 20 A (left) and 43 A (right). F_1 marker corresponds to SC_{M1} MOS, F_2 to $B2_{M3}$, L to $L_{out}1$. Fixed DC = 30 %, V_{in} = 54 V, $V_{IB1} = V_{IB2}$ = 7.6 V, f_{sw} = 348 kHz.

4.3.2 Fully-coupled buck stage

The fully-coupled buck modules are mounted on the bottom-side of the main board, as shown in Fig 4.23 and Fig 4.24, where core plates were removed to show the core structure. As they deliver the full CPU/ASIC supply current, the connection must be close to the socket and PDN must be carefully designed. To achieve these goals, an array of V_{core} ceramic capacitors is placed on the main board, beneath the FCB modules. *Power pins* are designed to yield the required space to this capacitor array and are parallelized to minimize series resistance.

Components are placed only on the *top* side of the module, while internal layers are used for windings implementation as anticipated in Fig 4.14. The bottom layer connects the *power pins* to the various signals and input/output power rails. In Fig 4.23 the FCB integrated half-bridge ICs (denoted as HB) are shown: these devices implement a full PWM-controller half bridge with internal drivers and adaptive dead-time generation. This structure is symmetrically repeated with a 90° around the Z axis, i.e. around the PCB-normal axis intersecting the core center.

This architecture is characterized by almost-constant phase currents (the same holds for the output current, which is the summation of the first ones). As a consequence, the current flowing in the power pins is not affected by high-frequency copper losses, therefore no *skin effect* manifests and the full conductive volume is exploited.

Fig 4.25 depicts the overall converter efficiency of a single module at nominal f_{sw} = 520 kHz, reaching a peak 95.5 % at 80 W[3]. Please note that this curve was measured in thermal steady state, therefore this was not measured during a load transient. Same-conditions thermal images are shown Fig 4.26, where the power modules and core temperatures are reported. These images show a small temperature imbalance affecting phases 2 and 3, which is due to the finite resolution of the pulse-wave generator used for these modules.

[3]This measurement was performed with the same approach described in 2.5.

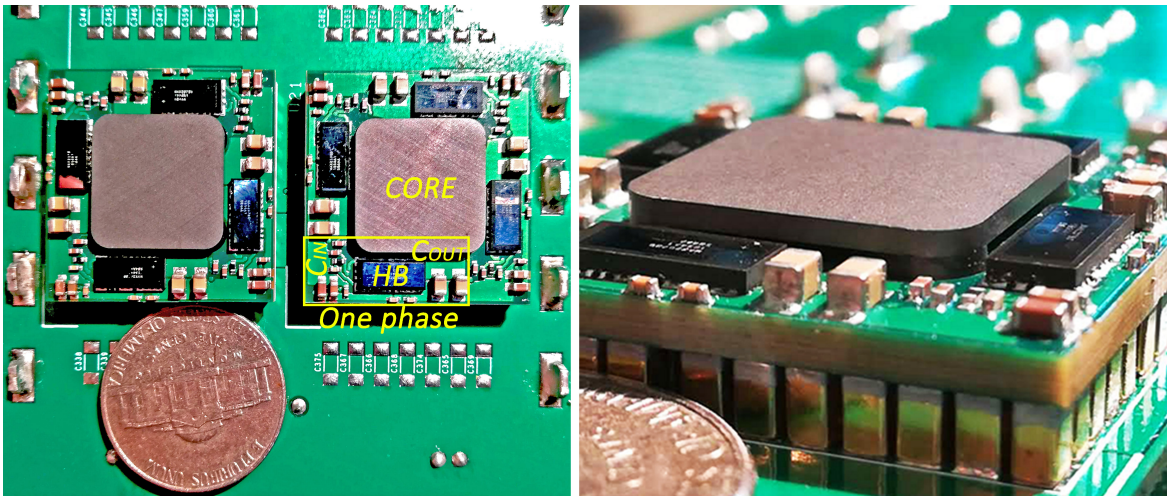


Fig. 4.23 Fully-coupled buck mounted on the bottom side of the main board (left) and detail of the brass *power pins* used for the connection.

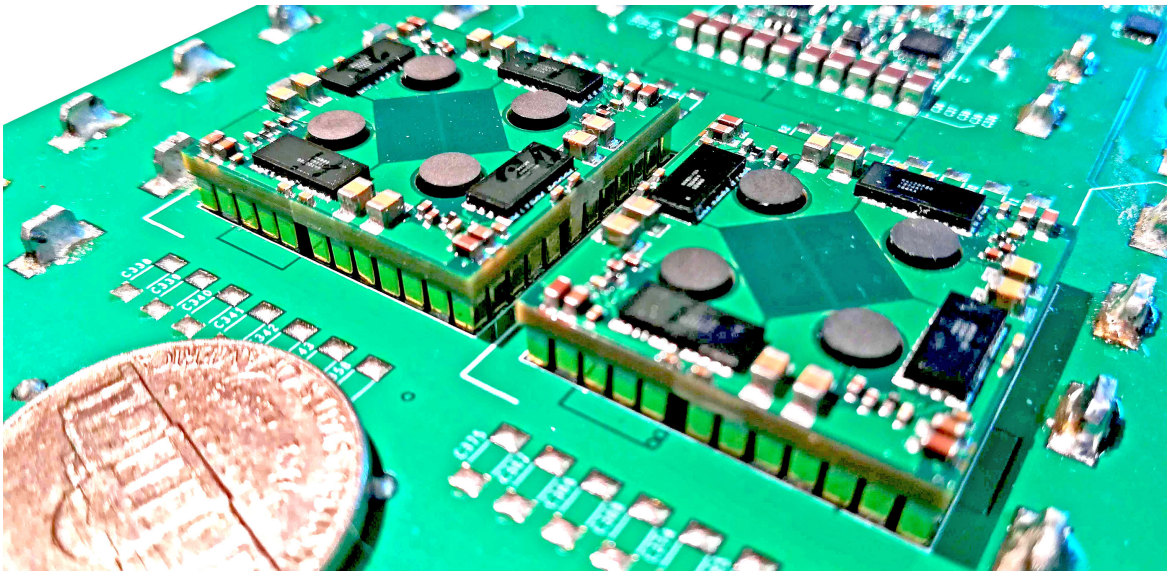


Fig. 4.24 Fully-coupled buck mounted on the bottom side of the main board without core plates.

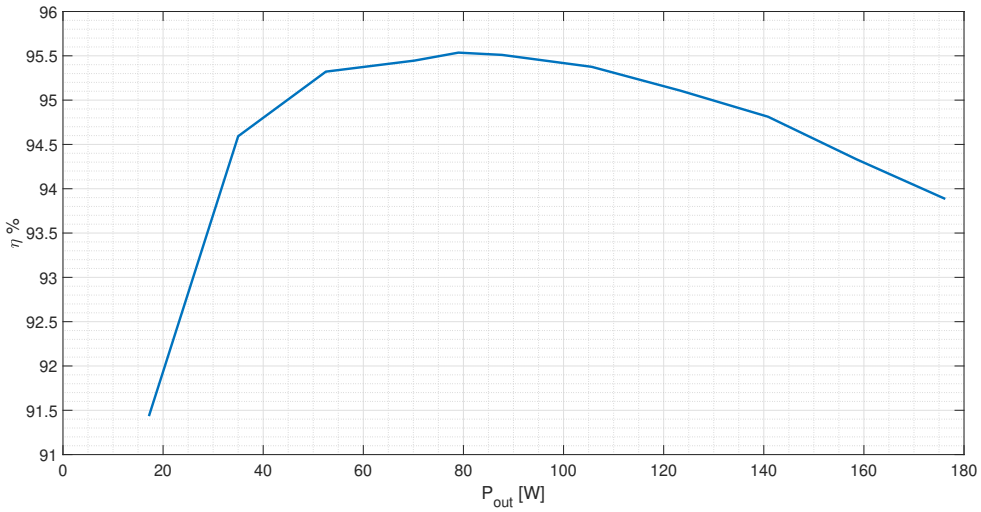


Fig. 4.25 Fully-coupled buck converter efficiency. V_{in} = 7.2 V, f_{sw} = 520 kHz. Single module. Thermal steady state.

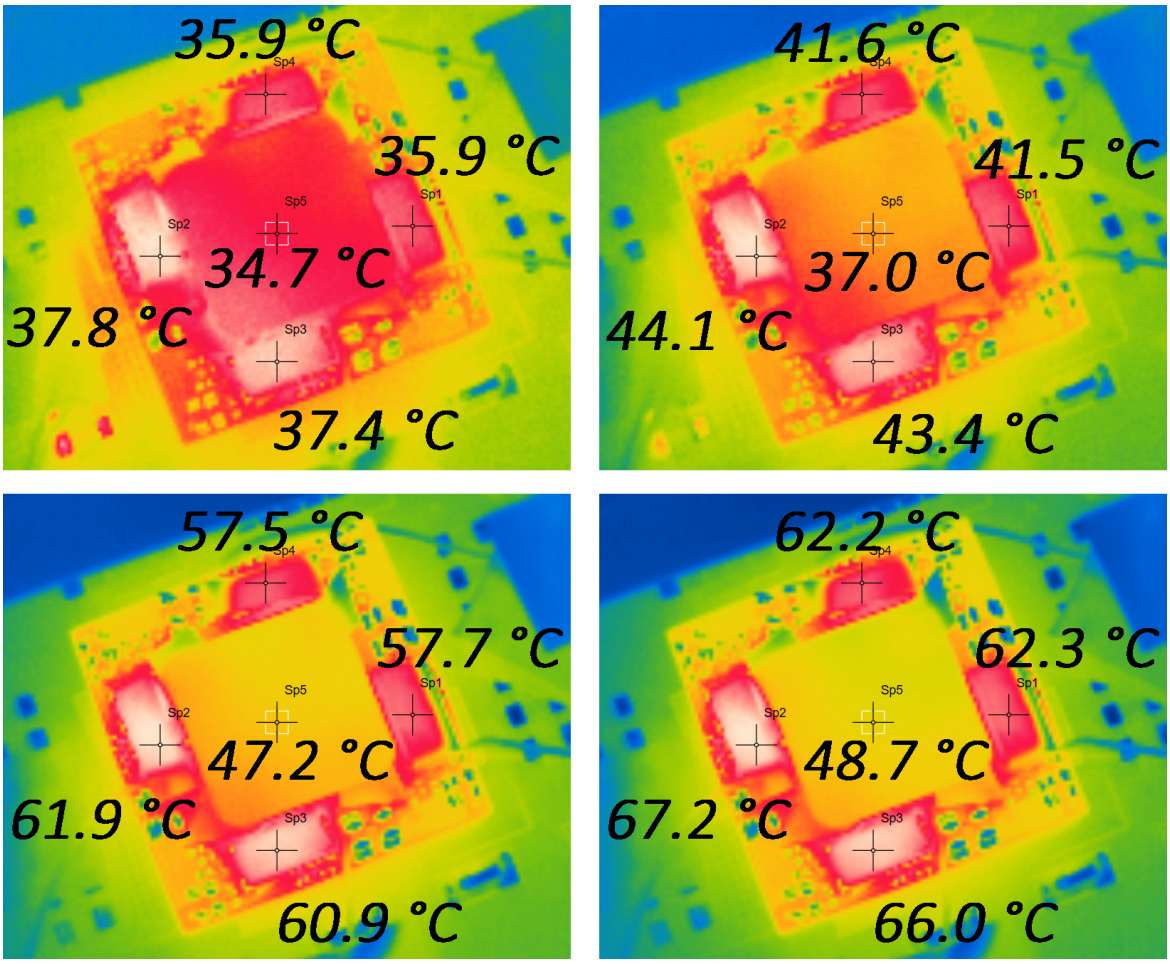


Fig. 4.26 Fully-coupled buck converter thermal images at different load conditions. V_{in} = 7.2 V, f_{sw} = 520 kHz. Only one module operating. I_{load} = 40 A (top left), I_{load} = 60 A (top right), I_{load} = 90 A (bottom left), I_{load} = 100 A (bottom right).

Power distribution network (PDN) performance was measured as impedance at the socket terminals, i.e. by injecting a frequency-sweeped current signal into the output connectors and measuring V_{core} voltage at the center of the socket, differentially. An impedance analyser was used to achieve this task, with the *setup* reported in Fig 4.27.

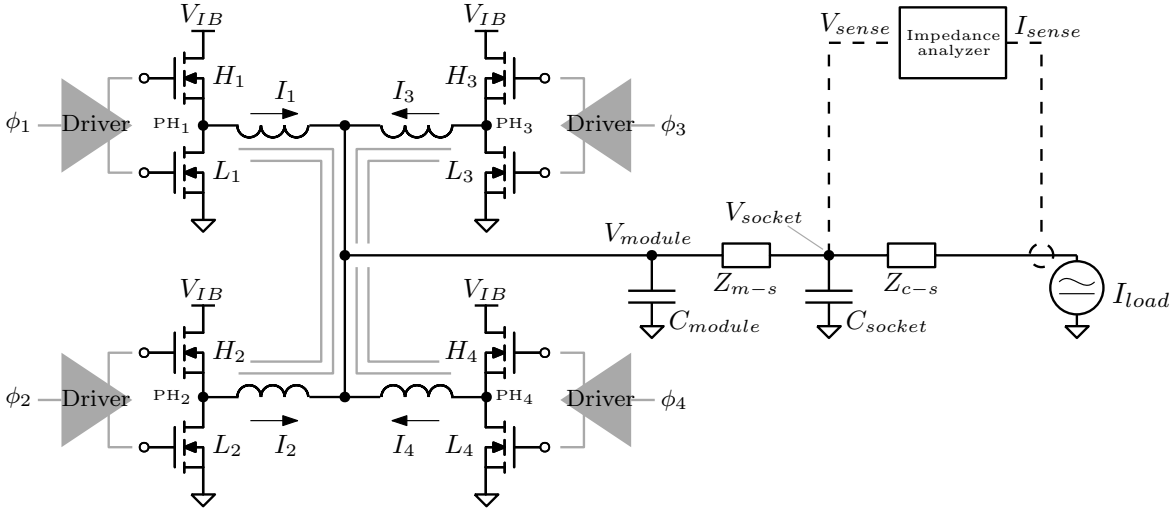


Fig. 4.27 Power distribution network analysis setup. Current is injected through high-power connectors and voltage is differentially measured at the center of the socket. Z_{m-s} is the impedance between the module and the socket (mainly related to the *power pins*); Z_{c-s} is the impedance between the power connectors and the socket, which is not relevant in this setup as I_{load} is measured.

Fig 4.28 shows the measured impedance Z_{out} for a single module. The low frequency range is determined by the C_{out} capacitors, while at high frequency their equivalent-series-inductance (ESL) manifests. Equivalent resistance can be observed in the range of 300-500 kHz, where it reaches $\simeq 400\ \mu\Omega$. As a consequence, the closed-loop can be set to yield a socket impedance as low as $200\ \mu\Omega$ with the two active modules. In this range the measurement is quite noisy, as impedance is extremely low and accuracy is degraded by the small measured voltage; nonetheless, the measured resistance value matches the FEM-simulated predictions.

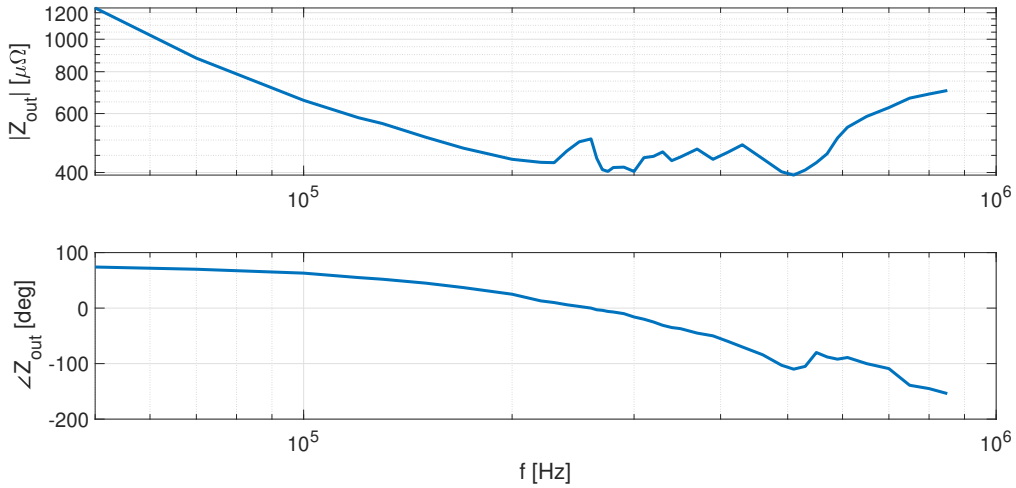


Fig. 4.28 Single-module output impedance Z_{out} measured with the setup of Fig 4.27.

4.4 Conclusions

This Chapter presented a complete, regulated solution for the 48 V to 1.8 V conversion. This architecture is built with a two stage approach: the first one is a three-level buck converter fed through a switched-capacitor voltage divider, which enables regulation via a constant-on-time controller; the second one, behaving like a 4:1 DC transformer, is a novel fully-coupled buck converter.

The core feature of the SC-3LB stage is the inductor voltage reduction, obtained by mean of the two series-connected, soft-charged capacitors C_{SC} and C_{Bx}. The capacitor stacking, and the resulting voltage stepping-down, allows high-density operation with a consistent efficiency as enables the use of small inductors, excited by only a fraction of the input voltage. Observing Fig 4.21, it is clear that this regulator operates in the most efficient manner when operated with a fixed duty-cycle, i.e. when close to the 4:1 conversion ratio. As already discussed, this is due to the reduced losses given by the less-resistive 300 nH inductor, which also operates with almost zero current ripple. As a matter of fact, this topology degenerates into a current-fed, soft-switched switched-capacitor converter composed of two stages in this condition, and output inductance is used only to avoid capacitor hard-charging. This operation increases output power capability up to 600 W for the same 1/8 brick prototype. Current sharing is intrinsically guaranteed by the switched capacitor of the first stage.

The fully-coupled buck fundamental innovation is indeed the complete cancellation of the DC magnetic flux inside the core. Combining all the phases around a single core has allowed to remove the constraint between DC current and core cross-section dimension. With

this architecture, it now depends only on the converted voltages and switching frequency. Current sharing can be easily achieved among module phases via duty-cycle repartitioning.

Chapter 5

Summary

Information technology is pervading our daily lives through a wide spectrum of digital devices. The recent shift towards the Internet of Things and artificial intelligence has moved computational power towards the decentralized and powerful resources of data centers, which are relentlessly increasing their power demands to follow the pace of the service providers market. The hardware required to maintain this digital ecosystem is composed of dense server boards powered by a complex energy distribution system, which was the topic of Section 1.3. The 12 V rack-level bus architecture has recently moved towards the 48 V solution, pushed by the needs of increased power densities and efficiency concerns.

The 48 V utilization not only substantially reduces front-end/motherboard distribution losses, but also decreases the complexity of the previous stages: with this choice the old *uninterruptible power supply* (UPD) double conversion is removed, backing up directly to a battery DC source in case of power outages and delivering the input voltage variations to the efficient rack front-end. In the 48 V environment a new family of converters has been proposed in literature, implementing the descent towards the digital core voltages through different architectures.

Widening the extents of this research field, this dissertation proposes three families of novel solutions to power digital loads from the 48 V bus; in particular, the converters hereby proposed are implemented directly on the main server board and were proven to increase efficiency and power density of the state-of-the-art literature.

In Chapter 2 the high-current digital ASIC package domain is analyzed: novel results are provided with a high-density technique to reduce power pin count and with a mathematical study of the power distribution network, enabling an unregulated 1.6-0.8 V switched capacitor voltage division in a 10 cm^2 area with a 300 A output current capability. This solution is paired with a resonant driver architecture that powers the MOSFET arrays with soft-gate-charging.

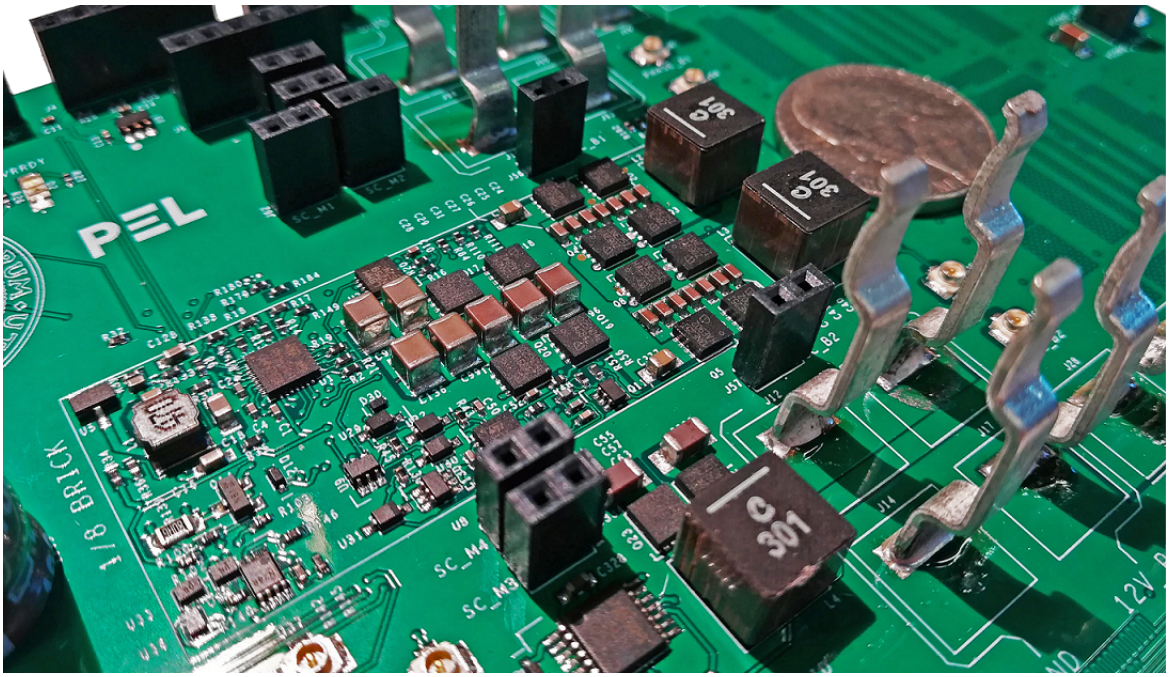


Fig. 5.1 The regulated 48 V to 1.8 V Switched-Capacitor converter with Fully-coupled Buck PoL of Chapter 4.

Chapter 3 describes two solutions for the intermediate bus conversion: the 48 V bus is stepped down by a factor of 4:1 with the converter of Section 3.2, while Section 3.3 shows a modified version that yields two voltage rails with a 10:1 and 5:1 ratio. Both the solutions derive from the transformation of soft-charged *hybrid converters* into unregulated, resonant and ZVS/ZCD-enabled versions by mean of full inductor coupling. It is proven in Section 3.2.2 that this solution allows significant magnetic volume reduction when the isolation is not required.

The full 48 V to 1.8 V V_{core} regulated step-down conversion is described in Chapter 4, where the combination of two different ideas are proposed. First, the regulated stage of Section 4.2.1 implements magnetic volume reduction with a soft-charged switched capacitor approach: output inductors of this stage withstand only a fraction of the input voltage and operate virtually without current ripple when a 4:1 conversion is needed. The last PoL stage, called *fully-coupled buck converter*, yields a novel solution to eliminate DC magnetic flux inside the VRM inductors. With this unregulated stage, the common inductor volume/efficiency trade-off is removed as the magnetic cross-section no longer depends on the output current. As the last stage is designed to power the CPU socket, the power distribution network is analyzed also in this case.

The proposed solutions aim to contribute to the next generation server energy distribution architecture: huge efforts were made to provide high-density, scalable and elegant devices.

5.1 Acknowledgements

None of this work would have been possible without the knowledge and support of my *supervisor* Prof. Stefano Saggini, which is now a close family friend. He helped me to develop and understand my potential during this PhD, a period of time in which I discovered new interests and point of views of subjects I didn't even know about. With his trust I've been able to achieve wonderful goals and travel the world.

I would like to thank my former colleague Roberto Rizzolatti, who introduced me to this new fascinating world which is the Power Electronics spending some time teaching me the use of FEM software, circuit simulations and other boring stuff.

A big thanks to the *STmicroelectronics* team that followed me during this journey.

I would like to dedicate this work to my newborn son Andrea and to my wife Sara, which await for me every evening when I return home.

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