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Sub-60mV/dec Swing and Drive Current in Dirac-Source FETs: a Design Study based on First-Principle Transport Simulations

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Abstract— By using a modelling framework consisting of NEGF-based *ab-initio* simulations, we investigate the operation and design of Dirac-Source FETs (DSFETs). First, we discuss some methodological aspects that we found pivotal to observe the sub-60mV/dec swing in *ab-initio* simulations. Then, we propose the novel HGr-DSFET based on hydrogenated graphene (HGr). We show that the HGr-DSFET has a robust sub-60mV/dec operation and an ON current between 2× and 4× larger than the graphene-MoS_2 DSFET counterpart. Our study addresses and elucidates several physical and design aspects of DSFETs, including the rethermalization effects due to phonon scattering.

I. INTRODUCTION

The energy efficiency has become a paramount figure as the CMOS technology is approaching the 1 nm node [1]. The IRDS identified steep-slope FETs as possible enablers of a widespread power reduction, but it also remarked that all device candidates have failed to deliver adequate on-current, I_{ON}, at the target V_{DD} [2]. Graphene (Gr) and Dirac semi-metals have a Density of States (DoS) proportional to $|E-E_{\mathrm{D}}|$ for an energy E close to the Dirac energy E_{D} [3] (see **Fig.1(a)**). Hence, in the source of a DSFET the electron density $n(E)$ decays more steeply than the tail of the Fermi-Dirac function (see **Fig.1(a)**), thus defeating the Boltzmann's tyranny [4], [5]. The different behavior of a 2D semiconductor is also shown in **Fig.1(b)**. Because in DSFETs the sub-thermionic mechanism does not rely on tunnelling, a large I_{ON} was claimed as a distinct advantage of DSFETs [1], [6]. Most fabricated DSFETs, however, are based on $\mathrm{Gr-MoS_2}$ heterojunctions [7], [8], thus implying interlayer tunnelling across a van der Waals (vdW) gap (see **Fig.1(c)**). The transport in vertical vdW heterojunctions has been widely explored for Tunnel FETs (TFETs), and **Fig.2** reports a collection of experimental and simulation data showing that: **a)** the experimental I_{ON} in vdW TFETs barely reaches 10μA/μm at $V_{\mathrm{DD}}\geq$0.3 V; **b)** the simulated I_{ON} values tend to overestimate experiments for most vdW systems.

This paper presents, for the first time, a comprehensive study of DSFETs based on *ab-initio* transport simulations. We exploit simulations to propose and design a novel HGr−DSFET leveraging the band gap opening in hydrogenated graphene [9]. We demonstrate that the HGr−DSFETs can conjugate a sub-thermionic behavior in the off-state and a high I_{ON} at V_{DD}=0.6 V. Our rigorous modelling framework helps clarify several physical and design aspects of DSFETs, including the electron rethermalization due to phonon absorption.

II. DEVICE STRUCTURES AND DFT SIMULATIONS

The $n-$type $\mathrm{Gr-MoS_2}$ and the $p-$type HGr−DSFET are sketched respectively in **Fig.1(c)** and **Fig.1(d)**. The $\mathrm{Gr-MoS_2}$ DSFET architecture is similar to the planar devices experimentally reported in [7], [8]. In the HGr−DSFET of **Fig.1(d)**, instead, we employ band gap modulation in graphene so as to achieve a Dirac source operation without introducing a vdW heterojunction. Several band gap opening techniques have been proposed for graphene, including a controlled strain [10], the growth on a SiC substrate [11] and the hydrogenation [12] (besides the nanotubes or nanoribbons option). We here chose the hydrogenation as the most compatible option with the use of plain graphene in the Dirac source region. Gr, HGr, MoS_2 and the necessary heterojunctions were first simulated with Quantum ESPRESSO (QE) [13], and with an orthorhombic unit cell necessary for transport [14]. To obtain a supercell with a manageable number of atoms for the non-commensurate Gr and MoS_2 lattices, we applied a 2.74% biaxial compressive strain to Gr enabling a $(\sqrt{7}\times\sqrt{7})$R19.11° Gr supercell that fits onto a 2×2 relaxed MoS_2 supercell (see **Fig.3(a)**). Spurious effects of the supercell replicas along z are suppressed using dipole corrections and a 1.8 nm thick vacuum region.

The relaxation of atomic positions was reached when the forces acting on each atom were less than 2.6 meV/Å and by setting an energy convergence criteria of $\sim10^{-7}$ eV. The kinetic energy cutoff was set to 1124 eV and a 12×12×1 Monkhorst-Pack $\mathbf{k}$-point grid was used. We employed scalar relativistic norm-conserving pseudo-potentials with GGA Perdew-Wang functionals with the DFT-D3 vdW corrections. After the relaxation procedure, the extracted distance between MoS_2 and Gr was 0.346 nm (**Fig. 3(a)**), which is consistent with [15], [16]. The energy offset between the MoS_2 conduction band minimum (CBM) and the Gr Dirac point is $E_{\mathrm{CBM\text{-}D}}\sim$25 meV (**Fig. 3(c)**). *Ab-initio* calculations and experiments reported $E_{\mathrm{CBM\text{-}D}}$ values ranging from tens meV up to 500 meV [17], [18]. The same methodology was used for the Gr and HGr system, whose orthorhombic cells are shown in **Fig. 4(a)-(b)**. Consistently with previous studies [9], our calculations reveal the opening of a large band gap in HGr (see **Fig. 4(c)**). The VBM is ∼220 meV below the graphene E_{D}, which suggests the exploitation of this system for a p-type DSFET. The geometrical dimensions a_x, a_y, a_z of the different supercells are shown in **Fig. 3** and **Fig. 4**.

III. *Ab-initio* DEVICE SIMULATIONS

To investigate the DSFETs in **Fig.1**, we used *ab-initio* simulations by employing the Green-Tea tool [14], *which provides a truly ab-initio description of the heterojunction coupling,*

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differently from previous numerical studies employing a model-Hamiltonian whereby interlayer tunnelling is controlled by an adjustable parameter [15], [19], [20].

NEGF transport simulations were performed for device structures including several hundred atoms (see **Fig. 1(c-d)**), by using a basis set of unit-cell restricted Bloch functions [14]. The transport simulations for the $Gr-MoS_2$ DSFET in **Fig.1(c)** involve three regions (Gr, the $Gr-MoS_2$ hetero-junction, MoS_2), while simulations for the HGr−DSFET in **Fig.1(d)** involve a Gr and an HGr region. The Hamiltonian matrices coupling the different regions were evaluated as explained in [21], [22]. If not otherwise stated, DSFETs have L_{G}=20 nm, L_{SP}=10 nm, L_{OV}=5 nm for the gate length, the spacing between the two gates, and the gate overlap onto Gr, respectively (**Fig. 1(c-d)**). The EOT of the top (bottom) oxide is 0.5 (32) nm, and the V_{CG} is used to electrostatically dope the Gr source with a degeneracy $|E_{\mathrm{F,S}}-E_{\mathrm{D,S}}| \simeq 260$ meV, namely a carrier density of $\approx 7.5 \cdot 10^{12}$ cm^{-2}. At drain, instead, we used a chemical doping concentration $5{\cdot}10^{12}$ cm^{-2}. The gate work function is set to have I_{OFF}=0.1 nA/μm at V_{GS}=0 and $|V_{\mathrm{DS}}|=V_{\mathrm{DD}}$=0.6 V. The temperature is T=300 K.

Fig.5 illustrates that, in *ab-initio* simulations of DSFETs, the sampling of the transverse k_{y} is critical to reconstruct the DoS(E) of Gr and observe a sub-threshold swing (SS) below 60 mV/dec. In fact, in **Fig.5(a)** the results for the smaller Δk_{y} can reconstruct well the graphene DoS(E)$\propto|E-E_{\mathrm{D}}|$, and the corresponding $I_{\mathrm{DS}}-V_{\mathrm{GS}}$ curve in **Fig.5(c)** shows SS<60 mV/dec. A larger Δk_{y}, instead, cannot accurately reproduce the Gr DoS in **Fig.5(b)**, and consequently results in an SS>60 mV/dec in **Fig.5(c)**. For discrete k_{y} values spaced by Δk_{y}, analytical derivations show that the Gr DoS is given by

$$DoS(E, \Delta k_{\mathrm{y}}) = \frac{2\Delta_{k_y}}{\pi^2\,\hbar v_F} \sum_{k_y} \frac{|E-E_{\mathrm{D}}|}{\sqrt{(E-E_{\mathrm{D}})^2 - \hbar^2 v_F^2 k_y^2}} \quad (1)$$

for $\hbar v_F|k_{\mathrm{y}}|<|E-E_{\mathrm{D}}|$. **Fig.5(a-b)** shows that **(1)** can reproduce well the numerical DoS.

A. *n-type, Gr-MoS$_2$ DSFET*

Fig.6 reports simulation results for two variants of DSFETs based on the Gr-MoS_2 heterojunction, where in the Gr/MoS_2 device the Gr is placed between the gate and MoS_2 (see **Fig.6(a)** and experiments in [7]), while in the MoS_2/Gr device the placement of Gr and MoS_2 is swapped (see **Fig.6(b)** and experiments in [8]). **Fig.6(c-d)** show that the two device variants have practically the same sub-60mV/dec sub-threshold swing. In the ON state, instead, the Gr/MoS_2 DSFET has a degraded I_{DS}, because the semi-metallic Gr tends to screen the bias exerted by the gate on MoS_2. This can be seen in **Fig.6(e)**, where the larger charging of Gr in the Gr/MoS_2 DSFET is confirmed by the lower E_{D} of Gr in the overlap region (**(e)-left**, green area), compared to MoS_2/Gr DSFET (**(e)-right**).

The better ON current of the MoS_2/Gr compared to the Gr/MoS_2 DSFET is consistent with experiments [7], [8].

B. *p-type, HGr-DSFET*

We ascribe the relatively poor drive current of the Gr-MoS_2 DSFETs in **Sec.III-A** to the vdW nature of these devices. Therefore, in this paper we propose and investigate the p-type, HGr-DSFET sketched in **Fig.1(d)**).

Fig.7(c) shows that the HGr-DSFET can reach a sub-threshold swing below ≈40 mV/dec, an I_{ON} approaching 100 μA/μm at V_{DD}=0.6 V, namely about 2× and 4× the I_{ON} of the two Gr-MoS_2 variants in **Fig.6**. The energy spectra of the electron concentrations in **Fig.7(a-b)** confirm that the device operation is consistent with the sketch in **Fig.1(d)**). **Fig.7(c-d)** also show that the DIBL is negligible and that the output curves of the HGr-DSFET exhibit good saturation.

As for the device, **Fig.8(a)** reveals that the scaling of the spacing L_{SP} between the gates (see **Fig.8(b)**) is important for the I_{ON} of DSFETs. In fact, a short L_{SP} favours the abruptness of the Gr $n-p$ junction at source (see **Fig.8(c)**), which reduces the junction resistance [23]. Likewise, the lack of a gate overlap onto Gr degrades I_{ON} as it makes the Gr $n-p$ junction less abrupt. The design options in **Fig.8** have a negligible influence on the sub-threshold region (not shown). **Fig.9** shows that, by reducing the degeneracy at source ($E_{\mathrm{F,S}}-E_{\mathrm{D,S}}$), the sub 60mV/dec swing occurs at larger I_{DS} values, but in a smaller I_{DS} range. Overall, the I_{ON} at fixed I_{OFF}=0.1 nA/μm is degraded by reducing the source degeneracy (not shown).

C. *Phonon Scattering and Rethermalization*

Rethermalization effects are here analyzed for the HGr-DSFET. If transport is elastic, then the electrons in HGr see a minimum in the available Gr states when the HGr VBM crosses the Dirac energy at source $E_{\mathrm{D,S}}$(see **Fig.7(b)**), thus leading to the sub-60 mV/dec operation. However, phonon absorption in Gr can assist inelastic transport paths. We included electron-phonon (el-ph) scattering in our NEGF formalism in the deformation potential approximation. The el-ph self–energies account for the dominant acoustic phonons in graphene by using D_{ac}=4.32 eV and an average sound velocity v_{s}=16.23 km/s [24]. For the dominant graphene optical phonon we used $\hbar\omega_{LO,TO}$=200 meV, D_{op}=$1.14{\cdot}10^9$ eV/cm [24], and repeated calculations for a weaker D_{op}=$3.43{\cdot}10^8$ eV/cm. **Fig. 10(b)** shows that el-ph interaction can indeed degrade the SS. **Fig.10(a)** reports the current spectrum calculated with or without el-ph scattering, showing an inelastic path promoting the electrons injected in Gr to energies close to $E_{\mathrm{F,S}}$, where density of empty states is much larger than at energy $E_{\mathrm{D,S}}$. In **Fig.10(b)** an SS<60 mV/dec operation is preserved in the presence of el-ph scattering, however the dominant D_{op} at the Dirac source is critical for the DSFET operation.

IV. Conclusions

First-principle transport simulations were used, for the first time, to explore the physics and design of graphene DSFETs. First, methodological guidelines were provided for *ab-initio* modelling of DSFETs. Then, we proposed the HGr DSFET and scrutinized several design options to optimize SS and I_{ON}. Simulations suggest that the el-ph interaction degrades the SS, but does not negate the sub-thermionic operation.

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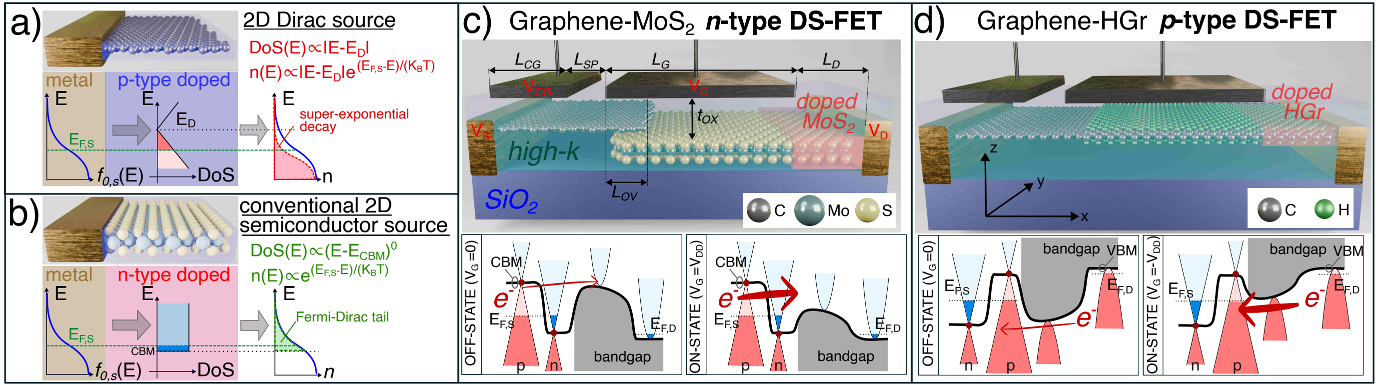

Figure 1: Comparison between: **(a)** a p-type source region for a 2D Dirac-material (e.g. graphene); **(b)** an n-type source region consisting of a conventional 2D-semiconductor. The DoS(E) and electron density $n(E)$ are sketched versus the energy E. In the Dirac source **(a)**, for $E{>}E_{\rm F,S}$ the $n(E)$ decays more steeply than the Fermi-Dirac function $f_{0,S}(E)$. **(c)** Conventional n–type DSFET based on a Gr-MoS_2 vdW heterojunction. Band profile either in the off–state, where the MoS_2 conduction band minimum (CBM) crosses $E_{\rm D}$ in the p–type Dirac source, or in the on–state, where the MoS_2 CBM crosses $E_{\rm F,S}$. **(d)** Newly proposed p–type HGr−DSFET based on a Gr source and a HGr channel region. Band profile either in the off–state, where the HGr valence band maximum (VBM) crosses $E_{\rm D}$ in the n–type Dirac source, or in the on–state, where the HGr VBM crosses $E_{\rm F,S}$. The control gate (CG) sets the electrostatic doping at the source. Chemical doping in the drain has an areal concentration $5{\times}10^{12}$ cm^{-2}, hence $E_{\rm F,D}$ is close to either the CBM (in **(c)**) or the VBM (in **(d)**).

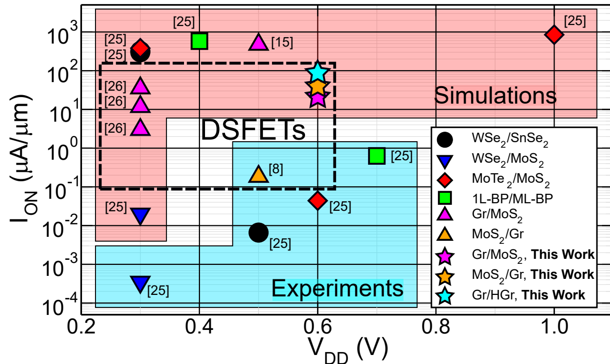

Figure 2: Experimental and simulated on-current at $|V_{\rm GS}|{=}\;|V_{\rm DS}|{=}\;V_{\rm DD}$ for vdW TFETs [25], and DSFETs [8], [15], [26], and for different material systems. Experiments from [25] were restricted to those reporting SS<60 mV/dec at $V_{\rm DS}{\geq}0.3$ V. For vdW TFETs, $V_{\rm GS}{=}0$ is taken where $I_{\rm DS}$ is minimum [25]. For DSFETs, $V_{\rm GS}{=}0$ is taken where $I_{\rm DS}{=}I_{\rm OFF}{=}0.1$nA/$\mu$m in the data in [8], [15], [26] in compliance with the IRDS requirements for *High Density* devices [2].

Figure 4: **(a)** Top and side view of the unit cell of graphene, HGr and of the orthorhombic supercell used for transport (red dashed line) (see **Fig. 1(d)**). **(b)** BZ of the supercell, where Gr Dirac points backfold at $\left(\pm0.\bar{6}\pi/a_x,0\right)$ (red circles). **(c)**. Band structures of Gr and HGr.

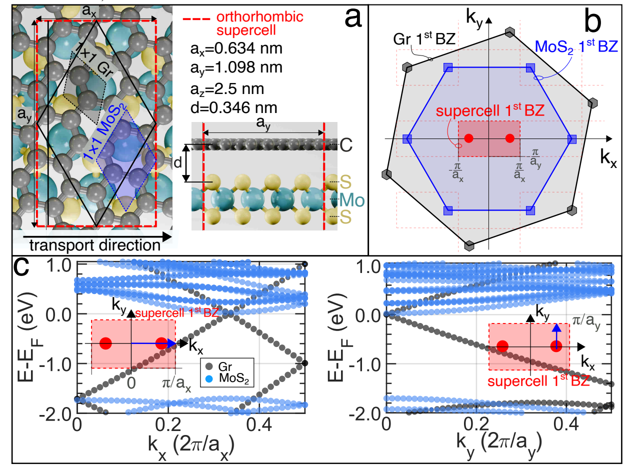

Figure 3: **(a)** Top and side view of the orthorhombic Gr-MoS_2 supercell used in transport simulations (red dashed line) (see **Fig. 1(c)**). **(b)** First Brillouin zone (BZ) of Gr, of MoS_2 and of the Gr-MoS_2 supercell, where the Gr Dirac points and the MoS_2 CBMs backfold at the position $\left(\pm0.\bar{6}\pi/a_x,0\right)$ (red circles). **(c)** Band structures along the paths highlighted by the blue arrows and projected on either Gr or MoS_2 orbitals.

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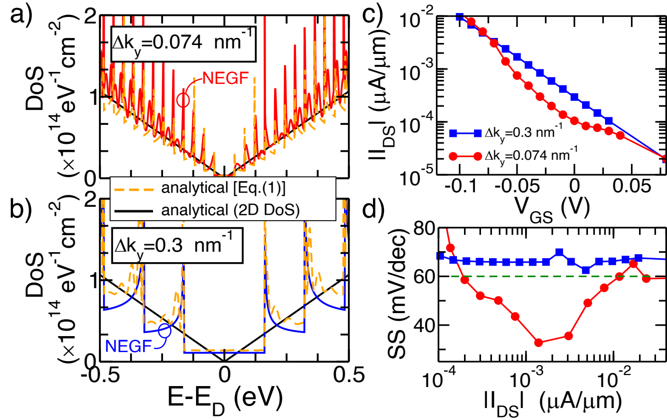


Figure 5: **(a-b)** DoS obtained from NEGF calculations in the Gr source region. **(a)** A fine k_y sampling employing $\Delta k_y = 5\times10^{-3}[2\pi/a_y] \simeq 0.074\text{nm}^{-1}$ can reconstruct well the graphene DoS(E). **(b)** A coarser k_y sampling with $\Delta k_y = 2\times10^{-2}[2\pi/a_y] \simeq 0.3\text{nm}^{-1}$, instead, leads to a stepped DoS(E) that is reproduced well by the analytical expression in **(1)**. **(c)** $I_{DS}-V_{GS}$ curve in sub-threshold for a HGr−DSFET simulated with the Δk_y of **(a)** or **(b)**. **(d)** Corresponding sub-threshold swing versus I_{DS} for different Δk_y.

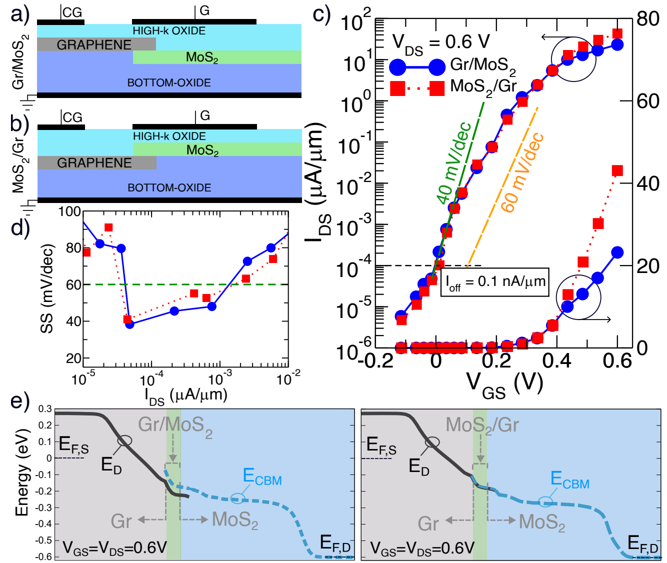


Figure 6: **(a-b)** Sketches of the Gr-MoS_2 DSFET (see **Fig. 1a**), featuring either a Gr/MoS_2 (in **(a)**) or a MoS_2/Gr (in **(b)**) vertical vdW heterojunction. **(c-d)** Corresponding I_{DS} versus V_{GS}, and SS versus I_{DS} curves at V_{DS}= 0.6 V. **(e)** Band profiles along the transport direction at V_{GS}=V_{DS}=0.6 V for either the Gr/MoS_2 DSFET **(left)** or the MoS_2/Gr DSFET **(right)**.

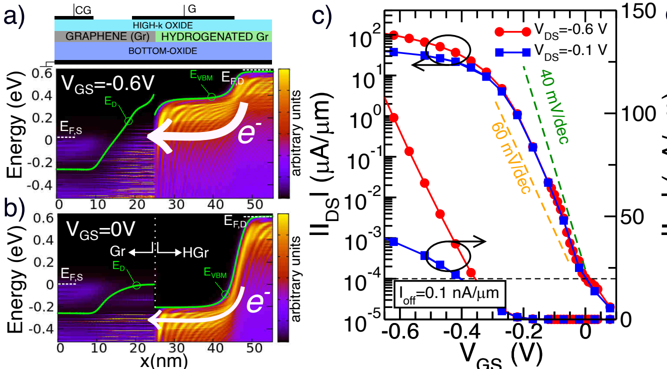


Figure 7: Electron density spectrum in the ON state **(a)** and OFF state **(b)** of the p–type DSFET shown in **Fig. 1(d)** at V_{DS}=−0.6 V. The solid green line shows the E_D profile in the Gr region, and the HGr VBM in the HGr region. The quasi-Fermi level is $E_{F,S}$=0 eV at the source and $E_{F,D}$=−qV_{DS}=+0.6 eV at the drain. **(c)** I_{DS} versus V_{GS} ballistic characteristics at V_{DS}=−0.1V and −0.6V, clearly showing a sub-60 mV/dec sub-threshold operation. **(d)** I_{DS} versus V_{DS} characteristics at different V_{GS} values.

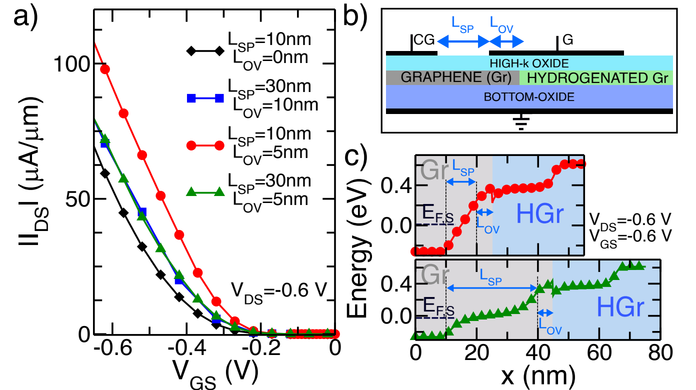


Figure 8: **(a)** I_{DS} versus V_{GS} curves of the HGr-DSFET at V_{DS}=0.6 V for different spacing L_{SP} between the gates, and with a gate to Gr overlap (L_{OV}=5 or 10 nm) or without such overlap (L_{OV}=0). **(b)** Sketch of the design options. **(c)** Band profiles corresponding to some of the different design options.

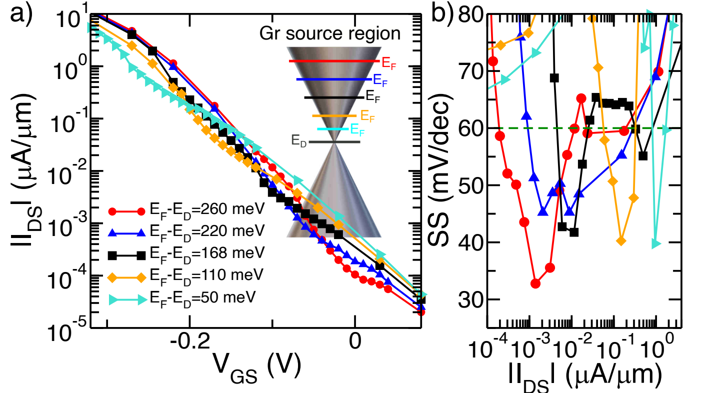
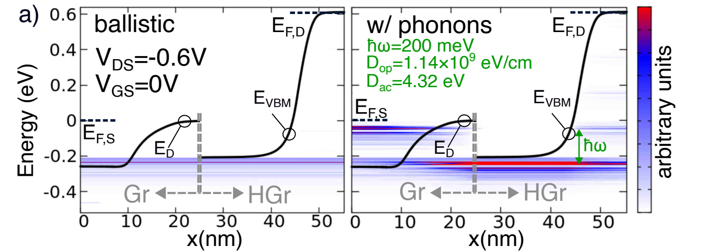


Figure 9: **(a)** I_{DS} versus V_{GS} curves of the HGr-DSFET in the sub-threshold region, at V_{DS}= −0.6 V and for different values of the electrostatic doping at the Gr source. **(b)** Corresponding SS versus I_{DS} curves.



b) V_{DS} = -0.6 V; Ballistic; D_{op} = 3.43×10^8 eV/cm; D_{op} = 1.14×10^9 eV/cm; 40 mV/dec; $|I_{DS}|$ (μA/μm); V_{GS} (V); inset: I_{DS} (μA/μm), SS (mV/dec)

Figure 10: Simulations including phonon scattering for the HGr−DSFET. **(a)** Spectral current density for ballistic and dissipative transport **(same color scale)**. **(b)** I_{DS} vs. V_{GS} curves with or without phonons; inset shows the SS vs. I_{DS} curves.

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