Operation and Design of Ferroelectric FETs for a BEOL Compatible Device Implementation

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Daniel Lizzit and David Esseni
DPIA, University of Udine, via delle Scienze 206, 33100 Udine, Italy
e-mail: daniel.lizzit@uniud.it

Abstract

We present a study based on numerical simulations and comparative analysis of recent experimental data concerning the operation and design of FeFETs. Our results show that a proper consideration of charge trapping in the ferroelectric-dielectric stack is indispensable to reconcile simulations with experiments, and to attain the desired hysteretic behavior of the current-voltage characteristics. Then we analyze a few design options for polysilicon channel FeFETs and, in particular, we study the influence of the channel thickness and doping concentration on the memory window, and on the ratio between the polarization dependent, high and low resistance state.

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1 Introduction

The slowing down of the CMOS geometrical scaling has steered the electron devices research to new functionalities for novel computational paradigms, as well as to the energy efficiency [1, 2]. In particular, there is a growing interest for memristors capable of multiple resistance levels, that have intriguing

applications in crossbar arrays for artificial deep neural networks [3], and in hybrid memristive-CMOS circuits for neuromorphic computing [4, 5].

The discovery of ferroelectricity in hafnium oxides opened new perspectives for ferroelectric CMOS devices [6], with applications ranging from negative capacitance transistors [7, 8], to non volatile memories and memristors [9, 10]. In particular, Ferroelectric FETs (FeFETs) with multiple resistance levels have been already reported in an industrial technology [11]. However, in order to unleash the potentials of FeFETs as synaptic devices, a Back-End-Of-Line (BEOL) compatible device architecture is in high demand. In fact the BEOL fabrication of FeFETs right on top of CMOS circuits holds the promise for great advantages in terms of performance and energy dissipation.

Because the polarization switching dynamic in FeFETs and the involved charge components are still debated [12–14], the operation and design of BEOL compatible FeFETs is still a stimulating and challenging research topic.

We here present a simulation based study that first investigates the operation of experimentally reported FeFETs [11], and then leverages the physical insight to discuss, on a sound ground, the design of BEOL compatible FeFETs.

2 Ferroelectric models and calibration

Device simulations were carried out using the Sentaurus-Device (S-Device) TCAD tool relying on drift-diffusion transport models and accounting for polarization effects within the Ginzburg–Landau–Khalatnikov framework [15].

We here assume the total polarization to be separated into the spontaneous polarization P_S and a background contribution [16, 17], described by the dielectric permittivity of the ferroelectric material. Because thin Hf-based ferroelectrics are tipically in a polycristalline state, and TEM/SEM images evidence grains that have a fairly uniform polarization [18–20], in our simulations we also introduced ferroelectric grains separated by a 5Å thick oxide, which is consistent with the size of the domain wall region reported in [21].

The calibration of Landau's anisotropic constants α, β and γ has been performed by comparing simulations against experimental data for an MFM capacitor. In Fig.1 we show the total polarization $P_T = \mathrm{P}_S + \varepsilon_0 \varepsilon_{r,F} E_F$ in the x direction and obtained under quasi-static triangular voltage ramps from -3 to +3V. To include the grain to grain variabily for the α, β and γ parameters in such large area devices, we considered a normal distribution

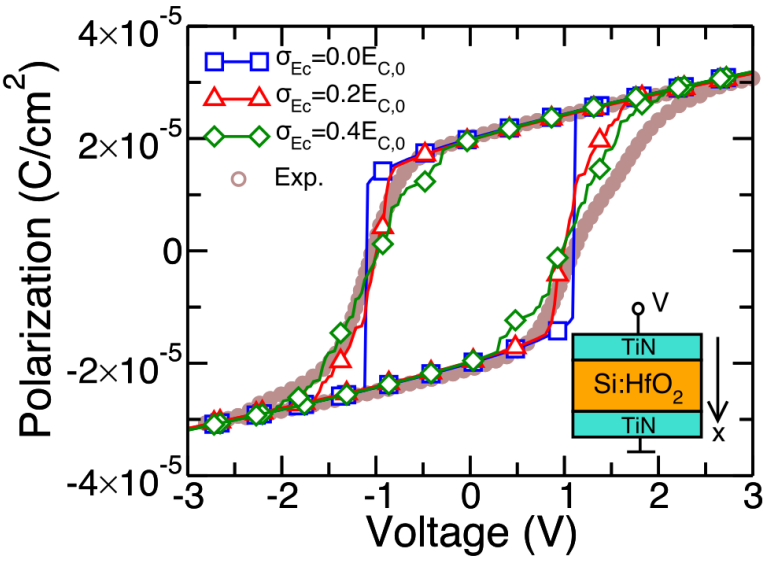

Figure 1: Total polarization P_T in a 10 nm Si doped HfO_2 MFM capacitor. Simulations were obtained with 100 ferroelectric grains and for different values of σ_{Ec}. Landau's coefficients for the coercive field $E_{C,0}$ (i.e. for σ_{Ec}=0) are α=-5.37×10^8 m/F, β=9.62×10^8 $m^5/(FC^2)$, γ=9.59×10^{10} $m^9/(FC^4)$. The relative dielectric permittivity of the ferroelectric oxide is $\varepsilon_{r,F}$=30 [24]. The tilting of the polarization switching branch depends on the dispersion of the coercive field. Experiments are from [25].

of the coercive field around the mean value ($E_{C,0}$) with standard deviation σ_{E_C}. The resistivity for the ferroelectric switching employed in simulations is ρ=30 Ω·m [26], resulting in a time constant τ=$\rho/2\,|\alpha|$=28 ns such that the ferroelectric operates in quasi-static conditions for all the bias waveforms explored in this paper. We see in Fig.1 that a fairly good agreement with experimental results is obtained for σ_{E_C}=$0.4E_{C,0}$.

3 Operation of experimentally reported Fe-FETs

We here report an analysis of the experimental results recently reported for fully depleted SOI FeFETs based on a silicon doped HfO_2 (Si:HfO_2) [11, 25, 27]; a sketch of the device is shown in Fig.2. Our main goal is to reproduce the qualitative features of the measured I_{DS}-V_{GS} curves, so as

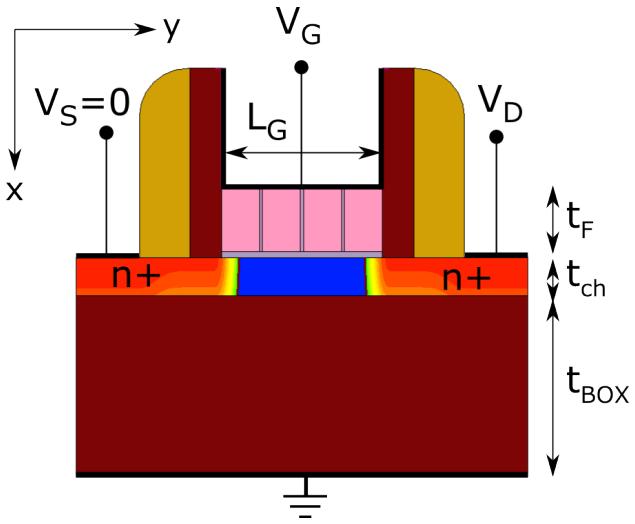

Figure 2: Sketch of the simulated FeFET. The gate length is L_G=24 nm and it is simulated by using 4 grains of 6 nm length. The thickness of the Si:HfO_2 and of the interfacial SiO_2 layer are t_F=10nm and t_{IL}=1nm, respectively [25,27]. The silicon channel has a thickness t_{ch}=6 nm, while the SiO_2 back oxide is 30nm thick. Each ferroelectric grain of length 6 nm is separated by the other grains by a 5 Å thick non ferroelectric oxide with the same relative permittivity of the Si:HfO_2 ferroelectric. The source and drain n-doping are 5×10^{20} cm^{-3} and the Si channel is undoped.

to gain an understanding of the device operation that will be used in Sec.4 for the design of BEOL compatible FeFETs. In order to describe the mobility in the fully depleted SOI transistors we used the thin-layer mobility model [15,22], that accounts for the mobility degradation due to the vertical electric field, and also for the scattering due to random fluctuations of the channel thickness and to surface phonons [15, 23]. In Fig.3 we compare the simulated and experimental I_{DS} versus V_{GS} curves [11]. The simulations neglecting any trapped charge (either at the ferroelectric-dielectric interface or in the dielectrics) exhibit essentially no hysteresis (red triangles), which is in stark disagreement with experiments; the lack of hysteresis is confirmed in corresponding P_S versus V_{GS} curve in Fig.4(a). We could find the onset of a very limited hysteretic behaviour by enlarging the simulated V_{GS} swing well above the 3V swing used in experiments (not shown), but still the hysteresis is much smaller than in the measured I_{DS}-V_{GS} curve.

In order to understand and overcome this large discrepancy between simulations and experiments we recall the experimental results in [12], which combined quasi-static split C-V measurements with Hall measurements to demonstrate that in bulk FeFETs only a small fraction of the ferroelectric

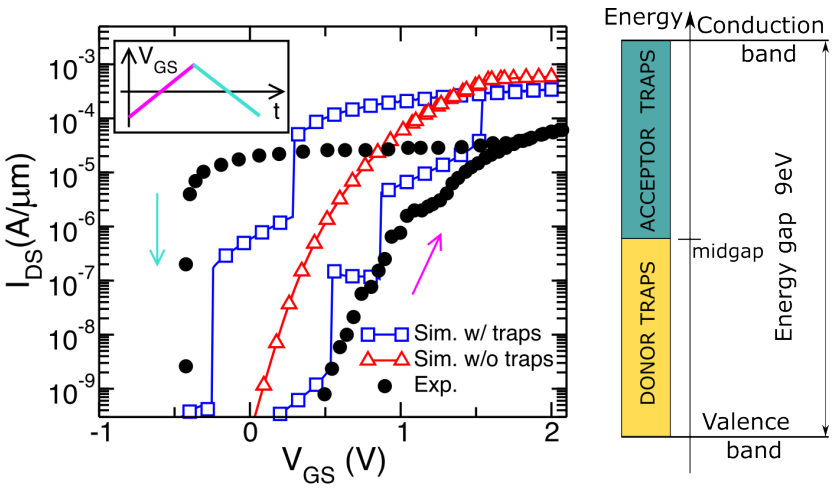

Figure 3: *(left)* I_{DS}−V_{GS} at a V_{DS} of 50mV consistent with the experiments from [11]. Simulations obtained with and without border traps. Experimental results have been horizontally shifted to ease comparison against simulations. The inset shows the forward and backward quasi-static gate sweeps used in simulations with a slew rate of ≈1V/s and peak-to-peak value of 3V consistently with experiments [11]. *(right)* Acceptor and donor border traps with uniform density energy distribution in the SiO_2 IL as used throughout this work. $D_{it,acc}$=8×10^{20} $eV^{-1}cm^{-3}$ and $D_{it,don}$=4×10^{20} $eV^{-1}cm^{-3}$. Traps are also uniformly distributed across the 1nm thick IL.

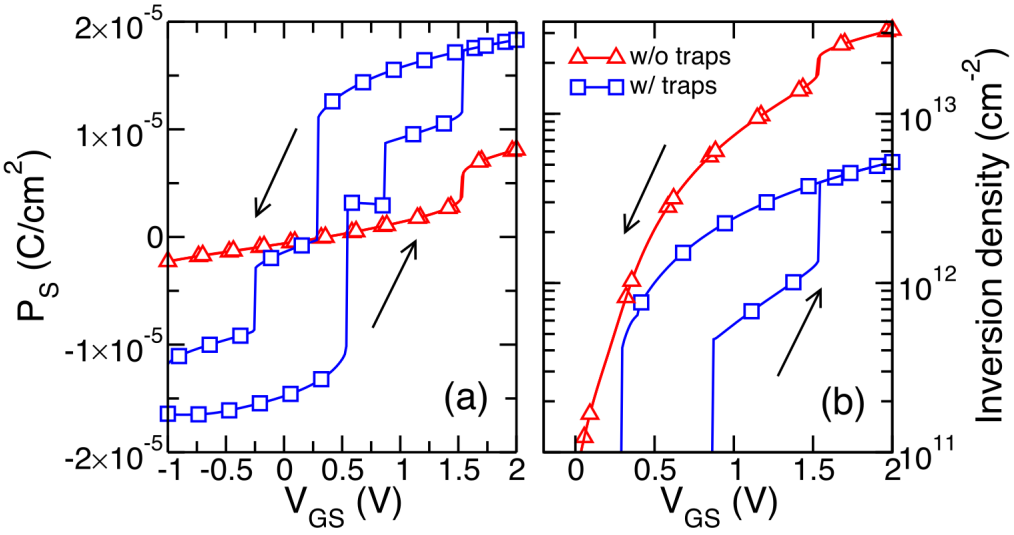

Figure 4: (a) Spontaneous polarization as a function of the gate voltage. (b) Semiconductor electron density obtained by integrating the volumetric free electrons in the channel and by dividing for the channel length.

polarization can be compensated by the free-carriers in the transistor channel, whereas most of the charge stems from trapping in the interfacial layer or at the ferroelectric-dielectric interface. In our simulation setup we described the charge trapping by using border traps in the interfacial SiO_2 layer (IL) oxide. Such traps are assumed to exchange carriers with the transistor channel via the tunnelling, as described by the Nonlocal Tunneling model accounting for both elastic and inelastic phonon-assisted processes [15].

Because we feel that there is no unique combination of traps that can be inferred from a comparison to experiments, after several tests we pragmatically opted for a simulation setup consisting of a donor and acceptor type trap density that is spatially and energetically uniform in the interfacial layer (see the sketch in Fig.3).

The influence of traps is illustrated in Fig.3, where a hysteretic window in the I_{DS}-V_{GS} curve comparable to experimental results can eventually be obtained (blue squares). In fact the trapped charge in the IL oxide tends to partly compensate the ferroelectric polarization, thus reducing the depolarization and opening a hysteresis loop, that can be also seen in the P_S-V_{GS} plot reported in Fig.4(a).

The inclusion of border traps in the IL helps reconcile simulations with experiments in several respects. In the absence of traps, the ferroelectric polarization results in unphysically large carrier inversion densities (see Fig.4(b)), and in a huge electric field in the IL (not shown). In the presence of traps, instead, the channel inversion density becomes much smaller than the trapped charge, which is in qualitative agreement with the findings in [12].

By comparing Fig.4(b) and 3 one can see that the strong reduction of inversion density caused by the inclusion of traps does not lead to a commensurate I_{DS} reduction. This is because the border traps reduce the transverse electric field in silicon, which improves the mobility and partly compensates for the loss of inversion charge.

We finally notice that the steps in the simulated I_{DS} versus V_{GS} curves in Fig.3 are due to the switching of a single ferroelectric grain. This effect is most probably exaggerated by the 2D simulation setup (here employed to reduce the computational burden), which neglects the multiple conduction paths possibly occurring in an actual 3D device.

4 Design of BEOL compatible FeFETs

In this section we consider different design options for a polysilicon channel FeFET compatible with a BEOL integration, whose device structure is illustrated in Fig.5. Our analysis will be carried out by employing the same trap

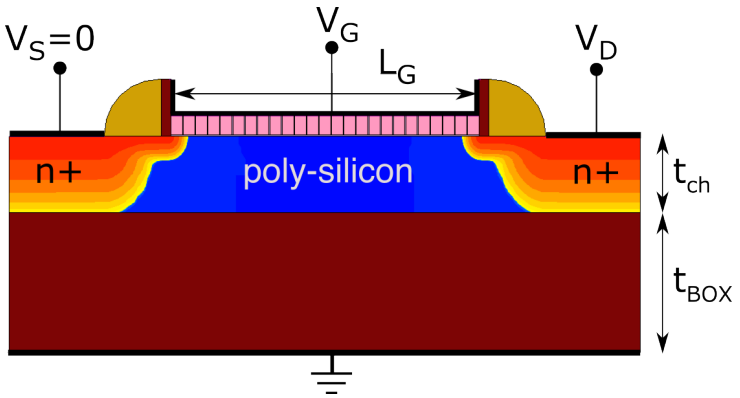

Figure 5: Cross sectional view of the simulated FeFET with L_G=150nm and t_{ch}=40nm. The polycrystalline ferroelectric oxide consists of 25 grains with a length of 6 nm and a 5 $\mathring{A}$-thick spacer between each grain has been used. Anisotropic constants were obtained with σ_{E_C}=0.4$E_{C,0}$ consistently with Fig.1. The IL SiO_2 is 1 nm thick. Source and drain donor doping concentrations are 5×10^{20}cm^{-3}, whereas the channel acceptor/donor doping ranges between 10^{16} and 10^{18} cm^{-3}. The silicon back oxide has a thickness t_{BOX}=200 nm.

distributions as for the SOI FeFET in Sec.3, that ensure a hysteretic I_{DS}-V_{GS} curve irrespective of the device thickness and channel doping concentration (see also Figs.6, 7).

We studied both a depletion and an enhancement mode version of the device in Fig.5, and for both options we considered channel doping concentrations ranging from 10^{16} cm^{-3} up to 10^{18} cm^{-3} and two different channel thicknesses, namely t_{ch}=40 and 80 nm. For the polysilicon thin-film channel we assumed a constant carrier mobility of 10 cm^2/Vs [28]. The channel length is L_G=150 nm and we studied the I_{DS} and resistance R_{DS}=V_{DS}/I_{DS} at V_{DS}=50mV. The carrier mobility and the longitudinal field (V_{DS}/L_G) are such that velocity saturation effects are negligible for the results of this section. In Fig.6 we see that large doping concentrations in the depletion-mode FeFETs tend to increase I_{DS} and, as expected, to reduce the I_{DS} modulation between the forward and backward quasi-static gate sweep. On the other hand the size of the memory window is approximately insensitive to the doping concentration. This is because the P_S versus V_{GS} hysteresis loop is mainly governed by the border traps in the IL, and it is thus fairly independent of the channel doping concentration, as illustrated in the inset of Fig.6. Fig.7 shows that the P_S hysteresis loop is independent of the channel doping concentration even in the enhancement-mode polysilicon FeFETs. In these latter devices, however, a large doping reduces the I_{DS} values and en-

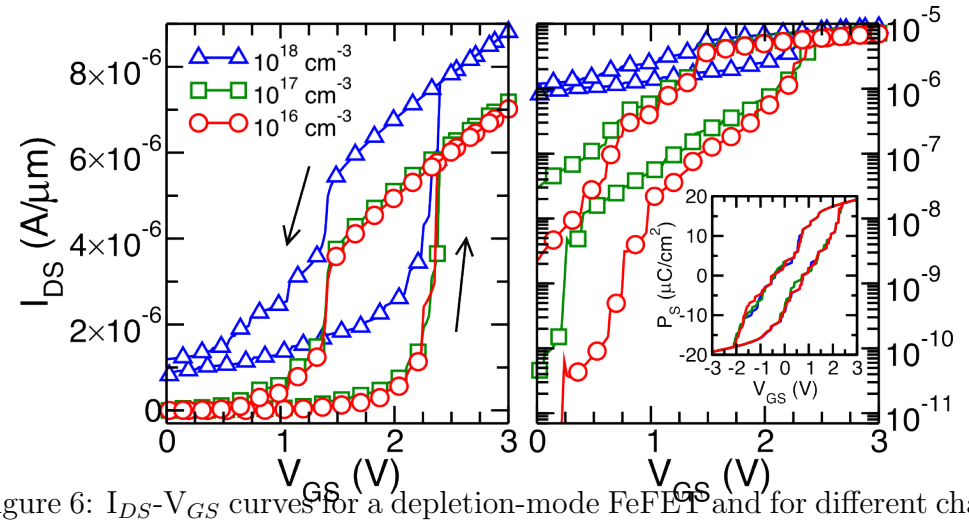

Figure 6: I_{DS}-V_{GS} curves for a depletion-mode FeFET and for different channel doping concentrations for a quasi-static gate sweep with V_{GS} from -3 to +3V. The channel thickness is t_{ch}=40nm. Results are shown either in linear or in semilogarithmic scales and for V_{DS}=50mV.

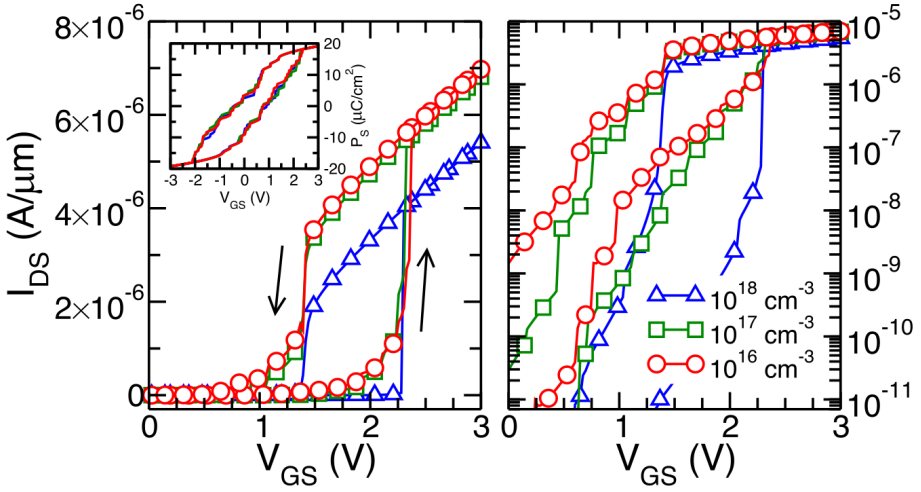

Figure 7: I_{DS}-V_{GS} curves for an enhancement-mode FeFET and for different channel doping concentrations for a quasi-static gate sweep with V_{GS} from -3 to +3V. The channel thickness is t_{ch}=40nm. Results are shown either in linear or in semilogarithmic scales and for V_{DS}=50mV.

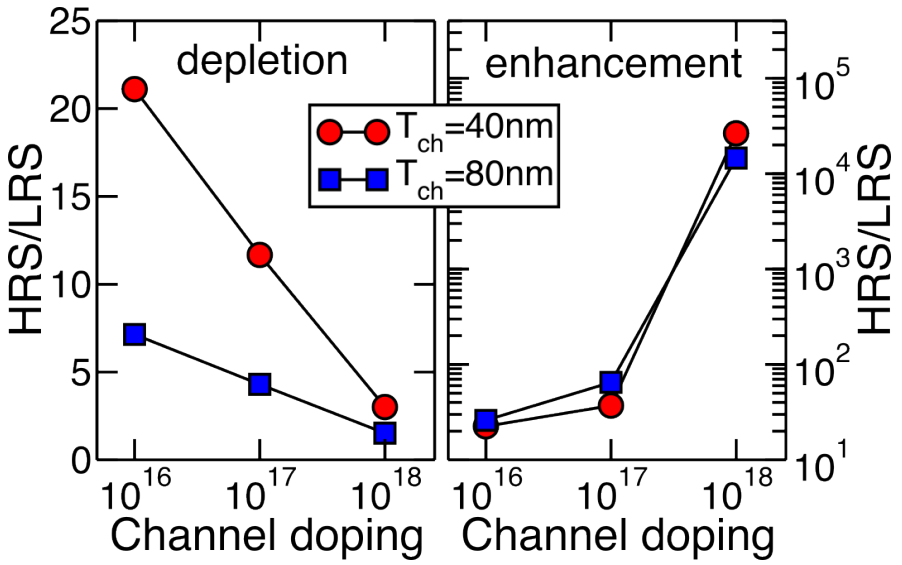

Figure 8: HRS/LRS ratio as a function of the channel doping and channel thickness and for enhancement- and depletion-mode FeFETs.

larges the I_{DS} modulation between the forward and backward quasi-static V_{GS} sweep.

The simulation results in Figs.6 and 7 were then used to determine the high resistive state (HRS) and low resistive state (LRS) value, evaluated at V_{DS}=50mV and V_{GS} of 1.75V, namely at the V_{GS} value approximately corresponding to the center of the I_{DS} memory window. The ratio between the HRS and the LRS are reported in Fig.8 for the different design options. As it can be seen, for the depletion-mode FeFET the high channel doping concentrations reduce the HRS over LRS ratio. Morever, the HRS over LRS ratio is smaller for the 80nm thick channel. This can be explained in terms of the effective thickness of the conductive channel that, for depletion-mode FETs, increases with t_{ch}.

Fig.8 also shows that for the enhancement-mode FeFETs the resistance modulation is less sensitive to t_{ch}, because in enhancement-mode transistors the current is carried by the electron inversion layer.

The large HRS/LRS ratios in Fig.8 suggest that a large number of intermediate resistance levels may be accommodated in the devices, particularly in the enhancement-mode FeFETs. A systematic investigation of this latter aspect, however, would require to explore also the use of a fast, pulsed read operation [11], which goes beyond the quasi static regime considered so far, and actually beyond the scope of the present work.

5 Conclusions

We have investigated through numerical simulations and comparisons to experiments the ferroelectric switching in FeFETs and the resulting device operation. We found that the trapping in the ferroelectric-dielectric stack plays a crucial role for the polarization switching and thus for the hysteresis of the I_{DS}-V_{GS} characteristics. Then we used such a physical insight to explore on a sound ground the design of BEOL compatible FeFETs with a thin polysilicon channel. While our present results have been limited to a quasi static operation, an extension to pulsed read conditions is an important extension that we foresee to undertake in the near future.

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