EUROSOI-ULIS CONFERENCE

CONFERENCE PROGRAMME

DATE

18th-20th May 2022

VENUE

Università degli Studi di Udine – Sala Convegni Gusmani – Palazzo Antonini.

ORGANIZING SECRETATIAT

Centro Congressi Internazionale srl
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CONFERENCE SPONSOR

8th Joint International EuroSOI Workshop and International Conference on Ultimate Integration on Silicon (EuroSOI-ULIS) 2022

May 18-20, 2022 – Udine, Italy

The conference will be held in presence at Università degli Studi di Udine – Sala Convegni Gusmani – Palazzo Antonini.

The Conference aims at gathering together scientists and engineers working in academia, research, and industry the field of SOI technology and nanoscale devices in MoreMoore and MoreThanMoore scenarios.

COMMITTEE

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Cezar Zota (IBM Zurich)
Joris LACORD (CEA-Leti, France)
Bogdan CRETU (ENSICAEN, France)

Invited speakers

Marco Pala

Title: Frontiers in the atomistic simulation of nanoscale electron devices

Abstract: Addressing accurate simulations of electronic and transport properties of nanoscale devices requires to consider physical models including quantum mechanical effects as well as phonon scattering and spatial fluctuations due to non-ideal surfaces and defects. Self-consistent quantum simulations based on the non-equilibrium Green's function formalism have been extensively used for this purpose during the last years. This talk will briefly discuss this methodology and show advantages and drawbacks of different Hamiltonian models used to describe the energy dispersion of the channel material, going from the effective mass approximation to the empirical tight-binding model. Illustrative results on FDSOI and nanowire FETs will be presented. Finally, the theory and application of a first-principles transport methodology employing a basis set composed of the Bloch functions will be introduced. Such an approach enables full ab-initio quantum transport calculations with a reasonable computational cost and permits to address self-consistent simulations of electron devices based on novel 2D materials.

Marco Pala received the physics degree and the PhD in electronical engineering from the University of Pisa, Italy in 2000 and 2004, respectively. From 2004 to 2005 he was post-doc at CEA-LETI, Grenoble, France. He joined the CNRS as research scientist in 11/2005 at IMEP-LAHC, Grenoble. From 2016 he is with the Centre for Nanoscience and Nanotechnology (C2N), Palaiseau, France, where is the leader of the computational electronics group. His main research interests concern the electronic and transport properties of nanoscale devices. Recently, he worked on quantum transport calculations based on ab-initio methods to assess the use of new materials in nanoelectronics. He is co-author of 73 papers in peer-reviewed journals and 48 proceedings in international conferences.

Denis Rideau

Title: **Modeling Advances for Single Photon Avalanche Diode: From optical simulation to Monte Carlo simulation.**

Abstract: Single Photon Avalanche Diodes (SPAD) are key optoelectronic detectors for medical imaging, camera ranging and automotive laser imaging detection and ranging (LiDAR) applications. The optimization of the SPAD Figure Of Merits is strategic at an industrial level. Currently, the Photon Detection Probability (PDE), the timing statistic response to avalanche (Jitter) and the SPAD quench probability must be co-optimized using advanced numerical methods.

In this presentation we report a rigorous simulations using Monte Carlo Breakdown Probability (BRP) predictions coupled to optical simulations of PDE and Jitter (see figure 1). We also discuss in detail, the quench probability of these diodes once in avalanche. This latter point, rarely discussed in literature, is addressed using a Mixed-Mode Monte Carlo approach including the quench circuit.

Denis Rideau received a Ph.D. degree in Physics from the University of Orsay, France in 2001, and an Engineering degree at ESIEE, Paris in 1996. He is now performing TCAD simulations at STMicroelectronics, Crolles in France. His research interests are modelling and simulation of semiconductor nanodevices, with emphasis on quantum effects, strain effects, wafer orientations, and alternative channel materials in FDSOI and FinFets. He has

developed several codes for computing the electronic bandstructures in strain Si, Ge, and SiGe devices using the k.p-Schrödinger approach. He investigates by means of TCAD simulations advanced devices, including alternative III-V channel materials. In parallel he developed advanced solvers (Monte Carlo and NEGF) to simulate the transport properties of single-gate and multi-gate devices featuring stress, substrate orientation, SiGe materials and high-k/metal gate. He is an expert in the calibration of industrial TCAD software aiming in providing parameters but also validation and benchmarking on experimental.

Athanasios Dimoulas

Title: Ferroelectric Tunnel Junction memristors for neuromorphic technologies

Abstract: Ferroelectric Tunnel Junction (FTJ) memristors show promise as electronic synapses for low power neuromorphic circuits. First, the progress will be reviewed in the field of perovskite and recently discovered Hafnia based ferroelectrics such as $Hf_{0.5}Zr_{0.5}O_2$ (HZO), considering both double and single- layer gate stack designs. Then, the focus will shift on Metal-Ferroelectric-Semiconductor (MFS)-FTJs where the bottom electrode is a semiconductor (Ge or Nb:STO) and the top is W or TiN metal. The metastability of ferroelectricity due to depolarization fields will be discussed and the lower limits of HZO thickness to obtain stable ferroelectricity will be determined. It will be shown that HZO based MFS-FTJ behave as analog memristive non-volatile memories with very good endurance and retention and with a number of intermediate states showing synaptic plasticity, that is long term potentiation and depression as a function of the number of sequential pulses of varying amplitude or width. The role in the FTJ switching behavior of the Schottky barrier near the semiconductor/HZO interface will be elucidated. The programming and reading voltage of the synaptic devices are below 1V which makes them suitable for ultra-low power in-memory neuromorphic computing. Performance characteristics determining speed and low power operation of neuromorphic circuits will be addressed. Integration with CMOS either in the FEOL or the BEOL will also be discussed.

Dr. Athanasios Dimoulas is Research Director at NCSR-DEMOKRITOS in Athens. He is founder and head of Epitaxy and Surface Science Laboratory (ESSL) of the Institute of Nanoscience and Nanotechnology since 1999 and currently member of the advisor committee for physical sciences of the Greek government. He has been EC Human Capital and Mobility fellow at the university of Groningen, post-doctoral fellow at CALTECH and Research Associate at the University of Maryland. He has been visiting research scientist at IBM-Zurich and he has been appointed as Chair of Excellence at CEA-INAC(IRIG), and U. Grenoble Alpes, France. He has coordinated several collaborative EU projects and has been awarded the ERC advanced and proof of concept grants. He has served as chair of INFOS and chair of TPC committees of ESSDERC and IEDM. His current interests include 2D materials, topological materials and Hafnia based ferroelectric memristors for neuromorphic computing technologies.

Jacopo Franco

Title: NBTI defects in SiO2: identification and low thermal budget annealing strategies for future CMOS technology architectures

Abstract: Future CMOS technology architectures (Nanosheets, CFETs, Sequential 3D tier stacking) will require the development of low thermal budget process modules, including gate stack. A high-quality SiO2 interfacial layer, obtained in existing technologies by high-temperature (≥850°C) oxidation or annealing, is crucial for pMOS NBTI reliability. In low temperature SiO2, unrelaxed interface strain induces large defect densities, which we have identified – based on their electrical signature as compared to ab-initio calculations – as hydroxyl-E' structures forming at stretched Si-O bonds. Based on theoretical insights, we

have developed a combination of atomic and molecular hydrogen treatments to passivate these oxide defects efficiently at low temperatures (100-400°C), yielding an SiO2 quality which outperforms a reference thermal oxide grown at 900°C and a contemporary Replacement Gate (RMG) stack exposed to a conventional high-temperature anneal. We elucidate the implications of hydroxyl-E' defect de-activation by hydrogen on the permittivity of the SiO2 interfacial layer, on its effectiveness as a tunneling barrier and on the carrier mobility in the underlying Si channel, beside the dramatic improvement in NBTI reliability. Finally, we demonstrate that this low temperature oxide defect passivation is sufficiently thermally stable to withstand Back-End-Of-Line processing in a complete CMOS IC fabrication flow.

Jacopo Franco is a Principal Member of Technical Staff in the Reliability group of the Advanced Reliability, Robustness and Test department of imec, Belgium. He received the B.Sc. (2005) and M.Sc. (2008) from the University of Calabria - Italy, and the Ph.D. degree from KU Leuven - Belgium (2013) in Electrical Engineering. His research focuses on CMOS FEOL reliability characterization, optimization, and modelling, and in particular: i) on gate stack development for novel device technologies (SiGe, Ge, III-V, IGZO), architectures (finFETs, FD-SOI, Nanowires, Nanosheets), and integration schemes (Sequential 3D tier stacking, CFETs); ii) on characterization and physics-based modelling of FEOL degradation mechanisms (BTI, Hot Carrier, Off-state degradation, TDDB, RTN, time-dependent variability); iii) on reliability compact models to accurately propagate individual device aging to circuit level. He has (co-)authored 250+ contributed or invited papers and 3 patent families, and he is a recipient of several IEEE awards: Best Student Paper at SISC (2009), EDS Ph.D. Student Fellowship (2012), Paul Rappaport Award (2011), Best (2012), Outstanding (2014), and Best Student (2016) paper awards at IRPS. He has been serving in various functions on the Technical Program Committees of IRPS (Chair of the 'XT-Transistors' subcommittee in 2020), SISC, IIRW, ESREF, WoDiM and InFOS conferences, and as an Editor of IEEE Transactions on Device and Materials Reliability (2017-2020) and of IEEE Transactions on Electron Devices (2020-).

Program at a glance

Wednesday May 18

8.15-10.00	**Registrations**
10.00-10.15	Conference Opening
10.15-11.00	**Invited talk: A. Dimoulas (NCSR-DEMOKRITOS, Athens, Greece)** **Ferroelectric Tunnel Junction memristors for neuromorphic technologies**
11.00-11.20	Coffee break
11.20-12.40	S1-Modeling and characterization of noise
12.40-13.50	Lunch
13.50-14.35	**Invited talk: J. Franco (IMEC, Leuven, Belgium)** **NBTI defects in SiO2: identification and low thermal budget annealing strategies for future CMOS technology architectures**
14.35-15.15	S2-Defects and reliability
15.15-16.15	S3-More-than-Moore applications
16.15-16.30	Coffee break
16.30-18.00	S4-Poster session
19.30	Cocktail reception

Thursday May 19

9.00-9.45	**Invited talk: D. Rideau (STMicroelectronics, Crolles, France)** **Modeling Advances for Single Photon Avalanche Diode: From optical simulation to Monte Carlo simulation.**
9.45-10.45	S5-Optoelectronic devices
10.45-11.10	Coffee break
11.10-12.30	S6-Cryogenic electronics
12.30-14.00	Lunch
14.00-14.45	**Invited talk: T. Detzel (Infineon Technologies, Villach, Austria)** **GaN at Infineon: A ten year's journey to develop high performance and reliable power devices**
14.45-15.45	S7-GaN and SiC devices
15.45-16.10	Coffee break
16.10-17.50	S8-2D semiconductors
18.30-19.30	Udine City Tour
20.00	Gala Dinner & Awards

Friday May 20

9.00-9.20	Presentation of EUROSOI-ULIS 2023
9.20-10.05	**Invited talk: M. Pala (Centre for Nanoscience and Nanotechnology, Palaiseau, France)** **Frontiers in the atomistic simulation of nanoscale electron devices**
10.05-10.45	S9-Modeling and Simulation
10.45-11.10	Coffee break
11.10-12.30	S10-FDSOI and nanowire devices
12.30-14.00	Lunch
14.00-15.40	S11-Memory and memristive devices
15.40-16.00	Conference closing

Detailed Programme

Wednesday May 18

10.00-10.15	**Conference opening**
10.15-11.00	**Invited talk:** A. Dimoulas (NCSR-DEMOKRITOS, Athens, Greece) Ferroelectric Tunnel Junction memristors for neuromorphic technologies
11.00-11.20	**Coffee break**
	Session 1 **Modeling and characterization of noise** Chairpersons: S. Cristoloveanu (IMEP-LAHC, France), C. Claeys (KU Leuven, Belgium)
11.20-11.40	Lorentzian Spectra as a Tool for Enhanced Statistical Detection of Random Telegraph Noise *O. Gauthie[1], S. Haendler[1], P. Scheer[1], Q. Rafhay[2], C. Theodorou[2]* *[1]STMicroelectronics, Grenoble INP, Crolles, France* *[2]IMEP-LAHC, Université Grenoble Alpes/Université Savoie Mont Blanc/CNRS/Grenoble INP, Grenoble, France*
11.40-12.00	DC and low a frequency noise analysis of p channel gate all around vertically stacked silicon nanosheets *B. Cretu[1], A. Veloso[2], E. Simoen[2]* *[1]CNRS, ENSICAEN, Caen, France* *[2]IMEC, Leuven, Belgium*
12.00-12.20	On the accuracy of the formula used to extract trap density in MOSFETs from 1/f noise *R. Asanovski[1], P. Palestri[2], L. Selmi[1]* *[1]Università degli Studi di Modena e Reggio Emilia, DIEF, Modena, Italy* *[2]Università degli Studi di Udine, DPIA, Udine, Italy*
12.20-12.40	Impact of the Channel Doping on the Low-Frequency Noise of Silicon Vertical Nanowire pFETs *E. Simoen, A. Veloso, P. Matagne, C. Claeys* *IMEC, UMP, Leuven, Belgium*
12.40-13.50	**Lunch**

13.50-14.35	**Invited talk**: J. Franco (IMEC, Leuven, Belgium) NBTI defects in SiO2: identification and low thermal budget annealing strategies for future CMOS technology architectures
	Session 2 **Defects and reliability** Chairperson: B. Cretu (ENSICAEN, France)
14.35-14.55	Investigation and Optimization of Traps Properties in $Al2O_3/SiO_2$ Dielectric Stacks *Y. Yan, V. Kilchytska, S. Faniel, D. Flandre, J.-P. Raskin* *ICTEAM, Uclouvain, Louvain la Neuve, Belgium*
14.55-15.15	Comparison of OFF-State, HCI and BTI degradation in FDSOI Ω-gate NW-FETs *C. Valdivieso, A. Crespo-Yepes, R. Miranda, D. Bernal, J. Martin-Martinez, R. Rodriguez, M. Nafria* *Autonoma University of Barcelona, Electronic Engineering, Bellaterra, Spain*
	Session 3 **More-than-Moore applications** Chairperson: L. Donetti (Univ. of Granada, Spain)
15.15-15.35	Signal to noise ratio in nanoscale bioFETs *C. A. Bergfeld Mori[1], K. Martens[2], E. Simoen[3], P. Van Dorpe[2], P. Ghedini Der Agopian[4], J. A. Martino[1]* *[1]Escola Politécnica da Universidade de São Paulo, São Paulo, Brazil* *[2]IMEC, Life Science Technology, Leuven, Belgium* *[3]IMEC, EPI Group, Leuven, Belgium* *[4]UNESP, São Paulo State University, São João da Boa Vista, Brazil*
15.35-15.55	Statistical Device Simulations of III-V Nanowire Resonant Tunneling Diodes as Physical Unclonable Functions Source *A. Rezaei, P. Maciazek, A. Sengupta, T. Dutta, C. Medina-Bailon, A. Asenov, V. Georgiev* *University of Glasgow, James Watt School of Engineering, Glasgow, United Kingdom*
15.55-16.15	Impact of Substrate Resistivity on Spiral Inductors at MM-Wave Frequencies *L. Nyssens[1], M. Rack[1], C. Schwan[2], Z. Zhao[2], S. Lehmann[2], T. Hermann[2], F. Allibert[3], C. Aulnette[3], D. Lederer[1], J.-P. Raskin[1]* *[1]Institute for Information and Communication Technologies, Electronics and Applied Mathematics, Université catholique de Louvain, Louvain-la-Neuve, Belgium* *[2]GlobalFoundries, Dresden, Germany* *[3]Soitec, Bernin, France*
16.15-16.30	**Coffee break**

16.30-18.00	**Session 4** **Poster session** A Frequency Tripler in 22-nm FDSOI Technology for FMCW spectrum *P. Kumar, D. Stajic, K. Narayanan Rama, E. Isa, L. Maurer* *IMS, EIT4, Universität Der Bundeswehr, Munich, Germany* Parallel Nanowire Sensors with High-k Gate Oxide for the Sensitive Operation in Liquids *V. Popov[1], F. Tikhonenko[1], V. Antonov[1], A. Zarubanov[2], A. Gluhov[2], A. Tatarintsev[3], A. Miakonkikh[3], K. Rudenko[3]* *[1]Rzhanov Institute of Semiconductor Physics, Silicon based materials, Novosibirsk, Russian Federation* *[2]JSC, Separate design bureau, Novosibirsk, Russian Federation* *[3]Valiev Institute of Physics and Technology RAS, Laboratory of Microstructuring and Submicron Devices, Moscow, Russian Federation* Structure Evolution and Charge Hysteresis in Hafnia-Alumina Buried Oxides *V. Popov[1], F. Tikhonenko[1], V. Antonov[1], A. Lomov[2], A. Miakonkikh[2], K. Rudenko[2]* *[1]Rzhanov Institute of Semiconductor Physics, Silicon based materials, Novosibirsk, Russian Federation* *[2]Valiev Institute of Physics and Technology RAS, Laboratory of Microstructuring and Submicron Devices, Moscow, Russian Federation* Assessing the effect of Scaling High-Aspect-Ratio ISFET with Physical Model Interface for Nano-Biosensing Application *R. Dhar[1], N. Kumar[1], C. P. Garcia[2], V. Georgiev[1]* *[1]University of Glasgow, Electronics and nanoscale engineering, Glasgow, United Kingdom* *[2]Luxembourg Institute of Science and technology, Luxembourg Institute of Science and technology, Belvaux, Luxembourg* Si GAA NW FETs Threshold Voltage Evaluation *D. Dobrescu[1], B. Cretu[2], E. Simoen3, A. Veloso[3], A. Voicu-Spineanu[1], L. Dobrescu[1]* *[1]University POLITEHNICA of Bucharest, Faculty of Electronics, Telecommunication and Information Technology, Bucharest, Romania* *[2]Normandie Univ, ENSICAEN, CNRS, Caen, France* *[3]IMEC, Leuven, Belgium* Scalability and Sensitivity Assessment of Programmable Transistor based 1T-DRAM *R. K. Nirala, S. Semwal, Y.V. Bhuvaneshwari, N. Rai, A. Kranti* *Indian Institute of Technology Indore, Department of Electrical Engineering, Indore, India*

	Cross-Coupling Effects Analysis in Common-Source Current Mirrors Composed by UTBB Transistors *F. Costa[1], R. Trevisoli Doria[2], R. Trevisoli Doria1* *[1]Centro Universitário FEI, Electrical Engineering, São Bernardo do Campo, Brazil* *[2]Universidade Federal do ABC, Electrical Engineering, Santo André, Brazil* Thickness-dependent dielectric breakdown in thick amorphous SiO_2 capacitors *F. Giuliano[1], S. Reggiani[1], E. Gnani[1], A. Gnudi[1], M. Rossetti[2], R. Depetro[2]* *[1]University of Bologna, ARCES and DEI, Bologna, Italy* *[2]STMIcroelectronics, Technology R/D, Agrate Brianza, Italy* Study of gate current in advanced MOS architectures *G.A. Gauhar[1], A. Chenchety[1], H. Yenugula[1], V. Georgiev[2], A. Asenov[2], O. Badami[1]* *[1]Indian Institute of Technology Hyderabad, Electrical Engineering, Hyderabad, India* *[2]University of Glasgow, James Watt School of Engineering, Glasgow, UK* Understanding Negative Capacitance Physical Mechanism in Organic Ferroelectric Capacitor *K. J. Singh, A. Bulusu, S. Dasgupta* *Indian Institute of Technology Roorkee, Roorkee, India* Finite Element Modeling of Spin-Orbit Torques *N. P. Jørstad[1], S. Fiorentini[1], J. Ender[1], R. L. de Orio[1], T. Hadámek[1], W. J. Loch1, M. Bendra[1], W. Goes[2], S. Selberherr[1], V. Sverdlov[1]* *[1]Institue for Microelectronics, TU Wien, Vienna, Austria* *[2]Silvaco, Silvaco Europe Ltd., Cambridge, United Kingdom* Comparison between Low-Dropout Voltage Regulators Designed with Line and Nanowire Tunnel Field Effect Transistors using Experimental Data *R. do Nascimento Tolêdo, W. de Lima Silva, W. Gonçalves Filho, A. de Moraes Nogueira, J. A. Martino, P. Ghedini Der Agopian* *University of São Paulo, LSI/PSI/USP, Sao Paulo, Brazil* CaF_2 as high-k dielectric for Si devices *J. Chen[1], Z. Zhang[1], Y. Guo[2], J. Robertson[1]* *[1]University of Cambridge, Electrical Engineering, Cambridge, United Kingdom* *[2]Swansea University, College of Engineering, Swansea, United Kingdom* Design methodology of a 28 nm FD-SOI Capacitive Feedback RF LNA based on the ACM Model and Look-up Tables *G. C. Britton Orozco[1], E. Lauga-Larroze[1], S. Mir[1], P. Galy[2]* *[1]TIMA, Univ. Grenoble Alpes, Grenoble, France* *[2]STMicroelectronics, Crolles, Crolles, France*
19.30	**Cocktail reception** at *Italian Secret Bar, Piazza Giacomo Matteotti, 18, 33100 Udine UD*

Thursday May 19

9.00-9.45	**Invited talk**: D. Rideau (STMicroelectronics, Crolles, France) Modeling Advances for Single Photon Avalanche Diode: From optical simulation to Monte Carlo simulation.
	Session 5 **Optoelectronic devices** Chairpersons: V. Georgiev (Univ. Glasgow, UK), M. Pala (C2N, Palaiseau, France)
9.45-10.05	Avalanche breakdown and quenching in Ge SPAD using 3D Monte Carlo simulation *P. Dollfus[1,2], J. Saint-Martin[2], T. Cazimajou[2], R. Helleboid[3], A. Pilotto[2], D. Rideau[3], A. Bournel[2], M. Pala[1,2]* *[1]CNRS, Palaiseau, France* *[2]University of Paris-Saclay / C2N, Palaiseau, France* *[3]STMicroelectronics, Crolles, Crolles, France*
10.05-10.25	Modeling of SPAD avalanche breakdown probability and jitter tail with field lines *R. Helleboid[1], D. Rideau[2], J. Grebot[2], I. Nicholson[2], N. Moussy[3], O. Saxod[3], J. Saint-Martin[1], M. Pala[1], P. Dollfus[1]* *[1]University of Paris-Saclay / C2N, Palaiseau, France* *[2]STMicroelectronics, Crolles, Crolles, France* *[3]CEA, LETI, Grenoble, France*
10.25-10.45	Parasitic Oscillation in the Low-Frequency Noise Characterization of Solar Cells *C. Wulles[1], Q. Rafhay[1], A. Kaminski[1], T. Desrues[2], C. Theodorou[1]* *[1]Grenoble INP, IMEP-LaHC, Grenoble, France* *[2]CEA, Liten, Le Bourget-du-Lac, France*
10.45-11.10	**Coffee break**
	Session 6 **Cryogenic electronics** Chairpersons: C. Zota (IBM Zurich, Switzerland), A. Kloes (THM Univ., Giessen, Germany)
11.10-11.30	Cryogenic Characteristics of UTBB SOI Schottky-Barrier MOSFETs *Y. Han, J. Sun, F. Xi, J.-H. Bae, D. Grützmacher, Q.-T. Zhao* *Peter Grünberg Institute (PGI-9), Forschungszentrum jülich, Jülich, Germany*
11.30-11.50	Interpretation of 28 nm FD-SOI quantum dot transport data taken at 1.4 K using 3D Quantum TCAD simulations *I. Kriekouki[1,2,3], F. Beaudoin[4], P. Philippopoulos[4], C. Zhou[4], J. Camirand-Lemyre[2], S. Rochette[2], S. Mir[3], M. J. Barragan[3], M. Pioro-Ladrière[2], P. Galy[1]* *[1]STMicroelectronics, Crolles, France* *[2]Institut quantique, Université de Sherbrooke, Sherbrooke, Quebec, Canada* *[3]TIMA, Université Grenoble Alpes, CNRS, Grenoble INP, Grenoble, France* *[4]Nanoacademic Technologies, Quantum Technology, Montreal, Canada*

11.50-12.10	TCAD Simulations of FDSOI devices down to Deep Cryogenic Temperature *E. Catapano[1,2], M. Cassé[1], F. Gaillard[1], S. de Franceschi[3], T. Meunier[4], M. Vinet[1], G. Ghibaudo[2]* *[1]CEA-LETI, Grenoble, France* *[2]IMEP-LAHC, Université Grenoble-Alpes, Grenoble, France* *[3]CEA-IRIG, Grenoble, France* *[4]CNRS, Institut Néel, Université Grenoble-Alpes, Grenoble, France*
12.10-12.30	Threshold voltage extraction method comparison from room temperature down to cryogenic temperature on 28nm FD SOI CMOS technology. *Q. Berlingard[1], J. Lugo-Alvarez[1], M. Bawedin[2], L. Contamin[1], P. Galy[3], S. De Franceshi[4], T. Meunier[5], M. Vinet[1], F. Gaillard[1], M. Cassé[1]* *[1]CEA - Leti, Univ. Grenoble Alpes, Grenoble, France* *[2]IMEP-LAHC, Univ. Grenoble Alpes, Grenoble, France* *[3]STMicroelectronics Grenoble, Grenoble, France* *[4]CEA-IRIG, Univ. Grenoble Alpes, Grenoble, France* *[5]CNRS - Institut Néel, Univ. Grenoble Alpes, Grenoble, France*
12.30-14.00	**Lunch**
14.00-14.45	**Invited talk**: T. Detzel (Infineon Technologies, Villach, Austria) GaN at Infineon: A ten year's journey to develop high performance and reliable power devices
	Session 7 **GaN and SiC devices** Chairpersons: F. Gamiz (Univ. of Granada, Spain)
14.45-15.05	Effect of doping on Al_2O_3/GaN MOS capacitance *B. Rrustemi[1], C. Piotrowicz[1], M.-A. Jaud[1], F. Triozon[1], W. Vandendaele[1], B. Mohamad[1], R. Gwoziecki[1], G. Ghibaudo[2]* *[1]CEA-Leti, University Grenoble Alpes, Grenoble, France* *[2]IMEP-LAHC Minatec, University Grenoble Alpes, Grenoble, France*
15.05-15.25	A Comprehensive Analysis of AlN spacer and AlGaN n-doping effects on the 2DEG Resistance in AlGaN/AlN/GaN Heterostructures *C. Piotrowicz[1], B. Mohamad[1], B. Rrustemi[1], N. Malbert[2], M.-A. Jaud[1], M. Charles[1], R. Gwoziecki[1]* *[1]CEA, LETI, Grenoble, France* *[2]IMS, University of Bordeaux, Bordeaux, France*
15.25-15.45	Group velocity of electrons in 4H-SiC from Density Functional Theory simulations *L. Balestra, S. Reggiani, A. Gnudi, E. Gnani* *University of Bologna, ARCES and DEI, Bologna, Italy*
15.45-16.10	**Coffee break**

	Session 8 **2D semiconductors** Chairpersons: F. Balestra (IMEP Minatec, France), D. Esseni (Univ. Of Udine, Italy)
16.10-16.30	Phonon-assisted transport in van der Waals heterostructure tunnel devices *A. M'foukh, J. Saint-Martin, P. Dollfus, M. Pala* *Centre des nanosciences et nanotechnologies, Université Paris-Saclay/CNRS, Palaiseau, France*
16.30-16.50	Modeling and optimization of graphene ballistic rectifiers *D. Truccolo, S. Boscolo, D. Esseni, M. Midrio, P. Palestri* *DPIA, University of Udine, Udine, Italy*
16.50-17.10	A study of metal-MoS_2 contacts by using an in-house developed ab-initio transport simulator *D. Lizzit[1], P. Khakbaz[1], F. Driussi[1], M. Pala[2], D. Esseni[1]* *[1]DPIA, University of Udine, Udine, Italy* *[2]Université Paris-Saclay - CNRS, Centre de Nanosciences et de Nanotechnologies, Palaiseau, France*
17.10-17.30	DFT-based layered dielectric model of few-layer MoS_2 *L. Donetti, C. Navarro, C. Marquez, C. Medina-Bailon, J. L. Padilla, F. Gamiz* *Universidad de Granada, Departamento de Electrónica, CITIC, Granada, Spain*
17.30-17.50	Reduced Contact Resistances for Moire Interfaces of Monolayer MoS_2 *Z. Zhang[1], Y. Guo[2], J. Robertson[1]* *[1]Cambridge University, Engineering Dept, Cambridge, UK* *[2]Wuhan University, Engineering, Wuhan, Cina*
18.30 – 19.30	**Udine City Tour,** m*eeting poit at 18.30 piazza Libertà, Loggia di San Giovanni*
20.00	**Gala Dinner & Awards** at *Casa della Contadinanza, P.le della Patria del Friuli, 2, Udine*

Friday May 20

9.00-9.20	**Presentation of EUROSOI-ULIS 2023**
9.20-10.05	**Invited talk:** M. Pala (Centre for Nanoscience and Nanotechnology, Palaiseau, France) Frontiers in the atomistic simulation of nanoscale electron devices
	Session 9 **Modeling and Simulation** Chairperson: D. Lizzit (Univ. Of Udine, Italy)
10.05-10.25	Implementation of Device-to-Device and Cycle-to-Cycle Variability of Memristive Devices in Circuit Simulations *C. Bischoff[1], J. Leise[1], E. Perez-Bosch Quesada[2], E. Perez[2], C. Wenger[2], A. Kloes[1]* *[1]THM University of Applied Sciences, NanoP, Giessen, Germany* *[2]IHP-Leibniz-Institut für innovative Mikroelektronik, Material Research, Frankfurt (Oder), Germany*
10.25-10.45	Performance of FDSOI Double-Gate Dual-Doped Reconfigurable FETs *C. Navarro, L. Donetti, J. L. Padilla de la Torre, C. Medina-Bailón, J. Ávila, J. C. Galdón, M. Recio, C. Márquez, C. Sampedro, F. Gámiz* *Universidad de Granada, Electrónica y Tecnología de los Computadores, Granada, Spain*
10.45-11.10	**Coffee break**
	Session 10 **FDSOI and nanowire devices** Chairpersons: A. Zaslavsky (Brown University, USA), J.A. Martino (Univ. of Sao Paulo, Brazil)
11.10-11.30	Extraction of small signal equivalent circuit for de-embedding of 3D vertical nanowire transistor *B. Neckel Wesling[1], M. Deng[1], C. Mukherjee[1], A. Kumar[2], G. Larrieu[2], K. Trommer[3], T. Mikolajick[3], C. Maneux1* *[1]IMS, University of Bordeaux, Bordeaux, France* *[2]LAAS-CNRS, Université of Toulouse, Toulouse, France* *[3]NaMLab gGmgH, Namlab gGmbH, Dresden, Germany*
11.30-11.50	Superiority of Core-Shell Junctionless FETs *S. Cristoloveanu, G. Ghibaudo* *IMEP, UGA, Grenoble, France*
11.50-12.10	Electrical Characteristics of n-Type Vertically Stacked Nanowires Operating up to 600 K *G. Mariniello[1], S. Barraud[2], M. Vinet[2], M. Cassé[2], O. Faynot[2], J. Calcade Rodrigues[1], M. A. Pavanello[1]*

	[1]Centro Universitario FEI, Sao Bernardo do Campo, Brazil *[2]CEA-LETI, Grenoble, France*
12.10-12.30	Experimental study of thermal coupling effects in FD-SOI MOSFET *M. Vanbrabant, J.-P. Raskin, D. Flandre, V. Kilchytska* *Université catholique de Louvain, ICTEAM, Louvain la Neuve, Belgium*
12.30-14.00	**Lunch**
	Session 11 **Memory and memristive devices** Chairpersons: F. Driussi (Univ. Of Udine, Italy), P. Palestri (Univ. Of Udine, Italy)
14.00-14.20	Double Reference Layer STT-MRAM Structures with Improved Performance *J. W. Loch[1], S. Fiorentini[1], N. P. Jørstad[1], J. Ender[1], R. L. de Orio[1], T. Hadamek[1], M. Bendra[1], W. Goes[2], S. Selberherr[1], V. Sverdlov[1]* *[1]Vienna University of Technology, Institute for Microelectronics, Vienna, Austria* *[2]Silvaco Europe, Cambridge, United Kingdom*
14.20-14.40	Versatile experimental setup for FTJ characterization *M. Massarotto[1], F. Driussi[1], A. Affanni[1], S. Lancaster[2], S. Slesazeck[2], T. Mikolajick[2], D. Esseni[1]* *[1]Università degli Studi di Udine, DPIA, Udine, Italy* *[2]NaMLab gGmbH, Dresden, Germany*
14.40-15.00	Hydrothermally formed copper oxide (CuO) thin films for resistive switching memory devices *R. Mroczynski* *Institute of Microelectronics and Optoelectronics, Warsaw University of Technology, Warsaw, Poland*
15.00-15.20	Interface Effects in Ultra-Scaled MRAM Cells *M. Bendra[1], S. Fiorentini[1], J. Ender[1], R. L. de Orio[1], T. Hadámek[1], J.W. Loch[1], N. P. Jørstad[1], W. Goes[2], S. Selberherr[1], V. Sverdlov[1]* *[1]Vienna University of Technology, Institute for Microelectronics, Vienna, Austria* *[2]Silvaco Europe, Cambridge, United Kingdom*
15.20-15.40	Effect of SOI substrate on Silicon Nitride Resistance Switching using MIS structure *A. Mavropoulis[1], N. Vasileiadis[1], C. Theodorou[2], L. Sygellou3, P. Normand[1], G. Sirakoulis[4], P. Dimitrakis[1]* *[1]Institute of Nanoscience and Nanotechnology, NCSR "Demokritos", Ag. Paraskevi Greece* *[2]IMEP-LAHC, Grenoble INP, Grenoble, France* *[3]Institute of Chemical Engineering Sciences, FORTH/ ICE-HT, Patras, Greece* *[4]Department of Electrical and Computer Engineering, Democritus University of Thrace, Xanthi, Greece*
15.40-16.00	**Conference closing**
17:00	**GETTING TOGETHER**

General Information

VENUE

Università degli Studi di Udine – Sala Convegni Gusmani – Palazzo Antonini
The "**Gusmani**" **hall** is on the ground floor of the **Palazzo Antonini Cernazai,** prestigious late-16th century building and today home to the **Humanities Faculty of the Udine university**.
Just a few metres from the rooms is a **large, internal park**.
The venue is located in Via Petracco 8, Udine. **Check on maps.**

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The conference room is equipped with a WiFi connection. The University regulation does not allow to have "guest" accounts: each account should be connected to a specific person. If your institution is in the Eduroam organization you can connect to the Eduroam network present in the conference room and in the University premises using the same WiFi account you use at your institution. Please check on **https://eduroam.org/** and **https://cat.eduroam.org/#.** From our experience, most of you can access this network. Personal accounts will be generated on request if your institution is not in the Eduroam organization.

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CCI adopts appropriate health safety protocols to prevent the risk of Sar-Cov-2 contagion, for its Staff and Partners, and during all external activities.

Health safety and prevention are essential standard requirements in current Sar-Covid-2 pandemic situation, but this will persist as a quality standard even when the virus will be defeated.

For this reason, CCI had adopted specific protocols to measure the biological risk in the event, allows its control and reduction, and guide through a correct practical application.

CCI protocol has been elaborated according to current Health Ordinances issued by the Italian Ministry of Health, to the "Guidelines for the reopening of Economic, Productive and Recreational Activities" issued by the Italian Government, and the specific Guidelines issued by Italian Trade Association of Professional Congress Organizers.

Further detailed information concerning how to manage and reduce the biological risk during events, outlined in the World Health Organization (WHO) Risk Assessment Document, are available for all CCI events Participants and Partners.

Do not hesitate to ask for them at info@ccicongress.com

PLEASE, BE AWARE THAT FACE MASK IS MANDATORY TO ACCESS THE CONFERENCE.

ORGANIZING SECRETATIAT

Centro Congressi Internazionale srl
Via Guarino Guarini, 4 - 10123 Torino - Italy
Tel. +39 011 2446911 - Fax +39 011 2446950
www.ccicongress.com