Minimum Subthreshold Swing in DS-FETs Based on Graphene and 3D Dirac Metals

Minimum Subthreshold Swing in DS-FETs based on Graphene and 3D Dirac metals

Erica Baccichetti, Riccardo Marcon and David Esseni, *Fellow, IEEE*

***Abstract*— We present analytical models and numerical simulations addressing the fundamental limits to the sub-threshold swing (SS) in Dirac-Source FETs (DS-FETs), based on either graphene or 3D Dirac semimetals. To this purpose, we devised and implemented a semi-analytical model for DS-FETs employing a 3D Dirac source. Numerical results confirm analytical predictions. Our findings help to clarify the physics behind the minimum SS in DS-FETs, and the possible advantages offered by 3D Dirac semimetals.**

***Index Terms*— Dirac semi-metals, Dirac-source FETs, Fundamental limits, Graphene.**

I. Introduction

In a scenario where AI applications are breathlessly increasing the computing and memory requirements, the energy efficiency of information technologies has become crucial [1]. Steep-slope FETs have been identified as possible enablers of a widespread reduction of the supply voltage, V_{DD}, and thus of the energy consumption in digital circuits [2]. Most device candidates, however, have failed to deliver an SS below 60 mV/dec and at the same time a large enough on-current I_{ON}.

Dirac Source FETs (DS-FETs) have been experimentally demonstrated as steep-slope FETs by using carbon nanotubes [3], or graphene and MoS_2 systems [4], [5], and modeling studies have discussed more design options [6], [7], [8]. The physics behind the steep-slope operation in DS-FETs is recalled in Fig. 1(a), where we see that in the p–type source of an n–type DS-FET, the electron density $n(E)$ decays more steeply than the Boltzmann limit for an energy E above the source Fermi level, $E_{F,S}$, and below the Dirac energy, E_D. DS-FETs have also potential advantages over Tunnel-FET in terms of I_{ON}, as DS-FETs do not rely on band-to-band-tunnelling [2]. The minimum SS in DS-FETs has not been discussed in details though, nor has the SS gain that could be delivered by 3D Dirac semimetals (e.g. CoSi,NbP) compared to graphene.

In this paper, we report analytical derivations and numerical simulations showing that the minimum SS for a DS-FET based on a 2D or a 3D Dirac source semimetal is respectively 37 mV/dec and 30 mV/dec at T=300 K. To this purpose, we also devised and implemented the first-to-our-knowledge semi-analytical model for a 3D Dirac source FET.

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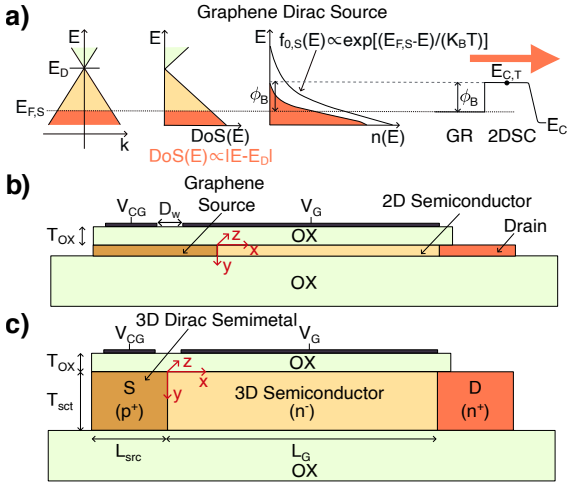

Fig. 1. **(a)** Schematic E(**k**), density of states $\boldsymbol{DoS(E)}$ and electron density $\boldsymbol{n(E)}$ for a $\boldsymbol{p}$-type graphene source, and thermionic electron emission over a potential energy barrier $\boldsymbol{\phi_B}$. **(b)** Sketch for a graphene-based $\boldsymbol{n}$–type DS-FET. **(c)** Sketch for an $\boldsymbol{n}$–type DS-FET having a 3D Dirac semimetal source. In both devices, the voltage $\boldsymbol{V_{CG}}$ at the control gate is used to exert an electrostatic doping in the source region.

II. Analytical Models for SS in DS-FETs

Inelastic phonon scattering can degrade the SS of DS-FETs [7], [8], therefore the minimum SS corresponds to a ballistic transport limit, whereby the current can be written using the Landauer approach as

$$I_{DS} = \frac{2q}{h}\int_{E_{C,T}}^{+\infty} M(E)T(E)[f_{0,S}(E) - f_{0,D}(E)]dE \quad (1)$$

where q and h are respectively the electron charge and the Plank constant, $E_{C,T}$ is the top of the semiconductor conduction band in the channel region (see Fig. 1(a)), and $f_{0,S}$ ($f_{0,D}$) is the Fermi function at the source (drain) reservoir. Moreover, $M(E)$ is the number of conduction modes, that we assume to be limited by the modes in the Dirac source [7], [9], and $T(E)$ is the corresponding transmission. Eq. (1) neglects the tunnelling current components for $E<E_{C,T}$, which is a good approximation if the channel region is longer than about 15-20 nm. Based on Eq. (1), SS is by definition given by

$$\frac{1}{SS} = \frac{1}{\ln(10)}\frac{1}{I_{DS}}\left|\frac{\partial I_{DS}}{\partial E_{C,T}}\right|\left|\frac{\partial E_{C,T}}{\partial V_G}\right| \quad (2)$$

where V_G is the gate voltage and $(\partial E_{C,T}/\partial V_G)$ is a figure linked to the device electrostatic integrity, with $|\partial E_{C,T}/\partial(qV_G)|\simeq 1$ being the ideal, maximum value [10].

The distinctive property of Dirac materials is the fact that, close to the Dirac energy E_D, the energy relation is approximately given by $E(\mathbf{k})=E_D \pm \hbar v_F|\mathbf{k}-\mathbf{k}_D|$, where v_F is the Fermi velocity, $\mathbf{k}$ is a two- or a three-component wave-vector (respectively for graphene and for 3D Dirac semimetals), and $\mathbf{k}_D$ is the wave-vector at the Dirac point. Based on such $E(\mathbf{k})$ relations, when E is close to energy E_D the number of modes in the device can be written as

$$\textbf{(a)}\ M_{2D}(E)=\frac{n_v W_z}{\pi\hbar v_F}|\epsilon|,\ \textbf{(b)}\ M_{3D}(E)=\frac{n_v T_{sct} W_z}{4\pi\hbar^2 v_F^2}\epsilon^2 \quad (3)$$

where $\epsilon=(E-E_D)$, n_v is the valley degeneracy, and T_{sct}, W_z are the device widths along the directions y and z normal to the transport direction x, as it is depicted in Fig. 1(b)(c).

For analytical derivations, we will hereafter assume $T(E)\approx 1$ for energies $E\geq E_{C,T}$ (see Fig. 1(a)), corresponding to a simple ballistic model that disregards the finite resistance of the p-n junction [9], [11], [12], and the influence of phonon scattering [7], [8]. These simplifications are in the spirit of an idealized analysis targeting the minimum subthreshold swing.

For a graphene DS-FET the electronic modes are given by Eq. (3)(a), which can be used into Eq. (1) to calculate I_{DS}. In subthreshold, $E_{C,T}$ is well above the Fermi levels $E_{F,S}$ and $E_{F,D}=(E_{F,S}-q\mathrm{V}_{DS})$ at source and drain, hence the Fermi functions $f_{0,S}$, $f_{0,D}$ in Eq. (1) can be approximated by a Boltzmann function for $E>E_{C,T}$. Assuming $T(E)\approx 1$ for $E\geq E_{C,T}$, Eq. (1) provides

$$I_{DS}\approx K_{I2}\left[2-e^{-\eta_{C,T}}(1+\eta_{C,T})\right](e^{\eta_S}-e^{\eta_D}) \quad (4a)$$

$$K_{I2}=\left[qn_v W_z (K_B T)^2\right]/\left(\hbar^2\pi^2 v_F\right) \quad (4b)$$

where $\eta_{S(D)}=(E_{F,S(D)}-E_{D,S})/(K_B T)$, $\eta_{C,T}=(E_{C,T}-E_{D,S})/(K_B T)$ and $\eta_D \ll \eta_S$ if $(q\mathrm{V}_{DS})$ is larger than a few $(K_B\mathrm{T})$. Equation (4a) assumes $E_{C,T}<E_{D,S}$, namely $\eta_{C,T}<0$. The SS corresponding to Eq. (4a) can be readily calculated from Eq. (2). For a device with a nearly ideal electrostatic integrity (i.e. for $|\partial E_{C,T}/\partial(qV_G)|\simeq 1$), we obtain

$$SS=(K_B T/q)\ln(10)\left[\left(\eta_{C,T}+1-2e^{\eta_{C,T}}\right)/\eta_{C,T}\right]. \quad (5)$$

An expression for SS similar to Eq. (5) has been already reported in [13]. The minimum of the SS given by Eq. (5) is $SS_{min}\approx 0.627\cdot\ln(10)(K_B T/q)$ for $\eta_{C,T}\approx -1.678$, namely $SS_{min}\approx 37 mV/dec$ at T=300 K.

For an ideal 3D Dirac material, the electronic modes are given by Eq. (3)(b). By substituting $M_{3D}(E)$ in Eq. (1), assuming Boltzmann statistics in the subthreshold region and taking $T(E)\approx 1$ for $E\geq E_{C,T}$, we readily obtain

$$I_{DS}=K_{I3}\left[\eta_{C,T}^2+2\eta_{C,T}+2\right]e^{-\eta_{C,T}}(e^{\eta_S}-e^{\eta_D}) \quad (6a)$$

$$K_{I3}=\left[qn_v T_{sct} W_z (K_B T)^3\right]/\left(4\pi^2\hbar^3 v_F^2\right). \quad (6b)$$

By using Eq. (6a) in Eq. (2) and assuming ideal electrostatic conditions (i.e. $|\partial E_{C,T}/\partial(qV_G)|\simeq 1$), we have

$$SS=(K_B T)/q\ln(10)\left[\left(\eta_{C,T}^2+2\eta_{C,T}+2\right)/\eta_{C,T}^2\right]. \quad (7)$$

The minimum of the SS given by Eq. (7) is found for $\eta_{C,T}=-2$ and it is $SS_{min}=(1/2)\ln(10)(K_B T/q)$, namely $SS_{min}\approx 30 mV/dec$ at T=300 K.

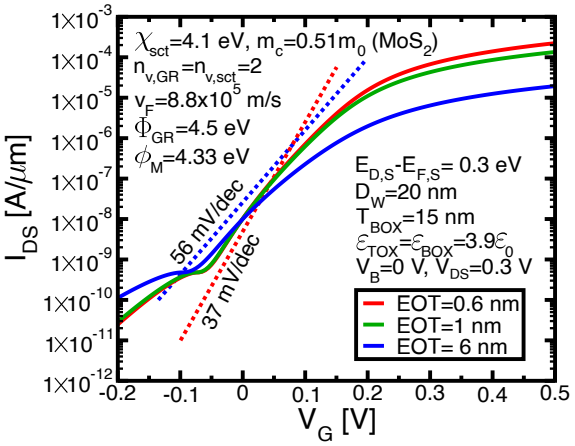

Fig. 2. Current $\boldsymbol{I_{DS}}$ versus $\boldsymbol{V_G}$ for the graphene-based DS-FET sketched in Fig. 1(b), and calculated using the approach in [9]. The hole concentration at source is $\boldsymbol{p\approx 8.75\times 10^{12}\mathrm{cm}^{-2}}$, corresponding to $\boldsymbol{E_{D,S}-E_{F,S}=0.3}$ eV. The transition width of the graphene $\boldsymbol{p-n}$ junction in the access region is $\boldsymbol{D_W=20}$ nm [9].

III. Numerical Simulations

Numerical results for the graphene DS-FET in Fig. 1(b) are here based on the transfer-matrix transport model recently reported in [9]. If not otherwise mentioned, all calculations correspond to T=300 K. In Fig. 2, we show the current in a graphene-based DS-FET for different values of the equivalent oxide thickness (EOT) of the top gate. In fact, because our one-dimensional electrostatic model implicitly assumes a long channel operation, here we modulate the electrostatic integrity of the DS-FET by changing EOT. As it can be seen, for an EOT of 1 nm or below the SS can approach the 37 mV/dec limit identified in Section II, as the electrostatics is close to the ideal condition $|\partial E_{C,T}/\partial(qV_G)|\simeq 1$. By increasing EOT, however, the SS is deteriorated. For the SS of a graphene-based DS-FET, we could confirm the 37 mV/dec limit even by using the *ab-initio* simulation approach of [8] (not shown).

We hereafter develop a simple semi-analytical model for the DS-FET in Fig. 1(c) employing a 3D Dirac source. We start with the electrostatic doping of the source and notice that, based on the energy relation $E(\mathbf{k})=E_D\pm\hbar v_F|\mathbf{k}-\mathbf{k}_D|$, the density of states for a 3D Dirac semimetal is given by $D(E)=K_D(E-E_D)^2$, with $K_D=2n_v/(2\pi^2(\hbar v_F)^3)$. Hence, in the zero temperature approximation, the equilibrium density of electrons, n, and holes, p, are proportional to $|E_D-E_F|^3$. The equilibrium charge density $\rho(E_D)$ may thus be written

$$\rho(E_D)\approx q[p(E_D)-n(E_D)]=q(K_D/3)(E_D-E_F)^3. \quad (8)$$

By defining the electrostatic potential $\varphi(\mathbf{r})$ in the 3D Dirac semimetal as $q\varphi(\mathbf{r})=-(E_D(\mathbf{r})-E_{F,S})$, the 1D Poisson equation in the Dirac source reads (see top-left inset in Fig. 3(a))

$$\frac{\partial^2\varphi(y)}{\partial y^2}=-\frac{\rho(\varphi)}{\varepsilon_{3D}}=\frac{q^4 K_D}{3\varepsilon_{3D}}\varphi^3(y) \quad (9)$$

where y is the vertical direction, and ε_{3D} is the dielectric constant of the 3D Dirac semimetal. The electrostatic doping of the 3D Dirac source was studied by solving numerically

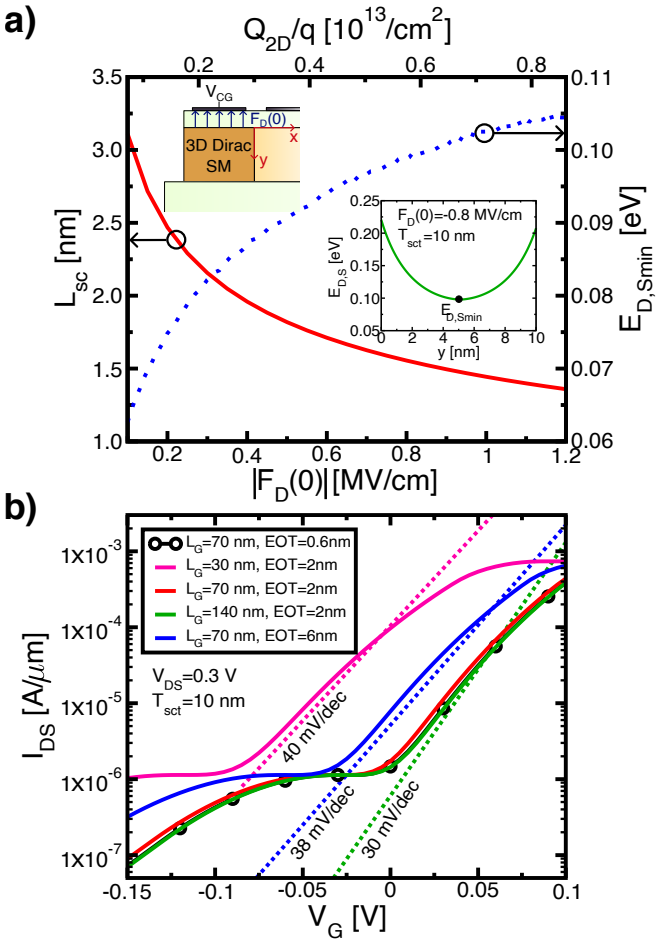

Fig. 3. **(a)** Minimum of the Dirac energy $E_{D,Smin}$ (blue dotted line, right y-axis) versus the field $F_D(0)$ at interface of the 3D Dirac metal (i.e. at y=0, see Fig. 1(c)) for a 10 nm thick layer of the 3D Dirac semimetal. The source Fermi level is $E_{F,S}$=0. Corresponding screening length calculated using Eq. (10) (red line, left y-axis). The top x-axis shows the charge per unit area, Q_{2D}, which is proportional to $F_D(0)$. The inset shows the $E_{D,S}$ profile along the layer thickness for $F_D(0)=-0.8$ MV/cm. **(b)** Current I_{DS} as a function of the gate voltage V_G for the DS-FET sketched in Fig. 1(c) with a 3D Dirac source. $\varepsilon_{OX}=3.9\varepsilon_0$, $\varepsilon_{sct}=15.15\varepsilon_0$, EOT, $T_{sct}=10$ nm are the dielectric constants and thickness of the oxide and semiconductor, $m_c=0.5m_0$, $\chi_{sct}=4.75$ eV are the semiconductor effective mass and affinity, and $\phi_M=4.85$ eV is the gate workfunction. The natural transistor length λ was calculated from the expression for ultra-thin body FETs in [14] ($\lambda=4.9$ nm for $EOT=0.6$ nm, $\lambda=7.17$ nm for $EOT=2$ nm and $\lambda=11.4$ nm for $EOT=6$ nm). The workfunction and dielectric constant of the 3D Dirac metal are $\Phi_{3D}=4.45$ eV and $\varepsilon_{3D}=13\varepsilon_0$ [15], and the Fermi velocity $v_F=2.6\times10^5$ m/s is representative of CoSi [16].

Eq.9, and Fig. 3(a) reports the charge density Q_{2D} versus the interface field $|F_D(0)|$.

As for the 2D electrostatics of the DS-FET, we recall that we are interested to the subthreshold operation, where the carrier density in the channel region is negligible. Therefore, for the semiconductor channel region of the DS-FET we used a model based on the natural transistor length λ [10], [17], [18], [19]. For the continuity conditions of the potential φ at the channel-drain boundary, we used the relations previously developed for ultra-thin body FETs [10], [20]. At the channel-source side, instead, we need a linear formulation of the Poisson equation along x. To this purpose, we linearized the dependence on φ of the charge density in Eq. (8) and introduced the screening length

$$L_{sc}^2 = \varepsilon_{3D}/\sqrt[3]{36q^4K_D(Q_{2D}/T_{sct})^2}. \quad (10)$$

The relation between L_{sc} and $|F_D(0)|$ or Q_{2D} in the source is displayed by the red line in Fig. 3(a) (left y-axis). The approximate expression $\varphi(x) \approx \varphi(0)e^{x/L_{sc}}$ was then used in the Dirac source (i.e. for x<0) to write the φ continuity condition at the channel-source boundary in x=0.

Once the band profile is known, I_{DS} can be calculated from Eq. (1) and by using the $M_{3D}(E)$ in Eq. (3)(b). Fig. 3(b) reports the I_{DS} versus V_G for a 3D Dirac source FET, where I_{DS} was obtained from Eq. (1) using the $E_{C,T}$ identified by the conduction band profile in channel region. The transmission is taken as $T(E)$=1 for energies $E>E_{C,T}$. The I_{DS} versus V_G curves are displayed for different channel lengths, L_G, at a fixed EOT=2 nm, and then for EOT=0.6, 2 and 6 nm at a fixed L_G; λ is either 4.9 nm, 7.17 nm or 11.4 nm respectively for EOT=0.6, 2 and 6 nm. As it can be seen, the trends observed at either fixed L_G or fixed EOT are qualitatively similar, namely the SS degrades when the natural length λ of the FET is not long enough compared to the gate length L_G.

IV. Discussion and Conclusions

This work focused on the theoretical limits for SS in DS-FETs which, however, may be difficult to approach in actual devices. Phonon induced re-thermalization is a challenge [7], [8], that may be mitigated in graphene because room temperature mean free path values of about 150-200 nm have been reported for graphene on common substrates (SiO2, SiC) [21]. This aspect is expected to be more problematic in 3D Dirac semimetals. Another issue with 3D Dirac materials is the presence of non-Dirac energy branches close to E_F [16].

The results from measured graphene DS-FET support fairly well our analysis for the minimum SS [3], [5]. In this respect, we also argue that the best experimentally reported SS values may be influenced by a possible, even unintentional bandgap opening in the graphene source. In fact, even a small bandgap in the graphene source can result in a sizeable SS improvement [6], [22]. Indeed, a bandgap opening of a few tens of meV has been experimentally reported in graphene/hBN [23], [24], as well as in graphene/SiC heterostructures [25].

While SS values close to the theoretical minimum have been experimentally reported in graphene-based DS-FETs [3], [5], DS-FETs based on 3D Dirac semimetals have not yet been demonstrated. One last remark about DS-FETs based on a 3D Dirac semimetal concerns the influence of an aggressive scaling of T_{sct} (see Fig. 1(c)). In fact, a size-induced quantization of the transverse electron wave-vector k_y in the semiconductor can affect the k_y of the electrons that can be effectively injected from the 3D Dirac source into the channel, namely it can alter the number of modes compared to the $M_{3D}(E)$ in Eq. (3)(b). While a quantitative assessment of this effect goes well beyond the scope of this work, a preliminary analysis suggests that the minimum SS is not significantly influenced for a T_{sct} down to about 10 nm, as in Fig. 3.

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