Compact expression to model the effects of dielectric absorption on analog-to-digital converters

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Abstract: An analytical model for the dielectric absorption on capacitors and its impact on the errors induced in ADC conversion is here proposed. The reported simulations are consistent with the results of the R-C model widely used in the literature and demonstrate that a large set of experiments can be fitted just calibrating a single model parameter.

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Introduction. The literature widely reports that the dielectric constant of insulators depends on frequency and it has a complex value [1]. While its real part is responsible for the capacitance of metal-insulator-metal (or semiconductor-insulator-metal) capacitors, the imaginary part results in an AC conductance in parallel to the capacitance. This effect is known as *dielectric absorption* or *dielectric relaxation* [1]. In the time domain, the effect manifests itself as a slow current transient going roughly as $1/t$ (inverse of the time) after application of a voltage step, that adds to the Dirac-delta current associated to the charging/discharging of a capacitor after a voltage step [2]. This long transient has a negative impact on the performance of analog-to-digital converters (ADCs) [3, 4, 5] since, during the hold phase, this current partially discharges/charges the sampling capacitors, lowering/increasing the voltage to be converted with respect to the voltage applied during the sampling phase.

Modeling framework. We model the frequency dependence of the dielectric constant by using Eq.1, that is essentially the model proposed in [6] for FR-4 substrates, just recast to display explicitly $\tan\delta$, that is the tangent of the loss-angle in the angular frequency interval between ω_1 and ω_2. Then, the complex capacitance C can be easily expressed by Eq.2. From the capacitance versus frequency equation, it is also possible to derive the current versus time relationship (see Eq.3), which indeed results in a $1/t$ trend of the current. Fig.2 shows that the model is able to reproduce well experimental results for integrated capacitors in terms of both capacitance and conductance versus frequency f [7]. Furthermore, in Fig.3, our model reproduces well both the current versus t experiments and the capacitance versus f data for MIM capacitors featuring different dielectrics reported in [4, 5] by using $\tan\delta$ values in the order of 10^{-3}.

Therefore, in this work we propose the use of Eq.2 to model the dielectric absorption, as an alternative to the widely used R-C model [5, 8] employing many R-C dipoles in parallel to the main capacitor (Fig.4, left). Although phenomenological, the R-C model is however helpful to understand the effect of dielectric absorption on the ADC performance. In Fig.4 (right), we see that during the sampling phase the capacitor C (completely discharged in the idle phase) is set to a voltage V. This is not the case for C_1 and C_2 that slowly charge. During the hold phase, the current flowing in the R-C branches discharges the capacitor C, lowering the voltage. When the conversion phase begins, the reduction of the stored voltage with respect to V is given by Eq.4 when considering a single R-C branch (with constant $\tau_1 = R_1C_1$ and where the capacitor C_1 is α times the value of the main capacitance C; Fig.4, left plot). Each additional i-th branch would add its own ΔV_i following Eq.4.

It can be demonstrated that, when considering that a voltage step of amplitude V is applied to the capacitor, the Fourier anti-transform of Eq.2 gives Eq.5. This approach avoids defining a set of R-C branches and sum up their contributions as from Eq.4 to obtain the total voltage loss ΔV in the capacitor.

Simulations and experiments. In this section, we first compare the predictions of Eq.5 with those of the R-C model of Eq.4. In the latter case, different R-C branches are considered, assuming τ_i values extending over different number of time decades and different numbers of τ_i per single decade (τ/dec). All R-C pairs share the same α value, which is related to the capacitance decrease per time decade. Comparing Eqs.4 and 5, it can understood that α and $\tan\delta$ of the capacitor are linked together [5]. In particular, Eq.6 is obtained if only one τ_i value is present in each single time decade (1 τ/dec). Otherwise the α value in Eq.6 must be divided by the assumed number of τ/dec.

Fig.5 shows that the R-C model perfectly matches Eq.5 if 15 time decades are considered, with 10 τ_i values per each decade. Otherwise, small differences arise. This is consistent with the assumption that Eq.4 is the R-C model when considering an infinite number of τ_i. The figure also reports experimental data for a sample and hold (S/H) circuit connected to an ADC. This system is meant to measure the actual voltage stored in the capacitor after sampling for a time t_s and holding the data for a time t_h. The system allows to configure both t_s and t_h. Fig.5 shows the good agreement between experiments and the two models when using $\tan\delta = 1.2 \cdot 10^{-3}$ and an α value consistent with Eq.6.

Fig.6 extensively compares the predictions of Eq.5 against experiments when varying the sample and hold times, showing that a model with very few parameters (in practice only $\tan\delta$ significantly affects the results) can nicely reproduce all the experiments. Best fit of the whole set of experiments provides $\tan\delta = 1.28 \cdot 10^{-3}$, which is in good agreement with the $\tan\delta$ values extracted through fitting of experiments available in the literature [4, 5] (Fig.3), although the $\tan\delta$ depends on both the technology and layout used for the capacitor.

The effects of dielectric absorption propagates also to the future sampling instants. Assuming that the ADC samples again the same V, it can be easily demonstrated that the error on the n-th sample for the model of Eq.2 is given by Eq.7. Fig.7 compares Eq.7 with circuit simulations using the R-C model. At present time experimental data are available only for the first sample and this latter is reported in figure as a reference. The simple Eq.7 nicely reproduces the predictions of more complex simulations with the discrete R-C model, demonstrating the usefulness of the proposed model.

Conclusion. We developed a model to predict the errors induced by the dielectric absorption to the ADC conversion of a sampled voltage. The proposed equations are able to reproduce experiments through the calibration of just a single parameter, namely $\tan\delta$. Although much simpler than the widely used R-C model, the analytical equations are also able to easily predict the errors induced on subsequent sampling. Finally, the model can be easily extended also to predict the impact of dielectric absorption on other electronic applications.

[1] Kwan Chi Kao, Electric Polarization and Relaxation. *Dielectric Phenomena in Solids*, Academic Press, 2004, p. 41114.

[2] H. Reisinger et al., "A comparative study of dielectric relaxation losses in alternative dielectrics", *International Electron Devices Meeting Technical Digest*, pp. 12.2.1-12.2.4, 2001.

[3] M. Kropfitsch, P. Riess, G. Knoblinger and D. Draxelmayr, "Dielectric absorption of low-k materials: extraction, modelling and influence on SAR ADCs", *IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 4, 2006.

[4] T. Matsui, K. Sento, T. Ebata and A. Ishibashi, "A Capacitor Dielectric Relaxation Effect Cancellation Circuit in a 12-Bit, 1-MSps, 5.0-V SAR ADC on a 28-nm Embedded Flash Memory Microcontroller", *Proc. of IEEE 45th European Solid State Circuits Conference (ESSCIRC)*, pp. 95-98, 2019.

[5] K.-H. Allers, P. Brenner, M. Schrenk, "Dielectric reliability and material properties of Al2O3 in metal insulator metal capacitors (MIMCAP) for RF bipolar technologies in comparison to SiO_2, SiN and Ta_2O_5." *IEEE BCTM*, vol. 3, pp. 35-38, 2003.

[6] Djordjevic, A. R. and Biljie, R. M. and Likar-Smiljanic, V. D. and Sarkar, T. K., "Wideband frequency-domain characterization of FR-4 and time-domain causality", *IEEE Trans. on Electromagnetic Compatibility*, vol. 43, n. 4, pp. 662-667, 2001.

[7] Peng Zhao et al., "Evaluation of border traps and interface traps in HfO2/MoS2 gate stacks by capacitancevoltage analysis", *2D Materials*, vol. 5, p. 031002, 2018.

[8] K. Kundert, "Modeling Dielectric Absorption in Capacitors", *The designer's guide community*, vol. 18, pp. 1-19, 2008.

$$\epsilon(\omega) = \epsilon_\infty \left[1 + \tan\delta \frac{2}{\pi} \ln\left(\frac{\omega_2 + j\omega}{\omega_1 + j\omega}\right)\right] \quad (1)$$

$$C(\omega) = \frac{\epsilon(\omega)}{d} = C_\infty \left[1 + \tan\delta \frac{2}{\pi} \ln\left(\frac{\omega_2 + j\omega}{\omega_1 + j\omega}\right)\right] \quad (2)$$

$$\frac{I(t)}{P} \approx \frac{I(t)}{C_\infty V_{IN}} = \frac{2\tan\delta}{\pi} \cdot \frac{1}{t} \quad (3)$$

$$\Delta V_i = \alpha V \left(e^{-\frac{t_s}{\tau_i}} - e^{-\frac{t_s+t_h}{\tau_i}}\right) \quad (4)$$

$$\Delta V = \frac{2V\tan\delta}{\pi} \ln\left(\frac{t_s + t_h}{t_s}\right) \quad (5)$$

$$\alpha = \frac{2\ln(10)\tan\delta}{\pi} \quad (6)$$

$$\Delta V^{(n)} = \frac{2V\tan\delta}{\pi} \ln\left(\frac{n(t_s+t_h)}{(n-1)(t_s+t_h)+t_s}\right) \quad (7)$$

Figure 1: Equations of the dielectric absorption models. ϵ is the dielectric constant of the insulator, ϵ_∞ is the dielectric constant at infinite frequency, d is the insulator thickness, C_∞ is the capacitance at infinite frequency, $\tan\delta$ is the loss tangent/dissipation factor of the capacitor, α is the relative capacitance decrease per frequency decade, $\tau_i = R_i C_i$ is the time constant of the i-th R-C branch in Fig.4(left), t_s and t_h are the sampling and hold times of the S/H system, respectively. ΔV_i is the voltage decrease due to the sole i-th R-C branch in Fig.4(left), ΔV is the total voltage loss after the first hold phase. $\Delta V^{(n)}$ is the voltage reduction after the n-th sample-and-hold phases of the same V value.

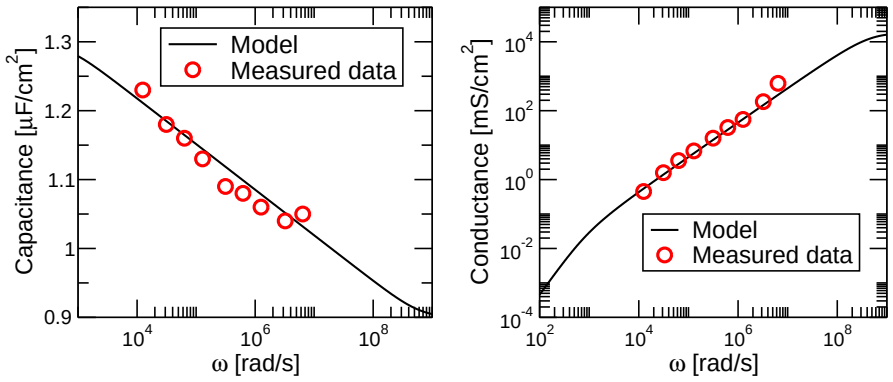

Figure 2: Comparison between the capacitance (left) and the conductance (right) calculated with Eq. 2 and the experiments in [7]. The model parameter values used to fit the measurements are $C_\infty = 0.9\ \mu\text{F/cm}^2$, $f_1 = \frac{\omega_1}{2\pi} = 100$ Hz, $f_2 = \frac{\omega_2}{2\pi} = 100$ MHz and $\tan\delta = 0.0502$.

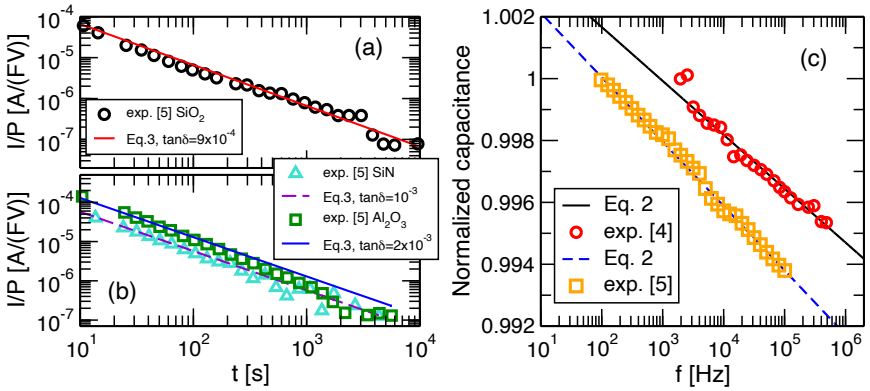

Figure 3: Comparison between our model and the experiments in [4, 5]. (a), (b) Eq. 3 is used to fit the current vs. time experiments in [5]. In this case the sole model parameter is $\tan\delta$. (c) Comparison of Eq.2 with the C vs. f curves measured in [4, 5]. Experiments are provided normalized to the capacitance measured at the lowest measurement frequency [4, 5]. In Eq.2, we used $f_1 = \frac{\omega_1}{2\pi} = 10$ mHz and $f_2 = \frac{\omega_2}{2\pi} = 500$ MHz. For the black solid line we used $\tan\delta = 1.2 \cdot 10^{-3}$, while for the dashed blue line we used $\tan\delta = 1.44 \cdot 10^{-3}$.

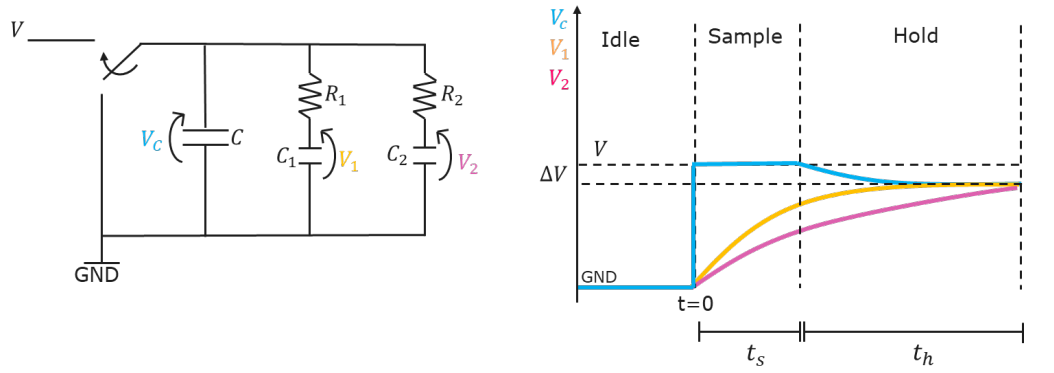

Figure 4: Left: sketch of the sample-and-hold circuit in which the dielectric absorption is modeled through discrete R-C circuits. The switch can assume three different positions: in the idle phase, C is connected to ground resulting in its complete discharge; in the sample phase, the voltage V charges C during the sample time (t_s); in the hold phase the switch disconnects C from the input and the measurement of the stored voltage occurs after the hold time (t_h). The hold time includes also the time required for data conversion (that is however much shorter). Right: time evolution of the voltages across the capacitors. The charge stored in C during t_h redistributes on C_1 and C_2 during t_h, decreasing the voltage V_C on the main capacitor. $\Delta V = V - V_C$ after t_h (see also Eq.4 in Fig.1).

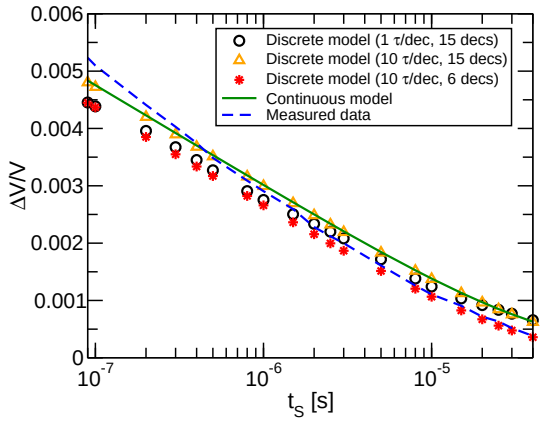

Figure 5: Normalized voltage error (V=5 V) vs. the sample time measured after $t_h = 51.6\mu$s. We fit the experiment with different models: the green solid line is Eq.5 with $\tan\delta = 1.2 \cdot 10^{-3}$; symbols are simulations with the R-C model assuming different number of branches (see Fig.4), i.e. different number of $\tau_i = R_i \cdot C_i$ distributed over different number of time decades. For 1 τ/dec, $\alpha = 1.76 \cdot 10^{-3}$, consistently with Eq.6; for 10 τ/dec, $\alpha = 1.76 \cdot 10^{-4}$. Increasing the number of τ_i, the R-C model tends to Eq.5. The coverage of more t_s decades improves the matching between the models. This is consistent with the hypothesis that Eq.5 is the R-C model in the case of $i = \infty$, with τ_i distributed over the whole time range.

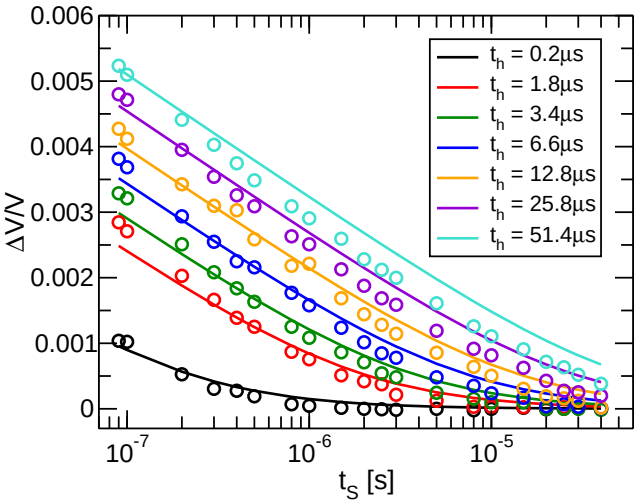

Figure 6: Comparison between experimental data measured for different hold times (symbols) and Eq.5 (lines). The fitting procedure provides $\tan\delta = 1.28 \cdot 10^{-3}$ which best fits the experiments. Eq.5 seems to precisely predict the normalized voltage error for all t_s and t_h.

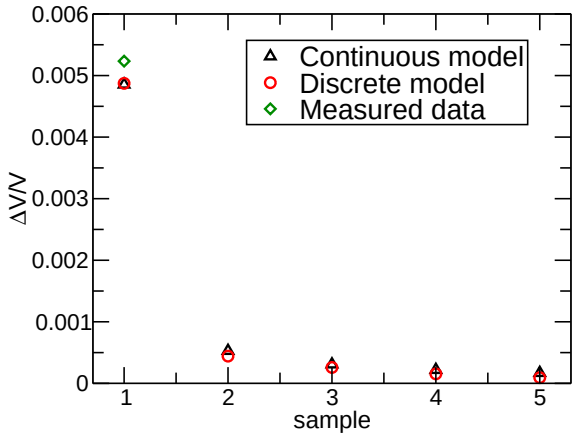

Figure 7: Normalized voltage error predicted by Eq.7 with $\tan\delta = 0.0012$ (black) and the R-C model (red) for successive samples of the same input data $V = 5$ V when using $t_s = 0.1$ μs and $t_h = 51.2$ μs. For the R-C model we used $\alpha = 1.8 \cdot 10^{-3}$ and $\tau_1 = 0.1$ μs, $\tau_2 = 1$ μs, $\tau_3 = 10\mu$s and $\tau_4 = 100\mu$s (1 τ/dec). The measurement after the first sample (green) is reported in figure as a reference.