A Novel Ferroelectric MemCapacitor Enabling Multilevel Operation

A Novel Ferroelectric MemCapacitor Enabling Multi-Level Operation

Daniel Lizzit, *Member, IEEE*, Mattia Segatto, David Esseni, *Fellow, IEEE*

Abstract

The progress of biologically inspired neuromorphic computing hardware in the last decade has been fostered also by the advancement in CMOS compatible memristors, providing a non-volatile storage of multi-conductance states mimicking the synaptic weights in biological systems. This paper is instead focused on the less-explored field of memcapacitors, that only very recently has attracted a renewed interest, and it is based on devices capable of tuning their capacitance. In particular, we present by means of extensive numerical simulations carefully calibrated against experimental data, the operation of a two-terminal ferroelectric memcapacitor exhibiting multi-level, polarization–dependent capacitance values. The memcapacitor exploits a ferroelectric Gated-Diode structure and it is thus fully compatible with CMOS processing. Our results show that multi-level operation is viable by using properly shaped pulse trains at the gate terminal and that, moreover, a non-destructive readout can be achieved by means of small-amplitude AC signals.

Index Terms

Ferroelectricity, neuromorphic, non-volatile, memcapacitor.

I. Introduction

Neuromorphic engineering is a new and actively evolving field aiming at the design of energy-efficient hardware for information processing [1]. Neuromorphic systems have been shown to be capable of sophisticated tasks such as tracking and motion detection [2], [3], touch sensors [4], and real-world sensory-processing [5]. The fundamental components of neuromorphic hardware are artificial synapses and neurons, and synapses largely outnumber neurons in artificial as well as in biological systems [6], [7].

Many implementations of artificial synapses have been proposed ranging from CMOS sub-threshold circuits [8], [9], to diverse kinds of memristors based on phase-change materials, conductive filaments in a resistive layer, magnetic and ferroelectric tunnel junctions, and ferroelectric field effect transistors. [10]–[14]. A tunable capacitor, or memcapacitor (MemCap), can be an alternative or complementary option to memristors [15]. The information is stored in the device capacitance rather than in its conductance, which can relieve some of the limitations inherent to memristors.

The read-out of MemCaps is performed by applying transient small–signals superimposed to a small or even zero DC bias, and the resulting currents are not inherently dissipative [16], [17]. Hence, the electric field in the ferroelectric during the read-out can be kept much smaller than the coercive field, thus alleviating read disturbs. Furthermore, the very large DC impedance not only improves the energy efficiency during read-out, but also helps reduce the hazards related to sneak-path currents compared to memristive crossbar array [18]. Device concepts so far proposed for MemCaps include a superlattice consisting of metal layers embedded into a parallel-plate capacitor [19], variable plate distance capacitors in micro-electromechanical systems [20], metal-oxide junctions exploiting changes in the oxygen vacancies [21], devices exploiting the shielding layer effect in a gated diode structure [22], and Flash memories [23]. Only recently a few ferroelectric–based solutions for MemCaps have been reported [22]–[29], that are naturally suitable for CMOS integration.

Ferroelectric MemCaps featuring the MFSM (Metal-Ferroelectric-Semiconductor-Metal) structure illustrated in Fig. 1b were proposed in [24], whereby the ferroelectric runs across a p^- type and an n^+ region. This device leverages the formation of

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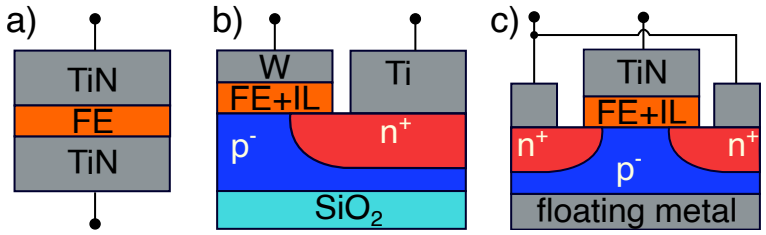

Fig. 1. CMOS compatible MemCap device concepts based on: a) an MFM capacitor [25]; b) an MFSM structure [24]; c) a GlobalFoundries' 28nm FeFET [26], [30].

an electron inversion layer for the high capacitance state, $C_{\rm HS}$, and the depletion capacitance of the p-type region for the low capacitance state, $C_{\rm LS}$. Authors reported a $C_{\rm HS}/C_{\rm LS}$ ratio reaching $\sim$125 (much larger than the $<$2 value achieved in the MFM structures of Fig. 1a [25]), as well as a multi-level operation [24]. The read-out is obtained by applying a low voltage square wave pulse to the MFSM connected to a charge transfer circuit [24]. In the MFSM device, however, while the n^+ region is a fast supply for electrons, holes are seemingly provided by band-to-band tunneling (BTBT) and/or trap-assisted tunneling (TAT). This implies large voltages ($>$6 V) for polarization switching [24], and possible limitations in the operation speed.

It has been also reported that FeFETs realized in a Global-Foundries 28nm technology can be effectively operated as two terminal MemCaps (Fig. 1c) [26], [30], where the read-out capacitance is measured between the metal gate and the shorted source-drain terminals. A $C_{\rm HS}/C_{\rm LS}$ of about 25 could be obtained for a gate length $L_{\rm G}$ =560 nm from the hysteretic C-V curves with a quasi-static sweep of the DC bias from $-$3.5 V to +3.5 V. Because $C_{\rm LS}$ is due to the overlap capacitance between the gate and the source-drain regions, however, the $C_{\rm HS}/C_{\rm LS}$ ratio tends to degrade by scaling $L_{\rm G}$, and authors reported simulations showing that $C_{\rm HS}/C_{\rm LS}$ drops to about 3.3 for the minimum simulated length $L_{\rm G}$ =100 nm [26]. In such MemCaps based on FeFETs a fairly low programming/erasing voltage of $\pm$3.5 V is used, and a 4–level operation has been reported by using potentiation write pulses with different amplitudes of 2.75, 3.0 and 3.5 V [31].

In the MemCaps proposed in [24], [26], $C_{\rm HS}$ is the gate capacitance in strong inversion and $C_{\rm LS}$ is the capacitance when the p^- region is not inverted, which is dominated by parasitic contributions. Hence, in order to accommodate intermediate capacitance states, it is required to exploit the capacitance transition at the onset of strong inversion which is typically steep, non–linear and difficult to engineer.

In this paper, we propose and design by means of numerical simulations a ferroelectric MemCap based on a silicon-on-insulator gated-diode (see Figure 2b), whose operation does not rely on BTBT or TAT mechanisms. In our device, $C_{\rm HS}$ and $C_{\rm LS}$ are respectively the capacitance in the accumulation and in the depletion region. Moreover, we propose a doping profile of the p-type channel region resulting in a good linearity in the transition between $C_{\rm HS}$ and $C_{\rm LS}$, which eases the multi-level operation obtained by using appropriate potentiation and depression write pulses. The paper is organized as follows. In Section II we describe the architecture of the proposed MemCap. In Section III we discuss the TCAD model for the ferroelectric material, and the calibration with experiments of the intrinsic ferroelectric dynamics. In Section IV trapping/detrapping mechanisms in the MFS stack are investigated through a comparison with experimental data. This is particularly important to set the time scale for the programming $V_{\rm G}$ pulses, which are then used in Section V for the design of the MemCap. In Section VI we finally offer a few concluding remarks.

II. Memcapacitor concept and operation

The MemCap here proposed provides a polarization–dependent capacitance by exploiting the semiconductor depleted region, as sketched in Fig. 2a. Figure 2b shows that the device architecture is similar to a 28 nm technology node FeFET [32], except for the use of short-circuited $n+$ and a $p+$ pockets. Such pockets can provide a fast and effective carrier supply for both gate voltage polarities [22], so that our device does not rely on BTBT or TAT mechanisms for the generation of carriers to support the ferroelectric polarization switching [26], [33]. Moreover, low-κ air–gap spacers and shallow-trench-isolation (STI) structures are used to suppress the parasitic capacitance between the gate electrode and the $n+$ and $p+$ regions. This can effectively reduce $C_{\rm LS}$ and improve the dynamic range of the MemCap (see also Section V). Air-gap shallow trench isolations (STI) structures have been previously reported in both experimental and simulations works [34], [35], demonstrating their effectiveness in reducing the fringing capacitances.

This device allows us to program the capacitance in a non-volatile fashion by using gate voltage pulses. Moreover, the read-out of the capacitance can be achieved by means of a small-amplitude AC-signal, possibly leveraging charge recovery schemes to further improve the energy efficiency [22], [36]–[38].

III. Modeling and calibration of the intrinsic ferroelectric properties

The ability to gradually modulate the polarization state of the ferroelectric layer by applying a train of $V_{\rm G}$ pulses is key to modulate the resistance and capacitance in ferroelectric memristors and memcapacitors. Thus, a calibration of the intrinsic ferroelectric switching dynamics is crucial.

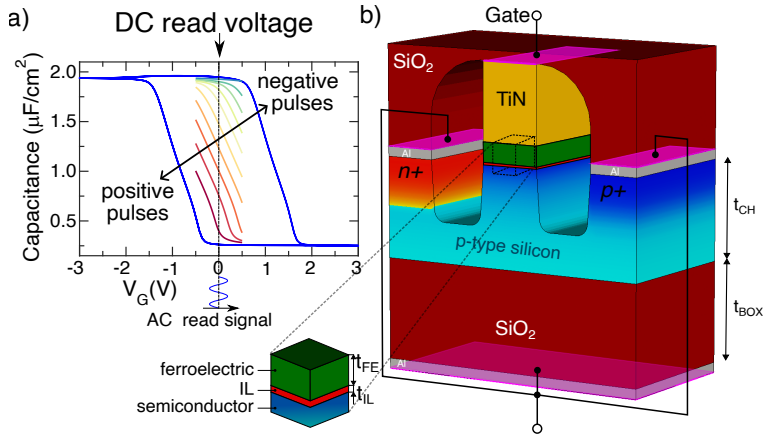

Fig. 2. a) Sketch of the working principle of the proposed MemCap, whereby gate voltage pulses modulate the depletion capacitance. b) Device structure used for the simulations of the ferroelectric MemCap. The ferroelectric oxide is a 10 nm thick HZO. The interfacial SiO_2 layer (IL) has a thickness t_{IL} =1 nm. $n+$ and $p+$ contacts are doped with a density of 1×10^{20} cm^{-3}, whereas the channel is p-type, and has a thickness t_{CH} = 50 nm. The SiO_2 back oxide has a thickness t_{BOX} = 50 nm. The channel length is L_G =30 nm and a non uniform p–type doping is considered. Air-gaps are used to suppress fringing capacitances.

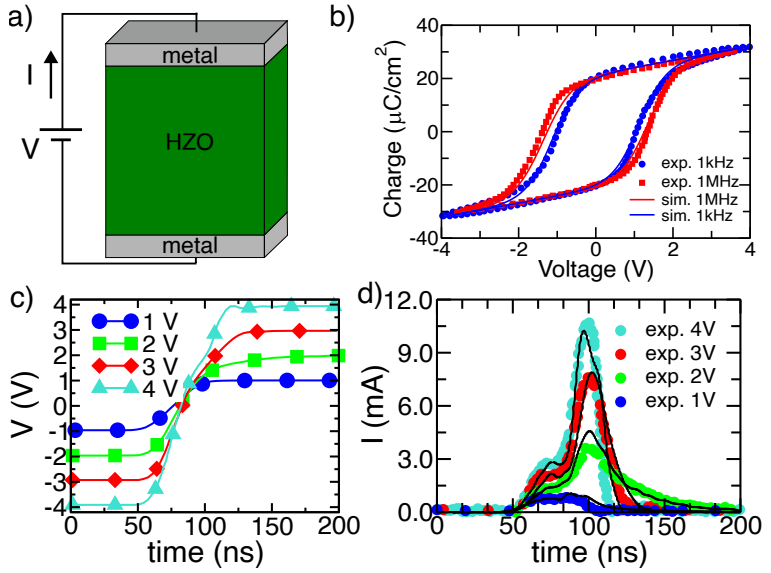

Fig. 3. a) Sketch of the 10-nm MFM HZO capacitor used for the calibration of the Preisach model parameters. b) Charge versus applied voltage obtained with large-signal triangular waveforms at low (blue) and high (red) frequency. d) Comparison between the simulated (solid line) and experimental results (circles) [41], for the current transients obtained by applying the voltage waveforms shown in (c).

The ferroelectric behavior is here described via the Preisach model and using the Synopsys TCAD Sentaurus [39]. Unlike the Landau-Ginzburg formalism, where the hysteresis loop of a single domain is abrupt close to the coercive field E_C [40], in the Preisach model the derivatives of the polarization over the electric field are always continuous functions, which makes the calculation of the differential capacitances numerically stable. The material parameters of the ferroelectric HZO were obtained by fitting the simulation data to the experimental results obtained for a metal-ferroelectric-metal capacitor featuring the same thickness t_{FE} =10 nm [41]. The dynamics of the ferroelectric polarization switching is based on differential equations that use relaxation times for both polarization (τ_P) and electric field (τ_E) variations in the ferroelectric oxide [39], [42]. The model parameters used in this work are reported in Table I. Figure 3 shows that, upon appropriate calibration of the parameters, the agreement between simulations (lines) and experiments (symbols) is very good in quasi–static regime, at high frequency (triangular waveform with f=1 kHz and 1 MHz, see Fig. 3b), and even in a fast transient operation (see Fig. 3d). From experimental results on MFM structures [41], we extracted τ_P =30 ns, that is smaller than in other simulation studies (τ_P =250 ns [43]). This could be due to the different thermal annealing conditions [44]–[46], and different measurement setups, considering the crucial role of circuit and sample parasitics in the dynamic device characterization [41].

TABLE I
PREISACH MODEL PARAMETERS USED FOR THE 10 nm HZO.

parameter	description	value
P_{R}	remanent polarization	19.4 μC/cm^2
P_{S}	saturation polarization	20.6 μC/cm^2
E_{C}	coercive field	1.16 MV/cm
τ_{E}	E-field relaxation time	3.75 ns
τ_{E}	polarization relaxation time	30 ns
k_{n}	non-linearity parameter	12
$\varepsilon_{\mathrm{FE}}$	background dielectric constant	35

IV. MODELING AND CALIBRATION OF THE TRAPPING DYNAMICS IN HZO-SiO$_2$

Several experimental and simulation studies of silicon based FeFETs have shown that the HZO-SiO$_2$ oxide stack features a large density of traps with values of $\sim 10^{14}$ cm^{-2}, thus leading to a trapped charge comparable to the polarization charge [47]–[50]. Trapped charges stabilize the HZO polarization charge, and also set the time constants of the polarization response to external V_{G} stimuli [33], [51]–[55], therefore a proper calibration is needed for realistic MemCap simulations. To this end, a thorough calibration of the interfacial trap density in an n-FeFET device shown in Fig. 4a is performed, to reproduce experimental charge *versus* V_{G} curves obtained with a Positive-Up-Negative-Down (PUND) measurement. PUND simulations are performed by applying triangular waveforms with a duration of 100 μs as shown in the inset of Figure 4c), consistently with the measurement conditions in Ref. [33]. Simulations include donor and acceptor interfacial traps at the IL-ferroelectric oxide

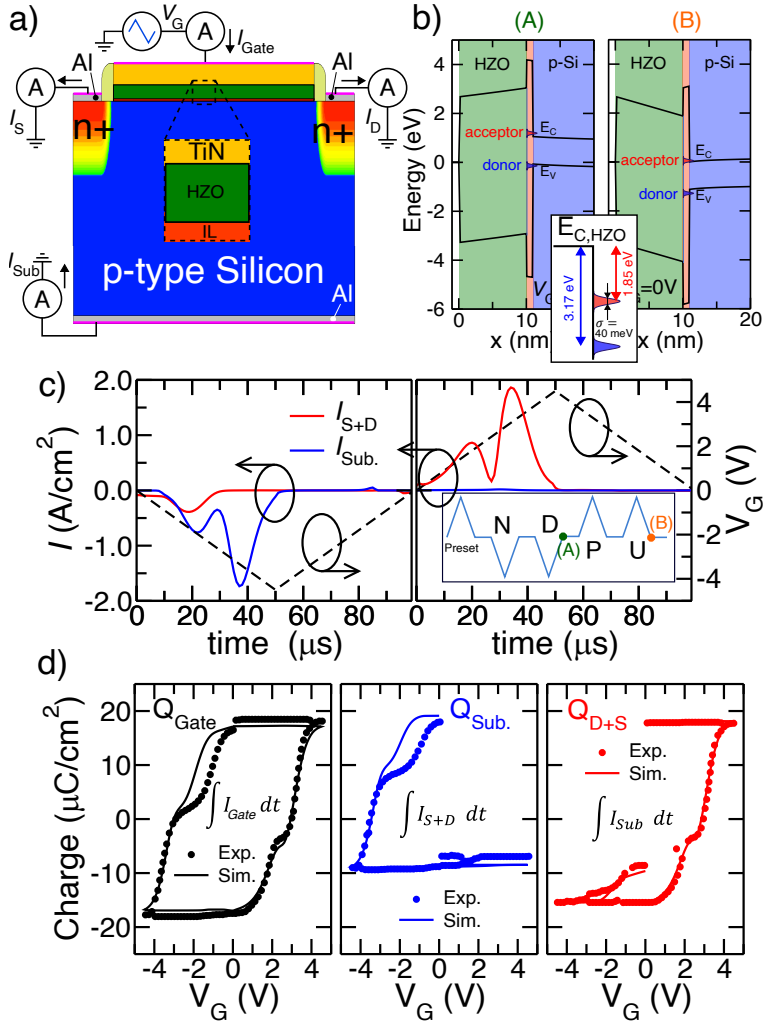

Fig. 4. a) Simulated n-type FeFET, consistent with [33]. b) Band diagrams corresponding to the different states (A) and (B) shown in the inset of c), and acceptor and donor interfacial trap states with Gaussian profile and densities of 2×10^{14} cm^{-2}. c) Simulated transient currents (normalized by the metal gate area) obtained using a split PUND scheme shown in the inset. d) Charges collected at the terminals obtained by integration of the transient currents in c) compared with experimental results [33] .

with a Gaussian energy distribution, and with a density of 2×10^{14} cm^{-2} consistently with Refs. [47], [52], [56]. Such traps

exchange electrons and holes via a non-local tunneling mechanisms across the IL, accounting for both elastic and multi-phonon assisted tunneling [39].

The simulated charges Q_{Gate}, $Q_{\text{Sub.}}$ and $Q_{\text{D+S}}$ at the device terminals shown in Fig. 4d, were calculated by integrating the transient PUND currents of Fig. 4c. More precisely, such charges were obtained by subtracting from the current in the first down (up) pulse the current in the second down (up) pulse. The good agreement with experimental results in Fig. 4d has been achieved by a fine tuning of the energy levels and densities of acceptor and donor interfacial traps (see Fig. 4b), and by using tunnel electron/hole effective mass 0.8 m_0 for the thin IL [57], [58], and a trap volume V_{T} of 10^{-12} μm^3. The extracted energy range for interface traps match the value experimentally measured in Si-doped ferroelectric HfO_2 for the acceptor states [59], are consistent with the findings in Ref. [33], as well as with the values that have been employed in the literature for the Si-HZO stack [49], [60]–[62].

V. Design of the Memcapacitor and Simulations

The simulated device is shown in Fig. 5a, where drift-diffusion and small signal CV simulations accounting for the ferroelectric gate oxide were performed by using the Sentaurus-Device package [39], and with ferroelectric and interface trap simulation parameters calibrated in Sections III and IV. To investigate the effect of the ferroelectric polarization on the capacitance, we performed simulations by superimposing a small signal with an AC frequency of 100 kHz to a quasi-static triangular voltage ramp. Figure 5b shows that the gate to ground capacitance (C_{G}) exhibits a hysteretic behavior, as a result of the polarization hysteresis of the HZO shown in Fig. 5c. Moreover, even though the magnitude of the HZO polarization is almost the same in points (A) and (B) of Fig. 5c, there is no inversion capacitance in point (B) of Fig. 5b. This is due to the high acceptor doping concentration at the IL–Si resulting from the non–uniform doping profile used in the device and displayed in Fig. 5a, which shifts the threshold voltage towards $V_{\text{G}} > 3$ V. Therefore, the polarization modulation shown in Fig. 5b is primarily supported by the trapped charge at the HZO-IL interface, rather than by the semiconductor free carriers. The feasibility of accommodating a large number of capacitance levels in the proposed MemCap depends on the ratio between

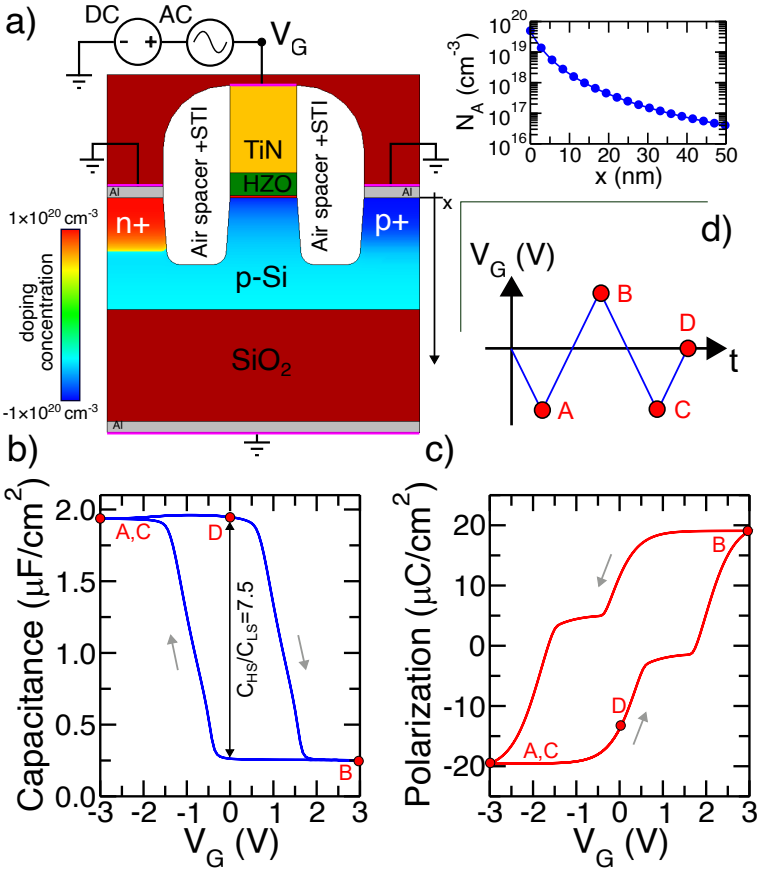

Fig. 5. a) Simulated device structure and channel acceptor doping profile described by Eq. (2) plotted along the vertical direction x; the A parameter has been set to 1 μF/(cm^{2}V). b) Small signal capacitance C_{G} obtained for an f_{AC} =100 kHz and with the quasi–static DC bias shown in (d). The high value of acceptor doping close to the IL-Si interface shifts the threshold voltage to $V_{\text{G}}>3$ V, thus no depletion to inversion transition is observed in the plot. c) Polarization hysteresis versus V_{G}. d) Quasi–static V_G bias used to obtain the C_{G} versus V_{G} curves in b).

the capacitance C_{HS} in the accumulated region and the minimum capacitance C_{LS} in depletion (see Fig. 6), and on the steepness of the transition from C_{HS} to C_{LS}. In our 30 nm–long MemCap, the fringe capacitance between the metal gate and the $n+$ and

$p+$ pockets would give a significant contribution to $C_{\rm LS}$ in the absence of the air-gap STI structures shown in Fig. 5a. This is confirmed in Fig. 6 by comparing the $C_{\rm LS}$ of Dev.B with trenches ($C_{\rm LS}{\simeq}0.25\ \mu F/{\rm cm}^2$) to the $C_{\rm LS}$ of the baseline Dev.A without trenches ($C_{\rm LS}{\simeq}0.7\ \mu F/{\rm cm}^2$). Of course the ratio $C_{\rm HS}/C_{\rm LS}$ may be improved in the Dev.A by increasing the gate to n^+/p^+ underlap, however low–κ trenches are an effective option to improve $C_{\rm HS}/C_{\rm LS}$ in scaled MemCaps.

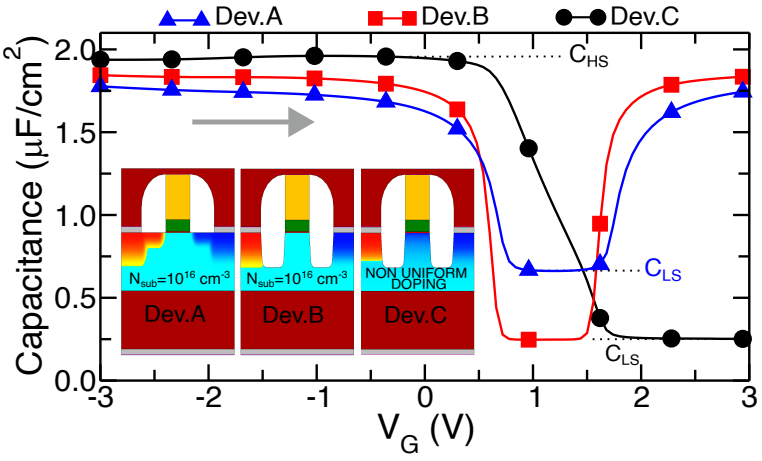

Fig. 6. Small signal capacitance values obtained with a positive quasi–static voltage ramp from -3 to +3 V (see the arrow), for the three different proposed devices shown in the inset. For the sake of clarity the negative ramp from +3 to -3 V is not shown. Dev.C corresponds to the device simulated in Fig. 5.

As for the transition from $C_{\rm HS}$ to $C_{\rm LS}$, we recall that for a uniform doping concentration N_A the overall capacitance $C_{\rm G}$ in the depletion region is a non linear function of $V_{\rm G}$ [63]. In particular, the capacitance $C_{\rm G}$ is given by the series of the oxide capacitance and the depletion capacitance of the semiconductor and it can be written as $C_{\rm G}(W_{\rm d})\ {=}C_{\rm oxe}\ \varepsilon_{\rm Si}/(\varepsilon_{\rm Si}{+}W_{\rm d}\,C_{\rm oxe})$, where W_d denotes the width of the depleted region and $C_{\rm oxe}$ is the effective capacitance of the gate oxide stack. In the following discussion $C_{\rm oxe}$ is assumed to be gate bias independent, namely we neglect the possible $C_{\rm oxe}$ modulation due to the response of the traps at the HZO–IL interface and to changes of the ferroelectric polarization. We also recall that, in the complete depletion approximation, the one-dimensional (1D) Poisson equation can be written as $(d^2\phi/dx^2){=}qN_{\rm A}(x)/\varepsilon_{\rm Si}$, where $\varepsilon_{\rm Si}$ is the silicon dielectric constant and x is the vertical abscissa (see Fig. 2). We show in the Appendix that, by combining $C_{\rm G}(W_{\rm d})$ $=C_{\rm oxe}\ \varepsilon_{\rm Si}/(\varepsilon_{\rm Si}{+}W_{\rm d}\,C_{\rm oxe})$ with the Poisson equation, the derivative of $C_{\rm G}$ with respect to $V_{\rm G}$ can be written as

$$\frac{dC_{\rm G}}{dV_{\rm G}} = \frac{dC_{\rm G}}{dW_d}\,\frac{dW_d}{dV_{\rm G}} = -\frac{{\varepsilon_{\rm Si}}^2 {C_{\rm oxe}}^3}{qN_A(W_d)\,(\varepsilon_{\rm Si}+W_d\,C_{\rm oxe})^3} \tag{1}$$

where $N_A(W_d)$ is the doping concentration at $x{=}W_d$, which depends on W_d for a non–uniform $N_{\rm A}(x)$ profile. We now recall that W_d depends on $V_{\rm G}$, hence Eq. (1) reiterates that, for a uniform N_A profile, $C_{\rm G}$ is a non linear function of $V_{\rm G}$ (see Dev.A, Dev.B in Fig. 6). Quite interestingly, Eq. (1) also suggests that a non–uniform $N_{\rm A}(x)$ can produce a $(dC_{\rm G}/dV_{\rm G})$ independent of $V_{\rm G}$, namely a fairly linear $C_{\rm G}$ versus $V_{\rm G}$ relation. More precisely, if we wish to have $(dC_{\rm G}/dV_{\rm G}){=}{-}A$ (with $A{>}0$), Eq. (1) returns

$$N_{\rm A}(x) = \frac{{\varepsilon_{\rm Si}}^2 {C_{\rm oxe}}^3}{q\,A\,(\varepsilon_{\rm Si}+x\,C_{\rm oxe})^3} \tag{2}$$

Figure 6 shows that, by using the $N_{\rm A}(x)$ profile given by Eq. (2) with A=1.0 μF/(cm^{2}V), the $C_{\rm G}$ ($V_{\rm G}$) in the depletion region of Dev.C is substantially more gradual and linear than for Dev.A and Dev.B.

In this paper, we investigate write schemes based either on constant or incremental voltage pulses. Regardless of the biasing scheme, the write pulses vary the ferroelectric polarization and consequently $C_{\rm G}$ through a change of the channel depletion width.

The two biasing schemes used in this work consists of a preset, a write and a read operation as shown in Fig. 7. After applying a preset pulse to the gate to set the ferroelectric oxide into a given polarization state, a series of gate voltage pulses are applied. Finally, the readout consists in applying to the gate a small AC signal superimposed to a DC voltage. In this work, a zero readout DC voltage is used. This is possible thanks to the hysteresis loop of the capacitance shown in Fig. 5c, that has been centered around $V_{\rm G}$=0 V by setting the metal gate work function to 4.7 eV (*i.e.* a value compatible with TiN metal). The readout at $V_{\rm G}$=0 V is very favorable to minimize the read disturbance, occurring when the ferroelectric polarization is unintentionally modified by the readout signal. Figure 8 reports both the potentiation and depression curves by using the two different pulse schemes of Fig. 7. While the constant amplitude write pulses (Pulse Scheme 1) can ease the design of peripheral circuitry, the increasing voltage pulses (Pulse Scheme 2) are beneficial for achieving a more linear dependence of the capacitance on the pulse number. Similar results were reported in several experimental data sets for ferroelectric memristors

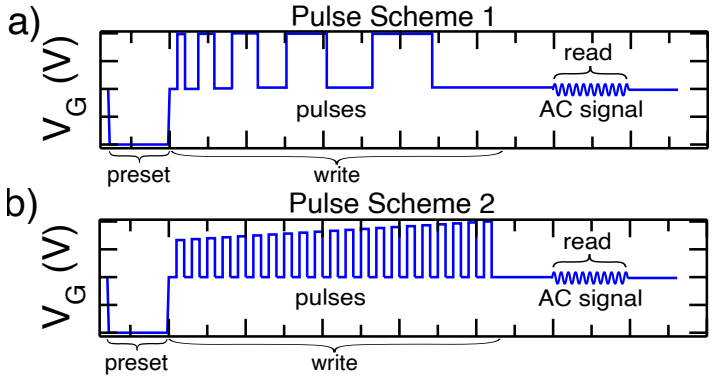

Fig. 7. Two write pulse schemes consisting of a) pulses with identical amplitude and increasing duration, and b) increasing amplitude with a fixed duration.

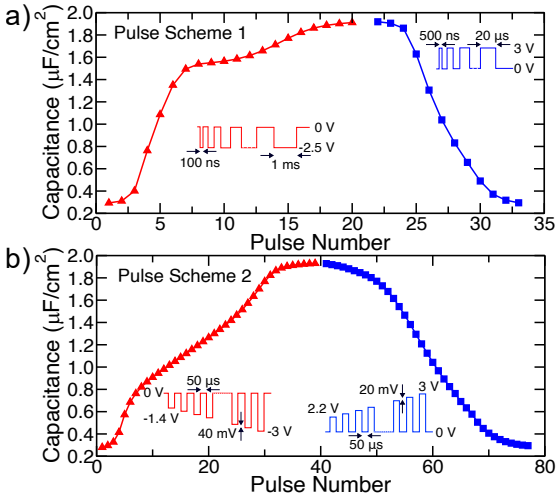

Fig. 8. Potentiation and depression of the memcapacitor small signal capacitance. Results obtained with: a) constant voltage pulses with increasing duration (Pulse Scheme 1, with V_{POT} =−2.5V and V_{DEP} =3V); b) increasing voltage pulses with same duration of 50μs. Each point in the graphs is obtained by first applying a preset pulse. The DC value for the readout is 0 V and the frequency of the small–signal AC is f_{AC} = 100 kHz.

[64]–[67], and memcapacitors [22], [24], [28], [31]. Figure 8b also displays a fairly good symmetry in the potentiation and depression curves obtained for different amplitudes of the positive and negative pulses as shown, which stems from the delicate interplay between the traps and ferroelectric dynamics. Indeed, the accumulative polarization switching is unlikely to be an intrinsic property of the ferroelectric oxide, but it is likely due to the trapping dynamics [47], [54]. The proposed device exhibits non volatile capacitance modulations within a range (C_{HS}/C_{LS}) $\simeq$10, which is comparable to some of the results recently reported for ferroelectric memristors [68], [69].

VI. Conclusions

A nanoscale CMOS compatible ferroelectric device has been proposed as a memcapacitor enabling low–energy operation, thanks to the high DC impedance and the small–signal AC readout. In a memcapacitor the readout current is proportional to the frequency of the AC readout signal, which provides an interesting design knob compared to the readout of memristors.

Even if simulation results depend on several material and device parameters, this work provides a proof-of-concept for the operation of the proposed ferroelectric memcapacitor.

Potential applications for memcapacitors encompass large passive crossbar arrays, where multiply-and-accumulate operations are implemented by using Kirchhoff's laws and AC displacement currents, instead of the DC conduction currents exploited in memristors–based crossbars. As already mentioned in the introduction, we reiterate that, in order to further improve the energy efficiency, a readout based on AC currents may also exploit charge recovery schemes [22], [36]–[38].

Appendix

In this appendix, we provide an analytical description of the V_G dependence of the depletion capacitance of the MemCap, with the ultimate goal of providing a derivation for Eq. (1). To this purpose, let us consider an MOS capacitor with a p-type substrate operated in the depletion region. The gate voltage equation reads

$$V_G = V_{FB} + V_{OX}(w_d) + \varphi_S(w_d) \tag{3}$$

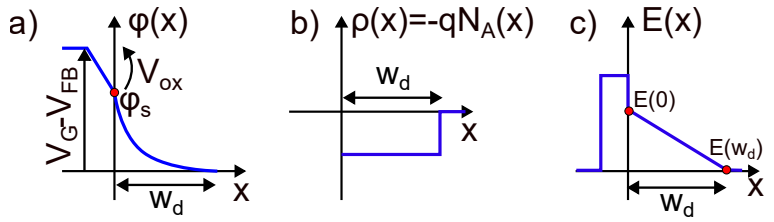

Fig. 9. Sketch of electrical quantities versus the abscissa x along the direction normal to the silicon-oxide interface for an MOS capacitor. a) electrostatic potential $\varphi(x)$; b) corresponding charge density; c) corresponding electric field.

where $V_{\rm FB}$ is the flat-band voltage, $V_{\rm OX}$ is the voltage drop across the oxide, $\varphi_{\rm S}$ is the surface potential at the oxide-semiconductor interface and $w_{\rm d}$ is the depth of the depletion zone. As implied by the notation in Eq. (3), $V_{\rm OX}$ and $\varphi_{\rm S}$ are in a one-to-one relation to $w_{\rm d}$, as we will see below. In Figure 9 the electrostatic potential, the space charge and the electric field are sketched along the direction x normal to the silicon-oxide interface.

In the p–type semiconductor, the 1D Poisson equation reads

$$\frac{dE}{dx} = -q\frac{N_{\rm A}(x)}{\varepsilon_{\rm Si}} \tag{4}$$

where $E(x)$ is the electric field and we have used the complete depletion approximation for the charge density. With the boundary condition $E(w_{\rm d})$=0, Eq. (4) provides:

$$E(x) = \int_x^{w_{\rm d}} q\frac{N_{\rm A}(x')}{\varepsilon_{\rm Si}}\,dx' \tag{5}$$

By integrating the field in Eq. (5) with the boundary condition $\varphi(w_{\rm d})$=0, we can write the interface potential $\varphi_{\rm S}$ as

$$\varphi_{\rm S} = \int_0^{w_{\rm d}} E(x)\,dx = \int_0^{w_{\rm d}} \left(\int_x^{w_{\rm d}} q\frac{N_{\rm A}(x')}{\varepsilon_{\rm Si}}\,dx'\right) dx. \tag{6}$$

We now insert $V_{\rm OX}$=$-Q_{\rm dep}(w_{\rm d})/C_{\rm OX}$ and Eq. (6) into Eq. (3) and obtain:

$$V_{\rm G} = V_{\rm FB} - \frac{Q_{\rm dep}(w_{\rm d})}{C_{\rm OX}} + \int_0^{w_{\rm d}} \left(\int_x^{w_{\rm d}} q\frac{N_{\rm A}(x')}{\varepsilon_{\rm Si}}\,dx'\right) dx \tag{7}$$

where $Q_{\rm dep}$ is the $w_{\rm d}$–dependent depletion charge

$$Q_{\rm dep}(w_{\rm d}) = -q\int_0^{w_{\rm d}} N_{\rm A}(x)\,dx. \tag{8}$$

The gate terminal capacitance $C(w_{\rm d})$ and its $V_{\rm G}$derivative may now be written as:

$$C(w_{\rm d}) = \frac{1}{\dfrac{1}{C_{\rm OX}} + \dfrac{w_{\rm d}}{\varepsilon_{\rm Si}}} = \frac{C_{\rm OX}}{1 + \dfrac{w_{\rm d}\,C_{\rm OX}}{\varepsilon_{\rm Si}}} \tag{9}$$

$$\frac{dC}{dV_{\rm G}} = \frac{dC}{dw_{\rm d}}\left(\frac{dV_{\rm G}}{dw_{\rm d}}\right)^{-1}. \tag{10}$$

The term $(dV_{\rm G}/dw_{\rm d})$ in Eq. (10) can be derived from Eq. (7)

$$\frac{dV_{\rm G}}{dw_{\rm d}} = \frac{-1}{C_{\rm OX}}\frac{dQ_{\rm dep}}{dw_{\rm d}} + \frac{d}{dw_{\rm d}}\left[\int_0^{w_{\rm d}} \left(\int_x^{w_{\rm d}} q\frac{N_{\rm A}(x')}{\varepsilon_{\rm Si}}dx'\right) dx\right]. \tag{11}$$

The first term in Eq. (11) can be readily calculated from Eq. (8), while for the second term we have

$$\begin{aligned}\frac{d}{dw_{\rm d}}\left[\int_0^{w_{\rm d}} \left(\int_x^{w_{\rm d}} q\frac{N_{\rm A}(x')}{\varepsilon_{\rm Si}}dx'\right) dx\right] &= \underbrace{\int_{w_{\rm d}}^{w_{\rm d}} q\frac{N_{\rm A}(x')}{\varepsilon_{\rm Si}}dx'}_{=0} + \int_0^{w_{\rm d}} \frac{\partial}{\partial w_{\rm d}}\left[\int_x^{w_{\rm d}} q\frac{N_{\rm A}(x')}{\varepsilon_{\rm Si}}\,dx'\right] dx \\ &= q\frac{N_{\rm A}(w_{\rm d})}{\varepsilon_{\rm Si}}\int_0^{w_{\rm d}} dx = q\frac{N_{\rm A}(w_{\rm d})}{\varepsilon_{\rm Si}}\,w_{\rm d}.\end{aligned} \tag{12}$$

By substituting back in Eq. (11) to obtain:

$$\frac{dV_{\rm G}}{dw_{\rm d}} = \frac{qN_{\rm A}(w_{\rm d})}{C_{\rm OX}} + \frac{qN_{\rm A}(w_{\rm d})}{\varepsilon_{\rm Si}}w_{\rm d} = qN_{\rm A}(w_{\rm d})\frac{\varepsilon_{\rm Si} + C_{\rm OX}w_{\rm d}}{C_{\rm OX}\varepsilon_{\rm Si}}. \tag{13}$$

By inserting Eq. (13) into Eq. (10) one obtains:

$$\begin{aligned}\frac{dC}{dV_{\mathrm{G}}} &= \frac{dC}{dw_{\mathrm{d}}}\left(\frac{dV_{\mathrm{G}}}{dw_{\mathrm{d}}}\right)^{-1} = \\ &= -\frac{{C_{\mathrm{OX}}}^2}{\varepsilon_{\mathrm{Si}}\left(1+\dfrac{w_{\mathrm{d}}C_{\mathrm{OX}}}{\varepsilon_{\mathrm{Si}}}\right)^2}\cdot\frac{C_{\mathrm{OX}}\varepsilon_{\mathrm{Si}}}{qN_{\mathrm{A}}(w_{\mathrm{d}})\left(\varepsilon_{\mathrm{Si}}+C_{\mathrm{OX}}w_{\mathrm{d}}\right)} = \\ &= -\frac{{C_{\mathrm{OX}}}^3{\varepsilon_{\mathrm{Si}}}^2}{qN_{\mathrm{A}}(w_{\mathrm{d}})\left(\varepsilon_{\mathrm{Si}}+w_{\mathrm{d}}C_{\mathrm{OX}}\right)^3}\,.\end{aligned} \tag{14}$$

Equation (14) completes the derivation of Eq. (1), that was the goal of this appendix.

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