Power Electronic Converters for Energy and e-Mobility: Topologies, Optimization, Modeling and Control

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Abstract

This comprehensive study dives deep into the realm of power electronics, addressing both the theoretical and practical aspects of advanced converter designs. A significant focus lies on the challenges posed by pulse-width modulation (PWM) inverters, particularly the distortions stemming from dead-times and switch voltage drops. Emphasizing the importance of a more nuanced approach, a novel compensation strategy grounded in a detailed physical model of power converters is introduced, followed by the assessment of innovative self-commissioning techniques employing Multiple Linear Regression.

The discussion further expands into the field of electric mobility, presenting an innovative system architecture tailored for range extender systems. Harnessing the potential of an integrated multi three-phase PMSM and high-frequency converter modules employing silicon carbide (SiC) power devices, this work pushes the envelope in creating a modular and fault-tolerant solution for electric vehicles.

In the second part of this thesis, DC/DC converters for On-Board charging application are studied, namely LLC and Dual Active Bridge (DAB).

This work addresses the limitations of traditional methods (FHA and EDF) used to identify the small-signal model of the LLC converter. Instead of relying on these conventional techniques, which often necessitate a resistive load assumption, this study proposes approximating the converter's small-signal output current response using a second-order discrete-time transfer function. This transfer function's coefficients adapt based on the operating conditions, like output voltage and switching frequency. To optimize the coefficient fitting, a data-driven approach using simulations and the LASSO machine learning method is employed. The research seeks to provide an accurate, efficient approximation of a resonant converter's output current response using machine learning.

Another commonly used converter in these kind of applications is the Dual Active Bridge. This converter has gained prominence for its features like bidirectional operation and galvanic isolation, making it ideal for interfacing with renewables, batteries, and smart grids. However, its control remains a challenge due to its intricate behavior. This work introduces a comprehensive model for the DAB converter, emphasizing its ability to adjust the average output current without external dynamics. This model offers insights into the design, operating point selection, and control of the DAB converter. A novel control loop and a Finite Control Set (FCS) that assures full ZVS method are proposed, both tested via simulations and experiments.

Moreover, this research examines various DC-DC converter designs for solid oxide fuel cell (SOFC) systems, focusing on their efficiency and gravimetric power density in hydrogen storage and energy distribution systems. Key performance metrics, like rise/fall times and ripple current limits, are outlined. Multiple converter topologies, such as the three-level multi-channel buck and buck with active filter, are assessed. Detailed design factors, from inductor values to switching frequencies, are explored for each topology. The study culminates in a design optimization procedure comparing the efficiency and weight of the converters through a Pareto analysis.

Lastly, the of hardware design of the previous converter is analyzed, focusing on the significance of PCB layout in the context of minimizing parasitic components. Silicon carbide's rising

prominence is underscored, setting the stage for discussions on gate driver designs that can harness SiC's rapid switching capabilities.
In totality, this work serves as a cornerstone in power electronics, bridging theoretical advancements with practical implementations, ensuring optimized performance across a spectrum of applications.

Chapter 1

Introduction

The present research is dedicated to the investigation and development of digital control systems and technologies tailored for electric motor drives and power electronics converters, with a particular focus on applications within the e-mobility domain. Recent years have witnessed an escalating trend towards the adoption of Electric Vehicles (EVs) and Plug-In Hybrid Vehicles (PHEV) as shown in Fig. 1.1. Projections and market analyses posit that these vehicular systems are poised to redefine the paradigm of transportation in the impending future [11].

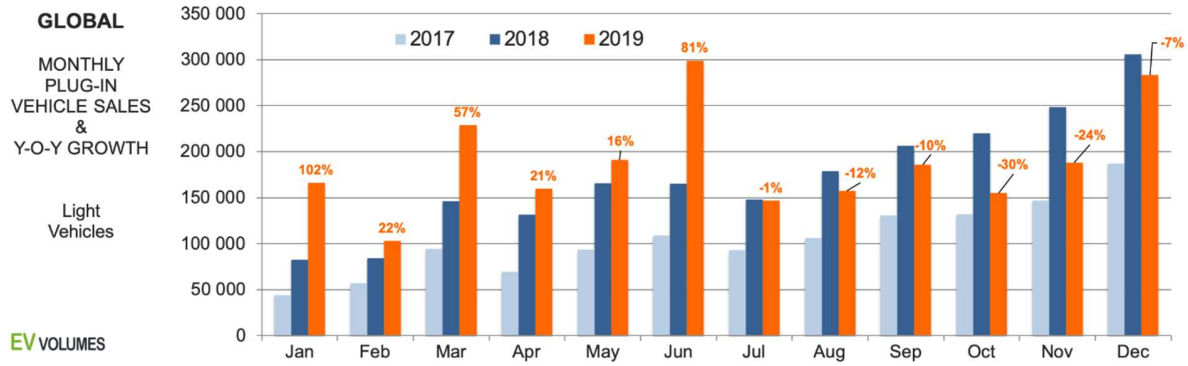


Figure 1.1: EV and PHEV sales in the three-years time frame 2017 ∼ 2019

On a system level, at least three components can be highlighted inside an EV whose purpose is to convert and exchange power, either from the electrical to the mechanical domain or the conversion from an electric source to another: traction inverter, high-voltage (HV) DC/DC and On-Board Charger (OBC). The complexity of these systems, along with very strict regulations, requires the design of the electric part to be compact, highly efficient, low cost and flawless.

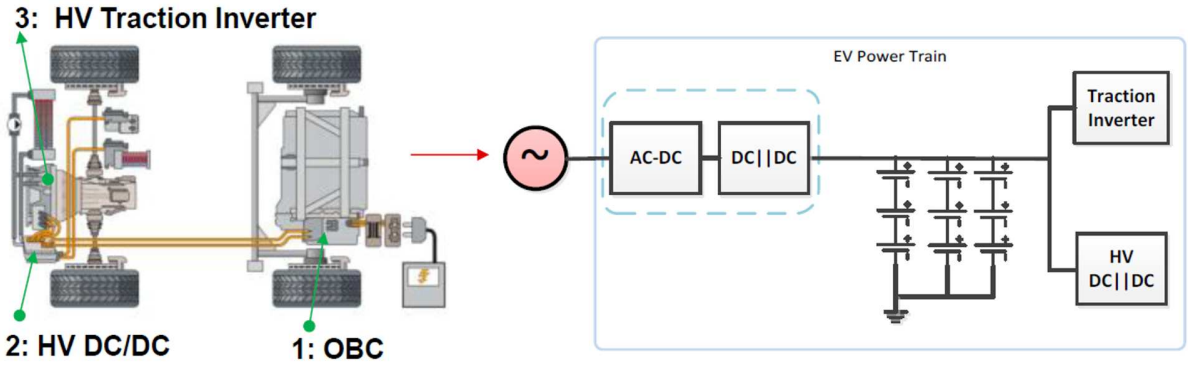
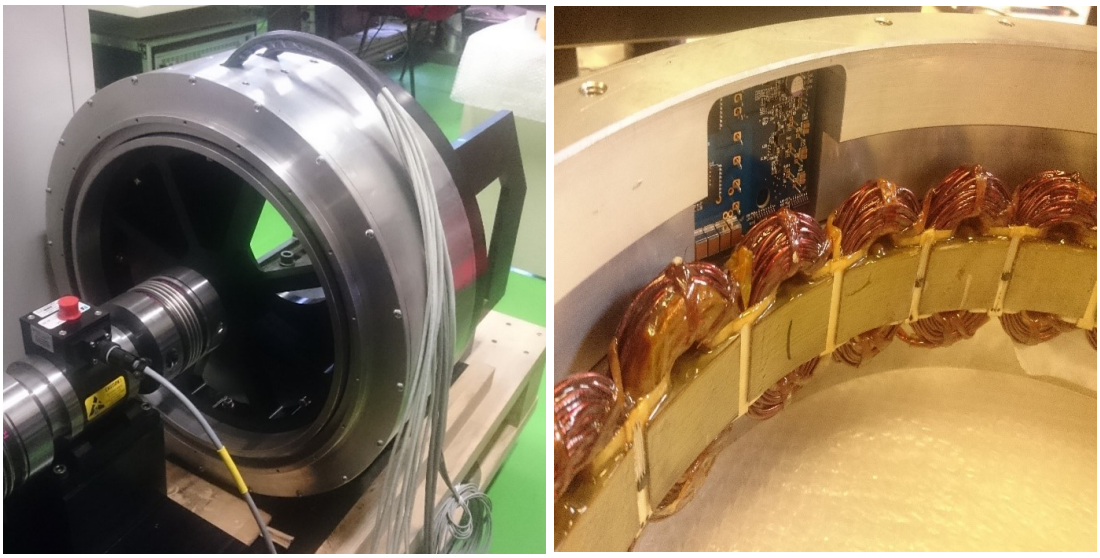


Figure 1.2: Block diagram of the power electronic system inside an EV

The shift towards electric road transportation necessitates that electric traction drive systems deliver enhanced capabilities, including improved fuel efficiency, longer travel ranges, and rapid charging features. This move towards increased electrification and evolving mobility signifies a growing need for high-power and efficient electric traction drives, which contribute to superior fuel economy per battery charge. In an effort to expedite the broad-scale acceptance of electric transportation, the U.S. Department of Energy (DOE), in partnership with the automotive sector, has set forth technical objectives for light-duty electric vehicles (EVs) aiming for 2025. This piece delves into the prevailing trends in electric drive technology for consumer electric and hybrid EVs, highlighting available innovations related to materials, inverter and electric machine design, peak speed, component temperature management, power density, and overall efficiency. The article also introduces emergent materials and technological advancements in the realms of power electronics and electric engines, pinpointing both the challenges and prospects for future-focused designs suitable for upcoming EV iterations. Furthermore, the discussion touches upon some cutting-edge drive and engine configurations that hold promise in achieving the DOE's 2025 aspirations [12].

Machine and drive selection varies based on specific requirements. While permanent magnet synchronous motors dominate the market, both induction machines and switched reluctance motors have found applications [13]. Recently, the shift towards multi-phase systems in traction applications has been evident due to their valuable attributes. These systems offer advantages such as power distribution, enhanced fault resilience (where losing one phase out of N still permits the remaining $N-1$ phases to function, unlike in traditional three-phase systems where losing a phase prevents the drive from starting) [14]. Additionally, multi-phase systems yield reduced torque fluctuations compared to standard three-phase systems [15–17]. They also present opportunities to decrease the size of the inverter, further allowing integration of the power electronics within the machine itself. An illustrative example can be seen in Fig. 1.3, showcasing the PERNA motor, which integrates a 12-phase machine with four independent 3-phase inverters situated within the stator slots. The maximum mechanical power rating is 13 kW (1000 rpm at 130 Nm) and each inverter is capable of delivering up to 3.5 kW of power to each sub-set of the machine. The inverter modules are fed by a common DC-bus voltage at 400 V (nominal), hence 16 A (rms) per three-phase set [18].



(a) **(b)**

Figure 1.3: PERNA motor (**a**) and PERNA close-up view of control board (**b**). The maximum mechanical power rating is 13 kW and each inverter is capable of delivering up to 3.5 kW of power to each sub-set of the machine.

1.1 Inverter and motor control

Given the need for a broad operational range in terms of speed and load torque, precise control techniques are crucial. The goal is to maximize the powertrain's efficiency to extend vehicle range, a paramount consideration in contemporary EV/HEV/PHEV design. Strategies like MTPA/MTPV (Maximum Torque Per Ampere/Volt [19]) and MLC (Minimum Loss Control [20]) aim to determine the most efficient operating state. MTPA primarily focuses on determining optimal stator currents to generate the required electromagnetic torque with minimized stator current magnitude. On the other hand, MLC considers both copper and iron losses in its optimization, identifying ideal stator currents for the intended electromagnetic torque [21]. As these methodologies cater to distinct objectives, discerning the scenarios where one is preferable over the other and fine-tuning them is essential for enhancing the power train's control strategy. Typically, the implementation of auxiliary sensing signals facilitates closed-loop control systems in tracing MTPA/MTPV/MLC paths instead of solving a closed-form problem directly [22]. However, the introduction of these signals might compromise the system's ability to achieve top speeds since some DC voltage designated for the inverter must be allocated for these sensing signals. This limitation can be addressed using VSI (Virtual Signal Injection), which incorporates a theoretical signal into a digital model rather than deploying an actual signal [23].
In this work, two important aspects of motor control and inverter design are studied. One of which is the integration of the power electronics converter inside the electric machine itself, especially in multiphase motors. The main issue limiting electric vehicles as viable partial solution to conventional mobility based on fossil fuels is the reduced range between charges. A possible solution is represented by range extender systems (RES), allowing to charge the main battery of the vehicle when needed, using a dedicated and reduced power internal combustion engine (ICE) coupled with an electric machine (EM) acting as a generator (Fig. 1.4). In the next chapters we study a novel system architecture, based on an integrated multi three-phase PMSM, fed by high-frequency converter modules (HFCMs) employing silicon-carbide (SiC) power devices. Magnetic coupling of three-phase modules is managed by a proper decoupling control strategy requiring a real-time communication among modules. Design of the system, including the power and control electronics, and the electric machine, as well as simulation and experimental results are reported to demonstrate the effectiveness of this proposal [24].
Another issue tackled in this work regarding Pulse-Width-Modulated (PWM) inverters, is dead-time and voltage drops distortion on the average output voltage [25]. This effect is related to the system parameters and to the operating conditions and in many drives applications it can be intolerable. A number of modeling approaches and compensation methods have been proposed in the past literature. A recent approach adopts an accurate physical model of the inverter, aiming at investigating the effects of parasitic capacitances and devices voltage drops by a fitting analytical characteristic. Model parameters are derived from a self-commissioning procedure, based on proper voltage injection and processing, both affecting the accuracy of achievable compensation. In this paper, these issues have been considered and two original enhancements have been proposed and validated, demonstrating the superiority of the results over state-of-the-art. Finally, the effects of the mentioned inverter distortion on the accuracy of current sampling and control loops are also analyzed for the first time, and an original compensation strategy is proposed and validated. Theoretical analysis and developments are fully reported, together with accurate simulations and experimental results based on a commercial drive.

1.2 On-Board Charger topologies

As of today by analyzing the current landscape and deployment of battery chargers, the power levels used for charging, and the infrastructure established for hybrid and plug-in electric vehicles we can characterize charging systems divided into two main categories: on-board and off-board, with options for either unidirectional or bidirectional power transfer [26]. While unidirectional

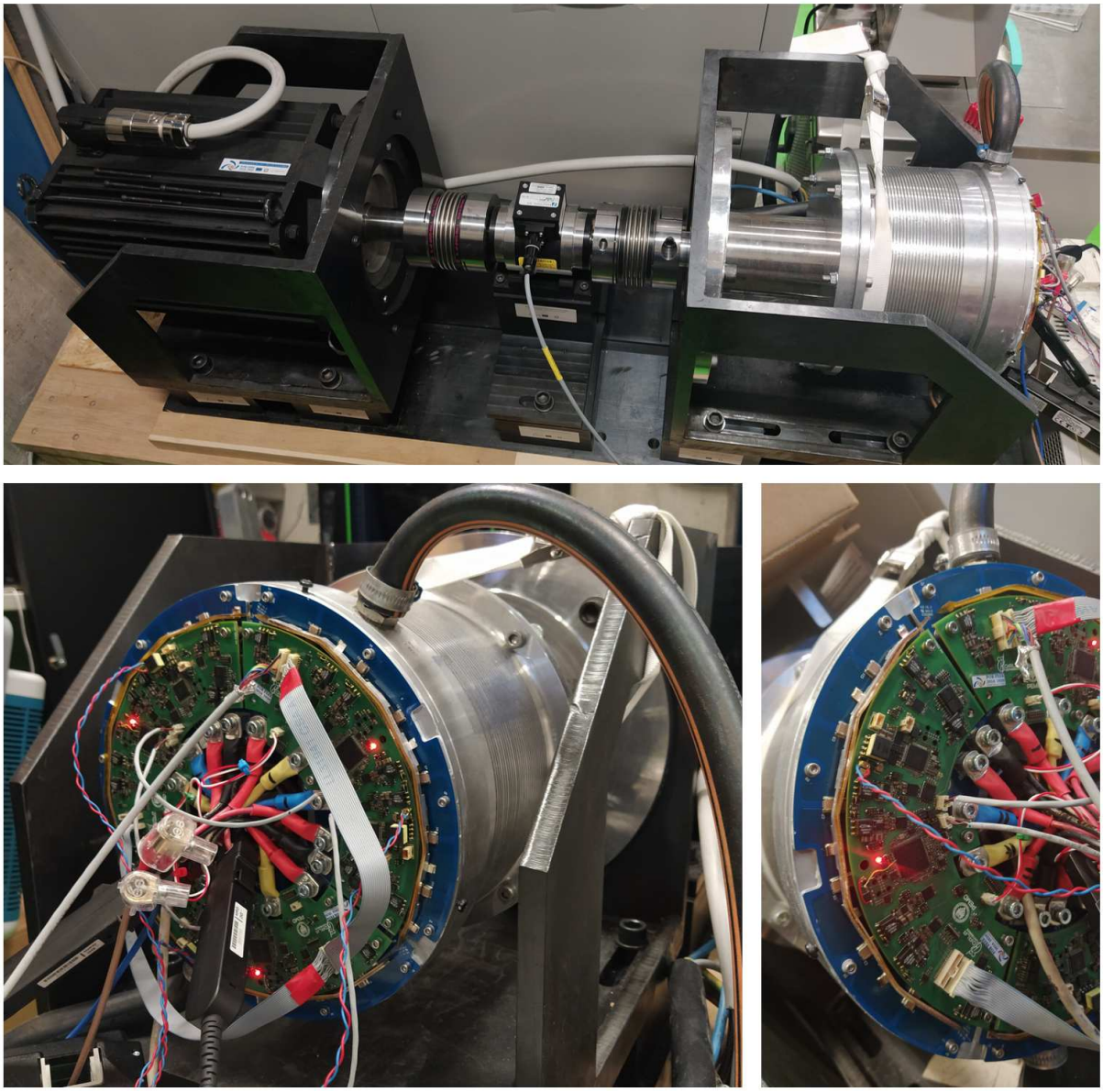


Figure 1.4: Photographs of the laboratory test bench.

charging simplifies hardware needs and connection complexities, bidirectional charging facilitates the possibility of returning battery energy to the grid. On-board chargers commonly face limitations in power due to concerns related to weight, space, and cost. However, merging them with the electric drive can mitigate these limitations. Having a well-established charging infrastructure can potentially reduce the necessity for on-board energy storage, subsequently lowering costs. On-board charger systems can be either conductive or inductive in nature. In contrast, off-board chargers, free from strict size and weight constraints, can be tailored for high-power charging.

The On-Board Charger (OBC) plays a pivotal role in the functionality of Plug-in Electric Vehicles (PEVs) and Hybrid Electric Vehicles (HEVs). Transitioning from conventional vehicles to electric vehicles is imperative to mitigate vehicular pollution's contribution to the pressing concern of global climate change. Electric vehicles derive the power for charging their battery from the electrical grid, making it crucial to maintain a power factor (PF) close to unity during this process.

Fig. 1.6 illustrates an on-board charger scheme, where the PFC stage is implemented with a

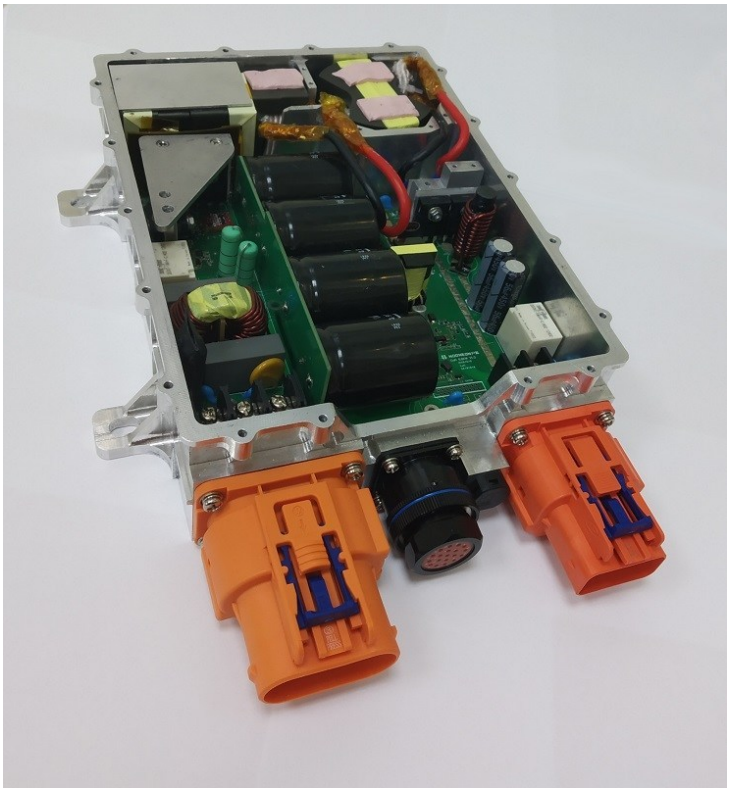


Figure 1.5: 6.6 kW On-Board Charger GaN based design by VisIC Technologies [1].

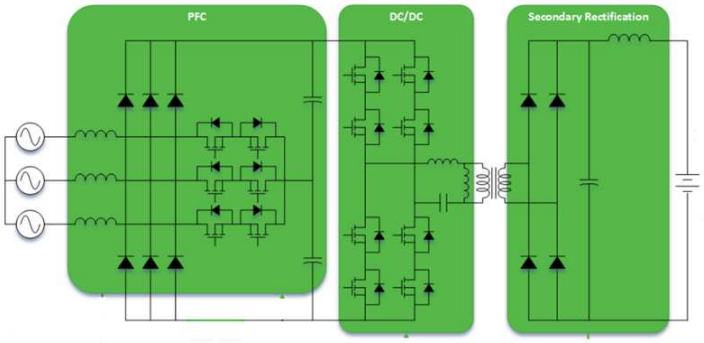


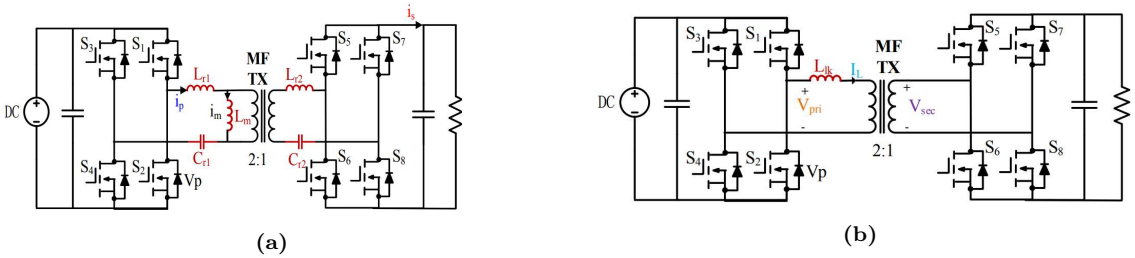
Figure 1.6: Three-phase OBC topology example

Vienna Rectifier while the isolation converter (DC/DC) is an LLC converter. In this case the secondary rectification is done via passive full-bridge rectifier while, because of the increasing power density of these converters, synchronous rectifiers might be used to increase the efficiency, decrease EMI, size and ultimately enabling bidirectionality.

In the AC/DC stage, the conversion is from alternating voltages and currents into DC values in order to feed the battery. Depending on the power requirements and/or grid line availability, they might be either single-phase or three-phase. In the AC/DC conversion phase, controlling the power factor (PF), efficiency and total harmonic distortion (THD) are the three main goals in order to achieve the maximum quality of the rectification process and ultimately make the charging process last as little time as possible while respecting the grid absorption constrains such as IEC 61000 for LF conducted emission regulations. A typical charger configuration comprises two primary sections: an input power factor correction (PFC) stage followed by an isolated DC-DC conversion circuit.

These converters are based off a full bridge rectifier and usually a boost converter that acts as

a PFC (Power Factor Corrector) in single-phase applications, or (in three-phase applications) bridgeless totem pole circuits. Recent studies show that the Vienna Rectifier is becoming more and more appealing for this purpose due to its high power factor and low mains distortion [27,28], but many others are used and have their pros and cons [26, 29, 30] i.e. interleaved PFC for its simplicity and control ease, Bridgeless PFC for its reduced inductor current ripple, various types of multilevel converters. Since the Vehicle-to-Grid (V2G) service is becoming more popular, bidirectional converters are often necessary. Some authors [31,32] presented some studies where the electric machine windings have been used in place of the magnetic components commonly used in power converter. The motor inverter automatically makes this solution bidirectional and might save some cost and space if the presence of a switching relay system for connecting the motor phases to the grid is accepted.



(a) (b)

Figure 1.7: LLC converter (**a**) DAB converter (**b**). [2]

Due to the necessity to isolate the rectified mains voltage from the HV battery, an isolated DCDC converter stage is necessary. This is usually implemented with an LLC converter, a DAB (Dual Active Bridge) or some form or resonant converter Fig. 1.7. The need for big magnetics components such as the transformer and resonant inductor introduces the problem of the big volume occupied by these converters and their prices. In order to have smaller magnetics, higher switching frequencies are chased thanks to new technologies in switching devices such as SiC and GaN [33, 34]. Higher switching frequency introduce, however, other problems related to switching energy loss and EMI. These issues can be limited by switching the devices in ZVS (Zero Voltage Switching), hence accurately knowing the model of the converter and their degrees of freedom and utilization can highly impact the quality of the power transfer. Two studies that tackle these issues are introduced in this work regarding the modeling and control optimization to reach a wide ZVS range with these converters. LLC small-signal model is often identified via FHA (First Harmonic Approximation) and/or EDF (Extended Describing Function) in order to analyse the dynamical behaviour of the converter and hopefully fine tune the controller. These approaches fail easily and force to consider a resistive load, which is a restrictive method since most of the times resonant converters are used to feed current or stabilize a voltage (e.g., in battery charging applications). In this work the small-signal output current response of the converter is approximated by a second order discrete-time transfer function, whose numerator and denominator coefficients change with the operating condition (i.e., output voltage and switching frequency). The coefficients are fitted using a sparse linear combination of functions in data-driven fashion (via simulation) adopting a well-known machine learning operator (Least Absolute Shrinkage and Selection Operator, LASSO). The aim is to report the first attempts made to obtain an accurate and computationally-optimized approximation of the output current response of a generic resonant converter based on machine learning techniques [35].

On the other hand, the Dual Active Bridge (DAB) topology has become very popular in recent years due to its characteristics (e.g., bidirectional operation and galvanic isolation), which are particularly suitable to applications such as interface to renewable energy sources, battery storage systems and in smart grids. Although this converter type has been extensively investigated, its analysis and control still pose many challenges, due to the multiple control variables that

affect the complex behavior of the converter. We present a theoretical model of the single-phase DAB converter. The proposed model is very general, i.e., it can consider any modulation technique and operating condition. In particular, the converter is seen as composed by four legs, each capable of generating voltage on the inductor, and by the two output legs, which can steer the resulting inductor current to the load. Three variables are considered as the control inputs, i.e., the phase shifts with respect to one leg. This approach results in a very simple yet accurate closed form algorithm for obtaining the inductor current waveform. Moreover, a novel analytical model is proposed for calculating the average output current, based on the phase shift values, independently of the output voltage. It is also shown that average output current can be varied cycle by cycle, with no further dynamics. In fact, average output current is not affected by the initial value of inductor current or by DC offset (which may arise during transients). The proposed models can be exploited at several stages of development of a DAB: during the design stage, for fast iteration, when selecting its operating points and when designing the control. In fact, based on the analytical results, a novel control loop is proposed, which adopts a "fictitious" (i.e., open-loop) inner current regulation loop, which can be applied to any modulation scheme (e.g., Single Phase Shift, Triple Phase Shift, etc.). The main advantage of this control scheme is that the simple dynamics of the output voltage versus the average output current can be decoupled from the complicated relationship between the phase shifts and the output current. Moreover, a Finite Control Set (FCS) method is proposed, which selects the optimal operating points for each operating condition and control request, ensuring full Zero Voltage Switching (ZVS) in all cases [36]. The analytical results obtained and control methods proposed are verified through simulations and extensive experimental tests, where the setup is displayed in Fig. 1.8. The DAB system is developed for a Type-2 11 kW three-phase on-board charger, with voltage rating of 800 V on primary side and up to 500 V on battery side.

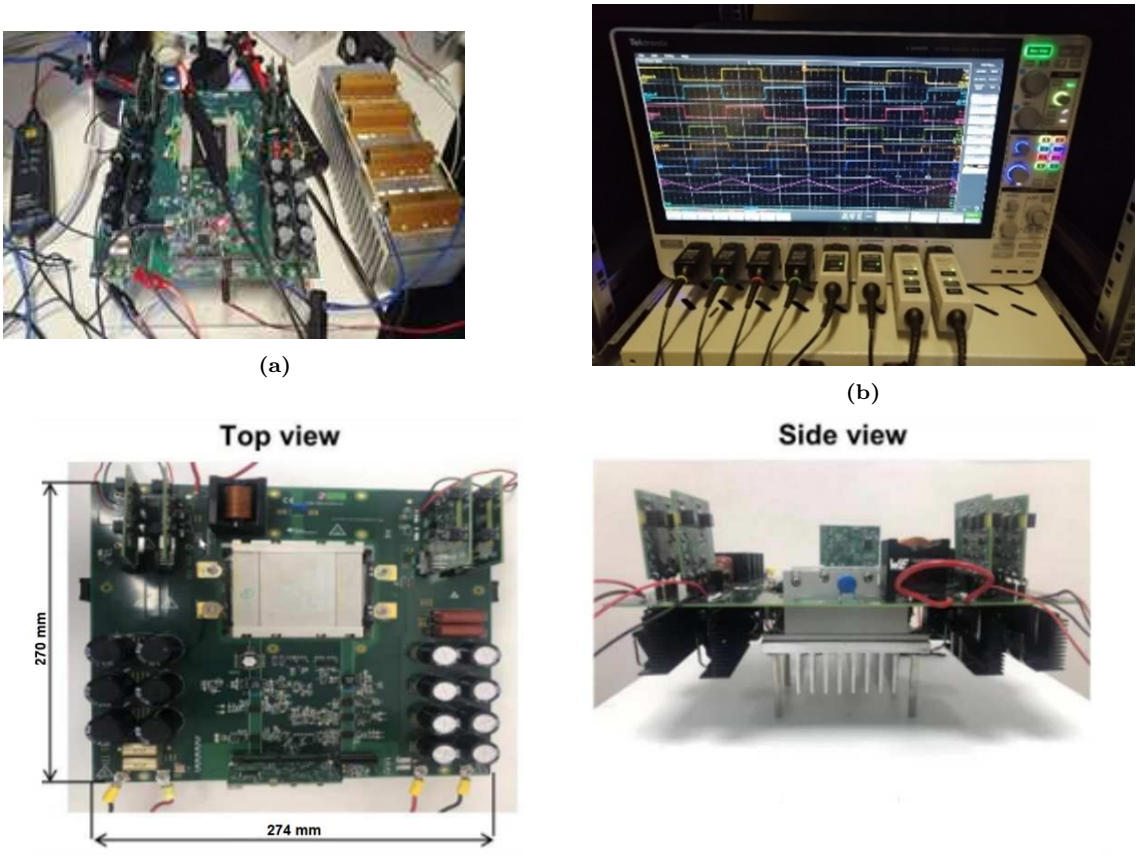
1.3 Power electronics converters for energy storage and hydrogen generation systems

The rising popularity of EV and PHEV puts a lot of strain in the energy distribution systems. The 2050 Net-Zero Emissions (NZE) goal set by the IPCC to remain consistent with the mean temperature increase of 1.5^{o}C. For this purpose, hydrogen has gain a lot of popularity lately since it helps driving the energy production and storage demand towards a more efficient and emission free scenarios.

Advancements in hydrogen technology have catalyzed a substantial expansion of electrolyser production capabilities and the synchronous evolution of novel hydrogen transportation systems. These strategic shifts have subsequently led to significant cost savings in both electrolyser production and hydrogen storage, with a particular focus on innovative solutions such as salt caverns. The strategic storage of hydrogen serves as an effective counterbalance to temporal irregularities in electricity demand as well as any potential incongruities between hydrogen demand and its delivery, especially from isolated renewable energy setups. Throughout the decade leading up to 2030, there's a marked surge in the adoption of hydrogen-centric equipment, exemplified by the proliferation of over 15 million hydrogen fuel cell vehicles [37].

Post-2030, the Net Zero Emission (NZE) framework witnesses a pronounced upswing in the adoption of low-carbon hydrogen across various industries. Within the electricity landscape, hydrogen and its derivative fuels emerge as pivotal contributors to low-carbon electricity system adaptability. This is chiefly manifested in the adaptation of extant gas-powered infrastructures to accommodate hydrogen co-firing and to a lesser extent, the modification of coal-driven power plants for ammonia co-firing. Despite contributing a modest 2% to the electricity production by 2050, this development signifies colossal hydrogen volumes, making the electricity sector a central hub for hydrogen demand.

The transportation sector sees a transformation with hydrogen accounting for approximately



(a) **(b)** **(c)**

Figure 1.8: Experimental setup for DAB converter (**a**) Top view. (**b**) Key DAB waveforms at rated power (i.e. 11 kW). (**c**) Board side view.

a third of fuel consumption in trucks by the mid-century, under the NZE blueprint. This trajectory, however, hinges on decisive policy formulations aimed at sculpting the requisite infrastructural landscape by 2030. Moreover, by 2050, hydrogen-derived fuels are slated to dominate maritime transport, catering to over 60% of its fuel demands.

Of the projected 530 Mt hydrogen yield in 2050, an estimated quarter will originate from industrial hubs, encompassing refineries. The remaining output predominantly emerges as commercial hydrogen. Close to 30% of the low-carbon hydrogen utilized in 2050 will metamorphose into hydrogen-induced fuels, encapsulating products like ammonia and synthetic liquids. Electrolysers, buoyed by grid electricity, region-specific renewables, and alternative low-carbon sources such as nuclear energy, are projected to contribute to 60% of total production by 2050. The accelerated deployment of electrolysers, as envisioned in the NZE, presents a formidable challenge, especially considering the current manufacturing constraints and the imperative of sustained electricity production. Lastly, the NZE anticipates a burgeoning global hydrogen trade, with prolific export trajectories stemming from resource-abundant zones in the Middle East, Central and South America, and Australia, channeling towards high-demand areas in Asia and Europe.

Fig. 1.11 depicts the H2@Scale® framework, a vision initiated in 2016 by the Department of Energy (DOE) and its National Laboratories [38]. This model underscores the potential of clean hydrogen derived from an array of domestic sources for multifaceted applications. Hydrogen production can be designed to fit various scales, from centralized to decentralized systems, and can operate in conjunction or independently from the power grid. Such adaptability speaks to hydrogen's capacity for scalability, flexibility, and regional specificity. Furthermore, clean hydrogen augments the traditional electric and natural gas grids, providing an alternative to the straightforward "electron-to-electron" flow, exemplified by battery storage. It offers a solution

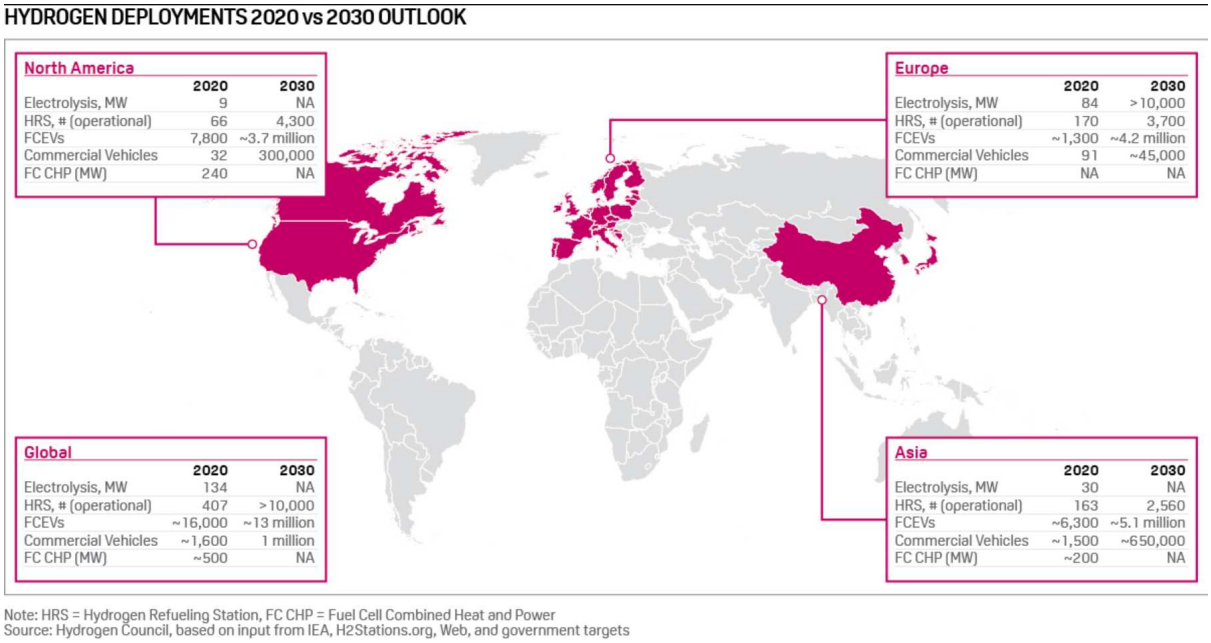


Figure 1.9: Hydrogen deployment outlooks: 2020 vs 2030

in areas where direct electrification might be untenable.
Numerous technological avenues exist for the generation of clean hydrogen. These encompass electrolyzers, which are energized by the ever-expanding portfolio of clean energy sources in the nation, methane reforming integrated with carbon capture and storage (CCS), biomass and solid waste gasification or thermal conversion (also complemented with CCS), and a myriad of nascent technologies. Initial integrations of clean hydrogen are anticipated to maximize regional energy assets and focus on sectors currently hinged on the conventional transformation of natural gas to hydrogen, devoid of CCS.
The Environmental Protection Agency (EPA) has postulated that a synergistic firing of hydrogen with natural gas represents an optimal approach for emission mitigation in certain subsets of fossil fuel-driven plants. Such a method could be integrated as a compliance mechanism for curbing CO2 discharges from these power units, aligned with Section 111 of the Clean Air Act [39]. While these sectors offer swift scalability and prompt impacts in emission curtailment, it's imperative to actively address community apprehensions related to NO_x emissions, leakage detection, and overall safety. Constructive community dialogue, augmented with enhanced transparency, should encapsulate both the inherent risks and the advanced safety protocols, monitoring techniques, and detection technologies in place. Such community outreach will be instrumental when rolling out new hydrogen technologies to supplant fossil fuels in various sectors. Furthermore, these pioneering applications often benefit from co-location, enabling them to tap into cost-effective hydrogen production without the added expenses of midstream distribution or storage.
In this context, obviously fuel cells start to rise as prominent source of interest. A fuel cell converts the chemical energy from hydrogen or alternative fuels directly into electricity in a clean and efficient manner. When hydrogen serves as the fuel source, the resultant by-products are merely electricity, water, and heat. What sets fuel cells apart is their versatile application spectrum. They can utilize an extensive array of fuels and feedstocks, and they are adaptable to power systems ranging from expansive utility power stations to compact devices like laptops. For these reasons, the power conversions system that aid the control and/or distribution of hydrogen generated energy are rising more and more in interest from an industrial standpoint. In this thesis, we present a study that analyses different DC-DC converter architectures and topologies suitable for solid oxide fuel cell (SOFC) systems operating in electrolysis and fuel cell modes.

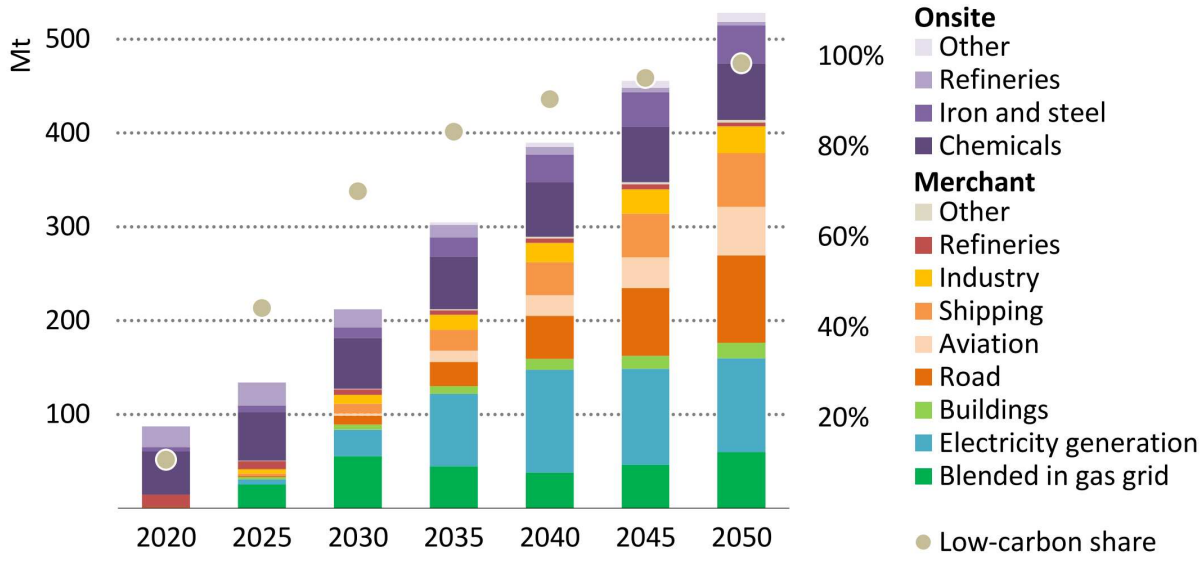


Figure 1.10: Global hydrogen and hydrogen-based fuel use in the NZE [3]

The goal is to determine the most suitable converter design based on efficiency and gravimetric power density. The two operating modes of the SOFC are illustrated, and the requirements for rise/fall times and maximum allowable ripple current are discussed. Several converter topologies, including three-level multi-channel buck, three-level four-switch buck-boost, and buck with active filter, are evaluated. The design considerations, including inductor values, switching frequencies, and current waveforms, are discussed for each topology. Finally, a multi-objective design optimization procedure is performed to compare the efficiency and weight (gravimetric power density) of the considered converters.

Achieving the Net-Zero Emissions (NZE) goal by 2050 supposes that the landscape of sustainable energy technologies will evolving rapidly. This dissertation aims at the exploration of three distinct yet interconnected domains that play pivotal roles in realizing a cleaner and more efficient future for our energy systems. In the First Part, DC-DC Converters for Fuel-Cell Applications in Hydrogen Storage and Distribution Systems are studied, delving into the crucial realm of hydrogen technology, a key player in the quest for net-zero emissions. Focusing on fuel-cell applications, an investigation on the design and optimization of DC-DC converters tailored for hydrogen storage and distribution systems is carried out. As hydrogen emerges as a prominent contender for energy production and storage, the efficiency and reliability of these converters become paramount in ensuring the seamless integration of such technologies into our energy infrastructure.

In the Second Part, DC-DC Converters Design for On-Board Charging Applications of Electric Vehicles are studied. Here the attention shifts to the realm of electric vehicles (EVs), a cornerstone in the transition towards sustainable mobility. The intricacies of DC-DC converters designed specifically for on-board charging applications are explored, specifically in the modeling and control of well known topologies widely used for this purpose. The efficiency and performance of these converters play a pivotal role in maximizing the charging capabilities of electric vehicles, addressing concerns related to weight, space, and cost. This section aims to contribute insights into advancing on-board charging systems, thereby enhancing the viability

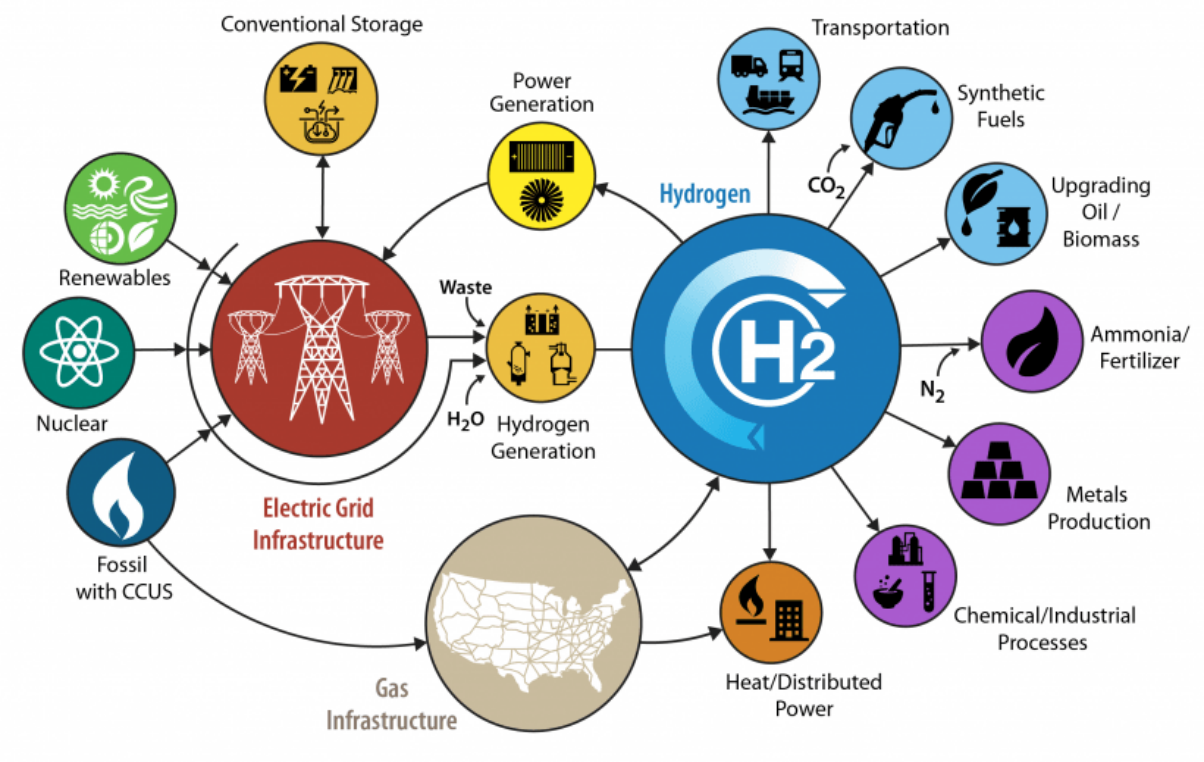


Figure 1.11: H2@Scale vision

and widespread adoption of electric vehicles.
Finally, the Third Part focuses on the critical role of inverters within the EV-automotive industry, illustrating two distinct projects. The first dedicated to traction applications, emphasizing the importance of precise control techniques to optimize the performance of electric vehicle powertrains whereas the second explores a more niche application (range-extender), aiming to extend the vehicle range and address one of the key challenges faced by electric vehicles. Both projects provide valuable insights, highlighting the significance in achieving efficiency and performance goals in electric vehicles.
While each part of this dissertation navigates specific domains within the broader scope of sustainable energy technologies, the collective insights gained from these investigations contribute to our understanding of the intricate interplay between various components in the pursuit of a cleaner and more sustainable energy future. Through these endeavors, we aim to propel advancements in technology that align with the overarching goal of achieving net-zero emissions by 2050.

Part I

Non-isolated DC-DC in energy storage systems

Chapter 2

Optimization of bidirectional DCDC converter

This study presents an analysis of different DC-DC converter architectures and topologies suitable for solid oxide fuel cell (SOFC) systems operating in electrolysis and fuel cell modes. The goal is to determine the most suitable converter design based on efficiency and gravimetric power density. The two operating modes of the SOFC are illustrated, and the requirements for rise/fall times and maximum allowable ripple current are discussed. Several converter topologies, including three-level multi-channel buck, three-level four-switch buck-boost, and buck with active filter, are evaluated. The design considerations, including inductor values, switching frequencies, and current waveforms, are discussed for each topology. Finally, a multi-objective design optimization procedure is performed to compare the efficiency and weight (gravimetric power density) of the considered converters.

2.1 Introduction

Solid oxide fuel cells offer a way to store and supply energy whilst producing limited to no carbon emission. During the fuel cell operating mode, the SOFC generates power using a wide range of fuels, including natural, gas, biofuels and hydrogen [40]. During the electrolysis operating mode, the SOFC produces hydrogen from steam with power input [41]. In this study, we present several potential DC-DC architectures and topologies that are suitable for the intended application. Additionally, we conduct a Pareto analysis comparing their efficiency to the gravimetric power density (η-ρ analysis) in order to determine the most suitable proposal for this specific purpose.

2.1.1 Solid Oxide Fuel-Cell operating modes

The requirement for the operation of the fuel-cell in *electrolysis mode* (hence when current is supplied to the SOFC) necessitates the use of pulsed current in the form of a square wave. The amplitude of the square is in the range of 0 to 50 A and the frequency is 2 kHz. Conversely, when the fuel-cell is operating as a voltage source in *fuel-cell mode*, a constant current of 20 A is expected. The DC-DC converter must ensure that both the current ripple and the rise/fall time of the square wave remain within acceptable limits for the specific application. Further details regarding these parameters will be provided in subsequent sections. There is no restriction or specification regarding the fuel-cell voltage, which ultimately shrinks the possible candidate topologies space to analyse.
In Fig. 2.1a and Fig. 2.1b, the two different operating modes are illustrated. The requirements on rise/fall times (t_Δ) and maximum allowable ripple current (Δi_o) will be discussed hereinafter.

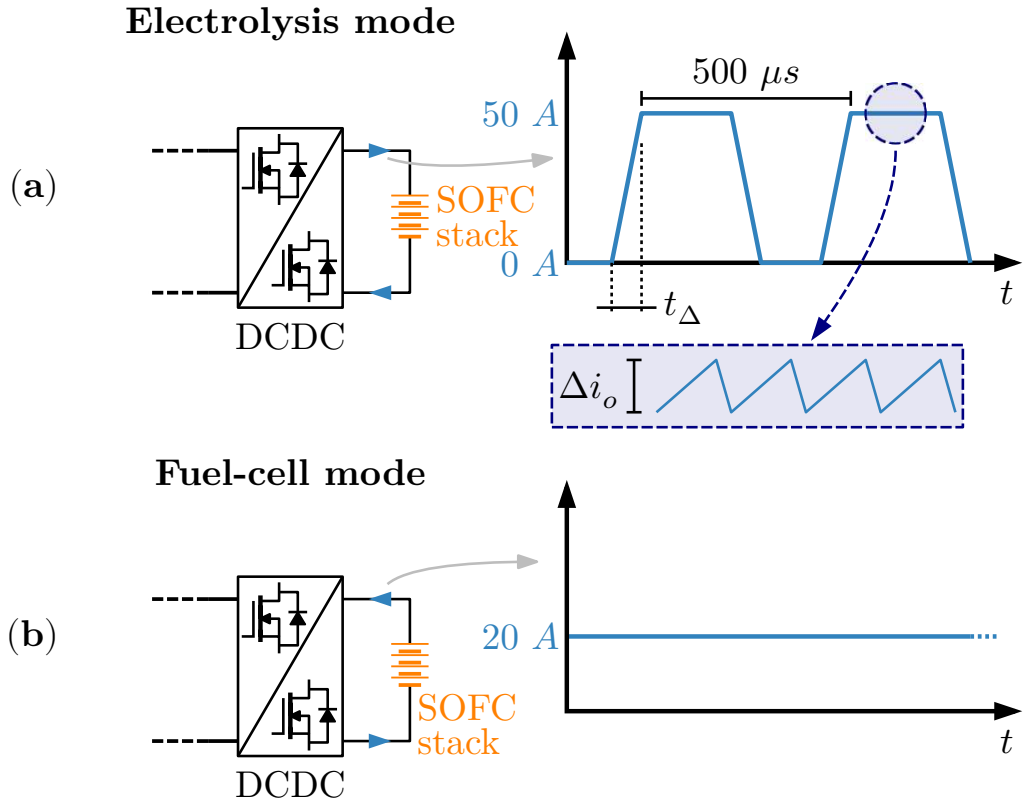


Figure 2.1: **(a)** The current fed in the SOFC is pulsed with 500 μs period (2 kHz) and amplitude 0 $\sim$ 50 A. **(b)** Fuel-cell mode, constant current discharge at 20 A.

2.1.2 System level overview

On a system level perspective, illustrated in Fig. 2.2, the plant is composed by multiple solid oxide fuel-cells which can be controlled (hence charged or discharged) independently. This means that a DC-DC converter for each fuel-cell stack is needed in order to control the current as previously described. Every DC-DC is linked to the same common DC-bus, which is generated by an active front end. The whole DC side is then locally grounded and the isolation is implemented by means of line frequency transformer. This design choice allows to avoid high-frequency isolation on the DC-DC converters, ultimately enabling higher overall system efficiency and cost reduction [42].

In order to reduce the total number of DC-DC converters to be used, the fuel-cells are stacked in two different 350-cells series connected stacks. The active front end used in this application is a three-level topology, hence the decision of designing a three-level DC-DC with grounded midpoint for every pair of series connected fuel-cell stacks as shown in Fig. 2.3. Every cell open circuit voltage (i.e. at 0 A) is 1.0 V while at full load in electrolysis operation (when feeding the cells in the stack with 50 A) the voltage across each cell can be measured at 1.33 V. In fuel-cell operating mode, hence when the stacks are used to feed the grid, the voltage measured across each cell is around 0.87 V when the nominal 20 A are drawn. This means that every stack voltage swings between 350 and 465 V in electrolysis mode (when the current jumps between 0 and 50 A), while in fuel-cell mode when drawing 20 A from each stack the voltage across a single stack will stand at around 300 V.

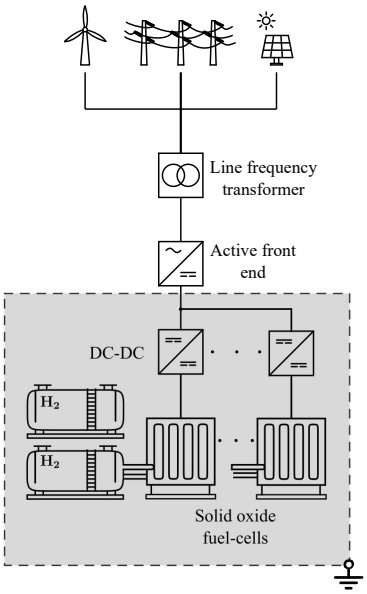


Figure 2.2: System level structure of the SOFC plant

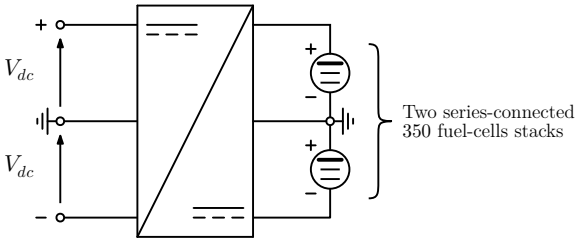


Figure 2.3: Two solid oxide fuel-cells stacks are series connected with grounded midpoint. The DC-DC controls the current in each of them, allowing for unbalanced operation and reduced overall number of converters per plant. Each stack is composed by 350 fuel-cells.

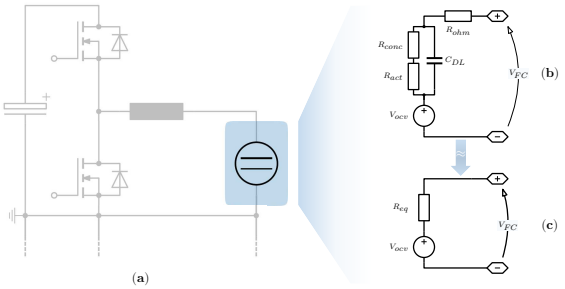


Figure 2.4: **(a)** Schematic view. **(b)** Actual SOFC electrical model as explained in [4]. **(c)** Approximated circuit model used in this work.

For these reasons, for the electric modelling of the SOFC stack and subsequent analysis, an E-R load is used where E is the open circuit voltage of the stack (350 V) and R is the equivalent fuel-cell stack series resistance which is approximately 2.32 Ω. The actual electrical model of a SOFC has been widely studied in literature [4] and the E-R approximation is accepted for the dynamical study in this work. In Fig. 2.4b the actual electrical SOFC model is shown, while in Fig. 2.4c the aforementioned approximation is displayed.

2.2 Candidate topologies

A handful of architectures and topologies have been evaluated for this application, with different characteristics in terms of performance, hence achievable ripple current, fuel-cell current transient time, cost, complexity and efficiency. When operating in electrolysis mode, the current on each fuel-cell must be pulsed with 500 μs period (2 kHz) and amplitude $0 \sim 50$ A. The transient time t_Δ and ripple current Δi_o are not strictly defined *a-priori* if not for their maximum allowed value (i.e. 10 μs and $\pm 10\%$ of full-load current). The converter will target this design point (or better) and 99 % efficiency. Out of the possible candidate converters a Pareto analysis for comparing efficiency and gravimetric power density is carried out in order to ultimately select the best topology for this application.

2.2.1 Multi-channel buck

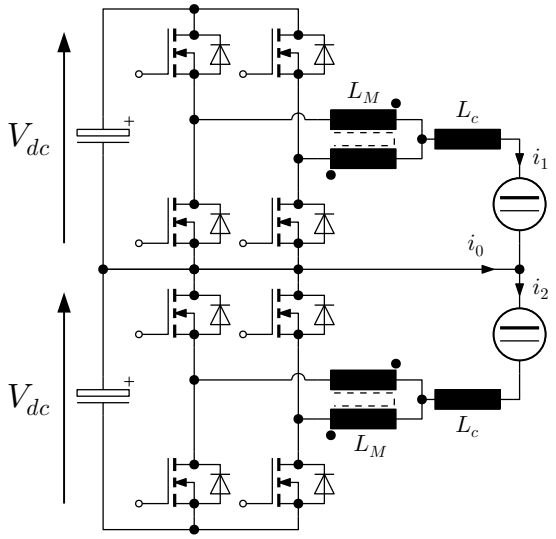


Figure 2.5: Schematic view of buck two channel

The three-level multi-channel buck is shown Fig. 2.5. The "top" and "bottom" converters control the top and bottom SOFC stacks respectively which, as explained before, are series connected. In this topology the different channels are operated at the same frequency and the relative phase-shift between different half-bridge legs depends on the number of channels. In Fig. 2.5 the specific case of a two-channel buck is shown, hence the interleaving requires 180^o phase-shift between gating signals in order to achieve maximum output current ripple cancellation [43]. The output inductance (here called L_c) is designed in order to satisfy the constraint on the maximum time needed to reach the 50 A steady-state point during a transient (t_Δ). The parameter t_Δ is a constraint given from system level and its value cannot exceed 10 μs.

$$\begin{aligned} L_{c\_rise} &= -\frac{R_s t_\Delta}{\log\left(1 - \frac{I_o R_s}{V_{dc} - V_{ocv}}\right)} \\ L_{c\_fall} &= \frac{R_s t_\Delta}{\log\left(1 + \frac{I_o R_s}{V_{ocv}}\right)} \\ L_c &= \min\left\{L_{c\_rise},\, L_{c\_fall}\right\} \end{aligned} \tag{2.1}$$

In Eq. (2.1) L_{c_rise} refers to the inductance needed so that the rise-time (i.e. time taken to make the SOFC current go from 0 to 50 A) constraint t_Δ is respected. The term L_{c_fall} refers to the value of inductance needed to respect the fall-time, hence the time to make the current fall from 50 to 0 A. The term R_s is the equivalent series resistance of the SOFC stack, V_{ocv} is the open-circuit voltage of the stack (hence 350 V), D is the duty cycle during the phase in which the converter is supplying the steady-state current (50 A) and V_{dc} is the DC-link voltage of a single (top or bottom) converter as shown in Fig. 2.5. As seen in the figure, there's no need of the usual output capacitor since limiting SOFC stack voltage ripple is not a concern in this application.

Once the output inductor L_c is designed, the switching frequency can be selected in order to comply with the constraint on the maximum acceptable output current ripple Δi_o. The load ripple current is another constraint given from system level and its value cannot exceed $\pm 10\%$ of full load (50 A), hence ± 5 A. Note that, during the zero-current time windows, no switching happens (the converter is simply shut down and all switches are turned off).

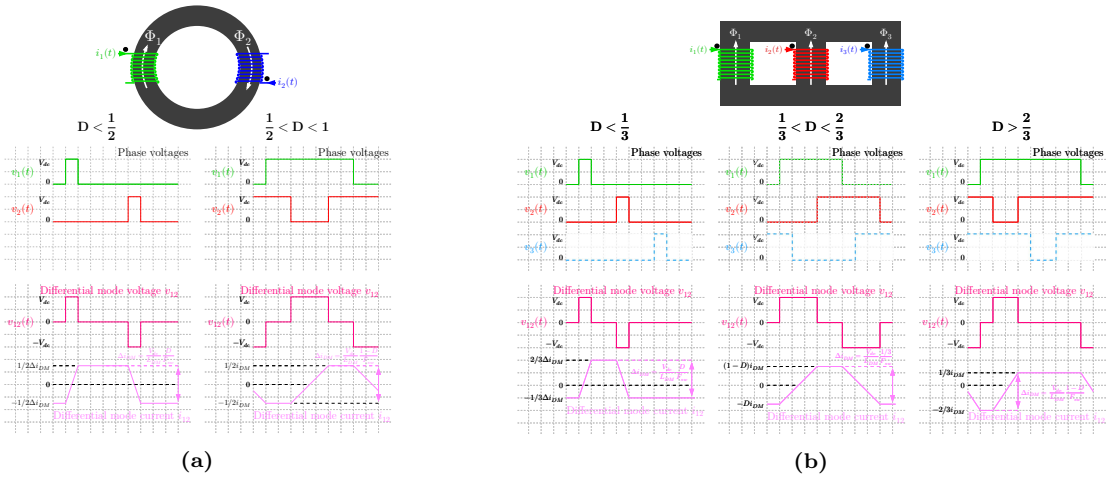


Figure 2.6: (a) Two channel DM-choke. (b) Three channel DM-choke

$$\begin{cases} m = floor(N\,D) \\ \xi = \dfrac{N}{D(1-D)}\left(D - \dfrac{m}{N}\right)\left(\dfrac{1+m}{N} - D\right) \\ F_{sw} = V_{dc}\dfrac{\xi}{N}\dfrac{D(1-D)}{\Delta i_o L_c} \end{cases} \tag{2.2}$$

In Eq. (2.2) the needed switching frequency in order to comply with the ripple current requirement Δi_o as a function of number of channels (N) and every other parameter is explained [44]. Once the switching frequency is selected, the differential mode choke (DM) indicated with L_M in Fig. 2.5 is designed. Note how L_M refers to the self inductance of a single winding. The DM-choke is used for limiting the circulating current between different phases. A small differential mode current allows for reduction of conduction losses in each half-bridge [45,46] and the amplitude of said current can be made smaller the bigger the L_M value is. Big DM-choke likely means that the volume and losses would become important, hence an optimal configuration can be found [47]. Fig. 2.6a and Fig. 2.6b represent the circulating currents in the DM-chokes for the two and three phase scenario, which are the topologies studied in this work. The DM-currents peak-to-peak amplitudes (named Δi_{DM}) is a function of different system and circuit parameters such as DC-link voltage V_{dc}, duty cycle D, switching frequency F_{sw} and DM-inductance L_{DM}. The differential mode inductance values can be calculated as in Eq. (2.3)

$$\begin{aligned} L_{DM\_2ph} &= 2L_M \text{ two channel} \\ L_{DM\_3ph} &= \frac{3}{2}L_M \text{ three channel} \end{aligned} \tag{2.3}$$

The peak-to-peak amplitude of the circulating currents, also shown in Fig. 2.6, is computed as in Eqs. (2.4) and (2.5).

$$\text{2-channel} \begin{cases} \Delta i_{DM} = \dfrac{V_{dc}}{L_{DM}}\dfrac{D}{F_{sw}}, \text{ for } D < \dfrac{1}{2} \\ \Delta i_{DM} = \dfrac{V_{dc}}{L_{DM}}\dfrac{1-D}{F_{sw}}, \text{ for } D > \dfrac{1}{2} \end{cases} \tag{2.4}$$

$$\text{3-channel} \begin{cases} \Delta i_{DM} = \dfrac{V_{dc}}{L_{DM}} \dfrac{D}{F_{sw}}, \text{ for } D < \dfrac{1}{3} \\ \Delta i_{DM} = \dfrac{V_{dc}}{L_{DM}} \dfrac{1/3}{F_{sw}}, \text{ for } \dfrac{1}{3} < D < \dfrac{2}{3} \\ \Delta i_{DM} = \dfrac{V_{dc}}{L_{DM}} \dfrac{1-D}{F_{sw}}, \text{ for } D > \dfrac{2}{3} \end{cases} \tag{2.5}$$

At this point in order to limit the circulating current peak-to-peak within a threshold value $\overline{\Delta i_{DM}}$, we need to design the DM-choke following the equations just now proven.
Fig. 2.7 represents the current on a fuel-cell stack during a 500 μs cycle when operating in electrolysis mode. Before the 100 μs mark no switching events happen hence the current fed to the fuel-cell stack is zero. At 100 μs the rise-time event happen and the current quickly goes to 50 A. In this specific case, the components have been designed in order to have $t_\Delta = 10\ \mu s$. The current is controlled to its steady-state value for about $\approx 390\ \mu s$ - in the rightmost zoomed window it is possible to see the switching content which, due to the accurate F_{sw} design, is contained within $\pm 5\ A$ - and finally goes back down to 0 at about 495 μs. In this work the two and three channel cases are studied. Note that in this section only the two-channel is shown for simplicity but the other cases will be thoroughly analysed in the following sections.

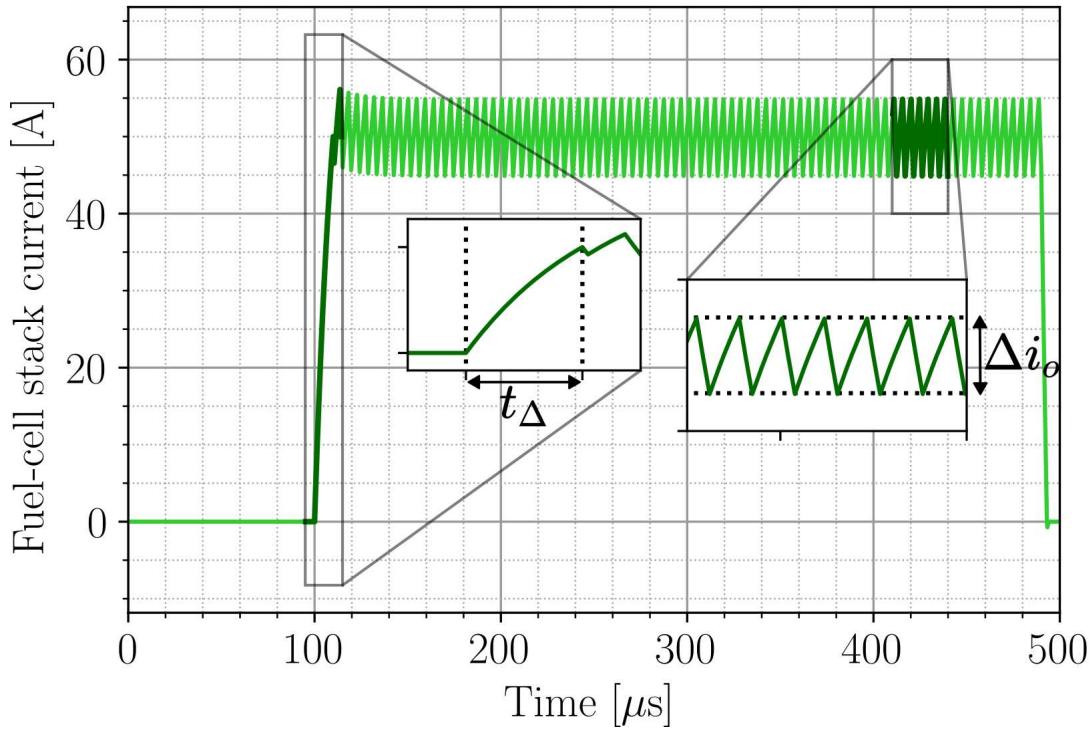


Figure 2.7: Output current simulation in electrolysis mode. Since the two SOFC stacks are series connected, it is expected to measure the same waveform here displayed on both stacks (i.e. both i_1 and i_2).

2.2.2 Three-Level Four-Switch Buck-Boost

The three-level four-switch buck-boost (3L-FSBB), shown in Fig. 2.8, allows to achieve both step-up and step-down voltage conversion in both directions [48]. The leftmost switches compose the buck stage while the rightmost ones act as boost. The combination between duty-cycles of these stages allows to achieve all possible voltage ratios. Often, another degree of freedom

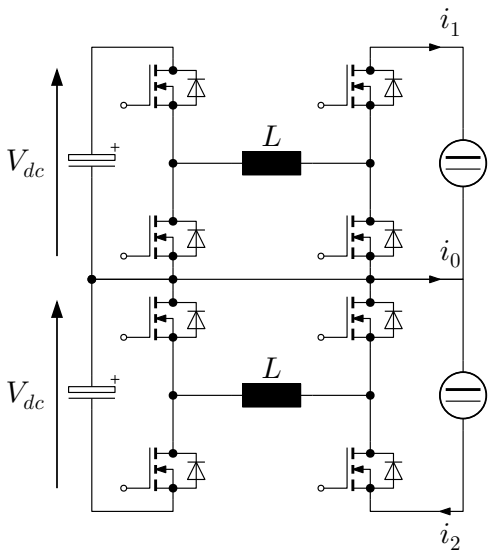


Figure 2.8: Schematic view of three-level FSBB

is added in the form of phase-shift between the two bridges allowing to achieve ZVS. This modulation is commonly known as Quadrangle Current Modulation (QCM) [49, 50]. However, in this application, we cannot use the converter as previously described when operated in electrolysis mode since the QCM modulation would not allow to produce a square-wave current on the load. The operating strategy for this converter consist into using the buck stage as a current controlled converter that sources 50 A continuously while the second stage devices are used as means of connecting or bypassing the SOFC stack.

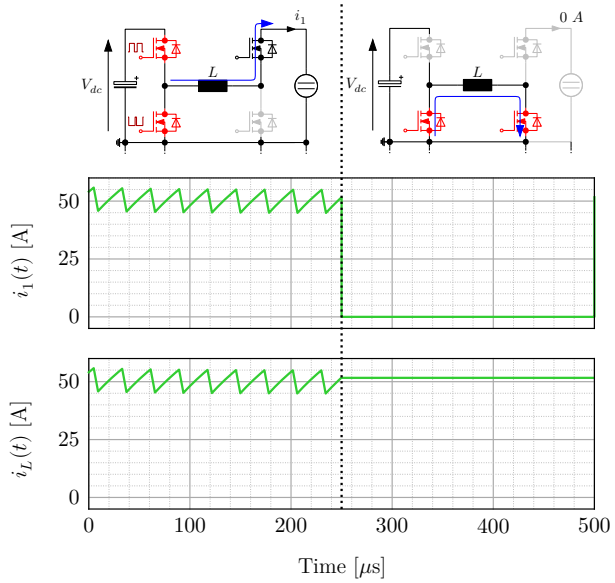


Figure 2.9: FSBB waveform operating modes during electrolysis operation

As illustrated in Fig. 2.9 during the first 250 μs the devices composing the buck stage (red) are switching in order to produce the desired current set-point whereas in the second stage the high-side is turned on while the low-side is off. This allows for the current to flow through the load (SOFC). In the second part of the waveform (after the 250 μs mark) the low-sides of both stages (first and second) are turned on in order to allow for the current to circulate while bypassing the SOFC. These two phases are continuously cycled one after the other in order to obtain the required load current form factor.

Adopting this modulation technique allows to reach very high rise and fall transient times on the SOFC stack current. The rise/fall time only depends on the di/dt of the devices adopted on the secondary stage which for this application is around tens of Ampère per nanoseconds. The SOFC current ripple is defined by the inductor value and switching frequency, two degrees of freedom to be optimized.
Adopting this modulation technique allows to reach very high rise and fall transient times on the SOFC stack current. The rise/fall time only depends on the di/dt of the devices adopted on the secondary stage which for this application is around tens of Ampère per nanoseconds. The SOFC current ripple is defined by the inductor value and switching frequency, two degrees of freedom to be optimized, as illustrated in Eq. (2.6).

$$\Delta i_o = V_{dc} \frac{D(1-D)}{F_{sw} L} \tag{2.6}$$

2.2.3 Buck with active filter

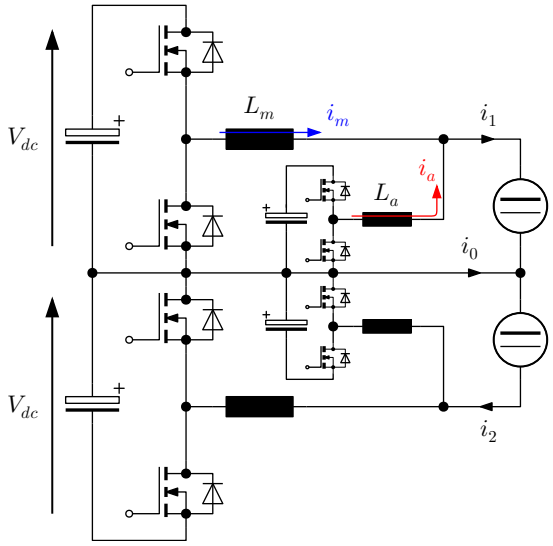


Figure 2.10: Buck with active filter schematic

The active filter topology (shown in Fig. 2.10) consists of two buck converters where the auxiliary one (red) aids the main DC-DC (blue) into achieving fast transient and actively cancelling the ripple component of the main bridge in order to produce fuel-cell stack load current with the target ripple requirement Δi_o. This concept is commonly used in single phase power factor correction circuits (PFC) [51, 52]. In the buck with active filter topology studied in this work the the two half-bridges are operated at different frequencies and the two inductors differ in value. Referring to Fig. 2.10, the goal is to design the inductors so that $L_m \gg L_a$ and $F_{sw\_m} \ll F_{sw\_a}$. The terms F_{sw_m} and F_{sw_a} are defined as the the switching frequency on the main (low-frequency) branch and switching frequency of the - so called - auxiliary (high-frequency) branch. This design constraint allows to achieve fast current transient due to L_a being small and paralleled with a much bigger inductor (L_m) during the SOFC current transition when operated in electrolysis.

The steady-state

Let's express the current on the main buck as $i_m(t) = I_m + \Delta i_m$, and the auxiliary converter current $i_a(t) = i_{am}(t) + \Delta i_a$, then the output current would be expressed as $i_o(t) = i_m(t) + i_a(t)$.

$$\begin{cases} i_m(t) = I_m + \Delta i_m(t) \\ i_a(t) = i_{am}(t) + \Delta i_a(t) \\ i_o(t) = i_m(t) + i_a(t) = I_o + \Delta i_o = \underbrace{I_m}_{I_o} + \underbrace{i_{am}(t) + \Delta i_m(t) + \Delta i_a(t)}_{\Delta i_o} \end{cases} \tag{2.7}$$

The term I_m refers to the DC current component provided by the main converter (i.e. the DC component of the load current), while $\Delta i_m(t)$ refers to the triangular AC ripple due the main inductance L_m and main switching frequency $F_{sw,m}$. Similarly, for the auxiliary branch, the quantity $\Delta i_a(t)$ is defined as the triangular ripple due to the auxiliary branch switching frequency $F_{sw,a}$. The auxiliary branch current (at steady state) contains no DC component hence it can be expressed as the sum of a low frequency content (that will be controlled so that it results proportional to $\Delta i_m(t)$) and the high-frequency triangular AC content due to its switching behaviour, $\Delta i_a(t)$.

$$i_a(t) = i_{am}(t) + \Delta i_a \begin{cases} i_{am}(t) & \text{low frequency content } @F_{sw,m} \\ \Delta i_a & \text{high frequency content } @F_{sw,a} \end{cases} \tag{2.8}$$

In the equation above, Fm is the switching frequency of the main bridge whereas Fa is the switching frequency of the active branch. We can define a proportionality between the ripple content of the main bridge and the LF content of the auxiliary bridge (which tries to counteract the main bridge ripple). Mathematically expressed as

$$i_{am}(t) = \gamma \Delta i_m \tag{2.9}$$

with $\gamma \in [-1, 0]$. The coefficient γ has been defined as a negative quantity which expresses how much of a cancelling effect the auxiliary bridge has on the main bridge, so that the ripple content on the output current can be kept within the constrain level. For $\gamma = -1$ we have that the auxiliary branch cancels the totality of the main branch ripple content.

$$\Delta i_o(t) = i_{am}(t) + \Delta i_m + \Delta i_a = (1 + \gamma)\Delta i_m + \Delta i_a \tag{2.10}$$

We can now derive Eq. (2.11)

$$I_o(t) = I_o + \Delta i_o(t) = I_m + (1 + \gamma)\Delta i_m + \Delta i_a \tag{2.11}$$

The trivial solution is obtained for and $\gamma = -1$, in which case the totality of the DC current is supplied by the main bridge and the auxiliary branch cancels out all of the low-frequency content, in which case Eq. (2.12) is obtained.
In order to comply with the load ripple current requirement the AC content of Eq. (2.11) must be kept below the target value $\overline{\Delta i_o}$.

$$I_o(t) = I_m + \Delta i_a \tag{2.12}$$

$$\Delta i_m + i_{ma}(t) + \Delta i_a = (1 + \gamma)\Delta i_m + \Delta i_a < \overline{\Delta i_o} \tag{2.13}$$

We can express the Δi_m and Δi_a analytically given the DC link voltage V_{dc}, the storage capacitor voltage V_{Ca} and the inductances L_m and L_a. An accurate selection of voltages, frequencies and inductance values allows for the total ripple current on the SOFC Δi_o to comply with the requirement.

$$\begin{aligned} \Delta i_m &= V_{dc} \frac{D_m(1 - D_m)}{F_{sw,m} L_m} \\ \Delta i_a &= V_{Ca} \frac{D_a(1 - D_a)}{F_{sw,a} L_a} \end{aligned} \tag{2.14}$$

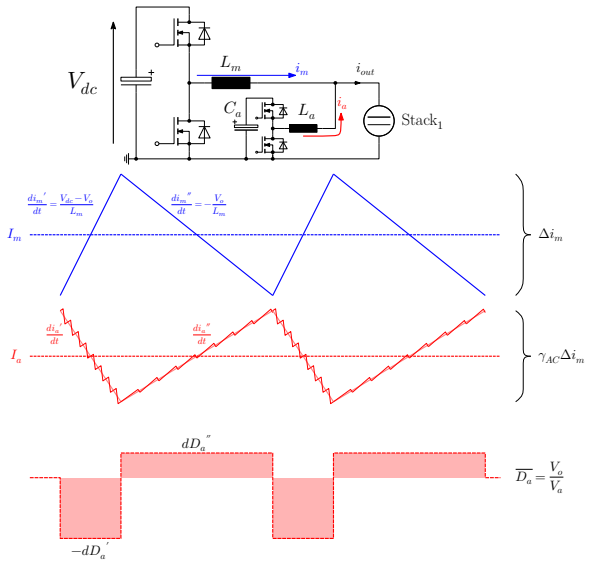


Figure 2.11: Active filter extended theory of operation

The main bridge supplies only DC current (and the "unwanted" ripple due to switching Δi_m) hence the duty cycle D_m is a constant value. On the other hand, the auxiliary half-bridge has to supply no DC content and a modulating component based on how much of the main half-bridge ripple it needs to cancel, given by the coefficient γ as previously explained. For this reason, the duty-cycle of the auxiliary bridge is not constant throughout a modulation cycle at F_m, as highlighted in Fig. 2.11. In Eq. (2.14), the term D_a is the average duty cycle of the auxiliary half-bridge during a modulation cycle and, from now on, it's going to be referred as such unless otherwise noted. By substituting (2.14) into (2.13), Eq. (2.15) is obtained.

$$(1+\gamma)V_{dc}\frac{D_m(1-D_m)}{F_{sw,m}L_m}+V_{Ca}\frac{D_a(1-D_a)}{F_{sw,a}L_a}=\overline{\Delta i_o} \tag{2.15}$$

The inductance values L_m and L_a are designed in order to comply with the rise-time requirement t_Δ. Solving Eq. (2.16) allows to design the inductances that allow to achieve the target rise-time. The system parameters are the series resistance of the SOFC R_s, the output current value at steady-state I_o, the DC-link voltage V_{dc}, the voltage of the floating auxiliary capacitor V_{ca} and the open circuit voltage of the fuel cell V_{ocv}. The term λ has been introduced and defines the ratio between main and auxiliary inductance, which is a degree of freedom to set. In the context of this work, the value λ will be optimized in order to design the configuration that allows for the smallest losses.

$$\begin{aligned} t_\Delta &= R_s\frac{L_aL_m}{L_a+L_m}\ln\left(\frac{1}{1-\frac{R_sI_o(L_mL_a)}{L_a(V_{ca}-V_{ocv})+L_m(V_{dc}-V_{ocv})}}\right) \\ L_m &= \lambda L_a \end{aligned} \tag{2.16}$$

In the trivial case in which the voltages of the DC-link and auxiliary capacitor are the same, the solution for computing the rise and fall time given the inductance values (and known the system parameters R_s, I_o, V_{dc} and V_{ocv} as previously explained) is shown in Eq. (2.17). By assuming the proportionality of between main and auxiliary inductances via parameter λ (to be computed as a goal of the multi-objective optimization), (2.17) can be used to compute L_m and L_a that satisfy the rise/fall time condition.

$$
\begin{aligned}
t_{rise} &= -\frac{L_m \| L_a}{R_s} \log\left(1 - \frac{I_o R_s}{V_{dc} - V_{ocv}}\right) \\
t_{fall} &= \frac{L_m \| L_a}{R_s} \log\left(1 + \frac{I_o R_s}{V_{ocv}}\right)
\end{aligned}
\tag{2.17}
$$

The duty-cycle change of the auxiliary bridge depends on how much, on average, the auxiliary branch is trying to deviate the current, as shown in Fig. 2.11. The 3rd panel shows how the duty cycle changes depending on the slope of the main current. The highlighted light-red areas are proportional to the Volt-seconds of the auxiliary inductor that, in a modulation period $T_m = 1/F_m$, must be null. Put into equations, Eq. (2.18) is obtained. Note that the average value of the duty-cycle in the active branch D_a must be so that $V_{ca} D_a = V_o$ (with V_o being the SOFC load voltage), hence the simplification on the second step of Eq. (2.18).

$$
\begin{aligned}
\frac{di_a{}'}{dt} &= \frac{V_a\,(D_a - dD_a{}') - V_o}{L_a} = -dD_a{}'\frac{V_a}{L_a} \\
\frac{di_a{}''}{dt} &= \frac{V_a\,(D_a + dD_a{}'') - V_o}{L_a} = dD_a{}''\frac{V_a}{L_a}
\end{aligned}
\tag{2.18}
$$

As previously explained a relation between the main and auxiliary bridge LF content is defined via coefficient γ (i.e. the cancelling effect of the auxiliary bridge) whereas in Eq. (2.16) the ratio between the inductors is defined via parameter λ. Rearranging Eq. (2.18) allows to obtain the relations illustrated in Eq. (2.19) where the duty-cycle variation of the auxiliary bridge during positive and negative di/dt generated by the main switching are made explicit as a function of system parameters (V_{dc}, V_{ca}, V_o) and user defined variables in the form of inductance ratio λ and cancelling effect γ.

$$
\left.
\begin{aligned}
\tfrac{di_a{}'}{dt} &= \gamma \tfrac{di_m{}'}{dt} \\
\tfrac{di_a{}''}{dt} &= \gamma \tfrac{di_m{}''}{dt}
\end{aligned}
\right\} \Rightarrow
\begin{cases}
-dD_a{}' V_{ca} = \dfrac{\gamma}{\lambda}\,(V_{dc} - V_o) \\
\\
dD_a{}'' V_{ca} = -\dfrac{\gamma}{\lambda} V_o
\end{cases}
\tag{2.19}
$$

It is important to keep these equations in mind if a limitation on the maximum variation of the auxiliary duty-cycle must be imposed, i.e. $D_a - dD_a{}' > D_{a,min}$ and $D_a + dD_a{}'' < D_{a,max}$. These two conditions will give an upper and lower bound to the ratio γ/λ, that can be found as in Eq. (2.20)

$$
\begin{cases}
\dfrac{\gamma}{\lambda} > (D_{a,min} - D_a)\dfrac{V_{ca}}{V_{dc} - V_o} \\
\\
\dfrac{\gamma}{\lambda} > (D_a - D_{a,max})\dfrac{V_{ca}}{V_o}
\end{cases}
\tag{2.20}
$$

We will now analyse how to setup the switching frequencies (namely $F_{sw,m}$ and $F_{sw,a}$) for the main and auxiliary bridges. By studying Eq. (2.15) it is possible to see how the main switching frequency cannot be smaller then a certain value

$$
F_{sw,m} > (1 + \gamma) V_{dc} \frac{D_m(1 - D_m)}{L_m \Delta i_o}
\tag{2.21}
$$

If the relation in Eq. (2.21) is not respected, Eq. (2.15) would mathematically return a negative value for $F_{sw,a}$. Of course γ and L_m must be carefully selected. As for L_m, its value follows the explanation given before for achieving the rise-time constraint. On the other end, the cancelling effect γ is a parameter that must be optimized. The more cancelling effect on the auxiliary bridge (i.e. the closer γ gets to -1) the more the main frequency lower bound is pushed towards 0. This means that, in the specific case of selecting $\gamma = -1$, an arbitrary lower bound on the main frequency must be defined anyway.

Now let's imagine a position where all the free parameters are set (i.e. γ, λ, $F_{sw,m}$, inductance values and voltages). By using Eq. (2.15) the auxiliary frequency that allows to achieve the ripple requirement can be computed as

$$F_{sw,a} = V_{ca} \frac{D_a(1-D_a)}{L_a \left[\Delta i_o - (1+\gamma) V_{dc} \frac{D_m(1-D_m)}{\lambda L_a F_{sw,m}} \right]} \tag{2.22}$$

Note how for $\gamma = -1$ (perfect cancelling) the main bridge does not produce harmonic content that flows through the load, hence only the auxiliary half-bridge contributes to the ripple content on the load. Not only, but in this case, the frequency of the auxiliary bridge would be the smallest, hinting that the perfect cancellation technique is the most valuable in terms of semiconductor loss reduction.

Transient operation

The transient operation for the buck with active filter is explained in this section. Fig. 2.12 shows in the detail all the working phases. In the first phase when the load current is zero, the fast turn on capability of the active filter is needed hence the high-sides of both the main and auxiliary branches are turned-on (Fig. 2.12a) until t_1, which is the point defined such that $i_a(t_1)+i_m(t_1) = I_o{}^*$. According to the previous definitions and allowing $V_{dc} \approx V_{ca}$, the analytical solution for these two values is shown in Eq. (2.23).

$$\begin{aligned} i_a(t_1) &\approx \frac{\lambda}{1+\lambda} I_o \\ i_m(t_1) &\approx \frac{1}{1+\lambda} I_o \end{aligned} \tag{2.23}$$

Note how the $\approx$ operator is valid only in case of $V_{dc} \approx V_{ca}$. The equations would become much more complicated otherwise, and they'll be shown in the Appendix of this document. By looking at Eq. (2.23) we can see how increasing λ (which as defined before is the ratio between main and auxiliary branch inductances) creates a bigger difference between the current on the inductances once this preliminary phase is over. Since in this time window no device is switching, the only losses are due to conduction. If the selection for L_a and L_m has been done by solving Eq. (2.16), then this phase completes the rising transition from 0 A to I_o in $t_1 = t_\Delta$. Once the first phase is over and the output current has reached its set-point value I_o, we'll need to wait for the main inductor to be fully charged (i.e. to have reached an average current $\text{avg}\{I_m(t)\} = I_o$). In order to do so, the auxiliary converter has to track the slope of the main current in order to assure that, from the moment t_1 to t_2 as highlighted in Fig. 2.12b, the output current can be kept around the set-point value I_o. During this phase, the main converter does not switch yet since the inductor L_m is not fully charged. This means that the main half-bridge will not experience switching losses, rather only conduction losses (on the high-side device). In order for the auxiliary converter to track the slope of the main converter, it will have to reach a switching frequency suitable for the output ripple constraint, computed as

$$F_{sw,a} = V_{dc} \frac{D_a(1-D_a)}{\Delta i_o L_a} \tag{2.24}$$

Note also that the area under the red curve in the time window $t_0 \sim t_2$ in Fig. 2.12b is the charge that the auxiliary capacitor will need to supply. At this point we also have all the information available for fixing a constraint on the maximum capacitor voltage variation (i.e. 2% deviation during transient) and calculating its value.

$$C_{aux} = \frac{i_a(t_1) \left(t_\Delta + \frac{i_a(t_1) L_m}{V_{dc} - V_o} \right)}{2\, \Delta V_{ca}} \tag{2.25}$$

In Eq. (2.25) the second term inside the numerator bracket is the time needed for the main inductor to get totally charged, starting from initial condition $i_m(t_1)$ as explained for the first phase (Fig. 2.16a). This time also corresponds to the length of the second phase.

$$t_{12} = \frac{i_a(t_1)L_m}{V_{dc} - V_o} = \frac{\lambda^2}{1+\lambda}\frac{I_o L_a}{V_{dc} - V_o} \tag{2.26}$$

During this phase, the equivalent circuit of the system is modelled in Fig. 2.13a, where the auxiliary branch is modelled as a controlled voltage source impressing a voltage v_x on the auxiliary inductance. It is possible to compute the duty-cycle that the auxiliary bridge needs in order to track the linear ascend on the main inductor which was already (partially) calculated in Eq. (2.19).

$$\begin{aligned} &(i) \quad \frac{v_x - V_o}{L_a} = -\frac{V_{dc} - V_o}{L_m} \\ &(ii) \quad v_x = D_{a,12}V_{ca} = V_o - \frac{L_a}{L_m}(V_{dc} - V_o) \\ &(iii) \quad D_{a,12} = D_{a,ss} - \frac{1}{\lambda}\frac{V_{dc} - V_o}{V_{ca}} \end{aligned} \tag{2.27}$$

Eq. (2.27) shows the duty-cycle of the auxiliary bridge during the phase t_{12} ($D_{a,12}$) where $D_{a,ss}$ is the average duty cycle in the steady-state phase (i.e. t_{23}), hence the ratio between output voltage and auxiliary capacitor voltage.
It is clear that this phase length (as well as the capacitor value) increases by increasing λ. This means that the bigger the ratio between main and auxiliary inductances, the bigger the duration of phase-2 and the bigger the auxiliary capacitor. This is an inconvenient finding since, during phase-2, the current on the auxiliary half-bridge will be relatively high (for a better insight, check Fig. 2.12c to visualize the difference between the average current on phase t_{12} and the current during steady-state, i.e. phase t_2+) but the switching frequency will be high too. This will cause a lot switching stress on the auxiliary half-bridge.
The descending phase (i.e. when going from full current to 0 current) is very similar to what happens in Fig. 2.12b. The auxiliary and main inductors start from an initial condition of $i_a(0) = 0$ and $i_m(0) = I_o$ (note that the 0 inside the brackets is simply used to indicate the initial condition for the currents when the falling transition starts). Closing the low-sides of both main and auxiliary half-bridges allow for a fast turn-off transient for the output current which, when completed, will leave the auxiliary inductor with a big negative current and the main inductor with a current slightly smaller then its initial condition. The auxiliary branch will then have to track the main branch in order to reach the next steady-state.
In Fig. 2.14 the illustration of all the phases just now described is given. Also in this case the current in the auxiliary inductor reaches very high (negative) values, hence the auxiliary half-bridge will have to sustain relatively high switching losses during this transition phase. Similarly to Eq. (2.26), it is possible to compute the duration of the falling-transient phase t_{45}, as in Eq. (2.28).

$$\begin{aligned} t_{45} &= \frac{\lambda^2}{1+\lambda}\frac{L_a}{V_{ocv}} \\ i_m(t_4) &\approx \frac{\lambda}{1+\lambda} I_o \end{aligned} \tag{2.28}$$

Note how the formula used here for estimating the current on the main inductor at t_4 ($i_m(t_4)$) is correct only under the specific assumption of $V_{dc} \approx V_{ca}$. During the time window t_{45} the output voltage is fixed at the open circuit value, hence the voltage value that the load offers when no current is being drawn ($V_{ocv} = V_{load}(0\ A)$) The equivalent circuit is the one shown in

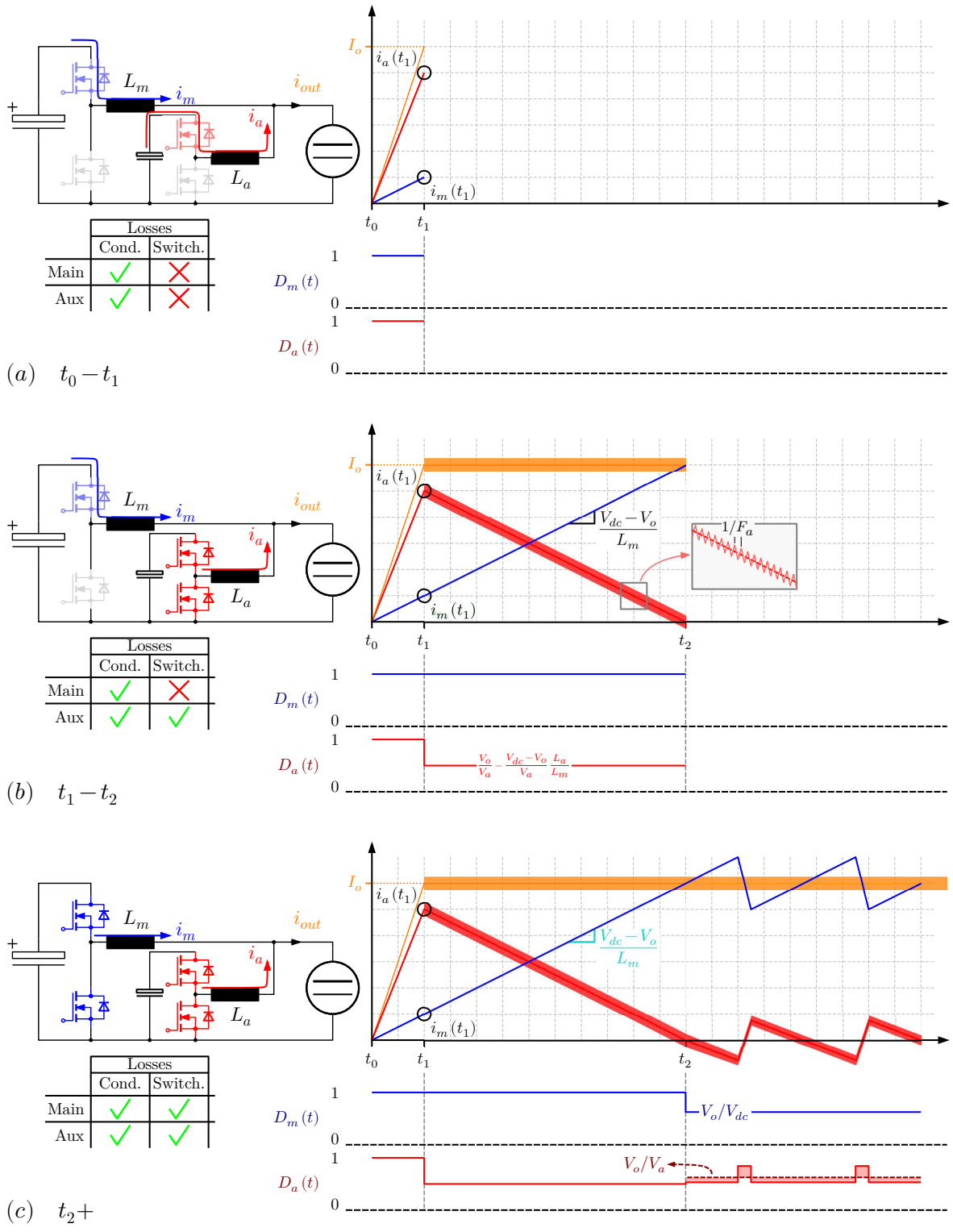
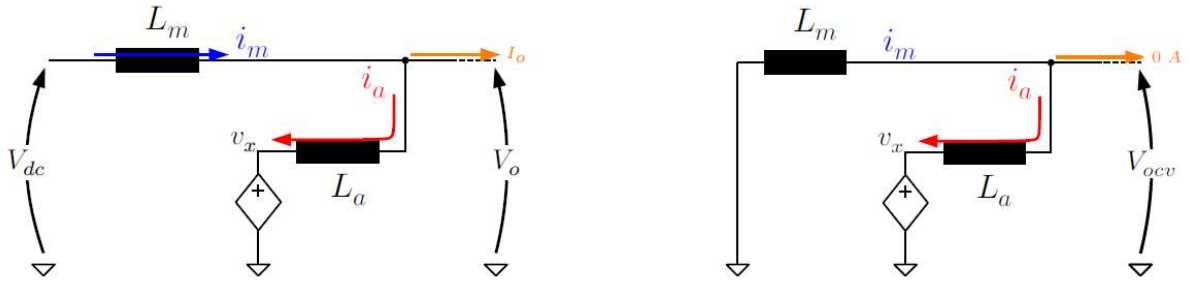


Figure 2.12: Active filter time diagrams



(a) Equivalent circuit during phase t_{12}

(b) Equivalent circuit during phase t_{45}

Figure 2.13: Equivalent circuits during rise and fall transients (i.e. t_{12} and t_{45})

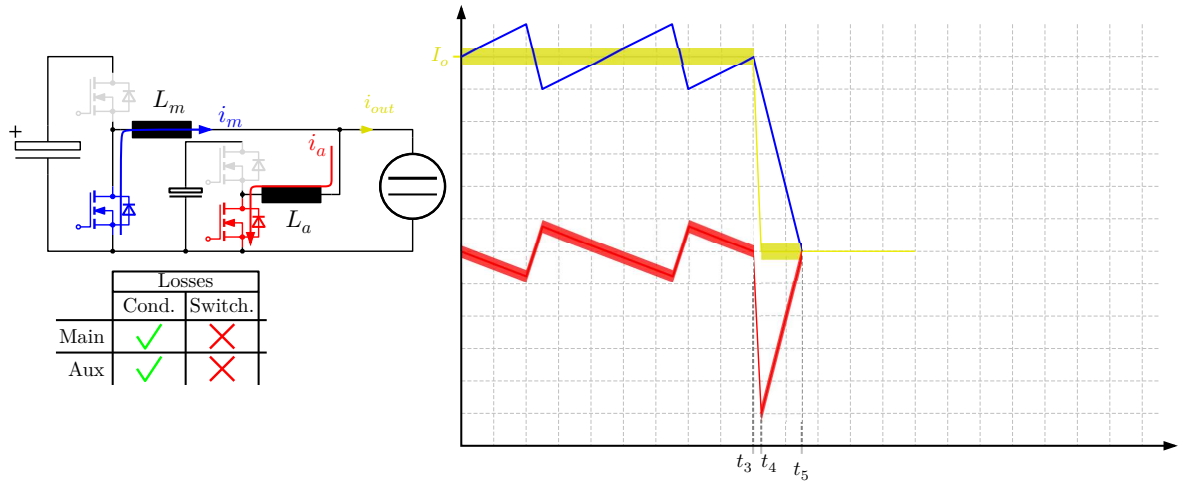


Figure 2.14: Falling transient. In t_3 the low-sides are turned on to allow the fast falling transient until t_4, moment when the load current has reached the zero point. From t_4 to t_5 the auxiliary bridge tracks the negative slope for the current in the main inductor, until the main inductor is fully discharged. After t_5 all switches are turned off and the load current will remain 0.

Fig. 2.13b, hence it is possible to compute the duty-cycle of the auxiliary branch during this phase, Eq. (2.29).

$$\begin{aligned} \frac{V_{ocv}}{L_m} &= \frac{v_x - V_{ocv}}{L_a} \\ v_x &= V_{ocv}\left(1 + \frac{L_a}{L_m}\right) \Rightarrow D_{a,45} = \frac{v_x}{V_{ca}} \\ D_{a,45} &= \frac{V_{ocv}}{V_{ca}}\left(1 + \frac{1}{\lambda}\right) \end{aligned} \tag{2.29}$$

The equations for $D_{a,12}$ and $D_{a,45}$ can be used to compute the feed-forward terms in the current tracking control loop of the auxiliary converter. During the phase t_{12}, the auxiliary branch must counteract the positive slope increase of the main inductor current, named $di_m{}'/dt$, which is computed as

$$\frac{di_m{}'}{dt} = \frac{V_{dc} - V_o}{L_m} \tag{2.30}$$

In order to keep the current on the load constant, the auxiliary branch will produce an *average* $di_a{}'/dt$ which opposes the one impressed by the main inductor

$$\begin{aligned} \frac{di_a{}'}{dt} &= -\frac{di_m{}'}{dt} \\ \frac{v_x - V_o}{L_a} &= -\frac{V_{dc} - V_o}{L_m} \end{aligned} \tag{2.31}$$

In the previous equation, the equality of the di/dt between main and auxiliary branch is imposed and their values are computed based on the respective V/L values. The term v_x refers to the voltage on the switching node of the auxiliary branch, which can be written as $v_x = D_a V_{ca}$.

$$\begin{aligned} v_x = V_{ca} D_{a,12} &= V_o - (V_{dc} - V_o)\frac{L_a}{L_m} \\ D_{a,12} &= \underbrace{\frac{V_o}{V_{ca}}}_{D_{a,ss}} - \underbrace{\frac{V_{dc} - V_o}{V_{ca}}\frac{1}{\lambda}}_{dD_{a,12}} \end{aligned} \tag{2.32}$$

Finally, in Eq. (2.32), the duty cycle $D_{a,12}$ needed in the phase t_{12} is calculated, which is the sum between the average duty ratio in steady-state $D_{a,ss}$ (i.e. ratio between output and capacitor voltages) and a term that takes into account the di/dt ($dD_{a,12}$). The latter, as previously specified, is used as a feed-forward quantity.

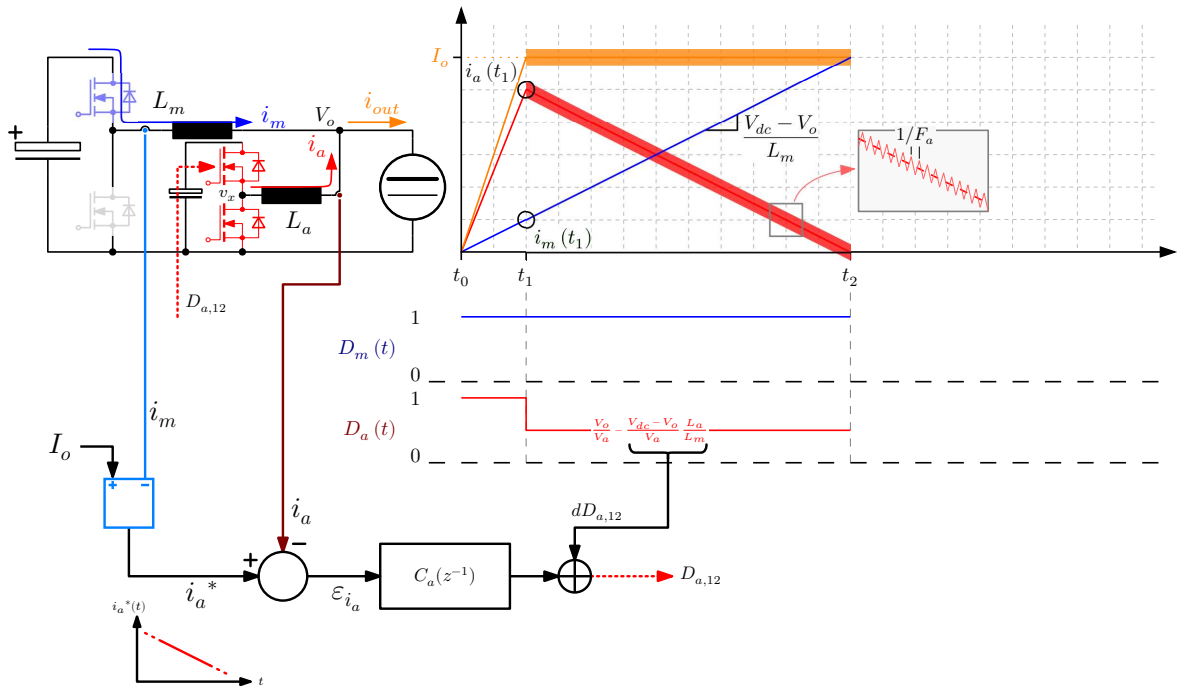


Figure 2.15: Control loop during main inductor charge phase (t_{12})

The control loop during phase t_{12} is depicted in Fig. 2.15. It illustrates how the reference $i_a{}^*$ is generated based on the measurement of the current on the main inductor. In this phase, the reference current $i_a{}^*$ takes the form of a ramp, as depicted in the image. By implementing the auxiliary current controller $C_a\left(z^{-1}\right)$ solely as a PI regulator, achieving zero error ($\varepsilon_{i_a} = 0$) during this phase would be unattainable. The inclusion of the feed-forward term $dD_{a,12}$, however, aids in achieving zero-error set-point tracking during linear transitions. Similar considerations apply to the main inductor discharge phase transition, t_{45}.

In Fig. 2.16 a simulation of the circuit described is shown. The blue trace shows the current measured on the main inductor; the ripple content lies in the lower frequency side of the spectrum, its amplitude exceeds the specified maximum limit of Δi_o. The red trace shows the

current on the auxiliary inductor that cancels out the LF ripple generated by the main bridge. The yellow trace shows the sum between the two currents, which is the one flowing in the SOFC stack during electrolysis operation.

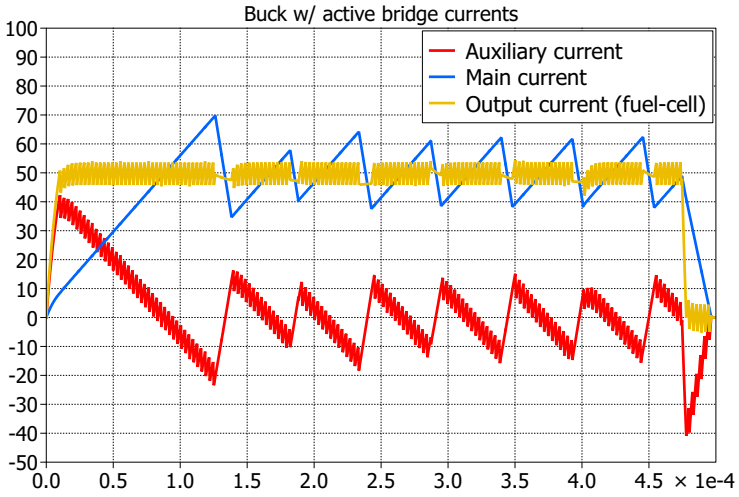


Figure 2.16: Buck with active filter circuit simulation

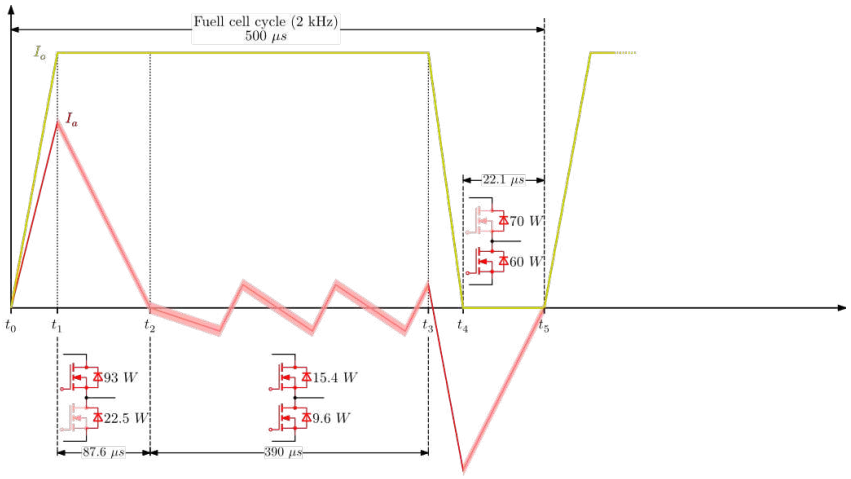


Figure 2.17: Loss profile of auxiliary half-bridge during the 500 μs fuel-cell cycle. Note that when, in the image, the diode is conducting (lower diode in t_{12} and higher diode in t_{45}) it means that that particular device is used as a synchronous-diode, hence switching losses can be neglected. The switching frequency of the auxiliary branch is 225 kHz and the device characterizing said leg is the C3M0065090J.

In Fig. 2.17 the simulation result of the loss profile in the auxiliary branch only (during a 500 μs fuel-cell cycle) is illustrated. Note that the image is representative only, while the numbers reported in the losses are simulated via PLECS. The red waveform represents the current absorbed/injected to cancel the main inductor ripple, whereas the yellow waveform shows the load (fuel-cell) current. In each phase the losses are distributed differently between high-side and low-side of the auxiliary bridge depending on the sign of the auxiliary current. In each phase the semiconductor losses are differently distributed, as explained in the active filter time diagrams Fig. 2.12a-c. The total semiconductor losses of the auxiliary leg, averaged in a fuel-cell cycle, are computed as:

$$\overline{P_{loss}} = \frac{1}{T_{FC}} \sum_{i=1}^{5} P_i \, t_i = \frac{P_{01}\, t_{01} + P_{12}\, t_{12} + P_{23}\, t_{23} + P_{34}\, t_{34} + P_{45}\, t_{45}}{T_{FC}}$$

As expected the losses during periods t_{12} and t_{45} are very high since the auxiliary bridge needs to cancel out a big current component to keep the fuel-cell current steady as explained beforehand. As illustrated in the previous part of this and in the steady-state operation subsections, the parameter λ (defined as the ratio between main and auxiliary inductances) plays a role in the duration of periods t_{12} (see Eq. (2.26)) and t_{45} (see Eq. (2.28)) which ultimately affects the losses. If λ is big, the main inductance is big meaning that the time to charge and discharge it is very long as well ($\propto \lambda^2/(1+\lambda)$). In this case, the auxiliary losses are relevant since the transient phases last very long. On the other hand, having smaller λ implicates the main inductance to be smaller, hence the ripple on the main inductor (and on the main bridge) becomes important and a big source of losses, whereas the transient phase t_{12} and t_{45} are smaller. This leads to believe that, once all variables are fixed and the only parameter left to sweep is λ, there is a optimal configuration that minimizes the semiconductor losses as displayed in Fig. 2.18.

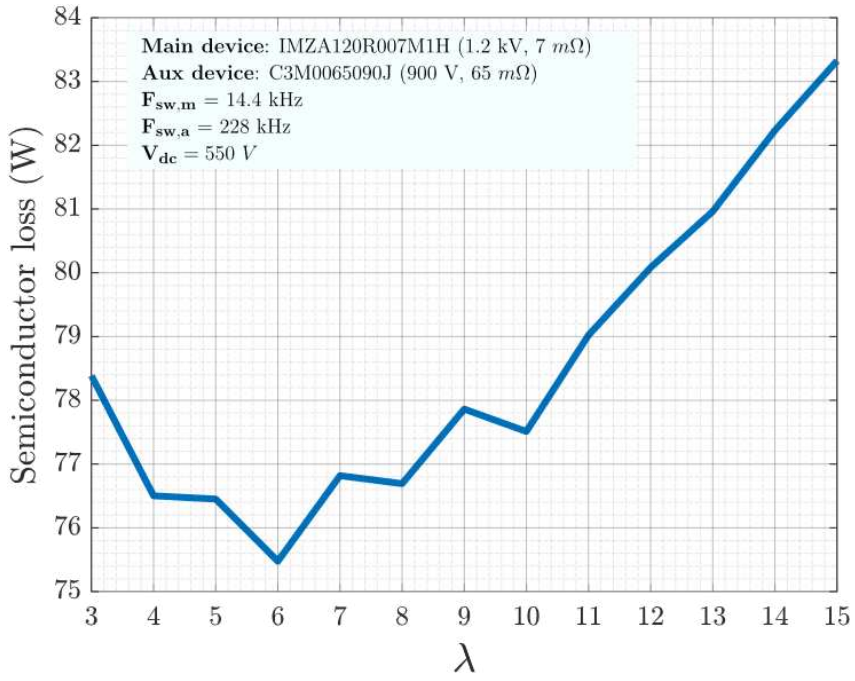


Figure 2.18: Semiconductor losses as a function of λ. All variables are fixed (as per legend displayed) and the minima is found when $\lambda = 6$.

2.3 Multi-objective optimization for power converters

For the purpose of comparing the proposed topologies a multi-objective design optimization procedure is run for all converters with the goal of producing a Pareto-analysis highlighting efficiency and weight (ρ-η-analysis) of the proposed solutions [53]. In this work the variable space is composed by the topology (explained in the previous section), DC-link voltage V_{dc}, semiconductor devices, passive components design, modulation scheme, control strategy. Each and every one of these degrees of freedom can be swept in a reasonable range in order to analyse a wide design space for each converter proposed in Section 2.2.

The optimization procedure to obtain the Pareto-analysis is illustrated in Fig. 2.19 and has been briefly explained for the specific topologies discussed. Three degrees of freedom (DoF) are swept between two boundaries in order to analyse a wide design space for the proposed

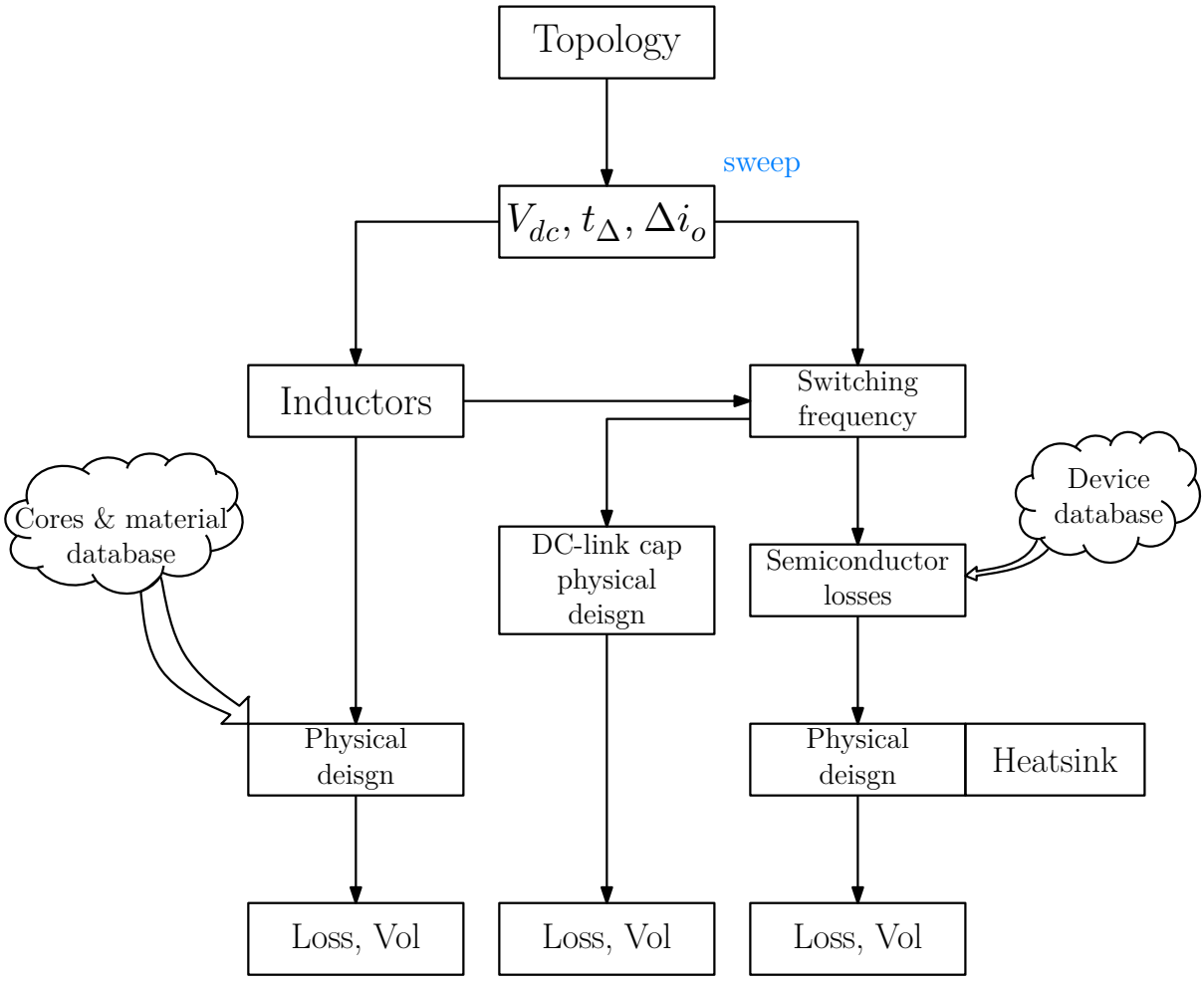


Figure 2.19: Optimization procedure

solutions. These DoF are the DC-link voltage V_{dc}, the transient time to reach steady-state t_Δ and the output current ripple Δi_o. These three variables allow to compute the inductance values and converter switching frequency. Once this information is known, the semiconductor losses are evaluated by sweeping different devices contained in a device database.

Once the required inductor value and switching frequency are known, the physical design allows to estimate the inductor losses and its volume/weight. Different configurations are tried by selecting cores and materials from a magnetic database.

Finally, the last element to be considered is the DC-link capacitor bank design whose design value is a function of the maximum allowed input voltage ripple.

2.3.1 Degrees of freedom sweeping

The swept variables are the DC-link voltage V_{dc}, the required rise time t_Δ and the ripple current on the SOFC, Δi_o. The bus voltage is allowed to be swept in a range of $500 \sim 750$ V. The reason why we decided to explore different DC bus voltage configurations rather then choosing the smallest value (to reduce switching loss stress) is due to the analysis on the interleaved topologies (two and three channels) and the possibility to exploit the interleaving. The project specifications dictate that the maximum transient time, denoted as t_Δ, and the current ripple, represented as Δi_o, must not exceed 10 μs and $\pm 10\%$ respectively. For this reason the decision to sweep them in the respective ranges of $2 \sim 10$ μs and $\pm 1 \sim \pm 5$ A has been taken.

2.3.2 Semiconductor devices

Given the application voltages and the voltage range exploration just described, devices with breakdown of 900 V and 1.2 kV are considered to be the best suited for this application. Due to the nature of the problem and relatively high voltages, the technology selected for the devices is Silicon Carbide (SiC).
A multitude of SiC devices from different manufacturers (such as Infineon, Cree, RHOM Semiconductor) have been used to fill a *device database* which is going to be used to test different switches for every possible configuration in order to estimate the semiconductor losses.

Table 2.1: SiC devices

Manufacturer	**Device**	$\mathbf{V_{BD}}$	$\mathbf{R_{ds\_on}}$
Cree	C3M0016120D	1.2 kV	16 $m\Omega$
	C3M0021120K	1.2 kV	21 $m\Omega$
	C3M0032120J1	1.2 kV	32 $m\Omega$
	C3M0040120J1	1.2 kV	40 $m\Omega$
	C3M0030090K	900 V	30 $m\Omega$
	C3M0120090J	900 V	120 $m\Omega$
	C3M0065090J	900 V	65 $m\Omega$
Infineon	IMZA120R007M1H	1.2 kV	7 $m\Omega$
	IMZA120R014M1H	1.2 kV	14 $m\Omega$
	IMZA120R020M1H	1.2 kV	20 $m\Omega$
ROHM Semi	SCT4018KW7	1.2 kV	18 $m\Omega$

In Tab. 2.1, we present a comprehensive list of devices selected for the application and included in the database. Various on-resistance devices were tested, as lower values of R_{ds_on} typically correspond to higher switching energy and smaller conduction losses. The opposite is true with higher R_{ds_on} switches.
The semiconductor loss can be divided in conduction losses, switching loss (turn-on and turn-off) and dead-time losses. The ohmic component can be easily computed as $P_\Omega = R_{ds\_on} {I_{rms}}^2$ where the rms value of the current depends on the topology and operating condition.
All the topologies here discussed are hard switched hence the switching losses must be considered alongside the conduction losses. In order to estimate the switching loss, the turn-on and turn-off energy as a function of voltage, current and temperature for the devices taken into consideration must be known.

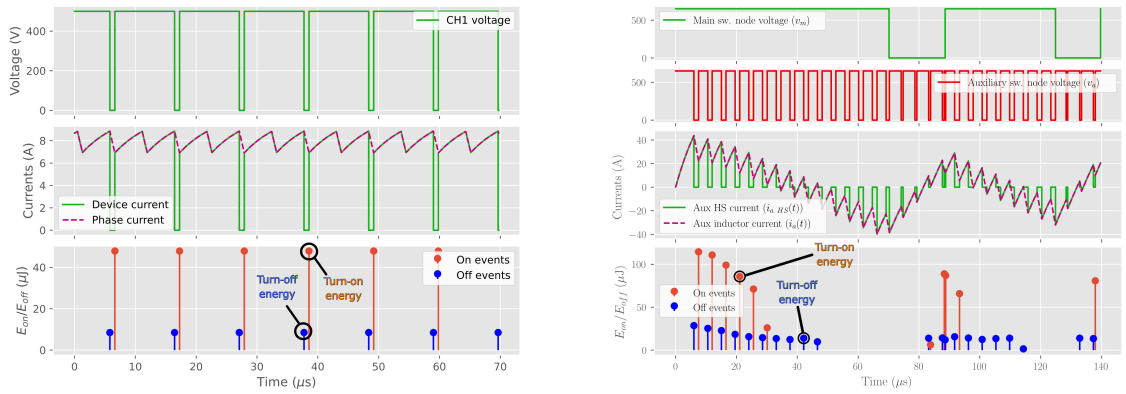
$$\begin{aligned} E_{on} &= \int_{T_{on}} v_{ds}(t) i_{ds}(t) dt \\ E_{off} &= \int_{T_{off}} v_{ds}(t) i_{ds}(t) dt \end{aligned} \tag{2.33}$$

In the previous equation the integral intervals T_{on} and T_{off} refer to the time intervals in which there's an overlapping on the drain-to-source current and voltage waveforms due to a switching event. The time evolution of $v_{ds}(t)$ and $i_{ds}(t)$ depend on the initial condition V_{ds} and I_{ds} at the start of the switching event and on the junction temperature T_j. If turn-on and turn-off currents and voltages are periodically repeating with period $1/F_{sw}$, the power loss can be computed.

$$P_{sw} = \left[E_{on}(V_{ds}, I_{ds}, T_j) + E_{off}(V_{ds}, I_{ds}, T_j) \right] F_{sw} \tag{2.34}$$

The functions E_{on} and E_{off} depend on the type of device and its parameters. There are different approaches used in literature to estimate these quantities, from pure model based

analytical calculation [54] to fitting data into a mathematical model [55]. In this work, the look-up tables (LUTs) implemented in PLECS are used inside a MATLAB script for estimating the losses more rapidly. The LUT accepts three inputs: switching voltage V_{ds}, switching current I_{ds} and junction temperature T_j. For simplicity, the junction temperature is fixed to the highest available record contained in the tables, since 2-D interpolation is much less computationally expansive then the 3-D counterpart.
Applying Eq. (2.34), as previously explained, for the estimation of semiconductor switching losses is straightforward in the case of repeating turn-on and turn-off currents. By looking at the example waveforms in Fig. 2.20a, the knowledge of turn-on and turn-off energy (which are function of voltage and current, easily predictable). Taken these energy levels on a switching period will give the switching losses of the device.



(a) **(b)**

Figure 2.20: (a) Two-channel buck waveforms and on/off energies. (b) Buck with active filter energy waveforms.

Fig. 2.20b shows a different scenario where it is not simply possible to estimate the switching losses by application of (2.34). The image represents a time frame simulation of the buck with active filter, where on the first panel the voltages on the switching nodes of the main (blue) and auxiliary half-bridge (red) respectively. In the second panel, the current on the auxiliary inductor (dashed blue line) is displayed alongside the current on the high-side and low-side of the auxiliary half-bridge (green and red respectively). The 3^{rd} panel shows turn-on and turn-off energies for the high-side device of the auxiliary bridge, and as it is possible to see the energy expenditure due to switching changes at every switching cycle, since the current varies with time. Finally the profile for on and off energy is shown in the 4^{th} waveform. Note also how no energy is lost when the current on the auxiliary inductor (dashed blue line on panel 2) goes negative, since in that case the high-side works as a synchronous device hence turning on at ZVS and off at ZCS. The computation of the switching loss can be done by assuming that each switching event can be represented as a Dirac-delta function. Let's then (arbitrarily) select an integration period T_m, while T_s is the switching frequency of the system. The total loss (in W) during said period, can be computed as

$$\begin{aligned} P &= \frac{1}{T_m}\sum_{k=1}^{N}\left(E_{on}(k)+E_{off}(k)\right) \\ E_{on}(k) &= E_{on}(V_{on}(k\,T_s), I_{on}(k\,T_s), T_j)\delta(t-k\,T_s) \end{aligned} \tag{2.35}$$

Eq. (2.35) explains how the switching energy assumes non-zero values only during switching instants (hence the product with the Dirac function at every $k\,T_s$ instant). By summing all the energy per switching event during the integration period T_m, we find the power loss due to switching.

The last element of losses is due to dead-time, when the diodes of the rectifying elements start conducting. In this case, the losses due to diode injection during dead-time are easily estimated

$$P_{dt} = V_f(I_f) I_f \frac{T_{dt}}{T_{sw}} \tag{2.36}$$

where V_f is the forward voltage drop of the SiC body diode as a function of the forward current, T_{dt} is the interlock duration and T_{sw} is the switching period.

2.3.3 Inductors design

The inductor design procedure used in this work is similarly adopted in [56], where different core shapes and dimensions are swept in order to have different configurations of weights and losses available to choose. The losses on the inductors are divided in copper losses (due to ohmic drop on the windings) and core losses. The first ones are easily computed as $P_{cu} = R_{wind} {I_{rms}}^2$ where R_{wind} is the total resistance of the winding.
The second source of losses lies in the ferrite core, caused by hysteresis and eddy currents resulting from high-frequency excitation. The volumetric loss density depends nonlinearly on the applied volt-seconds, frequency, and material properties. When the current excitation is sinusoidal, the core losses can be easily expressed using the Steinmetz equation $P_v = K_{fe}(F_{sw})^{\alpha}(\Delta B)^{\beta}$. The equation includes material coefficients (K_{fe}, α, and β provided by the manufacturer), the frequency of sinusoidal excitation (F_{sw}), and the maximum peak amplitude of flux-density variation (ΔB).
Due to the nature of the converters analysed in this work the assumption of sinusoidal current excitation (and consequently flux density) would yield wrong estimations. A multitude of different tools and simplified analytical solutions for these kind of applications have been developed throughout the years, such as the Modified Steinmetz Equation (MSE) [57], the Generalized Steinmetz Equation (GSE) [58], the Improved Generalized Steinmetz Equation (iGSE) [59], the Improved-Improved Generalized Steinmetz Equation (i^{2}GSE) [60]. Due to the current waveforms for the converters studied in this manuscript and given the hypotheses under which they operate (i.e. repetitive triangular ripple), the GSE have been used in the core loss estimation

$$\begin{aligned} P_v &= \frac{1}{T} \int_0^T k_1 \left| \frac{dB}{dt} \right|^{\alpha} |B(t)|^{\beta-\alpha} \, dt \\ k_1 &= \frac{K_{fe}}{(2\pi)^{\alpha-1} \int_0^{2\pi} |\cos(\theta)|^{\alpha} |\sin(\theta)|^{\beta-\alpha} \, d\theta} \end{aligned} \tag{2.37}$$

In Fig. 2.21 the optimization strategy for the magnetic components design is illustrated. The higher level optimization (see Fig. 2.19 for reference) returns as a result the inductor value needed for complying with the rise-time requirement (hereby called L_{target}) and the switching frequency for complying with the ripple requirement, as well as the current waveform (its peak, rms value and ripple amplitude). This information is used for the physical design of the inductor hence the number of turns, airgap (if needed) and finally allows for the estimation of losses and volume/weight. Different core shapes, size and materials are swept to obtain the same configuration as well as maximum allowable flux and current density.
The design strategy for inductors used as filters in various applications, such as the output inductor on a multichannel buck converter, auxiliary inductors on a buck converter with an active filter, or a filter inductor for a FSBB, follows a relatively straightforward procedure. First, we consider the physical configuration, including the core shape and material selection. This choice is crucial and is determined by factors like the loop illustrated in Fig. 2.21, which depicts the inductor optimization process.
Next, we establish the magnetic design variables, including the flux density (B) and current density (J). These variables are swept to ensure a comprehensive analysis of the operating

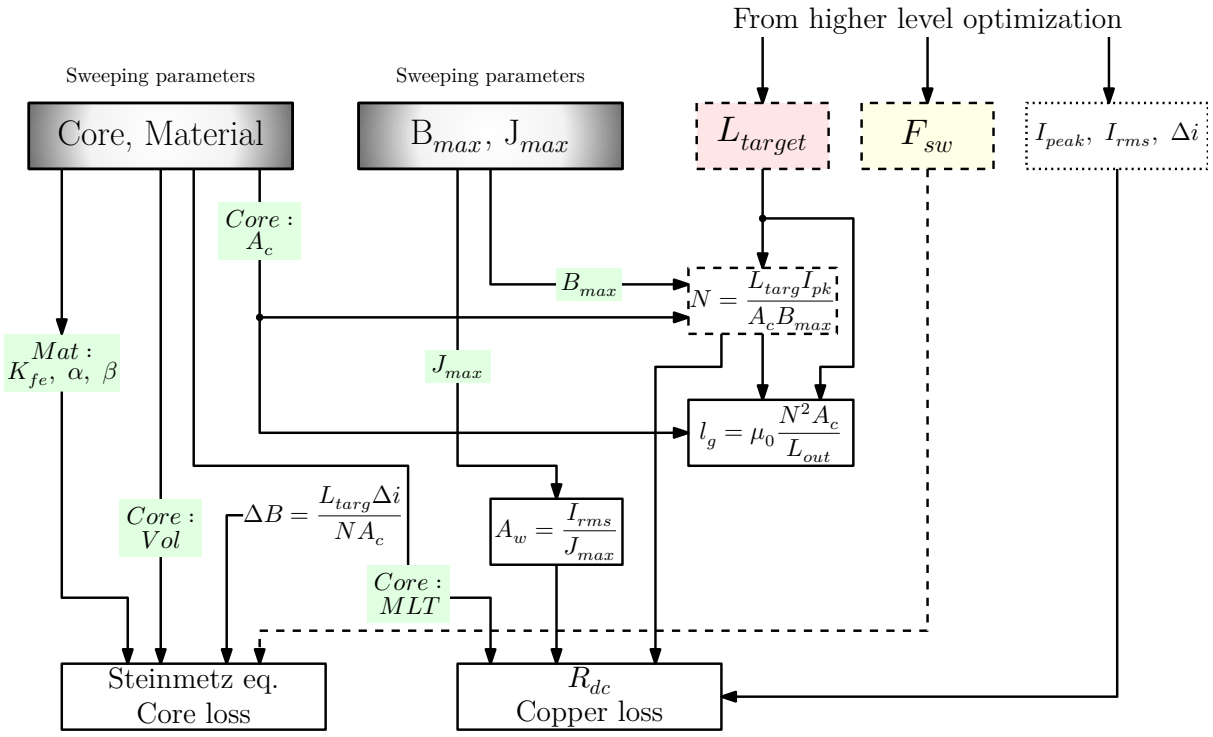


Figure 2.21: Inductor optimization strategy adopted for design of magnetic components

space. The current density value plays a significant role in determining the loss density in the windings, affecting factors such as winding resistance (R_{wind}). Meanwhile, the flux density defines the operating conditions of the inductor at a given current, and its variation (ΔB) directly impacts losses in the ferrite core.

Fig. 2.22 displays the BH loop for a material examined in this work, specifically 3F3 from Ferroxcube. This graph illustrates the relationship between the magnetic field (H) and flux density (B) while highlighting the saturation limit (B_{sat}). Notably, this saturation limit is highly dependent on temperature, varying from 350 mT at 100^oC to approximately 420 mT at 25^oC. Other variables, such as frequency and the type of ferrite, also play a role in determining B_{sat}. It's imperative to avoid magnetic saturation of the ferrite core because it leads to a decrease in the differential inductance ($l_{diff} = dB/dH$) compared to unsaturated operation. This, in turn, results in increased ripple current and raises the root mean square (rms) value of the inductor current, amplifying ΔB. Both these effects, on their own, contribute to higher core and copper losses. Additionally, core losses during saturated operation are more severe than during unsaturated operation. By analyzing suitable ferrite materials for this application, designing inductors that operate safely below the saturation limit sets an upper boundary for the allowable maximum flux density (B_{max}), typically set at 250 mT. Venturing beyond this value during the design process could lead to undesirable behaviour due to saturation.

In the case of DC inductor design, the flux density can be considered as the sum of two components: the first arises from the DC component of the current, while the second results from its ripple, creating a flux density ripple (ΔB), as explained earlier.

$$B(t) = B_{DC} + \Delta B = \frac{\Phi}{N\,A_e} = \frac{L_{targ}(I_{dc} + \Delta i)}{N\,A_e} \tag{2.38}$$

This equation allows us to calculate the minimum number of turns required to ensure that the flux density stays within the predetermined constraint, B_{max}. Here, A_e represents the equivalent core cross-sectional area, and I_{dc} and Δi denote the DC content and ripple current, respectively. For instance, in the context of designing the output inductor, these values might be

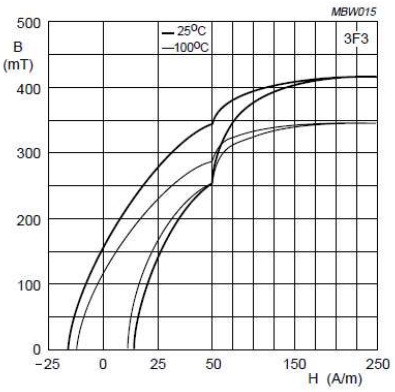
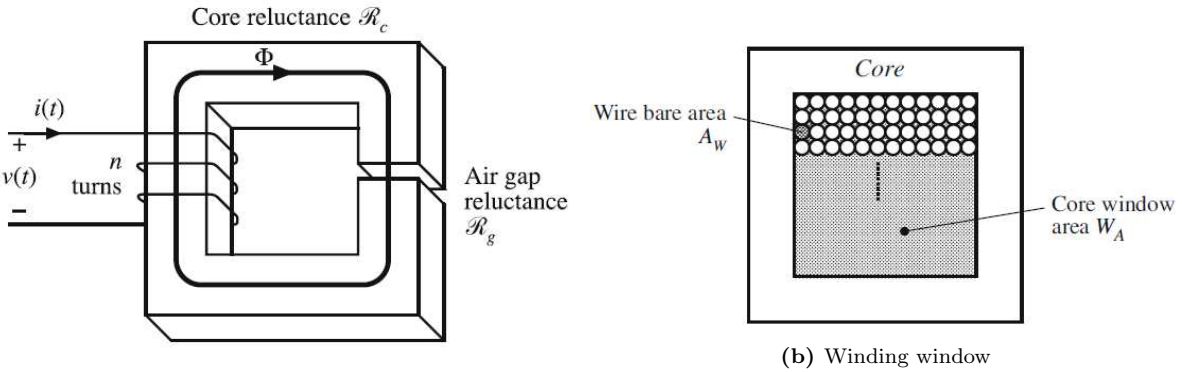


Figure 2.22: BH loop for 3F3 material from Ferroxcube [5]

50 A and 5 A, respectively. The ΔB component facilitates the immediate computation of core losses attributed to current ripple. If the current fluctuation is significantly smaller than the DC component, we can anticipate relatively small ferrite losses. For the purposes of this work, we assume a ratio between ripple and DC current content of 10%, resulting in $\Delta B_{max} \approx 23\ mT$ when $B_{max} = 250\ mT$ is considered.
At this stage, we must ensure that the number of turns (N) calculated earlier, based on the magnetic cross-sectional area (A_e) considered, guarantees that the inductance value reaches the target as required in the higher-level optimization. We do so by designing the airgap length.

$$l_g \approx \mu_0 \frac{N^2 A_e}{L_{targ}} \tag{2.39}$$

The $\approx$ operator indicates that said equation is correct if the airgap is sufficiently small and $\mu_r \gg 1$ (where μ_r is the relative permeability of the material under consideration).
Once this step is over, the wire design needs to be addressed. In Fig. 2.23b the total window area W_A and single wire bare (copper) area A_W are highlighted. We know that inside the winding area W_A we need to fit N turns, as computed before. We now define the *filling factor* K_u, also known as the ratio between the bare copper area and the maximum copper section that would be (theoretically) possible to fill, which is the winding section W_A.



(a) Cross section and airgap

(b) Winding window

Figure 2.23: Core dimensions

$$N A_w \leq K_u W_A \tag{2.40}$$

The filling factor is a design property that depends on which kind of wire is being used, isolation thickness, how the coils are wound, whether a coil former is used or not, among other

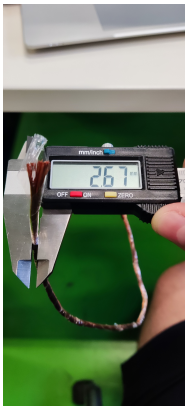


Figure 2.24: Wire diameter of 2.7 mm for a 130×0.2 basic Litz wire configuration. The copper-to-wire-area ratio is 70 %, without considering the strand insulation. Hence, a slightly smaller number is expected

factors. Ideally, we'd like to keep this number as close to unity as possible in order to use the whole winding area. From a practical perspective it is difficult to predict this quantity, whose estimation is only available once the coil is practically wound. As a matter of fact, the usage of Litz wire is suggested for this kind of application, since the frequencies analyzed are in the range of tens of kHz up to some hundreds of kHz. The filling factor of Litz wire depends on how many strands, bundles, and twisting configurations characterize the wire. For a basic Litz wire this number can be around $65 - 70\%$.
In Fig. 2.24 a 130×0.2 [1] basic Litz wire external diameter is measured at 2.7 mm. This means that the total cross section of the wire is 5.7 mm^2 while the bare copper is (almost) 4.1 mm^2, hence the filling factor for this Litz is around 70%.
Another factor to keep in mind is the spaces between two adjacent turns, due to the circular nature of the wire. This form factor takes up a space of $\pi/4 \approx 78\%$. Adding the presence of a coil former for mechanical stability, whose volume can take up to 10-20% of the winding area, and achieving 40-50% filling factor K_u becomes challenging. For this reason, we'll take 40% as a reference for the calculations that follow.
From Eq. (2.40), the copper section of the wire can be computed as

$$A_w \leq \frac{K_u W_A}{N} \tag{2.41}$$

where, as discussed, we can set the filling factor to 0.4, the winding area W_A is a geometrical property and N is the number of turns previously computed. It is now possible to compute the DC resistance of the winding, as

$$R_{dc} = \rho_{cu} \frac{l}{A_w} = \rho_{cu} \frac{N\, MLT}{A_w} \tag{2.42}$$

where MLT is the mean length of a single turn, another geometrical parameter. Finally, the AC resistance is estimated and the total copper losses can be finally computed. The AC resistance considers skin and proximity effects and is proportional to the DC resistance just computed $R_{ac} = F_R R_{dc}$

$$F_R = \begin{cases} 1 + \dfrac{1}{12}\left(\dfrac{K_u w_W d_r}{\delta^2}\right)^2 & \text{for } d_r < 3.17\delta \\ \dfrac{1}{\delta}\left(\dfrac{d_r}{4} + 8\dfrac{(K_u w_W)^2}{3 d_r}\right) & \text{for } d_r \geq 3.17\delta \end{cases} \tag{2.43}$$

[1] The notation 130×0.2 means the wire is composed of 130 strands, each of them having a diameter of 0.2 mm. The total copper area for a single wire can be computed as $A_w \approx (\pi/4)\, 130\, 0.2^2 = 4.1\ mm^2$. This does not consider the thickness insulation of each individual strand

The expression in Eq. (2.43) explains the ratio between AC and DC resistance in round conductors, by taking into account both skin and proximity effects [61, 62]. Here δ refers to the skin depth, w_W is the winding width and d_r is the conductor diameter. Hence, the thinner the strands that compose the Litz wire the more the AC resistance can be reduced, up to a point where the total copper losses are strongly dominated by the DC content rather then high frequency components. The total copper losses are estimated as Eq. (2.44). In the converters analyzed in this work the ripple is triangular and Δi refers to the peak-to-peak amplitude of said component. Hence, the rms value of the AC ripple content is computed as $I_{ac,rms} = \Delta i/(2\sqrt{3})$.

$$P_{cu} = R_{dc}{I_{dc}}^2 + R_{ac}{I_{ac,rms}}^2 = R_{dc}{I_{dc}}^2 + F_R R_{dc}\frac{\Delta i^2}{12} = R_{dc}\left({I_{dc}}^2 + F_R\frac{\Delta i^2}{12}\right) \tag{2.44}$$

Substitution of Eq. (2.42) in Eq. (2.44) results in Eq. (2.45) where r is the ratio between peak-to-peak current ripple and DC value, which for the purpose of this work cannot exceed 20%.

$$P_{cu} = \rho_{cu}\frac{N^2\,MLT}{K_u W_A}{I_{dc}}^2\left(1 + \frac{F_R}{12}r^2\right) \tag{2.45}$$

In case of coupled inductor design, such as the multichannel buck, used for limiting the circulating current between different converter legs, the design strategy presents some differences with respect to the DC inductor. In this case the actual inductance value is of secondary interest since the aim is to limit the differential mode current in order to reduce devices conduction losses while simultaneously minimizing inductor losses.

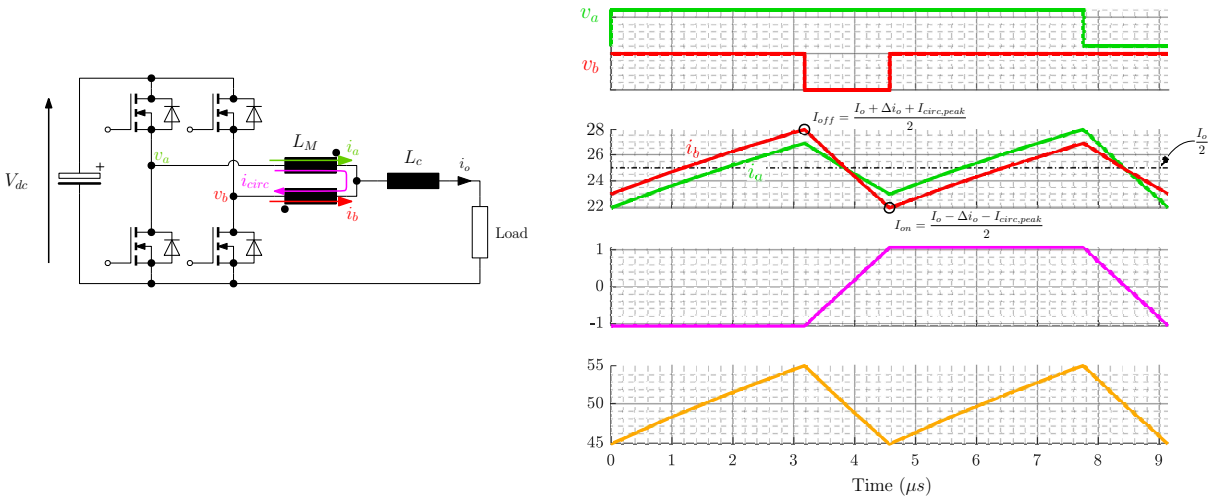


Figure 2.25: Two-channel buck and relative waveforms

In Fig. 2.25 the two-channel buck and relative waveforms are shown. The system illustrated works with a bus voltage of 500 V, switching at 94 kHz and the output inductor value is 15 μH. This configuration allows to achieve 10 μs rise-time (not shown in this picture, use Fig. 2.7 for reference) and 20% output ripple current, i.e. ± 5 A. The full-load current is 50 A, as it is possible to see from the second and last panels illustrating the phase currents around 25 A and the load current plus their ripple, respectively.
On the second waveform, the points highlighted with I_{on} and I_{off} are the turn-on and turn-off currents for the highside switches. These values are a function of the output ripple and circulating current peak, as highlighted in the picture. In the third plot the differential mode current flowing through the channels is shown (defined as $i_{circ} = i_a - i_b$), and its peak-to-peak value is computed as in Eq. (2.46), also explained in Fig. 2.6a.

$$\Delta i_{DM} = \frac{V_{dc}}{L_{DM}}\frac{1-D}{F_{sw}} \tag{2.46}$$

The coupled inductor design strategy is based off the ability to minimize the total losses. Let's first address the losses in the windings, which have been clearly analyzed before and the result has been presented in Eq. (2.45). For the coupled inductor, the copper losses are computed as

$$P_{cu\_coupled} \approx \rho_{cu} \frac{2\,N^2\,MLT}{K_u W_A} {I_{dc}}^2 \left[1 + \frac{F_R}{12}\left(\frac{\Delta i_{ph}}{I_{dc}}\right)^2\right] \tag{2.47}$$

Some notes must be highlighted in Eq. (2.47): the factor 2 indicates the presence of two windings and, of course, the term now called I_{dc} refers to half the value of the load current DC counterpart. The number of turns N refers to the turn of one of the two windings (same as L_M refers to the self inductance of a single winding while L_{DM} refers to the differential mode inductance, in this case being $L_{DM} = 2L_M$). Finally, the $\approx$ operator is used to indicate the inaccuracy on the estimation of the rms content for the AC ripple in each of the two channels. If the ripple is perfectly triangular (no matter the duty cycle) then

$$I_{ph\_AC,rms} = \frac{\Delta i_{ph}}{2\sqrt{3}}$$

The more the waveform form factor deviates from triangular, the more the previous result becomes inaccurate. Nonetheless the approximation holds true in this instance because, in the hypotheses of small circulating current, the phase ripple becomes almost triangular as shown in Fig. 2.25.
The flux density is computed as

$$B(t) = \frac{1}{N\,A_e}\int_0^{T_{sw}} v(t)dt \tag{2.48}$$

meaning that in the case of a two-channel topology, the flux density peak (maximum value) is computed in Eq. (2.49) (Fig. 2.6a can be used for better graphical understanding).

$$\Delta B = \begin{cases} \frac{V_{dc} D}{4\,N\,A_e\,F_{sw}} & \text{for } D < 0.5 \\ \frac{V_{dc}(1-D)}{4\,N\,A_e\,F_{sw}} & \text{for } D \geq 0.5 \end{cases} \tag{2.49}$$

The worst case scenario (i.e. when the flux density peak is the biggest) happens in case of duty-cycle 50%. For this reason, this case will be considered for the design from now on, where the maximum flux density peak ΔB now becomes

$$\Delta B_{max} = \frac{V_{dc}}{8\,N\,A_e\,F_{sw}}$$

If we assume that the flux density excitation is sinusoidal with amplitude ΔB_{max}, then we can use Steinmetz equation [63] to estimate the losses in the ferrite

$$P_{fe} = K_{fe} {F_{sw}}^{\alpha} {\Delta B_{max}}^{\beta}\,\text{Vol} \tag{2.50}$$

Substituting the expression for ΔB_{max} into Eq. (2.50) and rearranging the terms

$$P_{fe} = \text{Vol}\,K_{fe} {F_{sw}}^{\alpha-\beta}\left(\frac{V_{dc}}{8\,N\,A_e}\right)^{\beta} \tag{2.51}$$

The total inductor losses are

$$P_{tot} = \underbrace{P_{cu}}_{\propto N^2} + \underbrace{P_{fe}}_{\propto N^{-\beta}} \tag{2.52}$$

It is possible to analytically solve the previous equation in order to find the optimal number of turns that guarantees the minimum losses

$$\frac{\partial P_{tot}}{\partial N} = 0 \implies N_{opt} = \left(\frac{\beta}{2}\frac{c_2}{c_1}\right)^{\frac{1}{2+\beta}} \tag{2.53}$$

Eq. (2.53) shows the optimal number of turns that minimizes the total magnetic losses (c_1 and c_2 are defined in 2.54).

$$\begin{aligned} c_1 &= \rho_{cu}\frac{2\,MLT}{K_u W_A}{I_{ph}}^2\left(1+\frac{F_R}{12}r^2\right) \\ c_2 &= \mathrm{Vol}\,K_{fe}{F_{sw}}^{\alpha-\beta}\left(\frac{V_{dc}}{8\,A_e}\right)^{\beta} \end{aligned} \tag{2.54}$$

This is a famous result that can be found in literature [62, 64, 65]. This result is found based off an approximation on the flux density waveform shape factor being sinusoidal, whereas in the coupled inductor used as a DM choke this is not the case. As previously explained, the GSE is used in this instance. Eq. (2.53) however shows the physical meaning of what is done for the coupled inductor, and the optimal number of turns is solved semi-analytically (copper losses are computed analytically while core losses are estimated through GSE algorithm).

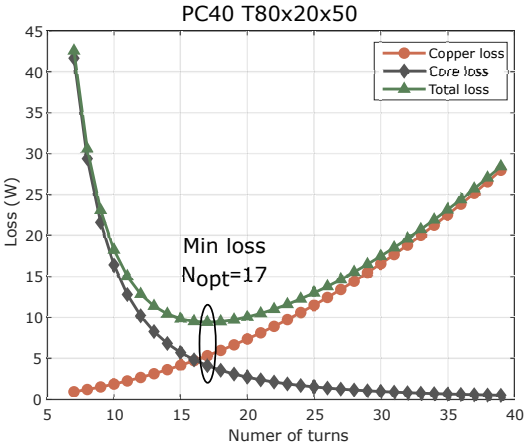


Figure 2.26: Losses of coupled inductor as a function of the number of turns. Given material properties (and no airgap), 17 turns would result in roughly 1.25 mH ($\pm 25\%$) [6] winding inductance (L_M). At 50% duty ratio, this would result in a peak circulating current of roughly 800 mA peak-to-peak at 500 V_{dc} and 94 kHz switching frequency. The resulting peak of flux density is 133 mT, well below saturation level for this material (380 mT at 100^oC, [7])

In Fig. 2.26 the loss profile as a function of number of turns is shown for a toroid used as a differential choke in a two channel buck (T80x20x50).

2.3.4 DC-link capacitor design

The capacitor design serves the primary role of effectively suppressing DC link voltage ripple due to the switching actions of the DC-DC converter. To achieve this, a capacitor design equation has been formulated for each candidate topology as outlined below

$$
\begin{aligned}
C_{dc} &= \frac{D(1-D)I_o}{F_{sw}\Delta v_{dc}}, \text{ for FSBB} \\
C_{dc} &= \frac{(D-0.5)(1-D)I_o}{F_{sw}\Delta v_{dc}}, \text{ for 2-channel buck} \\
C_{dc} &= \frac{(D-2/3)(1-D)I_o}{F_{sw}\Delta v_{dc}}, \text{ for 3-channel buck} \\
C_{dc} &= \frac{D_m(1-D_m)I_o}{F_{sw}\Delta v_{dc}}, \text{ for buck with active filter}
\end{aligned}
\tag{2.55}
$$

In this context, Δv_{dc} represents the maximum allowable DC link voltage ripple, which have been specified to be less than 5% of the nominal DC link voltage. Once the capacitance value is calculated using the respective design equation, the next step involves choosing the capacitor from the available library film capacitors. The selection process is based on two critical factors: minimizing losses and reducing weight. Both of these aspects are crucial considerations, and they must be carefully evaluated to ensure optimal capacitor performance.
The evaluation process takes into account the RMS current ripple that flows through the selected capacitor. This ripple value varies depending on the specific topology under investigation. By considering the RMS current ripple along with other design criteria, we can identify the capacitor that best suits the requirements of the DC link in terms of efficiency, performance, and reliability.

2.4 Optimization results and Pareto-analysis

The design procedure explained in Section 2.3 is applied to the three topologies proposed, hence the two and three channels buck, the four switch buck-boost and the buck with active filter in order to produce the Pareto-plot displayed in Fig. 2.27.

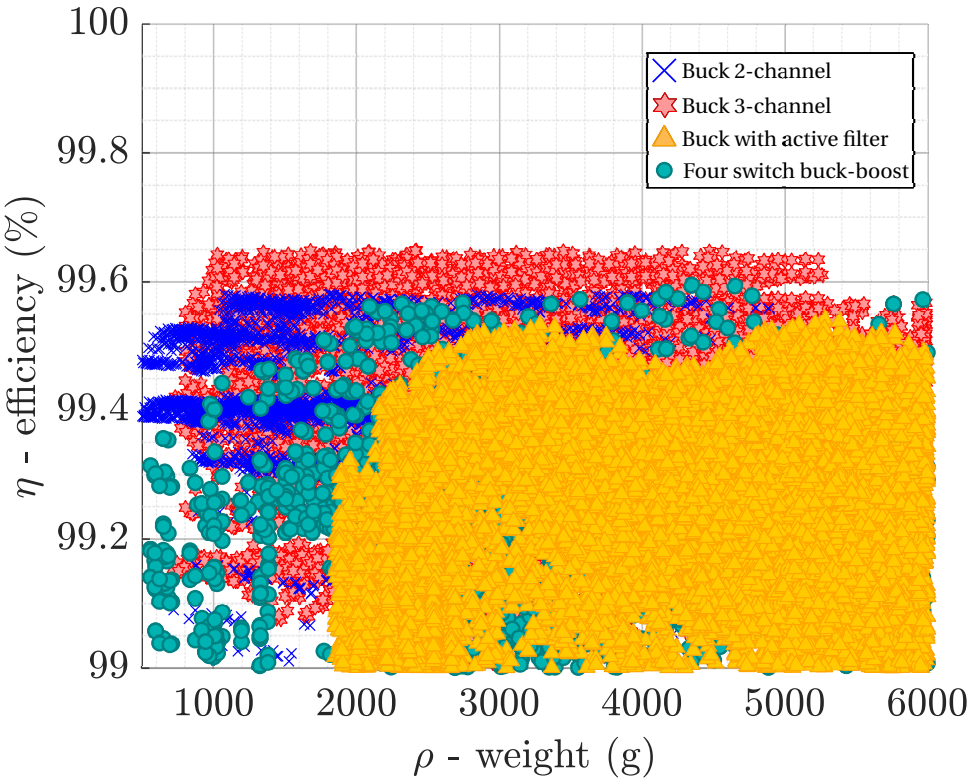


Figure 2.27: ρ-η-Pareto comparison of the proposed topologies

In this analysis the efficiency and weight configuration for each topology is highlighted using different markers with different colours. Each configuration is analysed considering the worst

case condition in which the converter can operate, hence when the SOFC requests charging with 50 A continuously (rather then a pulsating load). From this analysis we can conclude how the buck with active filter is strongly inferior when compared with multichannel bucks or FSBB. The reason is mainly due to the size and losses of the main branch inductor that needs to process the whole DC-current fed to the load and due to low switching frequency, a considerably high ripple. Hence a very high inductance value (and higher losses) is to be expected.
The FSBB shares the same concerns as the buck with active filter regarding the inductor, to some extent. Since only one magnetic component processes the whole current, its energy content LI^2 and consequently its volume would be relatively big.
Finally, the two and three channel bucks are the solutions scoring the best in the Pareto analysis. The possibility to, as previously highlighted, share the current between the phases allows to achieve higher efficiencies - when confronted with active filter solution and FSBB - at the same weight level.

Table 2.2: Components in two-channel design

Component	**Specification**
Highside devices	3× 65 $m\Omega$ 900 V SiC MOSFET C3M0065090J
Lowside devices	3× 65 $m\Omega$ 900 V SiC MOSFET C3M0065090J
Output inductor	2× 0P45528EC core sets (EE config.), 10 turns (15 μH)
Interchannel inductor	2× PC40-T80x20x50 core sets, 12 turns (1.2 mH)

In Tab. 2.2 the list of components for a two-channel interleaved solution lying in the Pareto line of Fig. 2.27 is shown. In this particular solution the DC-link voltage V_{dc} is set at 500 V and the switching frequency is 97 kHz.

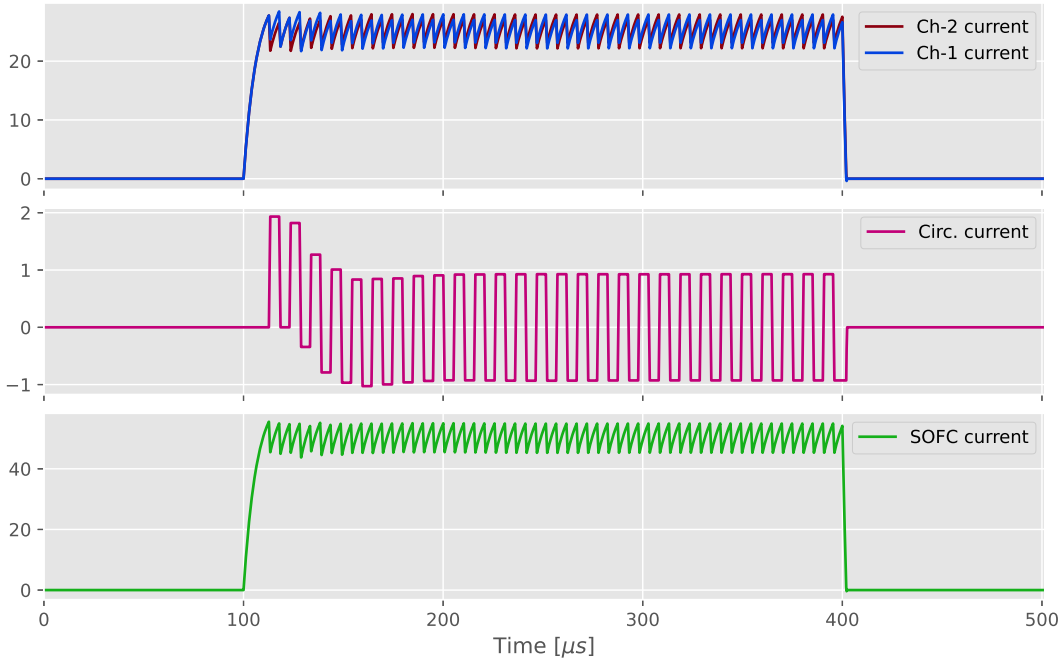


Figure 2.28: Simulation of 1 fuel-cell modulation cycle (500 μs) for the two-channel interleaved buck obtained via optimization

The plots in Fig. 2.28 display the simulation results of the converter just described and characterized by the components in Tab. 2.2. We can see how adopting this configuration allows for the time to reach steady-state to be 10 μs and the ripple within ±10%.
Fig. 2.29 illustrates the breakdown of losses in the target configuration. The losses were studied

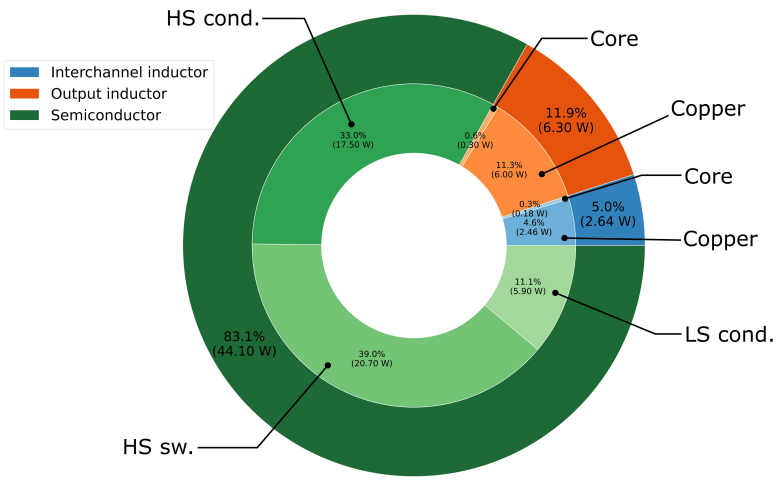


Figure 2.29: Loss breakdown of the two-channel interleaved converter discussed in this section

under the worst-case scenario, where a continuous current of 50 A is supplied to the fuel-cell (i.e. electrolysis mode). The majority of losses (83%) are attributed to semiconductors, primarily coming from the high-side devices. These losses take into account the combined losses of the three paralleled devices, including 17.5 W from conduction and 20.7 W from switching. The remaining 17% of losses are caused by magnetic components, particularly the output filter and the DM-choke (referred to as the interchannel inductor in the figure). In both cases, ohmic drops contribute significantly to the losses. This assumption is reasonable since core losses depend on the change in magnetic field strength (ΔB), which is proportional to the change in current (Δi), but as depicted in Fig. 2.28 the change in current is relatively limited.

2.5 Conclusions

The optimization procedure described in this section aims to achieve a Pareto analysis of different topologies for the proposed solutions. Three degrees of freedom (DoF), namely the DC-link voltage (V_{dc}), the transient time to reach steady-state (t_Δ), and the output current ripple (Δi_o), are swept to analyze a wide design space for the converters. These variables determine the inductance values and converter switching frequency, which, in turn, affect semiconductor losses. The optimization considers different topologies, including two-channel buck, three-channel buck, four-switch buck-boost and buck with an active filter. The goal is to find the best-suited devices for the application based on efficiency and overall converter size. The optimization process involves estimating losses and sizes for various components. Semiconductor losses are evaluated by sweeping different devices from a device database, considering breakdown voltages of 900 V and 1.2 kV. Copper losses and core losses in inductors are computed, taking into account factors such as resistance, winding structure, and material properties. The design of the DC-link capacitor bank is determined based on the maximum allowed input voltage ripple.
The results of the optimization procedure are analyzed using a Pareto comparison, where efficiency and overall weight are considered. The analysis shows that the buck with active filter performs poorly compared to the other solutions. The multichannel buck configurations demonstrate better efficiency at the same weight level due to the sharing of current between phases, allowing for smaller inductances and higher switching frequencies.
In summary, the optimization procedure considers various variables and components to obtain a Pareto analysis of different topologies. The analysis helps in selecting the most suitable devices and configurations for the specific application, balancing efficiency and overall converter size.

Chapter 3

Hardware design

This chapter discusses the design of the proposed hardware as analysed in the previous Chapter. This study explores the advantages of employing the printed circuit board (PCB) layout while trying to minimize critical parasitic components, such as loop inductances and inter-plane capacitances. Since silicon carbide (SiC) devices can operate at high switching speeds, they generate higher di/dt and dv/dt slew rates. Without minimizing trace inductance, there's a risk of overshoots and ringing occurring. To address this issue, stacking PCB traces on top of one another can help reduce the induced magnetic field, subsequently lowering the overall system inductance which, in turn, mitigates overshoot and ringing issues.
Moreover the increasing readiness of Silicon-carbide transistors for the power converter market has created a growing demand for high-performance gate driver design to fully utilize their fast switching characteristics. Specifically, the gate driver units designed for SiC devices, which undergo extremely rapid switching at medium-voltage levels, require robust driving capabilities, effective short-circuit protection and common-mode transient immunity. Paired with the necessity of paralleling multiple devices, the gate driving stage becomes a challenging stage to be taken into consideration during the power loop design.
This chapter will focus on the PCB design for the half-bridges and relative gate driving circuitry, with in-depth analysis on the choices made to minimize space utilization and parasitics.

3.1 Half-bridge

The two-channel buck is composed by two half-bridges and, as highlighted in Tab. 2.2, each device position is composed by three paralleled SiC MOSFET (C3M0065090J). The device is a 65 $m\Omega$ R_{ds_on} (at $25^o\,C$) with output capacitance C_{oss} of approximately 66 pF. The package is a TO-263-7, a bottom side cooled package that allows up to 32% stray inductance reduction if compared with classical through-hole solutions such as TO-247 [66]. In Fig. 3.1 a picture representing the comparison between TO-247 and TO-263-7 is shown where obviously the latter is more suitable for compact designs. On the other hand, bottom side cooled devices such as the one shown here suffer from cooling challenges if compared with common TO-247 where it is possible to screw a heat-sink to the cooling pad. In Fig. 3.2 the comparison between cooling strategy of TO-247 and TO-263-7 is shown. Allowing for the heat-sink to be closely contacted with the back of the package (where the cooling pad is) allows to decrease the total thermal resistance chain. On the other hand, in bottom side cooled designs the heat must be extracted from the back of the PCB (usually done by means of so called *thermal vias*, but other strategies are available). This poses some challenges both from a layout standpoint (some space must be predisposed to allow for the placement of thermal vias) and from a thermal one. On the other hand, the big advantage of having a more compact layout and allowing for higher switching frequencies due to the reduced parasitics, makes the TO-263 package a valid candidate for high power designs.

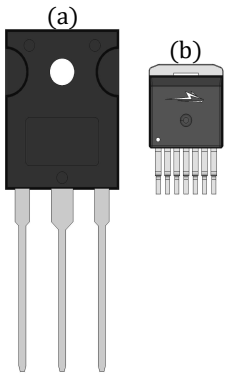
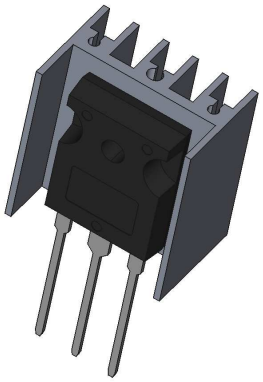


Figure 3.1: Two common packages. (a) TO-247. (b) TO-263-7



(a) TO-247 with heat-sink

(b) Cooling of TO-263-7 with thermal vias and heat-sink on the bottom. The $R_{th,PCB}$ is the thermal resistance introduced by the PCB by connecting the heat pad of the package to the bottom layer of the board with thermal vias. This is the biggest bottleneck in the thermal management chain, since usually $R_{th,PCB}$ is much higher then the others.

Figure 3.2: Core dimensions

3.1.1 Power loop design and discrete SiC paralleling considerations

One of the challenges to face in this design is the optimization of the power loop and the devices parallelization. As previously illustrated in Chapter 2, the optimization procedure suggests the usage of 3 C3M0065090J devices per position (i.e. 3 per high-side and 3 per low-side). Paralleling discrete devices poses different challenges mainly due to fabrication tolerances. Let's introduce the concepts of *static current sharing* and *dynamic current sharing*.

Static current sharing is the unbalance of current between two (or more) paralleled devices due to on-resistance inequality. In the device under consideration, the nominal R_{ds_ON} is 65 $m\Omega$ at 25^oC whereas its maximum deviation at the same temperature is 78 $m\Omega$, accounting for 20% difference. Let's imagine that due to fabrication uncertainties, a 65 $m\Omega$ and a 78 $m\Omega$ devices are paralleled. During the conduction 55% of the current would flow in the weaker device (hence the 65 $m\Omega$ one) while the remaining 45% flows in the 78 $m\Omega$ device.

$$\begin{array}{l|l|l} R_1 = 65\ m\Omega & i_1 = \frac{R_2}{R_1+R_2} i_{tot} = 0.5455\, i_{tot} & P_1 = R_1 0.5455^2 {i_{tot}}^2 \\ \hline R_2 = 78\ m\Omega & i_2 = \frac{R_1}{R_1+R_2} i_{tot} = 0.4545\, i_{tot} & P_2 = 1.2 R_1 0.4545^2 {i_{tot}}^2 \end{array} \tag{3.1}$$

The results in Eq. (3.1) allow to compute the power sharing difference between weak device (with lower R_{ds_ON}, R_1) and string device R_2, so that $P_1 = 1.2\, P_2$, meaning that the weaker device has to dissipate 20% more power then the strong one.

The PTC effect of the SiC technology helps mitigating this issue. The device with smaller R_{ds_ON} dissipates more power, hence its temperature increase is bigger if compared with the stronger device.

Dynamic current sharing is the unbalance of currents during transition (either on or off) due to inequality in the gate parameters. Controlling the switching losses is a crucial aspect of the design and the usage of parallel devices adds a layer of complexity on this matter. Any disparities in the distribution of current among parallel devices during a transient can lead to significant imbalances in losses between them. The transient current in is determined by the transconductance (g_{fs}) and threshold voltage (V_{th}):

$$i_d = g_{fs}(v_{gs} - V_{th}) \tag{3.2}$$

The equation above clearly highlights the challenge associated with unequal V_{th} or transconductance gain values among parallel devices. Devices with relatively lower V_{th} or higher g_{fs} will carry more dynamic current and thus experience greater switching losses.

Another factor contributing to current imbalances during switching transients is circuit layout. Even a minor mismatch in parasitic common source inductance (L_{CS}) between parallel devices can convert the high di/dt observed in SiC into negative gate voltage feedback. This feedback is evident in the equation for v_{gs}, and its impact on current difference is illustrated by Eq. (3.2), assuming equal g_{fs} and V_{th} [67].

$$\begin{aligned} v_{gs} &= V_{GD} - i_g(R_{g,ext} + R_{g,int}) - L_{cs}\frac{di_s}{dt} \\ i_{d1} - i_{d2} &= g_{fs}(L_{s1} - L_{s2})\frac{di_s}{dt} \end{aligned} \tag{3.3}$$

Consequently, during turn-on, a device with relatively high L_{cs} turns on more slowly, carrying less current and causing an imbalance in switching losses. During turn-off, a relatively high L_{cs} accelerates device turn-off, offsetting the turn-on effect by reducing losses.

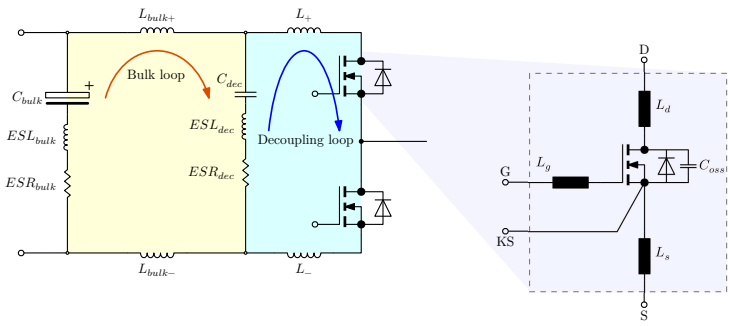


Figure 3.3: Half-bridge loops

In the context of static or dynamic current sharing, it is essential to recognize that while several variables influence this phenomenon, the uneven common source inductances stand out as the only factor that can be effectively controlled through meticulous layout design. Notably, factors such as internal gate resistance ($R_{g,int}$), transconductance (g_{fs}), threshold voltage (V_{th}), and on-resistance ($R_{ds,ON}$) are inherently susceptible to fabrication tolerance, rendering them uncontrollable. Therefore, a considerable amount of emphasis must be placed on the layout aspect of circuit design.

Within the schematic representation depicted in Fig. 3.3, we observe the configuration of a half-bridge loop, which serves as a pivotal element in power electronics circuits. The DC-link capacitor (C_{bulk}) typically exhibits significant equivalent series inductance (ESL) and presents challenges in terms of its proximity placement relative to the switching devices. Consequently, it is expected that the total loop area encompassing the bulk capacitor and the devices will be relatively substantial, resulting in elevated inductance within what is referred to as the "bulk loop".

To surmount this limitation, employment of low ESL decoupling capacitors (C_{dec}) positioned in close proximity to the drain-to-source connections of the half-bridge is crucial. This placement aims to minimize the inductance of the power loop, named the "decoupling loop" in Fig. 3.3, as detailed in [68]. It is worth noting that the parasitic inductances associated with the packaging of these components also contribute to the overall inductance of this loop.

As a practical guideline it is advisable that the decoupling capacitor be sized considerably larger than the output capacitance of the semiconductor device [69]. In the specific case at hand, where the output capacitance of the device approximates 66 pF, decoupling capacitor size in the order of 10 nF proves adequate and well-suited for this application.

Three different power loop configurations are proposed: *parallel half-bridges design*, *parallel devices design* and *double-sided return path design* [70].

Parallel half-bridges

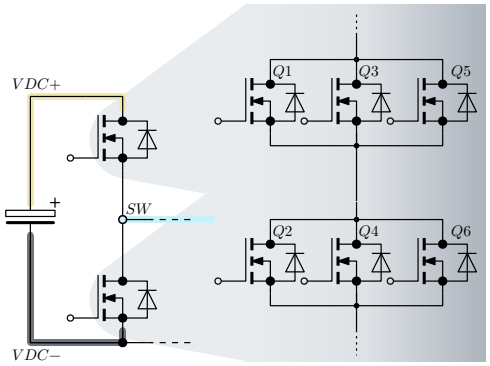


Figure 3.4: Schematic representation of a half-bridge composed by 3 paralleled devices per position.

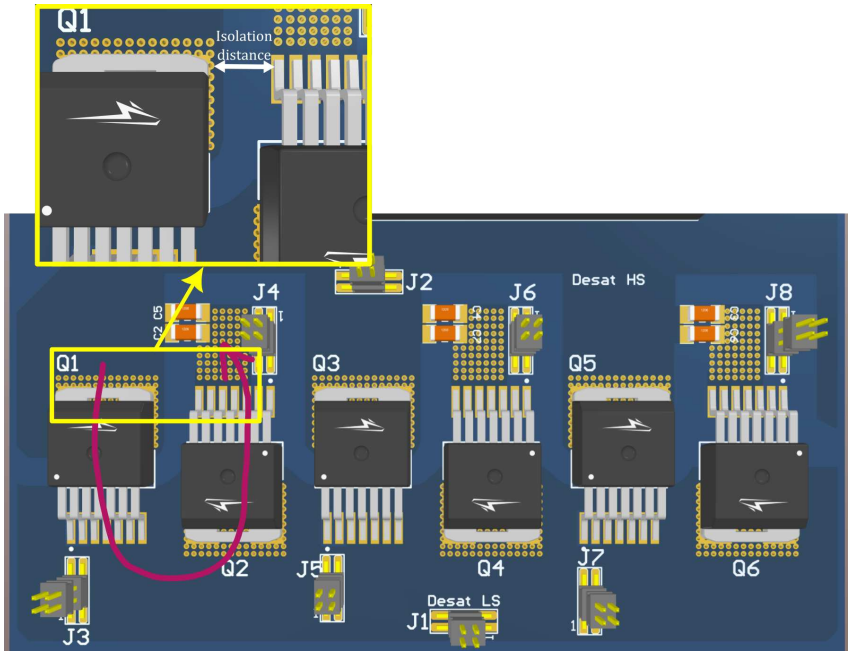


Figure 3.5: Paralleled half-bridges. Each has its own current loop with minimal area defined by the isolation distances between the drain pad of the high-side and the source pads of the low-side.

The schematic in Fig. 3.4 shows the details of the half-bridge plus some key names and color scheme that will be used in this chapter. The paralleled half-bridge configuration Fig. 3.5 consists into creating an optimal half-bridge cell which is then replicated for however many times is needed, in this work three times [71]. The power loop is minimized since it is possible to place the drain and source of the same half-bridge very close one another. Each half-bridge has its own current loop, that presents the minimum area of the three solution proposed before (purple arrow). The constraint on the loop area comes from the isolation distance needed between the drain of the high-side and the source of the low-side, where an average voltage difference of 500 V is expected. Compliance with IPC-2221B suggests 3 mm distance between the two nets (20% margin is taken into account), whereas if IPC9592 is considered 3.6 mm are suggested. To keep minimum footprint area, the placement of devices 1 to 6 can be done according to one of these two standards. Moreover, the distance between two different half-bridges can be kept the same as the one between two different devices of the same half-bridge as long as isolation constraint is respected, in contrast with what is shown in Fig. 3.5 where the three half-bridges are more spaced from one another. On Layer-1, the yellow copper pour represents the positive rail of the bus whereas the azure pour is the switching node. The return path (i.e. negative rail of the DC-bus) is on Layer-4 (grey shading) and it is accessed by the low-side devices 2, 4 and 6 thanks to vias close to the source pads. The return path is kept sufficiently distant from the switching node so to avoid parasitic capacitive effects that would increase switching losses during operation. The middle layers, 2 and 3, are populated with negative and positive rail (interleaved) to minimize copper dissipation due to increased conductor surface. The overlap of VDC+ and VDC- pours is not an issue from a capacitor standpoint since it results paralleled with the much bigger DC-Bus input capacitor.

Having the return path on Layer-2 is important since placing forward and reverse path close together allows to reduce the total loop inductance, at the expanse of likely bigger parasitic capacitances.

In Fig. 3.6 an half-bridge with its parasitics is shown. Firstly, we need to define the *nets* of the power loop. A *net* is any uninterrupted copper trace or plane. In the case of a half-bridge like the one shown in Fig. 3.6 there is three of them: the positive DC-rail named V_+ (or (1)), the

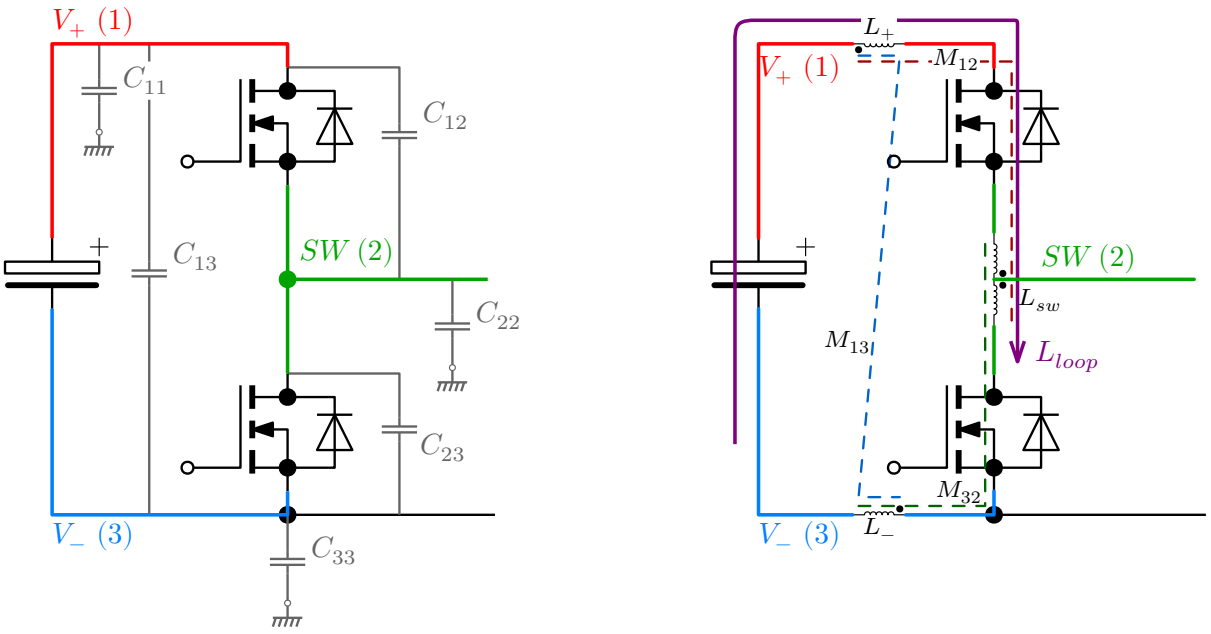


Figure 3.6: Half-bridge with its relative capacitive (left) and inductive (right) parasitics.

switching node SW or (2) and the negative DC-rail V_- or (3). It is then possible to define the capacitive and inductive matrices of the three conductors problem.

$$\mathbf{C} = \begin{bmatrix} C_{11} & C_{12} & C_{13} \\ C_{21} & C_{22} & C_{23} \\ C_{31} & C_{32} & C_{33} \end{bmatrix}$$
$$\mathbf{L} = \begin{bmatrix} L_{11} & M_{12} & M_{13} \\ M_{21} & L_{22} & M_{23} \\ M_{31} & M_{32} & L_{33} \end{bmatrix} \tag{3.4}$$

The element C_{ij} corresponds to the capacitance between conductor i and j where C_{ii} is intended as the capacitance between conductor i and a point infinitely distant, which can be represented by the protective earth connection (PE). By symmetry, it must be that $C_{ij} = C_{ji}$. The capacitances C_{12} and C_{23} are the ones that must be kept as small as possible because they are paralleled with the devices. Having big C_{12} or C_{23} is equivalent to having bigger C_{oss} device capacitance, hence increasing switching losses.
The stray inductance matrix is dually defined from the capacitance matrix. The most important parameter in this case in the *loop inductance*, defined as the inductance of a current loop that starts from the first conductor and ends in (3), as if they were series connected (hence $i_1 = i_2 = i_3 = i$). By definition of magnetic energy, it is then possible to compute the loop inductance once the L-matrix is known.

$$W_m = \frac{1}{2}\mathbf{i}^T\mathbf{L}\mathbf{i} = \frac{1}{2}L_{loop}i^2 \implies L_{loop} = \sum_{i=1}^{3}\sum_{j=1}^{3} L_{ij} \tag{3.5}$$

The stray inductance/capacitance analysis is performed by running a CGRL analysis on Ansys Q3D at 10 MHz frequency.
In Tab. 3.1 the numerical results are shown. The capacitances C_{12} and C_{23} are kept low (2.1 pF and 0.9 pF respectively) if compared with the device C_{oss} (around 60 pF). This is because there is no overlapping between positive rail and switching node or between switching node and return path. Applying Eq. (3.5) to compute the loop inductance results in $L_{loop} \approx 7.5$ nH.

$$\mathbf{L}\,(nH) = \begin{bmatrix} 4.86 & -0.23 & -0.73 \\ -0.23 & 1.46 & 0.12 \\ -0.73 & 0.12 & 2.89 \end{bmatrix} \quad \mathbf{C}\,(pF) = \begin{bmatrix} 1.1 & 2.1 & 423 \\ 2.1 & 1.2 & 0.9 \\ 423 & 0.9 & 1.6 \end{bmatrix}$$

Table 3.1: Stray inductance and capacitance matrices for configuration displayed in Fig. 3.6

The numbers obtained in the simulation are easily justified. The capacitance between positive and negative (return) planes is much bigger then all others since the positive V_{bus} is on Layer-1 while the negative is on Layer-2. There's no overlap between switching node and ground (that would affect the switching behaviour of the lowside) and between positive DC-bus and switching node.

Parallel devices

Similarly to what has been done in the case of parallel half-bridges, the loop inductance of the parallel devices is estimated via Q3D simulation. Differently from the case where the half-bridges are paralleled and each has its "own stray loop inductance", the possibility to place all high-sides and low-sides together respectively is the approach that would similarly be used in case of SiC module designs with paralleled devices or in case of half-bridge modules hard paralleling [72].

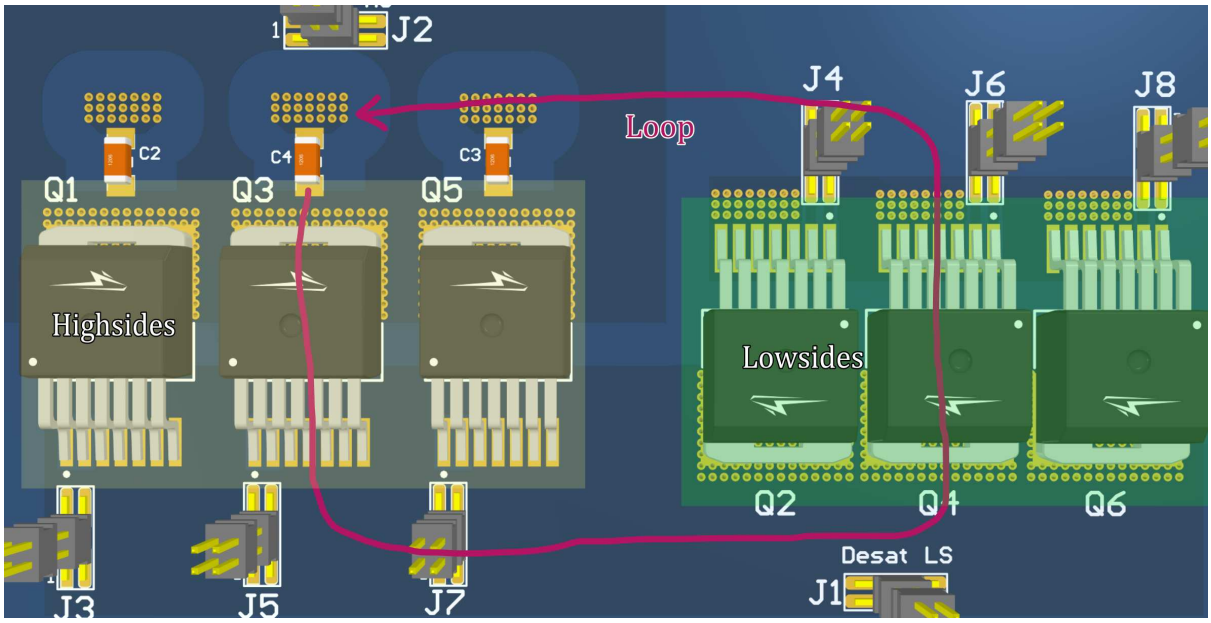


Figure 3.7: Half-bridge design with paralleled devices - highsides are on the left and lowsides are on the right.

In Fig. 3.7 the analysed configuration is illustrated, where the highsides are highlighted on the left-hand side while the lowsides on the right. The "average" loop is indicated by the pink trace. With this configuration, the stray inductance and capacitance matrices are shown in Tab. 3.2, where the loop inductance in this case accounts for $L_{loop} = 5.3$ nH.

$$\mathbf{L}\,(nH) = \begin{bmatrix} 2.05 & -1.00 & 0.00 \\ -1.00 & 0.16 & 0.00 \\ 0.00 & 0.00 & 5.11 \end{bmatrix} \quad \mathbf{C}\,(pF) = \begin{bmatrix} 0.8 & 1.6 & 312 \\ 1.6 & 1.1 & 1.4 \\ 312 & 1.4 & 1.5 \end{bmatrix}$$

Table 3.2: Stray inductance and capacitance matrices for configuration displayed in Fig. 3.6

Also this solution presents very small C_{12} and C_{23} elements, making it more appealing then

the *paralleled half-bridge* solution due to its slightly smaller L_{loop}. The main drawback of this solution lies in the positioning needed for the decoupling capacitor, that makes it so that the pulsed current component delivered to the load must funnel through the narrow spaces between the decoupling capacitors of each high-side switch.

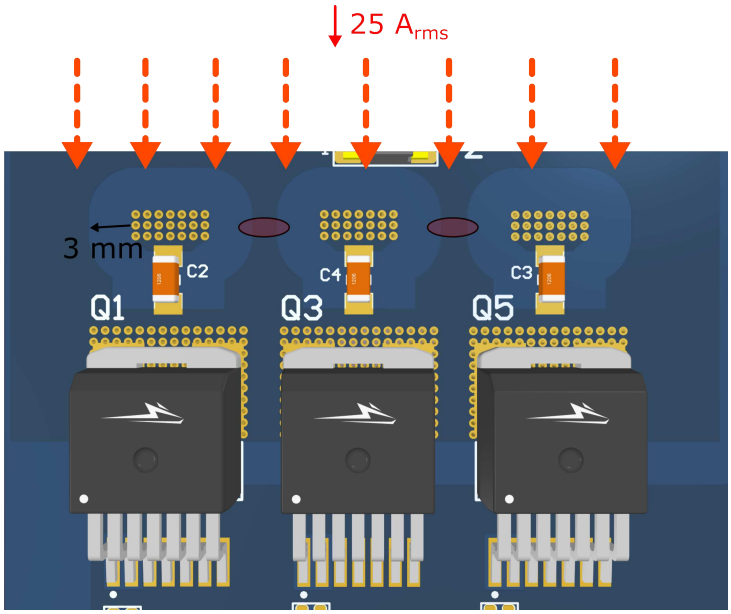


Figure 3.8: The decoupling capacitors make it so the high-side devices don't have all the available space due to the 3 mm isolation distance requirement.

The issue at hand is visually depicted in Fig. 3.8, where particular attention is drawn to the highlighted regions marked in red. These delineated areas correspond to copper pour sections that serve as critical conduits for channelling the current. It is assumed that current particularly comes from the upper side, where the positive terminal of the DC-bus capacitor and the input connector are found.

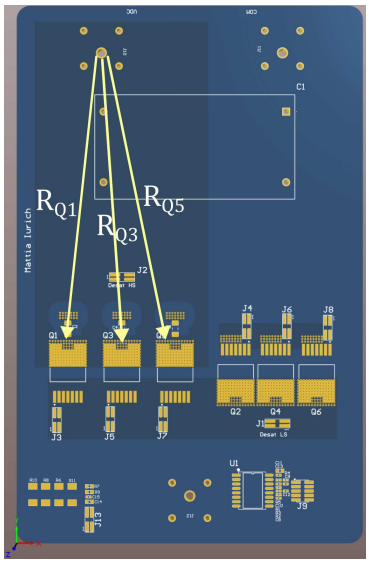


Figure 3.9: Whole board view where the connector J10 is the bus voltage input. The resistances are measured from this point to the drain of each high-side device.

A Q3D simulation is run in order to compute the DC resistances from the input connector to the drain of each high-side SiC device in order to validate the equal DC-current sharing. The

three resistance paths R_{Q1}, R_{Q3} and R_{Q5} (refer to Fig. 3.9) show approximately 1.2 mΩ each, confirming the correct current sharing among the three devices.

Double-sided return path

The double-sided return path is commonly used in bottom side cooled half-bridges [70] where each leg is designed vertically and the return paths are placed underneath the top layer, both on the left and right. This gives enough space to place the thermal vias for the high-side and low-side devices. The loop inductance obtained in this configuration is approximately 10.5 nH whereas the stray capacitance matrix is shown below

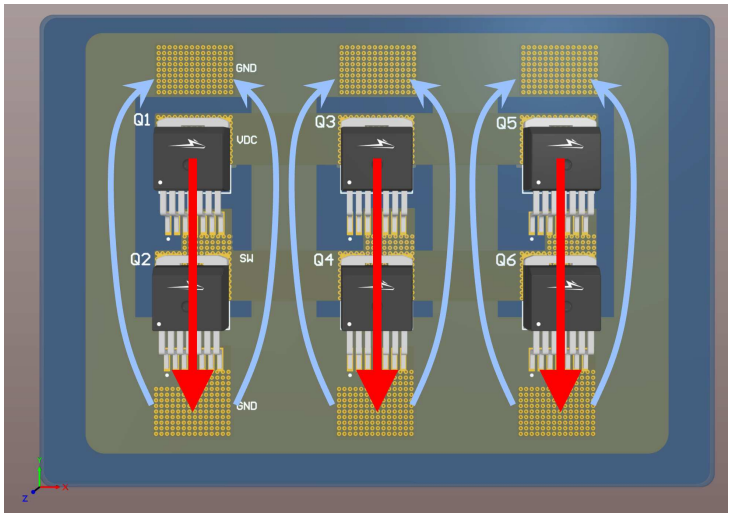


Figure 3.10: Double-sided return path layout, where the return lines are on the inner layer on both the right and left hand sides of the devices (blue arrows).

$$\mathbf{C}\,(pF) = \begin{bmatrix} 0.3 & 0.5 & 32 \\ 0.5 & 0.3 & 32 \\ 32 & 32 & 2.5 \end{bmatrix}$$

The element C_{23} is the capacitance between switching node and return path (ground), which measures 32 pF. Considering that the C_{oss} accounts for 66 pF, the output capacitance of the device is equivalently increased by 50%. This would result in higher switching losses in reverse operation. It is easy to understand why this is the case since the return path on the 2^{nd} layer overlaps with the DC-link and switching node copper pours laid on the 1^{st} layer. In Fig. 3.11 illustrates the case just described.
For these reasons the double-sided return path solution might be inferior if compared with the previous proposals, since increased loop inductance is expected as well as non-negligible parasitic capacitance on the low-side device.

Results comparison

Once the previous analysis is carried out, a circuit simulation (through LTSpice®) comparison between the proposed solutions is carried out in order to understand which configuration behaves the best. Only the paralleled half-bridges and paralleled SiC solutions are implemented since the double-sided return path would obviously perform much worse then these two. In Fig. 3.12 all the details about this analysis are highlighted. The dark and light blue traces refer to the V_{ds} voltage on one of the highside devices (Q_1 in this case) while the orange and red traces show the current on the same device. As highlighted in the legend, the clear trances (i.e. light blue and orange) refer to the circuit solution where the SiC MOSFETs are paralleled whereas the darker

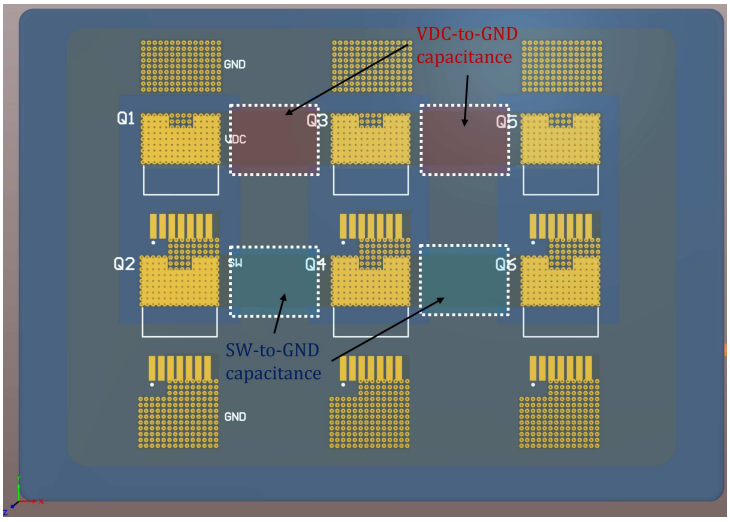


Figure 3.11: The return paths (on 2^{nd} layer) overlap with both the positive bus and switching node pours (on 1^{st} layer) creating big stray capacitances between bus and ground, and between switching node and ground. The latter is to be avoided since it increases the equivalent capacitance of the output node on the low-side devices, hindering their performance during boost operation (current flow from fuel-cell to bus) when they hard-switch.

lines (i.e. dark blue and red) refer to the solution where the modular paralleled half-bridges are employed.

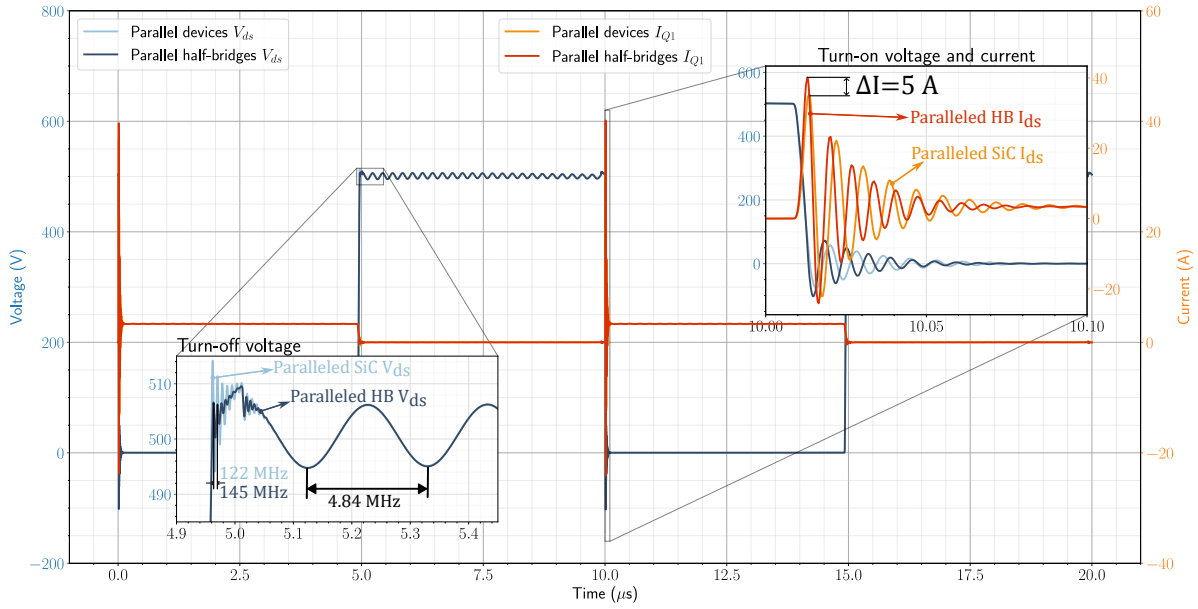
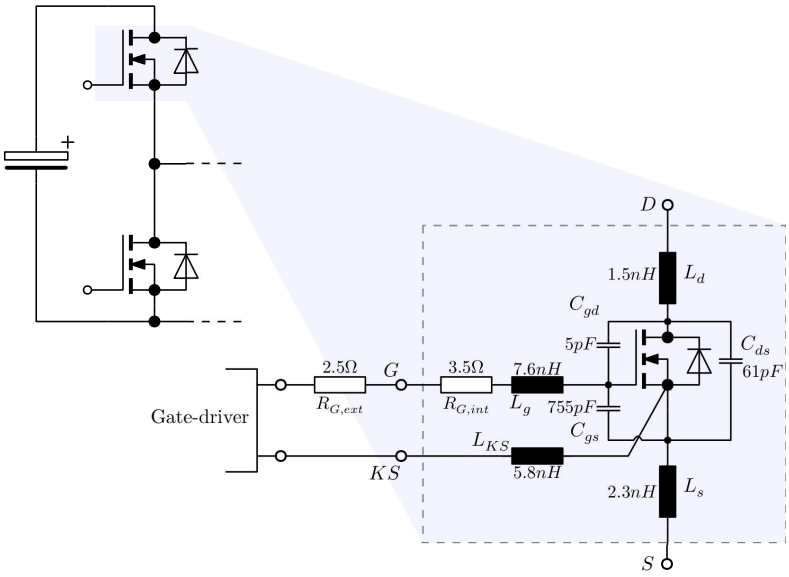


Figure 3.12: Circuit simulation comparison of parallel half-bridge solution and paralleled SiC.

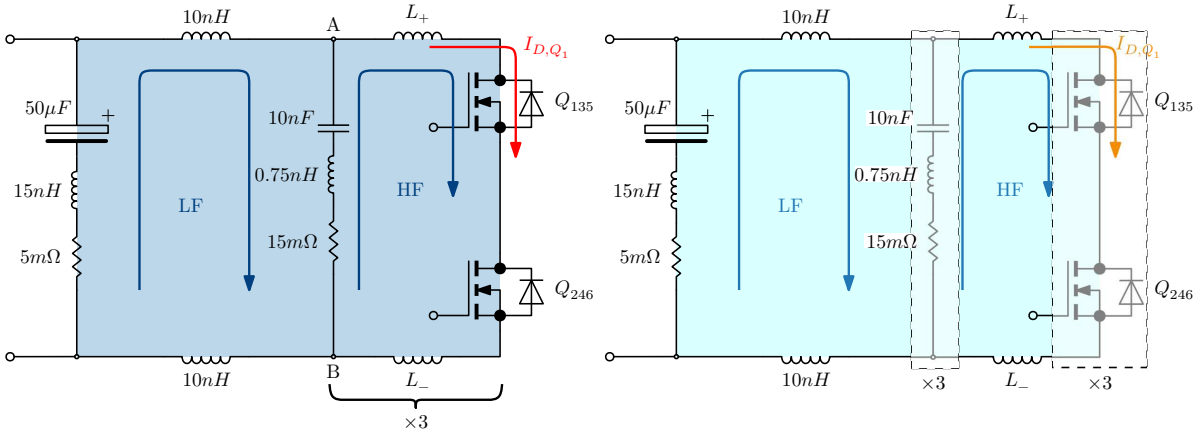
The SiC model used for the LTSpice® simulation is explained in Fig. 3.13a, belonging to the DUT (Device Under Test) hence C3M0065090J [73]. The Spice model takes into account all capacitive non-linearities, while the image shows static values of C_{GS}, C_{DS} and C_{GD} which are known to be a function of the operating condition. The values indicated in Fig. 3.13a are extrapolated at 600 V V_{ds} [74].

The test has been conducted by switching the half-bridge(s) at 50% duty cycle at 100 kHz and by measuring voltage and current on one of the 3 high-side devices. The DC-link voltage is 500 V and the load current is 10 A. The important quantities to look at are during the turn-on and turn-off transitions.

The turn-off event (highlighted in the left inset) shows the voltage overshoot and its dynamical settling after the device has completely turned off. The worst case scenario for the overshoot happens in the paralleled SiC topology, where the high-sides and low-sides are hard-paralleled together.



(a) View of device model, used in circuit simulations performed as in 3.13b and 3.13c.



(b) Circuit simulation schematic for paralleled half-bridges solution.

(c) Circuit simulation schematic for paralleled devices configuration.

Figure 3.13: SiC device model and simulation schematics. The colors in 3.13b and 3.13c match the ones used in Fig. 3.12

It is possible to analyze the frequency of such oscillation and confront the simulation results with a simple RLC model in order to understand its dynamics [69, 75]. During the turn-off even for the high-side switch, its voltage across the drain-to-source junction reaches approximately the value imposed by the input DC-bus, hence its C_{oss} matches very closely the datasheet information (i.e. 66 pF). On the other hand, the low-side is already in turned off position. The voltage across its drain-to-source junction is approximately 0 V, hence the C_{oss} for the bottom device is much bigger then the one of top SiC.

In Fig. 3.14 the equivalent circuit of the high-frequency loop is shown, where the detail of the current passing through the parasitic elements of the transistor is highlighted in the right side. The capacitive component is the series of the decoupling capacitor, the output capacitance of the high-side device and the ones of the low-side

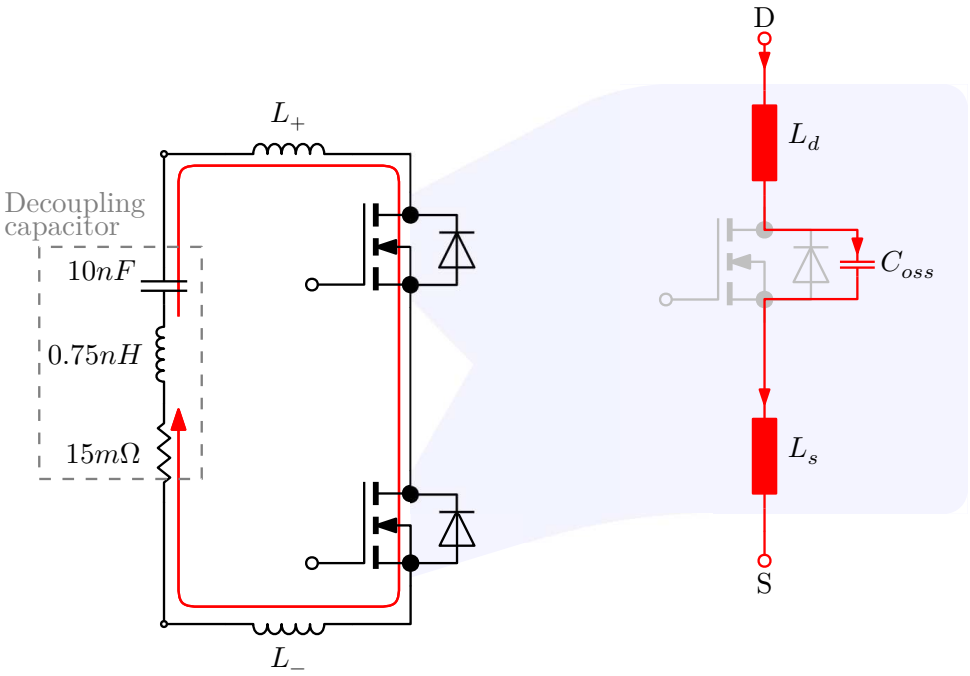


Figure 3.14: High-frequency loop equivalent circuit

$$C_{eq} = \frac{1}{\frac{1}{C_{dec}} + \frac{1}{C_{oss\_HS}} + \frac{1}{C_{oss\_LS}}} \approx C_{oss\_HS} \approx 66\ pF$$

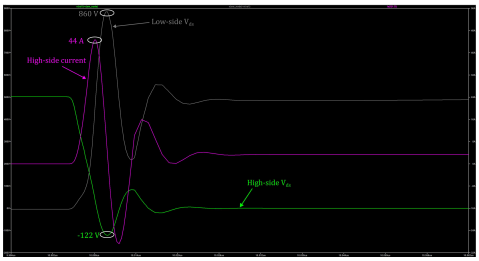
The inductive component is the sum of the loop inductance (L_+ and L_-), the stray inductances of the high-side and low-side packages and the ESL of the decoupling capacitor.

$$L_{eq} = L_{loop} + 2(L_d + L_s) + ESL_{dec}$$

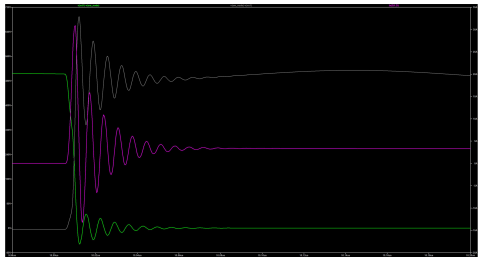
The loop inductance (of one half-bridge) for the paralleled half-bridge solution is $\sim$ 7.5 nH whereas the total loop inductance for the paralleled devices configuration is $\sim$ 5 nH. These results have already been shown coming out of the Q3D simulations.
By analyzing the differences between circuits in Fig. 3.13b (paralleled HB) and Fig. 3.13c (paralleled devices), the equivalent loop inductance of the latter solution $\sim$ 15 nH. Calculating the resonance frequencies for the two equivalent circuits here explained yields the results in (3.6), which are very close to the numbers shown in the simulations of Fig. 3.12.

$$\begin{aligned} f_{HF\_3\times HB} &= 151\ \text{MHz} \\ f_{HF\_3\times SiC} &= 125\ \text{MHz} \end{aligned} \tag{3.6}$$

When the high-side turns on, the voltage across its drain-to-source terminals quickly drops to zero since the current starts increasing until it reaches the load values. In the meantime the voltage on the low-side device rapidly grows. This fast increase leads to voltage overshoot in the bottom device, which can be potentially destructive if not taken care of. This overvoltage is a function of the loop inductance and di/dt. The first can be controlled through good layout but ultimately is limited by the package stray inductances, while the second factor can be adjusted through accurate selection of external gate resistor $R_{g,ext}$. In the simulation displayed in Fig. 3.15a the gate resistance is set at 2.5 Ω, which leads to an overvoltage on the low-side of approximately 860 V (i.e. +360 V). Since the devices are rated for 900 V, it'd be better to find a way to decrease said overshoot.
To do so, the external gate resistance is increased from 2.5 Ω to 7.5 Ω, leading to a maximum drain-to-source voltage of less then 700 V, resulting to an overshoot decrease of roughly 19%, as illustrated in Fig. 3.15b.



(a) Circuit simulation turn-on event for the high-side, in paralleled half-bridge configuration. Measurement on one device only (Q_1). Gate resistance is $R_g = 2.5\ \Omega$



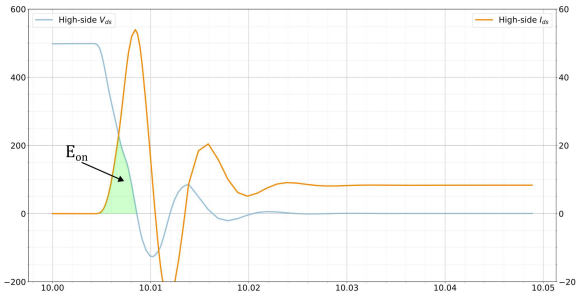
(b) Circuit simulation turn-on event for the high-side, in paralleled half-bridge configuration. Measurement on one device only (Q_1). Gate resistance is $R_g = 7.5\ \Omega$

Figure 3.15: High-side turn-on event - (green) V_{ds_HS}, (grey) V_{ds_LS}, (pink) I_{d_HS}

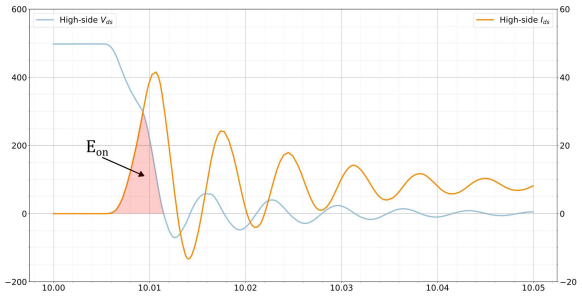
Of course the increase in gate resistor comes with a price in terms of increased losses during turn-on and turn-off. As illustrated in Fig. 3.16, the turn-on and turn-off energy of the highside changes depending on gate resistance. In case of $R_g = 2.5\ \Omega$ the (simulated) turn-on energy is 11 μJ whereas the turn-off point is 11.6 μJ. Increasing the the gate resistance to 7.5 Ω leads to $E_{on} = 20\ \mu$J and $E_{off} = 11.7\ \mu$J. The results shown refer to the energy expanse for turning on or off only 1 high-side device. The simulated load current is 25 A per half-bridge which is then divided in 3 devices (8.33 A each).

$$P_{diss} = (E_{on} + E_{off})\, f_{sw} + D\, R_{ds\_ON} {I_{rms}}^2 = \begin{cases} 6.2\ W & for\ R_g = 2.5\ \Omega \\ 7.0\ W & for\ R_g = 7.5\ \Omega \end{cases} \tag{3.7}$$

In Eq. (3.7) the calculation of total power loss per high-side device is shown for the two cases of different external gate resistor.



(a)



(b)

Figure 3.16: Turn on at $R_g = 2.5\ \Omega$ (**a**) and $R_g = 7.5\ \Omega$ (**b**)

3.2 Gate driving

In high-power applications, where it's necessary to parallel discrete silicon carbide (SiC) MOSFETs to increase the current rating, a critical challenge arises due to unbalanced dynamic currents during switching transients. This imbalance leads to unequal power losses and thermal distribution among paralleled devices. In [76] an Active Gate Driver (AGD) that employs di/dt feedback control and voltage-controlled current sources to adjust the gate drive current of SiC MOSFETs is proposed. By doing so, the switching trajectory of paralleled devices is altered, improving current sharing. The AGD also uses a master-slave control strategy, making it adaptable for multiple paralleled devices. Experimental tests confirm the effectiveness of the AGD, reducing turn-on and turn-off switching energy imbalances. The major drawback lies on the additional components needed that would ultimately decrease the reliability of the system.

Commanding paralleled devices comes with many challenges from an engineering standpoint, first of all the need to select the gate driver IC that satisfies the necessities of the power stage. As per datasheet suggestion [73] the driving voltage is set between +15 V and −4 V. These two voltage levels will be fed by the isolated power supplies, one dedicated to high-side devices and the other for the bottom ones.
In this chapter, we look at the important factors to take into account when choosing a gate driver IC for SiC (Silicon Carbide) MOSFET designs. It is emphasised that more isolation is necessary to reduce noise, and that gate driver ICs are preferable to optocouplers because of their broader functionality and small form factor.
SiC MOSFET gate driver IC selection should prioritise the following features and characteristics [77, 78]:

Propagation Delay Minimization it is crucial to achieve the least amount of propagation delay possible. It guarantees that the SiC MOSFET can react quickly to control signals from the controller, which is essential when working with high-frequency systems where the switching period might be as little as 10 μs (as in this case). Quick response times are necessary to keep duty cycle distortions to a minimum.

Undervoltage Lockout (UVLO) UVLO acts as a monitor to keep track on the state of the power supply in the driving loop. Its goal is to ensure that the power supply keeps the specified voltage levels. The device must instantly begin a shutdown procedure and notify the controller if the voltage drops below the designated threshold. Setting a somewhat higher UVLO threshold and simultaneously checking the positive and negative supply voltages for a thorough evaluation of the power supply are prudent approaches.

Short Circuit Protection given the vulnerability of the high-side signal path to common-mode (CM) noise, which may result in spurious turn-ons and short circuits when the low-side gate signal is high, this protection mechanism is essential. It entails the rapid detection of device current during its on-state, requiring high bandwidth and an agile response. Desaturation (DeSat) protection, which is what this procedure is often known as, is used in the gate driver as a secondary short circuit protection mechanism even though SiC MOSFETs are less effective than IGBTs at it. The driver IC must produce a threshold voltage that is in line with the SiC MOSFET's output characteristics with the shortest possible time between detection and device shutdown in order to successfully implement this DeSat feature.

Active Miller Clamp (AMC) in order to keep the device's gate loop in a low-impedance condition when it is off, the AMC capability is crucial. With the help of this feature, cross-talk-induced noise currents are significantly reduced, resulting in minimum noise voltage changes at the gate voltage (VGS). The Miller Clamp works by sensing the device's gate voltage and turning on the low-impedance route as soon as it rises above the predetermined threshold. The on-state resistance of the AMC transistor inside the driver IC is often not as important since an external bipolar transistor is usually used to create the low-impedance route. It is therefore crucial to consider delays caused by internal gate resistors in the device package and set the Miller Clamp's threshold voltage lower than the device's threshold voltage.

In conclusion, careful consideration of propagation delay, UVLO, and short circuit protection features is crucial when choosing a gate driver IC for SiC MOSFET designs. The goal is to minimise delays, provide robust protective measures, and efficiently reduce noise for maximum device performance. This is especially important in high-frequency applications.
These considerations led to the selection of the UCC21710 gate driver IC from Texas Instruments, which provides all the features previously described. The IC presents 5.7 kV_{rms} capacitive isolation between primary (logic side, *cold*) and secondary (power side, *hot*), very low propagation delay (approximately 130 ns), and minimum dv/dt immunity (CMTI) of 150 V/ns, along with 270 ns response time fast overcurrent protection and a 4 A internal AMC.

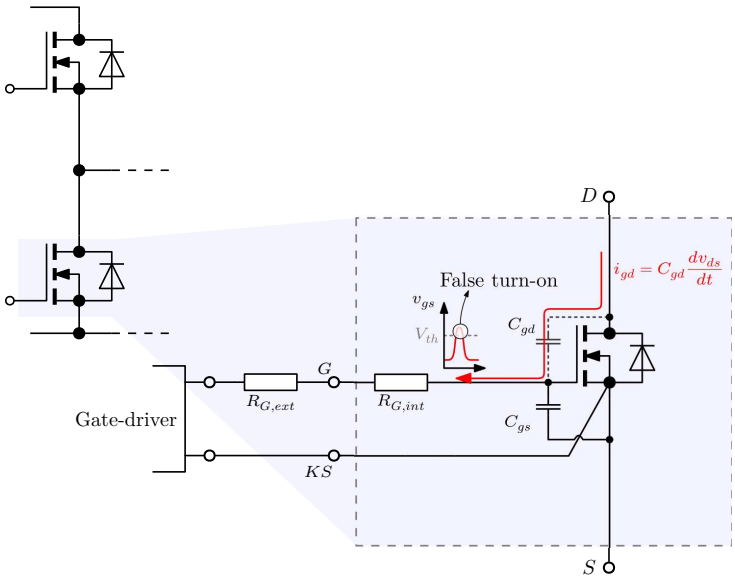


Figure 3.17: Cross-conduction due to current injection into low-side gate caused by C_{gd} Miller charging

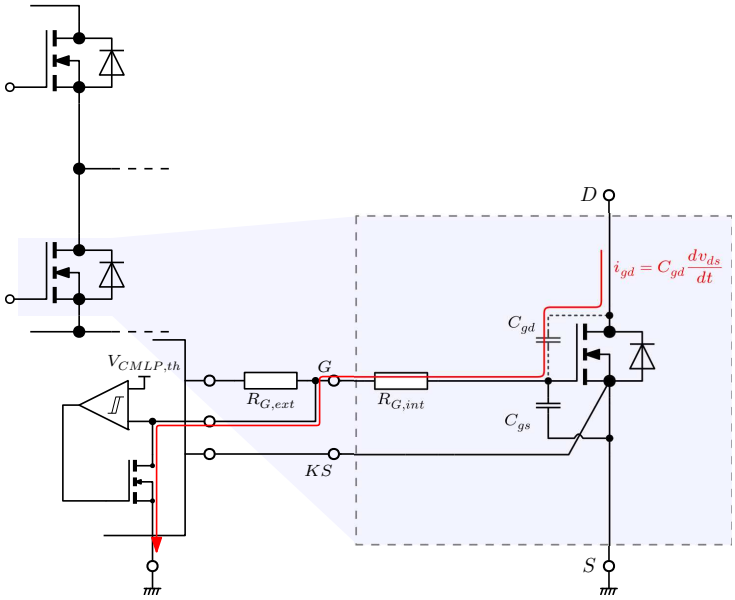


Figure 3.18: Miller clamp circuit, internally built on the selected GD IC (UCC21710)

To estimate whether or not the selected gate driver IC is good enough for the paralleled application. First and foremost let's analyze the Miller clamp capabilities of the device. When the upper SiC (Q1) is switched on in a half-bridge configuration, it induces a voltage change, dv_{ds}/dt, across the lower device (Q2). As a result, a current flows through the parasitic Miller capacitor C_{gd} and consequently the gate-to-source capacitance C_{gs} starts charging, carrying on the possibility of a false turn-on of the deactivated device as illustrated in Fig. 3.17.
The dv/dt of the device is around 150 V/ns while the C_{gd} is roughly 5 pF.

$$i_{gd} = C_{gd}\frac{dv_{ds}}{dt} \approx 750\ mA \tag{3.8}$$

The total Miller current is three times the value calculated in Eq. (3.8) because the devices are paralleled. However, the 4 A current specified in the datasheet is sufficient to accommodate the current requirements of all three devices.

The Active Miller Clamp (AMC) circuit, as detailed in Fig. 3.18, typically functions by monitoring the gate voltage when the device is in the off-state. It creates a low-impedance path to prevent the gate voltage from exceeding the threshold level [79]. However, a challenge arises when determining how to measure the gate voltage, especially when dealing with three paralleled devices. There's no guarantee that their gate voltages will behave the same during the Miller transition. The clamping circuit must effectively suppress any undesired current that might charge the gate interface during rapid dv_{ds}/dt. Therefore, deciding which of the three gate voltages should serve as a feedback line in the ACM circuit is a complex question.
To address this issue, a straightforward solution involves incorporating a diode in each of the three gate voltage measurements, as depicted in Fig. 3.19. This configuration ensures that the gate feedback voltage, i.e., the drain of the Miller switch (Q_{Mil}), will always assume the state of the highest of the three gate voltages. Consequently, it triggers the clamp as soon as one of the three devices surpasses the programmed threshold. Additionally, a pull-down resistor (approximately 10 $k\Omega$) is placed between the cathode node and ground. This prevents a floating state when the devices are turned on and all the gate voltages assume a +15 V state.

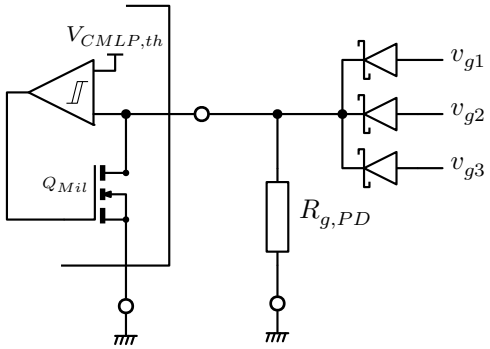


Figure 3.19: Miller clamp adaptation for the parallel case

The main drawback of the solution here presented lies in the voltage drop of the diodes. The ACM circuit will be triggered when the (highest) gate voltage reaches a value of $V_{CMLP,th} + V_f$ due to the forward biasing of the diode. The threshold $V_{CMLP,th}$ is set 2 V higher with respect to V_{EE} (i.e. the negative gate driver supply, $V_{EE} = -4$ V). Hence in this case the ACM is activated when

$$\max\{v_{gs1},\, v_{gs2},\, v_{gs3}\} > V_{EE} + 2\ V + V_f \approx -1.7\ V \tag{3.9}$$

In Eq. (3.9) a forward bias drop of 0.3 V is assumed, which is a reasonable value for a Schottky barrier diode such as XBS104V14R-G.
Each SiC device needs a certain amount of gate current in order to be turned on and off, which can be computed as

$$I_g = \frac{V_{CC} - V_{EE}}{R_{g\_int} + R_{g\_ext}} \tag{3.10}$$

To comply with the minimum sink/source capabilities of the GD IC, the following inequality must be respected

$$I_{sink/source} > 3I_g \tag{3.11}$$

For $R_{g\_ext} = 7.5\ \Omega$ the total gate current is ~ 5.25 A which is sufficiently smaller then the sink/source capability of the driver. In this case, an external gate resistor can be used for each SiC device in order to minimize imbalances in the gate loops

The main issue with this configuration lies in the difficulty on changing external gate resistor for further testing of the half-bridge units. Testing the case where $R_{g\_ext} = 7.5\ \Omega$ would be impossible, since that leads to $3I_g = 9.5$ A which is way too close to the maximum GD limitation. To overcome this problem, a current booster (CB) stage is added for every gate. In this way it's possible to decouple the weaker GD IC and let the CB handle the gate current of the device during turn-on and turn-off, at the expanse of added complexity and footprint area. The two solutions described are illustrated in Fig. 3.20

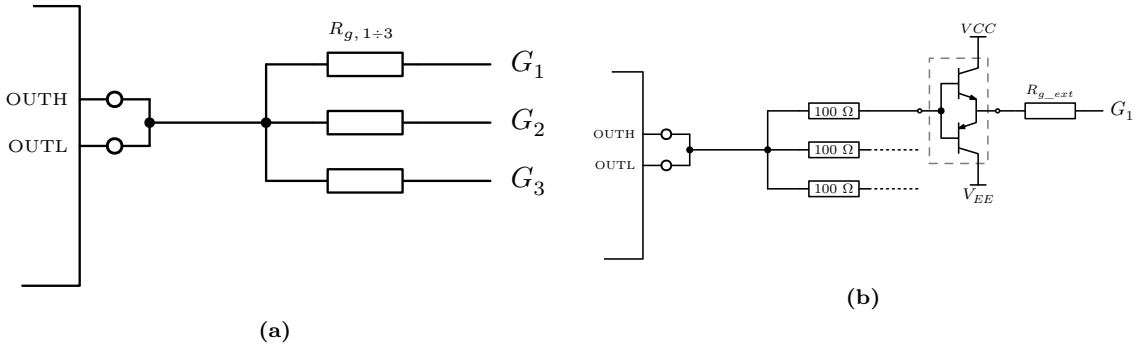


Figure 3.20: Each gate with its own gate resistance (**a**). Current booster solution (**b**)

Finally, the desaturation circuit is designed to tune the short-circuit intervention. The general scheme for desaturation is shown in Fig. 3.21.

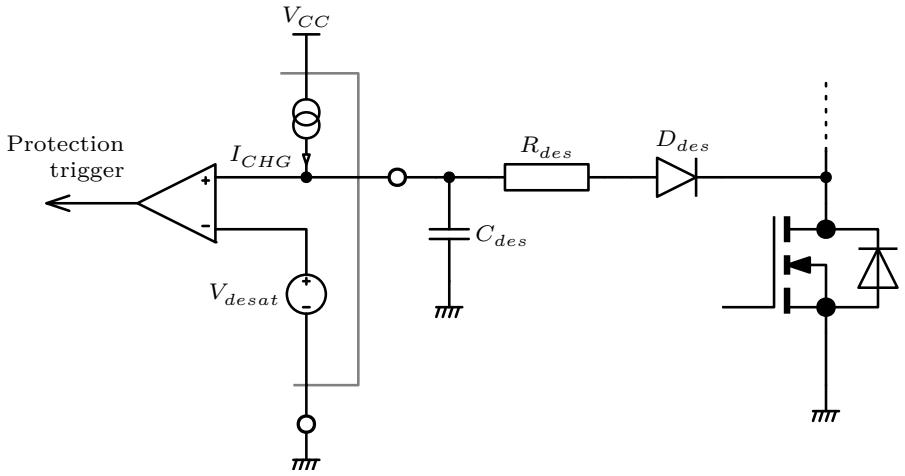


Figure 3.21: General desaturation scheme.

The desaturation strategy works by measuring the V_{ds} of the device while in ON-state. In this case, a small saturation voltage value is expected. If the voltage exceeds a user defined threshold (i.e. 6.5 V, that would trigger the protection when the drain-to-source current is around 100 A) the GD needs to turn-off the device. When operating correctly (in turn-on), C_{des} sits at the voltage level as $V_{ds\_ON} + V_f$ and the current I_{CHG} flows through the diode D_{des}. When an overcurrent event happens, the drain voltage becomes much bigger then the C_{des} voltage, hence the diode is reverse biased and the current I_{CHG} linearly charges the capacitor, until its voltage reaches V_{desat} (after which a shut-down process is initiated). The time it takes for the desaturation capacitor to fully reach the voltage threshold is called *blanking time*

$$t_{blank} = C_{des}\frac{V_{desat}}{I_{CHG}} \tag{3.12}$$

Many GD ICs implement the current source I_{CHG} internally, but this is not the case for this

particular design in which the current source for feeding the capacitor and setting the blanking time must be done externally.

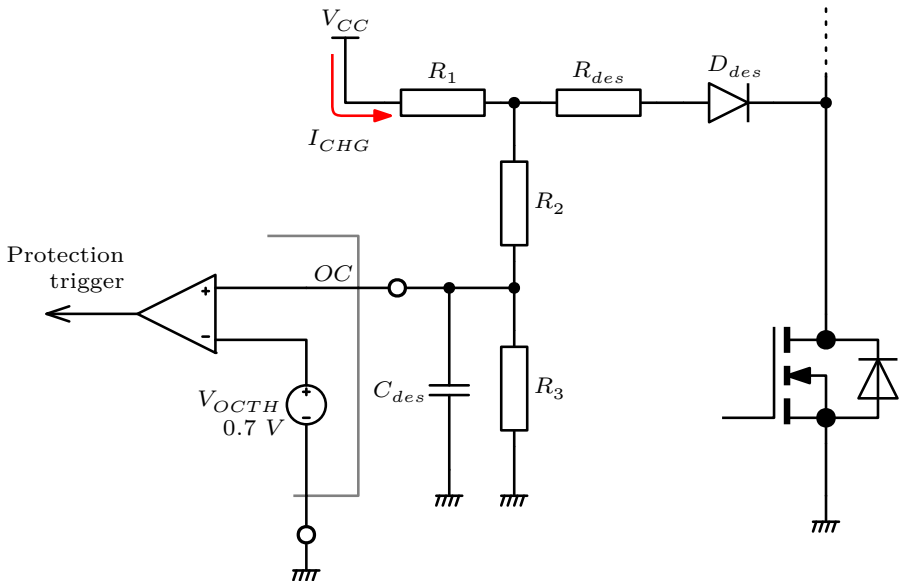


Figure 3.22: DeSat scheme of gate driver IC UCC21710.

In Fig. 3.22 the DeSat scheme for the UCC21710 is illustrated, which works similarly as the one already explained if not for minor differences. As anticipated there is no internal current source, hence the DeSat capacitor charging is done via resistor R_1 that acts as a current source. Finally, the voltage divider R_2/R_3 serves the purpose of selecting the desaturation voltage threshold. The equations for setting the DeSat threshold voltage and blanking time are

$$V_{DET} = V_{OCTH}\frac{R_2 + R_3}{R_2} - V_F \tag{3.13}$$

$$t_{BLK} = -\frac{R_1 + R_2}{R_1 + R_2 + R_3} R_3\, C_{blk}\, \ln\left(1 - \frac{R_1 + R_2 + R_3}{R_3}\frac{V_{OCTH}}{V_{CC}}\right) \tag{3.14}$$

In order to have a current source of roughly 500 μA, R_1 is selected as 30 $k\Omega$. The DeSat diode used in this work is the VS-E7MH0112-M3 [80] whose forward voltage drop V_F is around 0.6 and 1.0 V at low currents (depending on junction temperature). This allows to set R_2 and R_3 for defining the DeSat trip threshold, which is chosen to be 5 V. This would trip the GD in case of drain current exceeding 55 A at $T_j = 150^o$. These considerations lead to choosing $R_2 = 10\ k\Omega$ and $R_3 = 73\ k\Omega$.
Now that all parameters are known, setting t_{BLK} to 2 μs allows to find the needed capacitor value C_{blk}. After plugging in all the numbers, we obtain $C_{blk} = 300$ pF. The full schematic is illustrated in Fig. 3.23

3.3 Conclusions

Throughout this research, device layouts, particularly focusing on half-bridge configurations and the consequential parasitic effects, have been thoroughly explored. The detailed analysis of various design techniques, such as the double-sided return path, paralleled half-bridges, and paralleled SiC solutions, highlights the differences of layout strategies, crucial for optimizing switching performance. These findings emphasize the critical importance of understanding and mitigating parasitic elements in circuit design as well as the necessity of estimating their numerical quantities for a fair comparison.

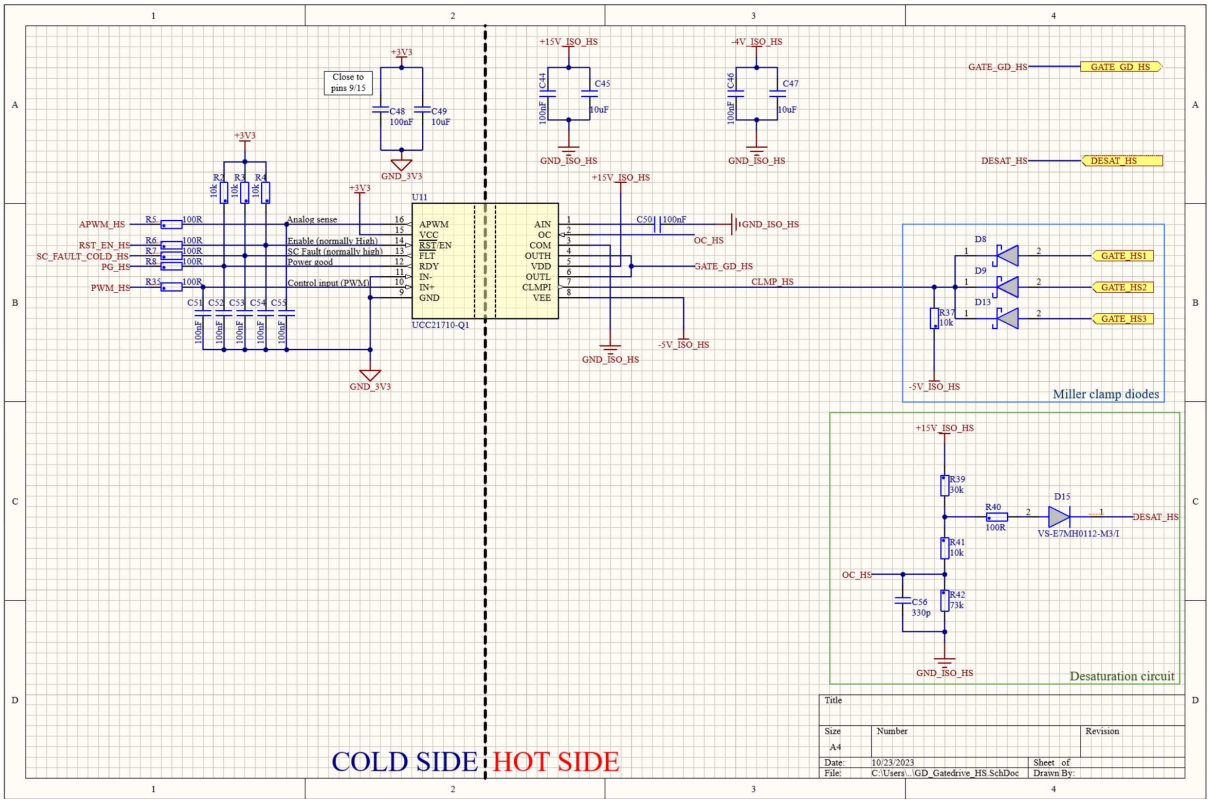


Figure 3.23: Full gate driver schematic.

Through meticulous LTSpice® simulations, the dynamic behaviors during the crucial turn-on and turn-off transitions of power devices have been analyzed. The research sheds light on the pivotal role of external gate resistance in controlling potentially destructive voltage overshoots, showcasing the delicate trade-off between system reliability and energy consumption.

We concluded this analysis by highlighting how paralleling the half-bridges is the best solution for this application, due to the possibility of decreasing by a factor of 2 the loop inductance if compared with the SiC hard-paralleling approach. The double-sided return path layout strategy has been discarded rather quickly since its unwanted added capacitance on the switching node would strongly increase the switching losses.

In conclusion, we emphasizes that in the ever-evolving field of power electronics, a holistic approach encompassing design, simulation, and real-world testing is indispensable. While challenges persist, through rigorous research and iterative optimization, we can continually push the boundaries of what's possible, driving the future of efficient, reliable, and high-performance power electronic systems. The findings of this research not only contribute significantly to academic understanding but also provide invaluable insights for industry applications, paving the way for more innovative and efficient electronic solutions in the years to come.

Furthermore n in-depth analysis led to the development and validation of the Active Gate Driver (AGD) which effectively leverages di/dt feedback control and master-slave strategy to ameliorate current sharing issues among paralleled devices.

This research presents a reduced BOM solution to the Miller clamp's challenges in a paralleled environment. Through a diode-based approach, we ensured that the Miller clamp engages whenever any of the paralleled devices gate voltage surpasses the GD Miller threshold.

The limited current capabilities of the state of the art gate driver ICs led to the necessity of incorporating a current booster stage, trading simplicity for footprint area.

In wrapping up, it's evident that engineering optimal gate driving designs for paralleled SiC MOSFETs requires a careful balance of theoretical foundations and design considerations. The

insights and methodologies delineated in this work present a substantial contribution to the power electronics domain, fostering advancements in high-power applications.

Chapter 4

Conclusion

This work explores the field of power electronics in extensive detail, including both the theoretical and practical elements of sophisticated converter systems. Starting from the difficulties faced by pulse-width modulation (PWM) inverters, in particular the distortions resulting from dead-times and switch voltage dips, are given considerable attention. Highlighting the need for a more sophisticated approach, a new compensation plan based on an intricate physical model of power converters is presented, and then creative self-commissioning methods using Multiple Linear Regression are evaluated.

The topic of electric mobility is covered in more detail, and a cutting-edge system architecture designed for range-extender systems is shown. By using silicon carbide (SiC) power devices in high-frequency converter modules and an integrated multi-phase PMSM, this study pushes the boundaries of developing a fault-tolerant and flexible solution for electric cars.

The LLC and Dual Active Bridge (DAB) DC/DC converters for on-board charging applications are examined in the second section of this thesis. The constraints of conventional techniques (FHA and EDF) for locating the LLC converter's small-signal model are addressed in this study. This research suggests employing a second-order discrete-time transfer function to approximate the converter's small-signal output current response rather of depending on these traditional methods, which frequently need a resistive load assumption. The coefficients of this transfer function vary according to the operational parameters, such as switching frequency and output voltage. A data-driven strategy utilising simulations and the LASSO machine learning method is used to optimise the coefficient fitting. The goal of the research is to use ML to approximate the output current response of a resonant converter in a precise and effective manner.

The Dual Active Bridge is another converter that is frequently employed in these kinds of applications. Bidirectional operation and galvanic isolation, two aspects that make this converter stand out, make it perfect for integrating with batteries, smart grids, and renewable energy sources. Due of its complex behaviour, control of it is still difficult. The capacity of the DAB converter to change the average output current without the aid of external dynamics is highlighted by this work's introduction of a thorough model for the device. This model provides information on the DAB converter's architecture, operating point choice, and control. Tested through simulations and tests, a novel control loop and a Finite Control Set (FCS) that guarantees the whole ZVS approach are proposed.

Furthermore, this study investigates several DC-DC converter designs for solid oxide fuel cell (SOFC) systems, emphasising their effectiveness and gravimetric power density in hydrogen storage and energy delivery systems. There are descriptions of important performance indicators such as ripple current limitations and rise/fall timings. We evaluate a number of converter topologies, including the three-level multi-channel buck and buck with active filter. For every topology, certain design elements are examined, ranging from switching frequencies to inductor values. The study's design optimisation process compares the converters' weight and efficiency using a Pareto analysis.

Last but not least, the hardware design of the prior converter is examined, with an emphasis on the value of PCB layout with regard to reducing parasitic components. The growing importance of silicon carbide is highlighted, paving the way for talks on gate driver designs that may take use of SiC's quick switching capabilities.
All things considered, this study is a cornerstone of power electronics, connecting theoretical developments with real-world applications to guarantee optimal performance in a variety of settings.

Part II

Isolated DC-DC converters for charging applications

Chapter 5

Steady-state solver for LLC

A literature review if the methods used for computing the steady-state solution of LLC converter is discussed. Since the input excitation of the system is periodical, there's no real steady-state solution intended as the nullifying of the state derivative, since every state variable is a periodic signal with same period as the one given by the excitation input. In this mathematical dissertation, no dead-times are considered.

$$\begin{aligned} \dot{\mathbf{x}}(t) &= \mathbf{f}(\mathbf{x}(t),\, \mathbf{u}(t)) \\ \mathbf{y}(t) &= \mathbf{g}(\mathbf{x}(t),\, \mathbf{u}(t)) \end{aligned} \tag{5.1}$$

where

$$\begin{aligned} \mathbf{x}(t) &= \sum_{k=-\infty}^{\infty} \mathbf{X_k} e^{jk\omega t} \\ \mathbf{u}(t) &= \sum_{k=-\infty}^{\infty} \mathbf{U_k} e^{jk\omega t} \end{aligned} \tag{5.2}$$

The following definitions apply: $\mathbf{x}$ is a N-column vector where N identifies the number of space-state variables; $\mathbf{u}$ is a M-column vector where M identifies the number of input variables of the system; $\mathbf{X_k}$ and $\mathbf{U_k}$ are $N \times 1$ and $M \times 1$ complex column vectors representing the state-variables amplitude (for space-state and input variables respectively) for the k^{th} harmonic. The idea of steady-state of a system indented as the condition where $\dot{\mathbf{x}}(t) = 0,\ \forall t \in [t,\, t+T)$ (with T being the period of the fundamental harmonic of the excitation signal $\mathbf{u}$) is not applicable here since, due to the definitions given in Eq. (5.2), this condition does never happen unless the trivial solution $\mathbf{X_k} = \mathbf{0},\ \forall k$ is wanted. Instead, a transformation to the Fourier domain is used. From Eq. (5.2), we find

$$\dot{\mathbf{x}}(t) = \sum_{k=-\infty}^{\infty} j\omega k \mathbf{X_k} e^{jk\omega t} \approx \sum_{k=-K}^{K} j\omega k \mathbf{X_k} e^{jk\omega t} \tag{5.3}$$

In Eq. (5.3) we introduced an approximation, where the state variable are approximated by a finite sum of Fourier harmonics.
The problem with the previous formulation is that there's no way to define the $\mathbf{X_k}$ and $\mathbf{U_k}$ quantities arithmetically unless a time-domain approach is adopted. From here on we will discuss an (semi-)analytical model for then finally being able to turn back to the Fourier analysis. More depth on the modelling approach that will be used hereinafter can be found in [81,82]. The assumption that allows the analytical computation of the critical state-variables during the steady-state operation is that after a full switching cycle, any state variable must assume the same value as the one given by the initial conditions at $\theta = 0$. This will be critical for the mathematical development. It can be proven that in half a switching period, there are at most 5 events that can happen (which ones and how many will depend on the working condition

of the converter) and all of them have an analytical formulation. Let's define some quantities. The normalized time variable is

$$\theta = \omega_0 t \tag{5.4}$$

where ω_0 is the main resonant frequency of the tank defined as:

$$\omega_0 = \frac{1}{\sqrt{L_r C_r}} = 2\pi f_0 \tag{5.5}$$

Let's define a normalized switching semi- period (half a period) as

$$\gamma = \omega_0 \frac{T_{sw}}{2} = \frac{\pi}{f_n} \tag{5.6}$$

where f_n is the normalized switching frequency with respect to the main resonance

$$f_n = \frac{f_{sw}}{f_0} \tag{5.7}$$

The base quantities that will be used from now on are

$$\begin{aligned} V_{\text{BASE}} &\equiv V_2 = nV_o \\ \omega_{\text{BASE}} &\equiv \omega_0 = \frac{1}{\sqrt{L_r C_r}} \\ Z_{\text{BASE}} &\equiv Z_0 = \sqrt{\frac{L_r}{C_r}} \\ I_{\text{BASE}} &\equiv \frac{V_2}{Z_0} \\ P_{\text{BASE}} &\equiv \frac{V_2^2}{Z_0} \end{aligned} \tag{5.8}$$

When the rectifying diodes do not conduct, a secondary resonance rises (hence the LLC is a multi-resonant topology)

$$\omega_1 = \frac{1}{\sqrt{(L_m + L_r) C_r}} \tag{5.9}$$

The ratio between resonant and magnetizing inductance is defined as

$$\lambda = \frac{L_r}{L_m} \tag{5.10}$$

thanks to which we have the following relations

$$k_1 \equiv \frac{\omega_1}{\omega_0} = \sqrt{\frac{\lambda}{1+\lambda}} \tag{5.11}$$

The normalised quantities are voltages and currents. The voltages will be indicated as $m_X(\theta)$ while the currents are $j_X(\theta)$. The system state variables are resonant capacitor voltage, resonant inductor current, magnetizing current, magnetizing voltage (corresponding with output voltage reflected to the primary) and output current. Symbolically, these are represented respectively by m_C, j_L, j_M, m_M and j_O.

$$\begin{aligned} m_X(\theta) &\equiv \frac{v_X(\theta/\omega_0)}{V_{BASE}} \\ j_X(\theta) &\equiv \frac{i_X(\theta/\omega_0)}{I_{BASE}} \end{aligned} \tag{5.12}$$

Half a switching period has (by definition) duration γ, and in this time frame 5 events denoted α_i happen. Every one of these smaller periods is contained between two angles θ_{i-1} and θ_i, such that

$$\begin{aligned}
\alpha_1 &\in [0, \theta_1) \\
\alpha_2 &\in [\theta_1, \theta_2) \\
\alpha_3 &\in [\theta_2, \theta_3) \\
\alpha_4 &\in [\theta_3, \theta_4) \\
\alpha_5 &\in [\theta_4, \gamma)
\end{aligned} \tag{5.13}$$

$$\sum_{i=1}^{5} \alpha_i = \gamma \tag{5.14}$$

It is possible to write the time dependant equations for all the currents and voltages in an half period as illustrated in Eq. (5.15). Depending on the operating condition, some of these equations will be used while some will be discarded.

$$\left.\begin{aligned}
m_C(\theta) &= \left(m_C(0) - \tfrac{1}{M} - 1\right)\cos\theta + j_L(0)\sin(\theta) + \tfrac{1}{M} + 1 \\
m_M(\theta) &= -1 \\
j_L(\theta) &= \left(-m_C(0) + \tfrac{1}{M} + 1\right)\sin\theta + j_L(0)\cos\theta \\
j_M(\theta) &= j_M(0) - \lambda\theta \\
j_O(\theta) &= j_M(\theta) - j_L(\theta)
\end{aligned}\right\} \quad \alpha_1,\ 0 \le \theta \le \theta_1$$

$$\left.\begin{aligned}
m_C(\theta) &= \left(m_C(\theta_1) - \tfrac{1}{M}\right)\cos(k_1(\theta-\theta_1)) + \tfrac{j_L(\theta_1)}{k_1}\sin(k_1(\theta-\theta_1)) + \tfrac{1}{M} \\
m_M(\theta) &= \left(\left(\tfrac{1}{M} - m_C(\theta_1)\right)\cos(k_1(\theta-\theta_1)) - \tfrac{j_L(\theta_1)}{k_1}\sin(k_1(\theta-\theta_1))\right)/(1+\lambda) \\
j_L(\theta) &= \left(\tfrac{1}{M} - m_C(\theta_1)\right)k_1\sin(k_1(\theta-\theta_1)) + j_L(\theta_1)\cos(k_1(\theta-\theta_1)) \\
j_M(\theta) &= j_L(\theta) \\
j_O(\theta) &= 0
\end{aligned}\right\} \quad \alpha_2,\ \theta_1 \le \theta \le \theta_2$$

$$\left.\begin{aligned}
m_C(\theta) &= \left(m_C(\theta_2) - \tfrac{1}{M} + 1\right)\cos(\theta-\theta_2) + j_L(\theta_2)\sin(\theta-\theta_2) + \tfrac{1}{M} - 1 \\
m_M(\theta) &= 1 \\
j_L(\theta) &= \left(\tfrac{1}{M} - 1 - m_C(\theta_2)\right)\sin(\theta-\theta_2) + j_L(\theta_2)\cos(\theta-\theta_2) \\
j_M(\theta) &= j_M(\theta_2) + \lambda(\theta-\theta_2) \\
j_O(\theta) &= j_L(\theta) - j_M(\theta)
\end{aligned}\right\} \quad \alpha_3,\ \theta_2 \le \theta \le \theta_3 \tag{5.15}$$

$$\left.\begin{aligned}
m_C(\theta) &= \left(m_C(\theta_3) - \tfrac{1}{M}\right)\cos(k_1(\theta-\theta_3)) + \tfrac{j_L(\theta_3)}{k_1}\sin(k_1(\theta-\theta_3)) + \tfrac{1}{M} \\
m_M(\theta) &= \left(\left(\tfrac{1}{M} - m_C(\theta_3)\right)\cos(k_1(\theta-\theta_3)) - \tfrac{j_L(\theta_3)}{k_1}\sin(k_1(\theta-\theta_3))\right)/(1+\lambda) \\
j_L(\theta) &= \left(\tfrac{1}{M} - m_C(\theta_3)\right)k_1\sin(k_1(\theta-\theta_3)) + j_L(\theta_3)\cos(k_1(\theta-\theta_3)) \\
j_M(\theta) &= j_L(\theta) \\
j_O(\theta) &= 0
\end{aligned}\right\} \quad \alpha_4,\ \theta_3 \le \theta \le \theta_4$$

$$\left.\begin{aligned}
m_C(\theta) &= \left(m_C(\theta_4) - \tfrac{1}{M} - 1\right)\cos(\theta-\theta_4) + j_L(\theta_4)\sin(\theta-\theta_4) + \tfrac{1}{M} + 1 \\
m_M(\theta) &= -1 \\
j_L(\theta) &= \left(-m_C(\theta_4) + \tfrac{1}{M} + 1\right)\sin(\theta-\theta_4) + j_L(\theta_4)\cos(\theta-\theta_4) \\
j_M(\theta) &= j_M(\theta_4) - \lambda(\theta-\theta_4) \\
j_O(\theta) &= j_M(\theta) - j_L(\theta)
\end{aligned}\right\} \quad \alpha_5,\ \theta_4 \le \theta \le \gamma$$

Now all the necessary instruments are ready in order to build an algorithm that allows to find the steady-state solution of an LLC converter given parameters and switching frequency.

5.1 Buck conversion ($M < 1$)

In buck mode, the voltage conversion ratio is smaller then unity ($M < 1$). In this case, the operating frequency can be bigger or smaller then resonance (f_0) and, for both subcases, it is possible to identify two operating modes: CCM (Continuous Conduction Mode), DCM (Discontinuous Conduction Mode) and cut-off (no energy transferred to the load). There is a total of 5 modes in buck-case: two CCM modes (above and below resonance), two DCM modes (both

above resonance) and one cut-off band (at higher frequencies). In Fig. 5.1 the operating modes are shown through a wide range of frequencies, while keeping constant the voltage conversion ratio M.

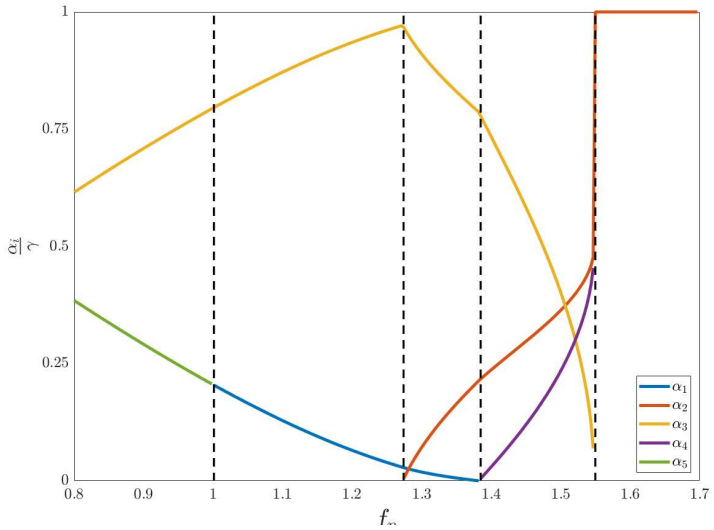


Figure 5.1: Operating modes in buck conversion with $\lambda = 0.5$, $M = 0.8$

5.1.1 Continuous Conduction Mode Above Resonance (CCMA)

In buck mode, when the frequency is bigger then the resonance point f_0, one of the possible modes is the Continuous Conduction Mode Above Resonance. The frequency range interested by this operating conditions is $1 < f_n < f_{crit}$, where f_{crit} is the critical frequency that separates the CCMA-mode by the DCMA-mode (we'll see later how to define this quantity). In this mode the magnetizing inductance voltage is always clamped to reflected the secondary voltage, hence the magnetizing inductance never participates in the resonance which is only composed by the resonant capacitor and inductor C_r and L_r respectively. This mode is also called (α_1, α_3) since these are the only two regions available. By considering Eq. (5.14) it is trivial to deduce the following relations valid in CCMA mode

$$\begin{aligned}
&\alpha_1 = \gamma/2 - \phi \\
&\alpha_3 = \gamma/2 + \phi \\
&\alpha_2 = \alpha_4 = \alpha_5 = 0 \\
&\theta_2 = \theta_1,\ \theta_3 = \theta_4 = \gamma \\
&\theta_1 = \alpha_1 = \frac{\gamma}{2} - \underbrace{asin\left(\frac{\gamma\lambda}{2}\cos\left(\frac{\gamma}{2}\right) + M\sin\left(\frac{\gamma}{2}\right)\right)}_{\phi}
\end{aligned} \tag{5.16}$$

The angle θ_1 is the one where the rectifier changes polarity and the normalized magnetizing voltage switches from $m_M(\theta)|_{\theta\in[0,\theta_1)} = -1$ to $m_M(\theta)|_{\theta\in[\theta_1,\gamma)} = +1$. The normalized magnetizing current is a triangular wave whose minimum happens at θ_1 and it is easy to prove it's value $j_M(\theta_1) = -\gamma\lambda/2$. In order to compute all the relative quantities, use Eq. (5.15, α_1) for $\theta \in [0, \theta_1)$ and Eq. (5.15, α_3) for $\theta \in [\theta_1, \gamma)$. In Fig. 5.2, an example of this condition is illustrated. It is possible to compute the boundary conditions analytically

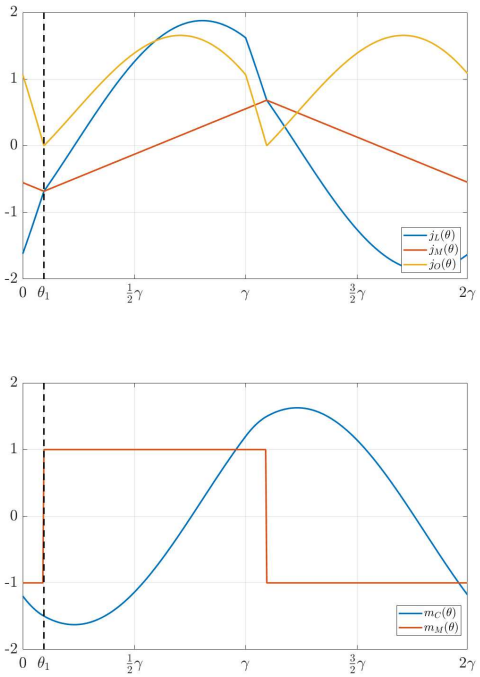


Figure 5.2: CCMA mode in buck conversion with $f_n = 1.15$, $\lambda = 0.5$, $M = 0.8$

$$
\begin{aligned}
m_C(0) &= 1 - \frac{\cos(\phi)}{\cos\left(\frac{\gamma}{2}\right)} \\
m_C(\theta_1) &= \frac{m_C(0)}{M} \\
j_L(0) &= \frac{\gamma\lambda M}{2} + \left(M - \frac{1}{M}\right)\tan\left(\frac{\gamma}{2}\right) \\
j_M(0) &= -\lambda\phi \\
j_M(\theta_1) &= -\frac{\gamma\lambda}{2}
\end{aligned}
\tag{5.17}
$$

The normalized output power p is equal to the average normalized output current $\overline{j_O}$, whose general formulation is

$$
p = \overline{j_O} = \frac{1}{\gamma}\sum_{i=1}^{5}\alpha_i \int_{\theta_{i-1}}^{\theta_i} j_O\left(\varphi\right) d\varphi \tag{5.18}
$$

which is possible to compute analytically in *CCMA* as

$$
p = \overline{j_O} = -\frac{2m_C(\theta_1)}{\gamma} \tag{5.19}
$$

5.1.2 Continuous Conduction Mode Below Resonance (CCMB)

The continuous conduction mode below resonance happens at frequencies smaller then resonance f_0 and it is interested by the modes (α_3, α_5) and has closed form solution.

$$
\begin{aligned}
\alpha_3 &= \frac{\gamma}{2} - \phi \\
\alpha_5 &= \frac{\gamma}{2} + \phi
\end{aligned}
\tag{5.20}
$$

where ϕ is computed as in (5.16), $\phi = asin\left\{(\gamma\lambda/2)\cos(\gamma/2) + M\sin(\gamma/2)\right\}$.

$$
\begin{aligned}
m_C(0) &= \frac{\cos(\phi)}{\cos(\frac{\gamma}{2})} - 1 \\
m_C(\theta_3) &= \frac{-m_C(0)}{M} \\
j_L(0) &= \frac{\gamma\lambda M}{2} + \left(M - \frac{1}{M}\right)\tan\left(\frac{\gamma}{2}\right) \\
j_L(\theta_3) &= j_M(\theta_3) = \frac{\gamma\lambda}{2} \\
j_M(0) &= -\lambda\phi
\end{aligned}
\tag{5.21}
$$

The angle θ_3 is the one where the polarity change on the rectifying diodes happens, hence for the magnetizing voltage we have $m_M(\theta)|_{\theta\in[0,\theta_3)} = +1$, $m_M(\theta)|_{\theta\in[\theta_3,\gamma)} = -1$. In Fig. 5.3 the waveforms obtained in mode are shown. Also in this condition the normalized output power

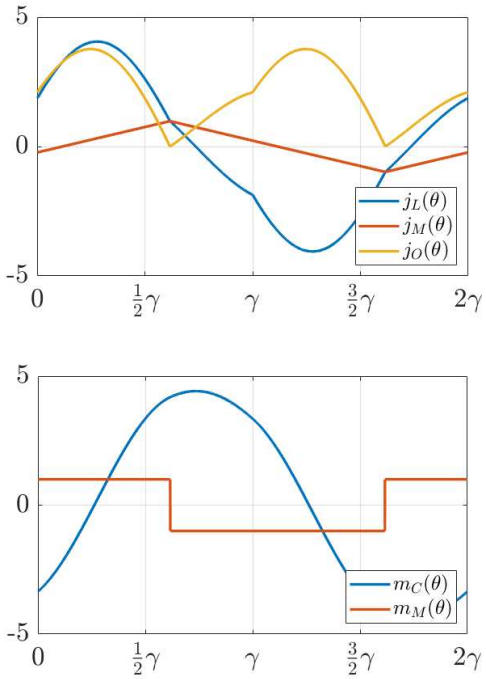


Figure 5.3: CCMB mode in buck conversion with $f_n = 0.80$, $\lambda = 0.5$, $M = 0.8$

can be compute analytically as

$$p = \overline{j_O} = \frac{2m_C(\theta_3)}{\gamma}$$

5.1.3 Discontinuous Condution Mode Above Resonance (DCMA)

This mode at higher frequencies after the CCMA mode. The frequency that separates these two intervals can be found by realizing that at the boundary CCMA/DCMA, $m_M(\theta_1) = 1$. It is possible to compute analytically the critical value of the conversion ratio M_{crit} such that the previous is valid. The result is shown below:

$$M_{crit} = \frac{1}{\sqrt{1 + \left[2\lambda + \lambda^2 + \left(\frac{\gamma\lambda}{2}\right)^2\right]\cos^2\left(\frac{\gamma}{2}\right) + \frac{\gamma\lambda}{2}\sin(\gamma)}} \tag{5.22}$$

If the conversion ratio is a given parameter and the frequency is unknown, solving numerically (i.e. via *secant method*) the above for γ_{crit} allows to find the solution after $f_{crit} = \pi/\gamma_{crit}$.
The DCMA mode is also called (α_1, α_2, α_3) and is distinguished by the CCMA due to the presence of the α_2 mode, where the magnetizing inductance joins the resonance and no power is delivered to the load. Since the presence of a new mode, the following must apply

$$\begin{aligned} \alpha_4 &= \alpha_5 = 0 \\ \alpha_1 &= \theta_1 \\ \alpha_2 &= \theta_2 - \theta_1 \\ \alpha_3 &= \gamma - \alpha_1 - \alpha_2 \end{aligned} \tag{5.23}$$

where θ_1 and θ_2 are two of the four unknowns along with $m_C(0)$ and $j_L(0)$, so that the vector of unknowns that is found by solving the non-linear system (discussed hereinafter) is

$$x = \begin{bmatrix} m_C(0) \\ j_L(0) \\ \theta_1 \\ \theta_2 \end{bmatrix} \tag{5.24}$$

Authors in [81] say that the equations governing this mode can be applied the same way here as it was done in the CCMA case, hence the formulas for computing $m_C(0)$, $m_C(\theta_1)$, $j_L(0)$, $j_L(\theta_1)$ and θ_1 apply here as well. The new unknown is the value at which the diode starts conducting again and power is delivered to the load, which happens at the angle θ_2. I am not sure that the formulas used in CCMA can be applied here without any "tailoring", since now the balance of magnetizing voltage and currents behave a little differently and the risk is that said equations can be used in DCMA just as an easy approximation for understanding the system behaviour. A more accurate approach would be to compute these quantities numerically by setting up a system containing all the necessary constrains.
Let's setup the non-linear system of equations to solve numerically like we will do from now on

$$\begin{cases} m_C(0) + m_C(\gamma) = 0 \\ j_L(0) + j_L(\gamma) = 0 \\ j_L(\theta_1) - j_M(\theta_1) = 0 \\ m_M(\theta_2) - 1 = 0 \end{cases} \tag{5.25}$$

This system is solved numerically by applying a trust-region-dogleg method [83] and the solution x of (5.24) is found. In Fig. 5.4 the waveforms for this working condition are shown.
The *DCMA* mode extends from frequency $f_n = f_{crit}$ to the point where α_1 goes to 0, after which the *DCMAB* mode takes place and the α_1 mode is substituted by α_4. In order to find this upper bound f_{DCMAB}, we need to write a system of equation where γ is not a parameter, but rather an unknown that we have to solve so that $f_{DCMAB} = \pi/\gamma_x$

$$\begin{cases} m_C(0) + m_C(\gamma_x) = 0 \\ j_L(0) + j_L(\gamma_x) = 0 \\ j_L(\theta_1) - j_M(\theta_1) = 0 \\ m_M(\theta_2) - 1 = 0 \\ \theta_1 = 0 \end{cases} \tag{5.26}$$

Maybe there is a more clever way to find this upper bound, but at the moment being this is the best solution that comes to my mind.
In this condition there is a dead-band (hence why it is a DCM working mode) where in α_2 no power is transferred to the load ($j_O(\theta) = 0$ for $\theta_1 \leq \theta < \theta_2$). The average normalized output current can be computed by applying Eq. (5.18) as follows

$$\overline{j_O} = \frac{\alpha_1}{\gamma} \int_0^{\theta_1} j_O(\varphi)\, d\varphi + \frac{\alpha_3}{\gamma} \int_{\theta_3}^{\gamma} j_O(\varphi)\, d\varphi \tag{5.27}$$

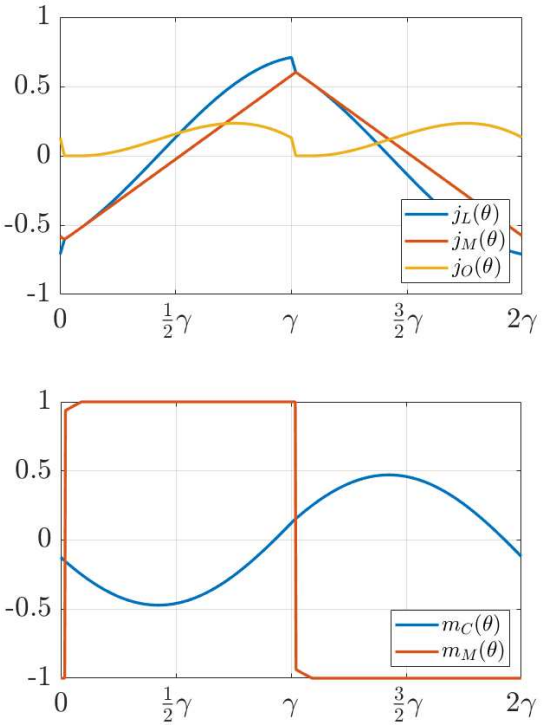


Figure 5.4: DCMA mode in buck conversion with $f_n = 1.30$, $\lambda = 0.5$, $M = 0.8$

5.1.4 Discontinuous Conduction Mode Above/Below in step down (DCMAB)

This mode presents the same behaviour in buck and boost conversion, where two non-power transfer modes arise and only one mode out of three transfers power to the load. This conversion state is reached at low power levels and consists of the regions (α_2, α_3, α_4). By considering (5.14) we have that:

$$\begin{aligned} &\alpha_1 = \alpha_5 = 0 \\ &\alpha_2 + \alpha_3 + \alpha_4 = \gamma \\ &\alpha_2 = \theta_2 \\ &\alpha_3 = \theta_3 - \theta_2 \\ &\alpha_4 = \gamma - \alpha_2 - \alpha_3 \end{aligned} \tag{5.28}$$

Literature does not seem to investigate in a full analytical solution for this mode (or for discontinuous modes in general for what is worth it), hence the solution must be sought numerically by solving the square problem in (5.29) with unknowns $x = [m_C(0),\, j_L(0),\, \theta_2,\, \theta_3]^\intercal$.

$$\begin{matrix} (*^I) \\ (*^{II}) \\ (*^{III}) \\ (*^{IV}) \end{matrix} \begin{cases} m_C(0) + m_C(\gamma) = 0 \\ j_L(0) + j_L(\gamma) = 0 \\ j_L(\theta_3) - j_M(\theta_3) = 0 \\ m_M(\theta_2) - 1 = 0 \end{cases} \tag{5.29}$$

This problem is solved numerically via trust-region-dogleg algorithm [83] and allows to find the four unknowns $m_C(0)$, $j_L(0)$, θ_2 and θ_3. The first two equations of (5.29) force the continuity for voltage and current. The terms $m_C(\gamma)$ and $j_L(\gamma)$ are computed using (5.15, α_4) and setting $\theta_4 = \gamma$. We now have two equations depending on unknowns $m_C(0)$, $j_L(0)$, $m_C(\theta_3)$, $j_L(\theta_3)$ and θ_3. Since $m_C(\theta_3)$, $j_L(\theta_3)$ do not belong to the problem formulation, we substitute these variables with their respective equations computed by applying (5.15, α_3). This operation leads to new equations where another set of unknowns shows up ($m_C(\theta_2)$ and $j_L(\theta_2)$). These are substitute by their respective equations in (5.15, α_2) in order to finally obtain equations that

contain the searched unknowns x. This process is illustrated in Eq. (5.30) only for the m_C.

$$\begin{aligned} m_C(\gamma) &= \left(\underline{m_C(\theta_3)} - \frac{1}{M}\right)\cos(k_1(\gamma-\theta_3)) + \frac{j_L(\theta_3)}{k_1}\sin(k_1(\gamma-\theta_3)) + \frac{1}{M} \\ \Rightarrow \underline{m_C(\theta_3)} &= \left(\underline{\underline{m_C(\theta_2)}} - \frac{1}{M} + 1\right)\cos(\theta_3-\theta_2) + j_L(\theta_2)\sin(\theta_3-\theta_2) + \frac{1}{M} - 1 \\ \Rightarrow \underline{\underline{m_C(\theta_2)}} &= \left(m_C(0) - \frac{1}{M}\right)\cos(k_1\,\theta_2) + \frac{j_L(0)}{k_1}\sin(k_1\,\theta_2) + \frac{1}{M} \end{aligned} \tag{5.30}$$

Equations $(*^{III})$ and $(*^{IV})$ of (5.29) are very easy to prove

$$\begin{aligned} &j_L(\theta_3) - j_M(\theta_3) = 0 \\ &j_L(\theta_3) - (j_M(\theta_2) + \lambda\,(\theta_3-\theta_2)) = 0 \end{aligned} \tag{5.31}$$

where $j_L(\theta_2)$ can be substituted by the relative equation as explained shortly before. Finally, solving $(*^{IV})$ using (5.15, α_2).

$$\left(\frac{1}{M} - m_C(0)\right)\cos(k_1\,\theta_2) - \frac{j_L(0)}{k_1}\sin(k_1\,\theta_2) - (1+\lambda) = 0 \tag{5.32}$$

In Fig. 5.5 the waveforms obtained in this mode are illustrated.

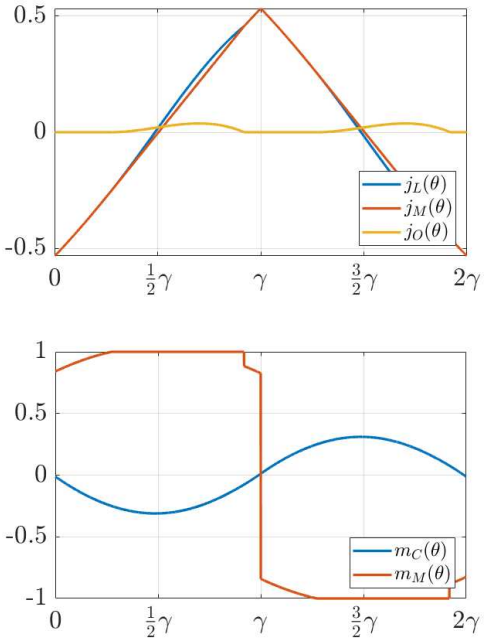


Figure 5.5: DCMAB mode in buck conversion with $f_n = 1.43$, $\lambda = 0.5$, $M = 0.8$

5.1.5 Cut-off Mode in step down

The cut-off is reached at higher frequencies where only the α_2 persists for the whole period. In cut-off, the diodes never turn on and the magnetizing inductance always participates in the resonance. In this mode the equations can be computed in closed form by taking (5.15, α_2) and solving for $m_C(0)$ and $j_L(0)$ the continuity boundary conditions

$$\begin{cases} m_C(0) + m_C(\gamma) = 0 \\ j_L(0) + j_L(\gamma) = 0 \end{cases} \tag{5.33}$$

we find that

$$\begin{aligned} m_C(0) &= 0 \\ j_L(0) &= -\frac{k_1}{M}\tan\left(\frac{k_1\gamma}{2}\right) \end{aligned} \tag{5.34}$$

If the frequency at which the cut-off mode starts is requested, the following considerations are made: at half-way through the half-period, when $\theta = \gamma/2$, the peak of magnetizing voltage is reached. If the frequency is such that we are exactly at cut-off (i.e. $f_n = f_{CO}$ hence $\gamma = \gamma_{CO}$), the following relation holds

$$m_M\left(\frac{\gamma_{CO}}{2}\right) = 1 \tag{5.35}$$

Since the cut-off region is composed by the mode α_2, we use the relative equations to solve the previous selecting γ_{CO} as an unknown

$$\begin{aligned} \gamma_{CO} &= \frac{2}{k_1} acos\left(\frac{1}{M(1+\lambda)}\right) \\ \Rightarrow f_{CO} &= \frac{k_1\frac{\pi}{2}}{acos\left(\frac{1}{M(1+\lambda)}\right)} \end{aligned} \tag{5.36}$$

If

$$M(1+\lambda) < 1$$

Eq. (5.36) cannot be solved any more due to the *acos* function argument becoming bigger the 1. This means that, physically, there exists no frequency that allows to regulate down to zero current. This of course only happens in buck conversion for

$$M_{nCO} < \frac{1}{1+\lambda}$$

5.2 Boost conversion ($M > 1$)

In boost mode the voltage conversion ratio is bigger then unity ($M > 1$). In this case, the operating frequency can only be smaller then resonance (f_0) since there exists a frequency point (*cut-off*) above which no transfer power to the load is seen. This frequency limit is computed exactly the same way as it would be in buck conversion. At lower frequencies, we can see the following modes (from left to right): CCMB (α_3, α_5), DCMB1 (α_3, α_4, α_5), DCMB2 (α_3, α_4), DCMAB (α_2, α_3, α_4) and cut-off.

5.2.1 Discontinuous Conduction Mode Below Resonance 1 (DCMB1)

This mode, known also as (α_3, α_4, α_5), is unique to the boost operation and is separated by the CCMB mode at the frequency point where $m_M(\theta_3) = -1$. The separation point between CCMB and DCMB1 (in boost conversion) is computed exactly as it is in buck for defining the threshold between CCMA and DCMA, hence by using Eq. (5.22).
Given as parameters the conversion ratio and working frequency (hence γ), we need to find the unknowns for this working mode which are the current and voltages initial conditions $m_C(0)$, $j_L(0)$ and the two angles θ_3 and θ_4 that distinguish this operating condition. No analytical solution is available for this problem, which means that a numerical approach needs to be implemented by non-linear functional minimization (a trust-region-dogleg algorithm was used in this case [83]), where the problem formulation is illustrated in Eq. (5.37) with unknowns $x = [m_C(0),\, j_L(0),\, \theta_3,\, \theta_4]^\intercal$

$$\begin{cases} m_C(0) + m_C(\gamma) = 0 \\ j_L(0) + j_L(\gamma) = 0 \\ j_L(\theta_3) - j_M(\theta_3) = 0 \\ m_M(\theta_4) + 1 = 0 \end{cases} \tag{5.37}$$

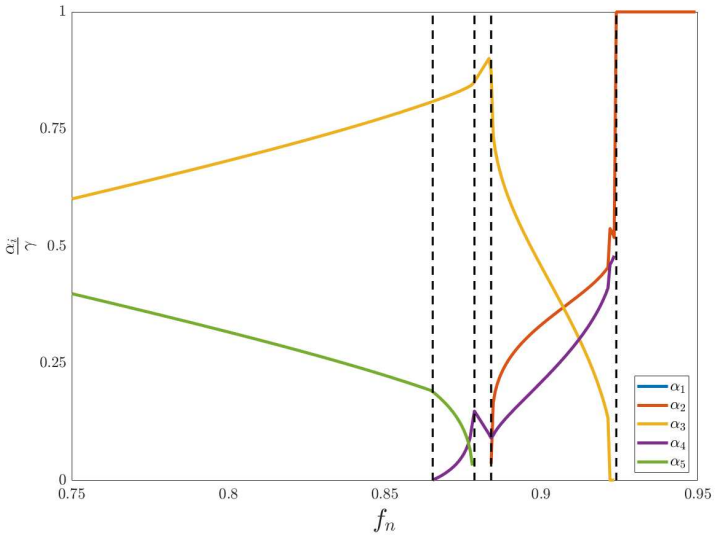


Figure 5.6: Operating modes in boost conversion with $\lambda = 0.5$, $M = 1.2$

A more in-depth explanation on how to set up the system is illustrated from here on out. The DCMB1-mode only contains the time evolutions (α_3, α_4, α_5). This means that $\alpha_1 = \alpha_2 = 0$ and $\theta_0 = \theta_1 = \theta_2 = 0$. By applying (5.14) we have that $\alpha_3 + \alpha_4 + \alpha_5 = \gamma$. Given this information the following relations are found

$$\begin{aligned} \alpha_3 &= \theta_3 \\ \alpha_4 &= \theta_4 - \theta_3 \\ \alpha_5 &= \gamma - \alpha_3 - \alpha_4 \end{aligned} \tag{5.38}$$

The terms $m_C(\gamma)$ and $j_L(\gamma)$ are computed using (5.15, α_5) setting $\theta = \gamma$ hence the first two equations of (5.37) can be written as

$$\begin{aligned} &m_C(0) + \left(m_C(\theta_4) - \frac{1}{M} - 1\right)\cos(\gamma - \theta_4) + j_L(\theta_4)\sin(\gamma - \theta_4) + \frac{1}{M} + 1 = 0 \\ &j_L(0) + \left(-m_C(\theta_4) + \frac{1}{M} + 1\right)\sin(\gamma - \theta_4) + j_L(\theta_4)\cos(\gamma - \theta_4) = 0 \end{aligned} \tag{5.39}$$

$m_C(\theta_4)$ and $j_L(\theta_4)$ are computed using (5.15, α_4) and setting $\theta = \theta_4$. This leads to a pair of equations where unknown terms in θ_3 arise (specifically $m_C(\theta_3)$ and $j_L(\theta_3)$), which still "do not belong to the problem". At this point, using (5.15, α_3) we will obtain terms depending on θ_2 (specifically $m_C(\theta_2)$ and $j_L(\theta_2)$) which, by constrains, is null $\theta_2 = 0$. This leads to a pair of equations (5.39) that only depend on the unknowns $x = [m_C(0),\, j_L(0),\, \theta_3,\, \theta_4]^\intercal$. Finally, the last two equations of (5.37) need to be studied. Let's start from the 3^{rd} term:

$$\begin{aligned} &j_L(\theta_3) - j_M(\theta_3) = 0 \\ &j_M(\theta_3) = j_M(0) + \lambda\theta_3 \\ &j_M(0) = j_L(-\theta_4) + \lambda\,(\gamma - \theta_4) = -j_L(\theta_4) + \lambda\,(\gamma - \theta_4) \\ &\Rightarrow j_L(\theta_3) + j_L(\theta_4) - \lambda\,(\gamma + \theta_3 - \theta_4) = 0 \end{aligned} \tag{5.40}$$

The last line of (5.37) is the easiest, since the equation describing the magnetizing voltage $m_M(\theta)$ needs to be set equal to -1 using (5.15, α_4). A solution of this operating mode is shown in Fig. 5.7.

5.2.2 Discontinuous Conduction Mode Below Resonance 2 (DCMB2)

This mode is found right after the DCMB1 and happens when α_5 portion goes to zero, therefore only the (α_3, α_4) sections remain. The unknowns in this case are only three $x = [m_C(0),\, j_L(0),\, \theta_3]^\intercal$,

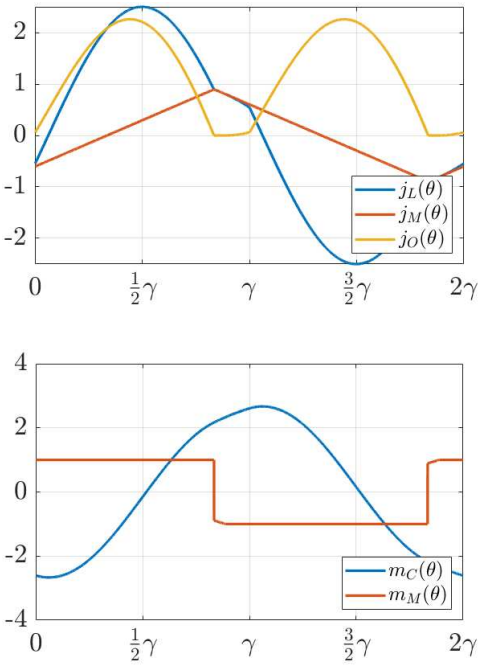


Figure 5.7: DCMB1 mode in boost conversion with $f_n = 0.875$, $\lambda = 0.5$, $M = 1.2$

which can easily be found following the usual process of problem minimization

$$\begin{aligned} m_C(0) + m_C(\gamma) &= 0 \\ j_L(0) + j_L(\gamma) &= 0 \\ j_L(\theta_3) - j_M(\theta_3) &= 0 \end{aligned} \tag{5.41}$$

In Fig. 5.8 the waveforms for this mode are shown. The main problem of this mode is that

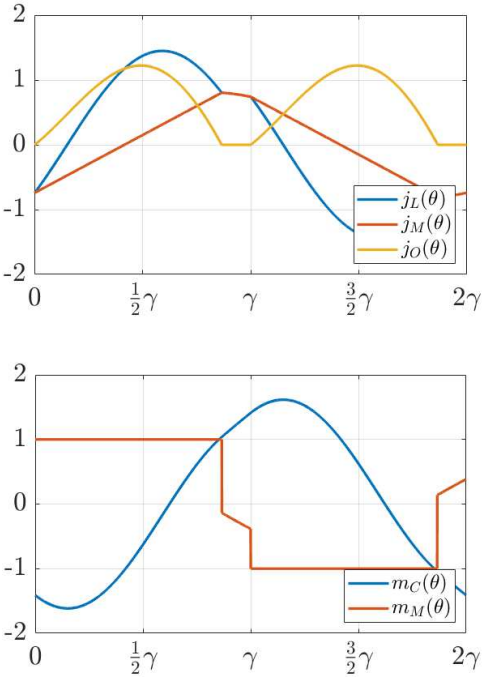


Figure 5.8: DCMB2 mode in boost conversion with $f_n = 0.880$, $\lambda = 0.5$, $M = 1.2$

it is not easy to understand its boundary with the DCMBAB. I couldn't figure out a clever

way to understand the DCMB2/DCMBAB threshold, hence I implemented something similar to the strategy proposed in [82] which is a bit cumbersome to some extent. They define a "test variable" $m_{m2}(\theta)$ that is defined as the magnetizing voltage value at some crucial point where the discontinuity happens.

$$m_{m2}(\theta) = \frac{\frac{1}{M} - m_C(\theta)}{1+\lambda} \tag{5.42}$$

They use this variable computed at precise values of θ in order to understand if their initial guess was correct or not. For example, imagine that the converter is working in boost mode $M > 1$ at some frequency f_n. They first solve the *DCMB1* problem and finally test for $|m_{m2}(0)| \geq 1$ and $|m_{m2}(\gamma)| \leq 1$. If both these conditions hold, the initial *DCMB1* assumption was correct; if not, another solution is computed for a different working mode and the test is once again evaluated until it returns positive result. This method is somewhat laborious and having a trick for defining exactly the boundaries between modes is to be preferred. In some cases, these barriers can be computed analytically while is some other cases numerically. Here none of the two is an available choice therefore, only for this case, we use the m_{m2} test method. If $f_{DCMB2} < f_n < f_{CO}$, the *DCMB2* mode is assumed and the relative test is computed after solving the system

$$\begin{cases} |m_{m2}(0)| \geq 1 \\ |m_{m2}(\theta_3)| \leq 1 \\ |m_{m2}(\gamma)| \geq 1 \end{cases} \tag{5.43}$$

If the test in (5.43) holds, the system is working in *DCMB2*-mode, if not it is in *DCMAB* and a new solution shall be computed.

5.2.3 Discontinuous Conduction Mode Above/Below in step up (DCMAB)

This mode presents exactly the same principles as the DCMAB seen in buck conversion. When operating in boost this operation is seen *below* resonance, unlike the step down case where it happens above the resonance point. See Section 5.1.4 for more information. In Fig. 5.9 the waveforms of this mode are shown.

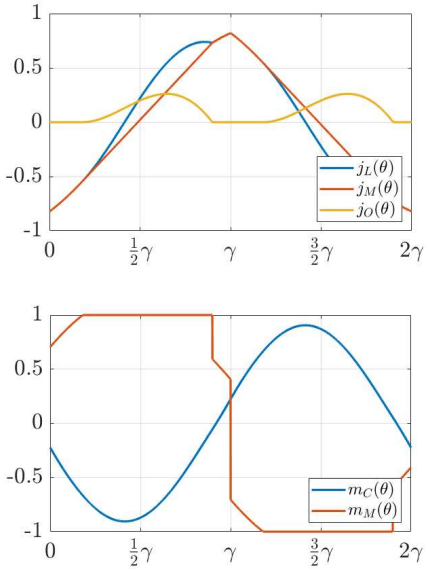


Figure 5.9: DCMAB mode in boost conversion with $f_n = 0.885$, $\lambda = 0.5$, $M = 1.2$

5.3 Critical aspects of this approach

The most critical aspect of this approach is the initial condition selection for the minimization algorithms. Up to this point whenever a problem was brought up, we limited ourselves into writing the set of equations describing said problem and stating that it is possible to solve it by using some algorithm widely studied in literature. All the functions are continuous and differentiable since they can be written as sums of trigonometric components, hence the Jacobians needed to compute the minimization is real and bounded meaning that the problem is "easy to solve". The possibility of accepting multiple zeros, however, poses a non trivial challenge for many of the previously discussed solutions. If a minimization procedure locks on a wrong zero solution, everything that comes afterwards will be not reliable even though - mathematically speaking - the result appears to be correct. Avoiding these misbehaviours and being sure that the solution is always the correct one should become a priority and, at the same time, is a though challenge to face since at the eyes of the solver a zeros solution is no different from all the others. Let's take as an example Eq. (5.22) which is needed to find the threshold between CCMA and DCMA in buck conversion. This formula is solved numerically via *secant method*, which needs two initial conditions (we call them x_0 and x_1). If the conversion rate M is set to a value of 0.8 (and the parameter λ is kept to 0.5 as has been done up to this point) and try to find critical frequency starting from $x_0 = 2.4166$ and $x_1 = 2.0944$, the algorithm reaches convergence after 9 iterations with an error of approximately $\epsilon \approx 4 \times 10^{-5}$ resulting in a value of $\gamma_{crit} = 2.4685$ which leads to $f_{crit} = 1.2727$. However, if we change the initial conditions to $x_0 = 31.4159$ and $x_1 = 1.4280$ we reach the opposing result (hence $\gamma_{crit} = -2.4685$ and $f_{crit} = -1.2727$) in 13 iterations, but this value is completely wrong! A better approach would be to adopt an algorithm that takes into account some boundary conditions (i.e. $f_{crit} > 1$) and to update the initial guess $[x_0, x_1]$ (somehow, still to be discussed) depending on the working conditions. These cues should be applied to this specific case and every other problem that needs an initial estimation to converge correctly.

Chapter 6

LLC Small-signal modelling

To understand the small-signal model of the CL^{2}C it is better to start from the LLC (Fig. 6.1) since it is mathematically easier. Once the small-signal model is complete, these results will be used for control system design and tuning.

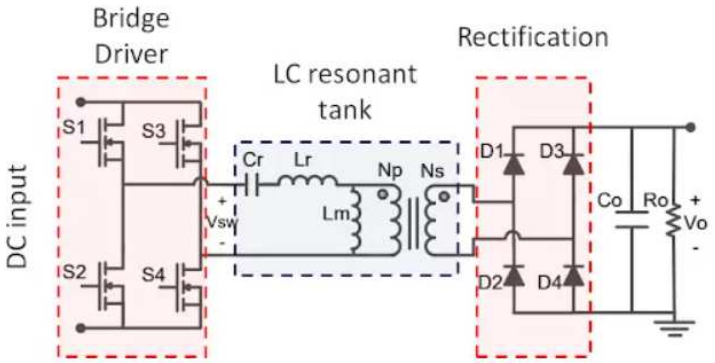
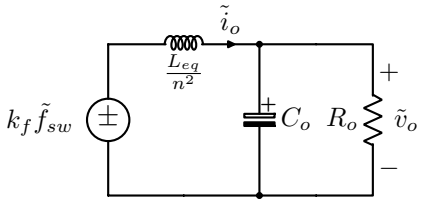
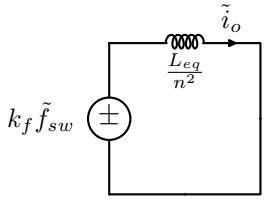


Figure 6.1: Unidirectional LLC schematic

Many authors have developed different approaches for designing the control system once the small-signal model is available [8,84]. As stated in [8], usually the most critical design point is the resonant condition (f_r) where the output voltage response v_o due to a modulation frequency variation δf_{sw} in the vicinity of the resonance resembles a second order system with poor dumping. The authors in this case propose a 2^{nd} order small-signal model equivalent circuit obtained by analysing dominant poles and zeros of the system around the resonance point, illustrated in Fig. 6.2a. In Fig. 6.2b the proposal of the authors in [84] is illustrated, where they approximate the small-signal circuit for the current-to-frequency response with a pure integrator.



(a) Equivalent small-signal II-order circuit as in [8]



(b) Equivalent small-signal circuit as in [84]

Figure 6.2: Equivalent circuits for small-signal modelling of the LLC converter. The proposal in 6.2b will be proven to be way too approximated, and often time completely wrong

As it is possible to see in Fig. 6.3 the matching between analytical and simulated result is good up until a frequency variation comparable with the resonance of the equivalent circuit (namely

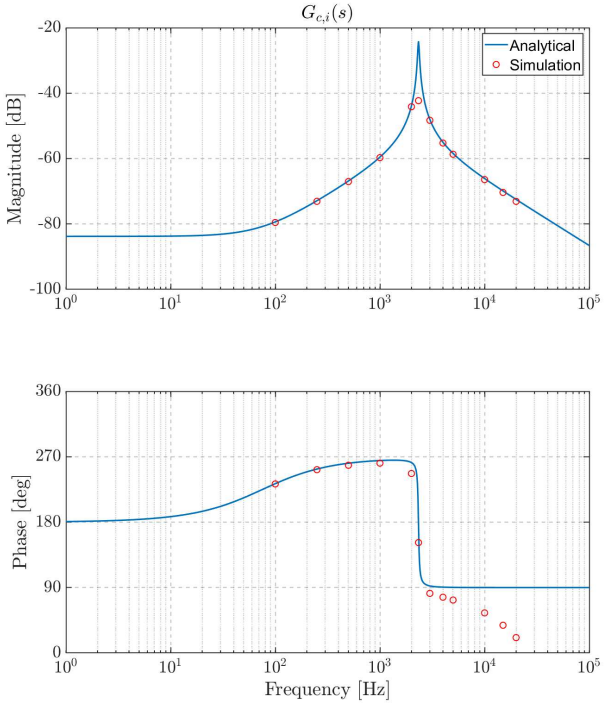


Figure 6.3: Comparison between equivalent second order output current small signal circuit and actual simulation of the LLC small-signal behaviour around the resonant point

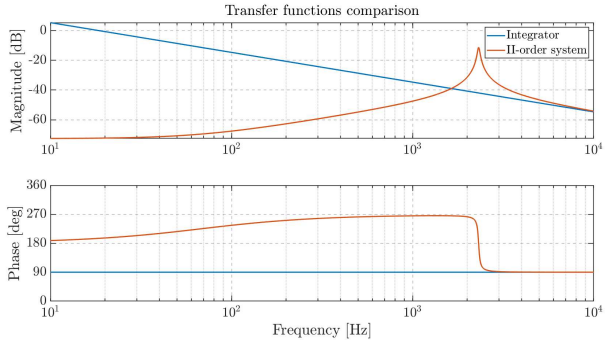


Figure 6.4: Comparison between the two proposed small-signal models for the $\tilde{i}_o/\tilde{f}_{sw}$ transfer function

f_{eq} as defined in [8]) which in this example is $f_{eq} \approx 2.34$ [kHz], after which the phase starts to differ. Also, the gain at this point seems not be predicted accurately by the analytical model. We obviously assumed that the simulation result is correct (as one would do when testing an analytical approximation), hence this mathematical model candidate might not be the best when trying to close loops at high bandwidths. In this particular case, 1 kHz bandwidth might be unreachable since the behaviour around f_{eq} is not easy to predict. Also, the transfer function behaviour depends on the equivalent output load as shown in Fig. 6.5, which makes controlling the current right after the rectifier (but before the output filter, indicated as i_o in Fig. 6.1) a very challenging task.

As per the control design, in [84] a proposal is made which aims at taking into consideration the plant and digital control delays in order to tune a PI controller that allows for a certain stability margin set by the user. However a huge mistake was made in their analysis, making their proposal wrong. The plant transfer function they used is strongly approximated. There are two cases which are interesting to analyse: the *voltage-to-frequency* and *rectified-current-to-frequency* transfer functions. In the context of this analysis the term transfer function is used for identifying the small signal behaviour of an observed quantity (i.e. output voltage

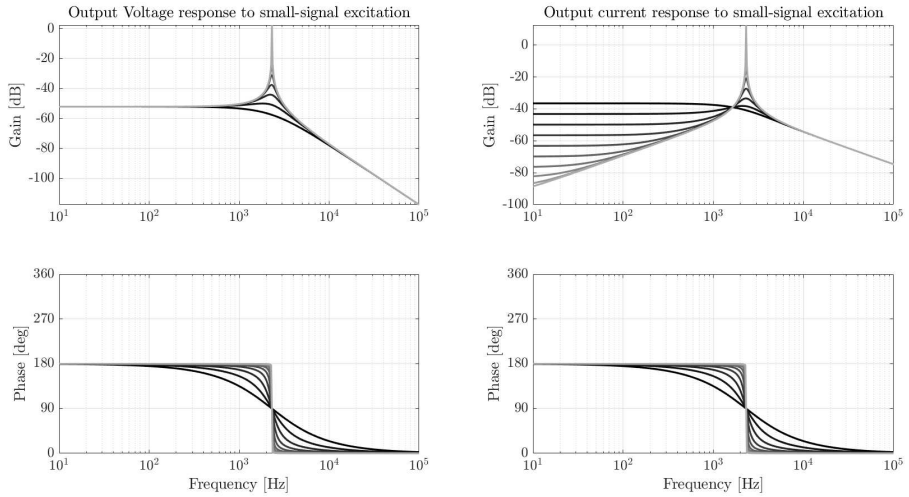


Figure 6.5: On the left the voltage-to-frequency ($\tilde{v}_o/\tilde{f}_{sw}$) transfer function is plotted for different resistive loads while the current-to-frequency characteristic ($\tilde{i}_o/\tilde{f}_{sw}$) is on the right. Darker lines are used for smaller load resistances (i.e. bigger output power) while brighter ones indicated higher loads (i.e. smaller output power).

or current) caused by a small variation of the modulation frequency which, for the moment being, is composed by the summation of a carrier component Ω_0 at resonant frequency and a sinusoidal modulating function around that point. The aforementioned operation is equivalent to a narrowband frequency modulation (FM) where the sidebands are much smaller then the carrier in terms of amplitude (i.e. -40 dBc) and the total signal bandwidth is narrow, hence the modulating function bandwidth (which for simplicity is chosen to be *isofrequential* i.e. sinusoidal) is much smaller then the carrier. Specifically, it has to be lower then Nyquist frequency. The spectral lines are composed so that the modulation frequency is $\omega_s = \Omega_0 \pm \Delta_\Omega$, as highlighted in Fig. 6.6.

Table 6.1: Two different ways of approximating the current-to-frequency small-signal transfer function

$G_{c,i}(s)$ for [8]	$G_{c,i}(s)$ for [84]
$\frac{k_f\left(\frac{1}{R_o}+sC_o\right)}{1+s\frac{L_{eq}}{n^2R_o}+s^2\frac{L_{eq}C_o}{n^2}}$	$\frac{n^2k_f}{sL_{eq}}$

In Tab. 6.1 the red transfer function assumes that the plant is a pure integrator, which is not true in the whole frequency range since it has been proven by simulations in Fig. 6.3 that the model highlighted in blue is a better candidate for understanding the small-signal behaviour of the converter, even though some adjustments can be made so that the matching accommodates a wider modulation range. When $\tilde{f}_{sw} \gg f_{eq}$, then the pure integrator approximation introduced by [84] might be valid. In terms of equations we have (6.1), where the *hf* superscript indicates the high-frequency approximation which results in the pure integrator small-signal plant. The equations transfer function Bode plots are shown in Fig. 6.4.

$$\begin{aligned} G^{hf}_{c,i}(s) &= \frac{\tilde{i}_o}{\tilde{f}_{sw}} \approx \frac{n^2 k_f}{sL_{eq}} \\ G_{c,i}(s) &= \frac{\tilde{i}_o}{\tilde{f}_{sw}} \approx \frac{k_f\left(\frac{1}{R_L}+sC_o\right)}{1+s\frac{L_{eq}}{n^2R_L}+s^2\frac{L_{eq}C_o}{n^2}} \end{aligned} \tag{6.1}$$

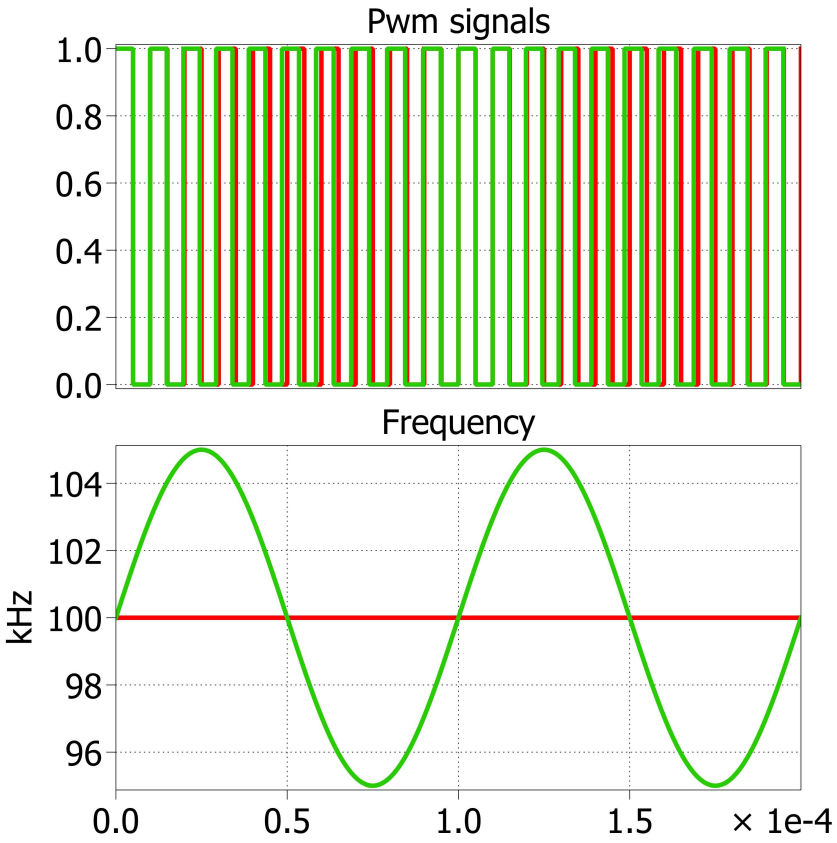


Figure 6.6: PWM command signals and frequency signal under FM modulation. In red there's no frequency modulation, while in the green plots a 5% modulation at 10 kHz is applied. The modulation function can be written as $f_\Delta \cos(2\pi f_m t)$ where f_Δ is 5% of the carrier frequency (i.e. 5 kHz) and f_m is the modulation frequency, set at 10 kHz

6.1 Control design with high-frequency approximation

Let's start from the control design supposing that the high frequency approximation is valid. In order to do so, we need to make sure that the current controller bandwidth is high enough, hence the compensator parameters (which in this case are $K_{p,i}$ and $K_{i,i}$ since for now we're using this in order to start with things as easy as possible) need to be tailored so that the open loop response cut-off frequency is on the high-end side of the spectrum, hence much bigger than f_{eq} but small enough to respect the Nyquist limit i.e smaller then $F_c/2$, where F_c is defined as the control frequency. For the case in exam, we have the parameters shown in Table 6.2 Just by looking at the parameters set, we realize it is difficult to satisfy both the high-frequency and Nyquist condition at the same time. Consider also an important factor: the Nyquist point is decided by the control frequency F_c which in this example has been chosen equal to the resonance but in many cases needs to be set smaller due to computational burden constrains, hence reducing the Nyquist limit even more. In the face of these considerations, a current controller cut-off frequency in the order of $f_{0,i} \approx 10$ kHz is selected, leading to the question on how to pick the proportional and integral gain in order to meet this requirement. In [84] the authors offer a set of equations for calculating the current controller parameters once phase margin m_φ and k_z (defined as the ratio between crossover frequency and the PI controller zero). These set of equations also takes into account the delays introduced by the digital control. Some approximations in (6.2) and (6.3) are introduced when $k_z \ll 1$.

Parameter	Description	Value
V_{DC}	Input bus voltage	400 [V]
n	Transformer ratio (N_p/N_s)	1
L_r	Resonant inductance	8.7 [μH]
L_m	Magnetizing inductance	25.3 [μH]
C_r	Resonant capacitor	147 [nF]
C_o	Output capacitor	220 [μF]
R_o	Output resistance	10.167 [Ω]
f_r	Resonant frequency	140.6 [kHz]
F_c	Control frequency	140.6 [kHz]
f_{Ny}	Nyquist frequency	70.3 [kHz]
f_{eq}	Resonant freq of ss-circuit	2.32 [kHz]
L_{eq}	Equivalent circuit inductance	21.5 [μH]
k_f/V_{DC}	Normalized TF gain	-6.22e-06 [1/Hz]

Table 6.2: Parameters table

$$\begin{aligned}\omega_{0,i} = & \frac{1}{T_c}\frac{\sqrt{\left[1+k_z^2\right]\left[1+\tan^2\left(m_\varphi\right)\right]}-k_z-\tan\left(m_\varphi\right)}{1-k_z\tan\left(m_\varphi\right)} \\ \overset{k_z\ll 1}{\approx} & \frac{1}{T_c}\left[-\tan\left(m_\varphi\right)+\sqrt{1+\tan^2\left(m_\varphi\right)}\right] \\ \omega_{z,i} = k_z\omega_{0,i} = & \frac{K_{i,i}}{K_{p,i}}\end{aligned} \tag{6.2}$$

$$\begin{cases} K_{p,i} = \omega_{0,i}\frac{L_{eq}}{n^2}\frac{1}{\sqrt{1+k_z^2}} \overset{k_z\ll 1}{\approx} \omega_{0,i}\frac{L_{eq}}{n^2} \\ K_{i,i} = \omega_{z,i}K_{p,i} \end{cases} \tag{6.3}$$

The problem with this approach is that there's no way to set the cut-off point $f_{0,i}$ beforehand, since frequency ratio k_z and phase margin m_φ are requested at first. What one should do, is chose these two parameters so that the wanted cut-off point is reached. Let's solve the non-approximated version of (6.2) for these two independent variables (for being as accurate as possible), keeping in mind some constrains:

$$\begin{aligned} k_z &\in (0,1) \\ m_\varphi &> \overline{m_\varphi} \end{aligned} \tag{6.4}$$

where $\overline{m_\varphi}$ is some minimum phase-margin requirement for the current controller (i.e. 30^o).

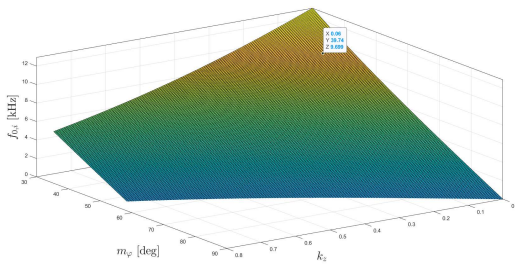


Figure 6.7: Controller cut-off frequency as a function of k_z and m_φ. The point with phase-margin of 39.74^o and k_z of 0.06 has been selected in order to achieve approximately 10 kHz of current bandwidth. Note that in this particular system, no cut-off frequency of ∼12.5 kHz is reachable. Some systems might behave even worse, cancelling out totally the "high-frequency" approximation.

In Fig. 6.7 the $f_{0,i}$ depending on k_z and m_φ is illustrated. The point $(k_z,\, m_\varphi) = (0.06,\, 39.74^o)$ has a $f_{0,i}$ of $\sim$10 kHz with $K_{p,i} = 2.5529$ and $K_{i,i} = 18216$ by using Equations (6.3). In Fig. 6.8 the control scheme implemented for the validation of such theory is illustrated.

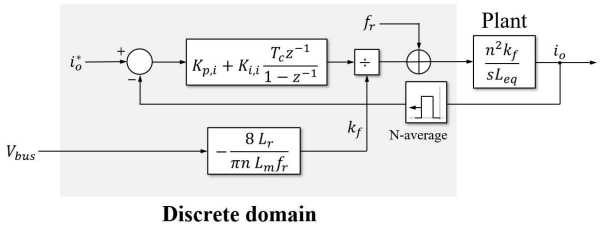


Figure 6.8: Digital control scheme implemented by taking account the high frequency approximation.

Note that the feed-forward term in this case is f_r since the tests are done in this operating condition for validation purposes. As is explained in [84] a LUT that given the operating point selects the feed-forward frequency is needed, even though is some cases this might be a questionable solution.
Let's try and close the loops, first analytically (i.e. with transfer functions) then by PLECS simulation in order to see if the results are matching. If we suppose that the plant is actually the one showed in Fig. 6.8, then the analytical solution is trivial since the design has been tailored perfectly for this purpose. Write down all the equations and analyse the full open-loop transfer function and everything that needs to be monitored. We defined $R(s)$ as the regulator transfer function and $G_d(s)$ as the continuous-time transfer function due to digital implementation delays. The overall equivalent system "topology" is illustrated in Fig. 6.9.

$$\begin{aligned} G_d(s) &\approx \frac{1 - sT_c}{1 + sT_c} \\ G_{c,i}^{hf}(s) &= \frac{n^2 k_f}{sL_{eq}} \\ G_{c,i}(s) &= \frac{k_f\left(\frac{1}{R_L} + sC_o\right)}{1 + s\frac{L_{eq}}{n^2 R_L} + s^2\frac{L_{eq}C_o}{n^2}} \\ R(s) &= \frac{1}{k_f}\left(K_{p,i} + \frac{K_{i,i}}{s}\right) \end{aligned} \tag{6.5}$$

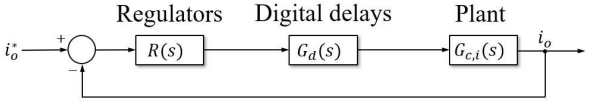
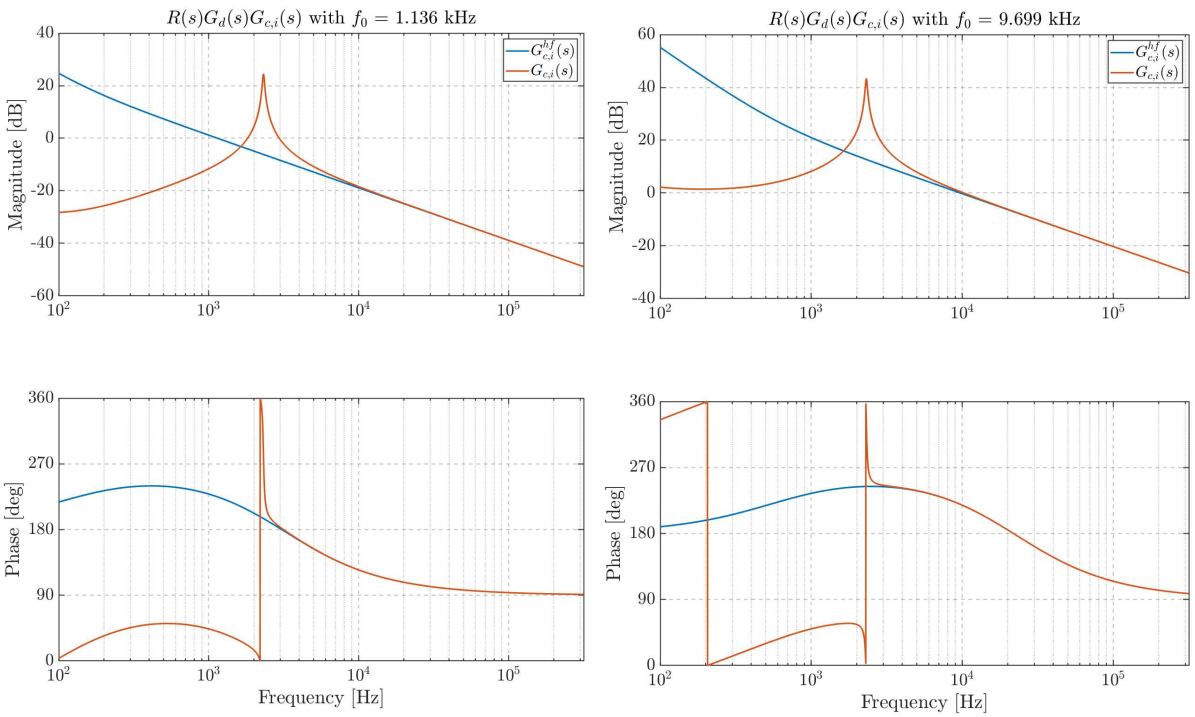


Figure 6.9: Equivalent system control topology (simplified)

Once the transfer functions are known, we can plot all the Bode plots of both the open and closed loop overall system, which are illustrated in Figs. 6.10. In Figs. 6.11, the feedback is introduced and the transfer functions are compared. A total of 4 cases is analysed so that all the combinations where the two proposed small-signal functions $G_{c,i}$ and $G_{c,i}^{hf}$ are analysed with two different bandwidths ($\sim$1 kHz and $\sim$10 kHz). As it is possible to see from the figures, there is a big difference in terms of closed loop frequency response if the plant is the II-order system or the integrator hypothesis, hinting that one of the two approximations is a very poor approximant. As we introduced previously and as it can be seen from Fig. 6.3, the integrator hypothesis is not that good.
Let's set the controller gains as in Equations (6.2) and (6.3) and see if the response in Time Domain Analysis (TDA) conducted via PLECS is consistent with the analytical approximations.

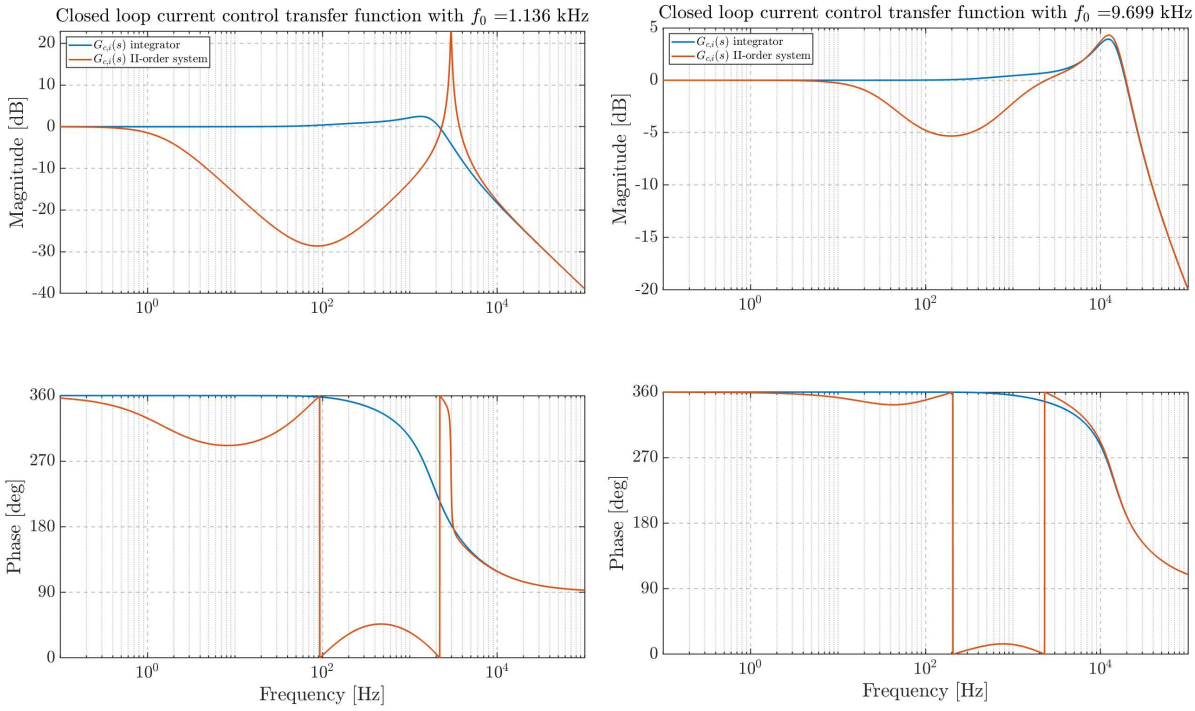


(a) R(s) is designed such that $f_{0,i} \cong 1$ kHz

(b) R(s) is designed such that $f_{0,i} \cong 10$ kHz

Figure 6.10: Comparison between **open**-loop transfer function(s) where in one case the plant is modelled as an integrator (blue) while on the other it is a II-order system (orange).

In Figs. 6.12a and 6.12b the step response of the system is illustrated in two different scenarios. In both figures the test conditions are the same. The reference is initially set at gain 0.95 (so that the synthesized frequency will be very close to the resonant and the small-signal hypothesis is safely applicable) and at $t_1 = 0.5\,s$ a reference step is given so that the system will slide exactly at resonance point. In both the pictures, the TDA simulation respects the dynamical behaviour of the II-order analytical model, while the step response of a filter whose cut-off frequency is (respectively) 10 kHz and 1 kHz is much quicker in both cases when confronted with simulation and analytical results, hindering that the integrator approximation cannot be used consistently to design the current controller. I believe that if one were to close the loop at much higher frequency (i.e. 100+ kHz), then maybe this approximation would hold. The differences in terms of high dynamics modes, might be cause by adopting a simple II-order transfer function to model a strongly non-linear and complex system. For better analytical matching, I'll be working on a more accurate model soon.
In Fig. 6.12a the selected bandwidth is in the order of ∼10 kHz in order to comply as much as possible with the "high-frequency approximation". In this example the control frequency is equal to the resonant one (i.e. 140.7 kHz) and TDA simulation, analytical model from II-order transfer function and low-pass filter with 10 kHz bandwidth step-response are compared with one another. The low-pass filter response tries to emulate the system behaviour when the plant is a pure integrator. The same procedure is done in Fig. 6.12b where the cut-off frequency is selected to be approximately around ∼1 kHz. We can easily see that the real system response (TDA) and the II-order approximant show a decent matching, while the low-pass filter responses appears to be much faster, hinting the incorrectness of the I-order integrator approximation. Moreover, in Figs. 6.13 the comparison between analytical and PLECS simulations are shown in both operating cases ($F_c = 20$ kHz with BW∼ 1.1 kHz and $F_c = f_r$ with BW∼ 10 kHz), further proving the incorrectness of the integrator approximation.



(a) R(s) is designed such that $f_{0,i} \approxeq 1$ kHz

(b) R(s) is designed such that $f_{0,i} \approxeq 10$ kHz

Figure 6.11: Comparison between **closed**-loop transfer function(s) where in one case the plant is modelled as an integrator (blue) while on the other it is a II-order system (orange).

6.2 State-feedback control

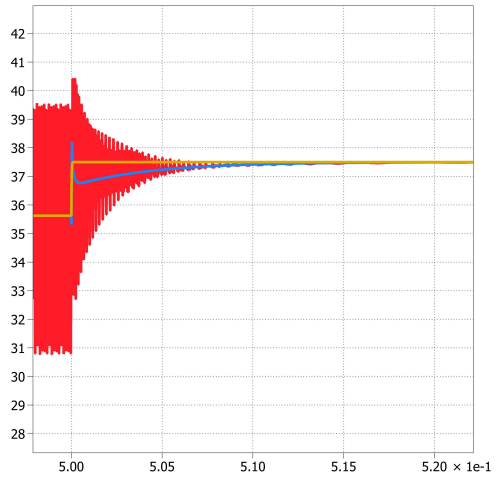
By analysing the plant of Fig. 6.9 and realizing that the most correct $G_{c,i}$ function is the II-order, one could theoretically create a compensator $R(s)$ that completely annihilates the unwanted zeros and poles. For simplicity, let's start from the assumption that $G_d(s) \approx 1$. The idea is to cancel completely all the poles/zeros of the transfer function and add an integrator whose time constant is decided to reach the wanted bandwidth. Finally, add as many high-frequency poles as needed in order to make the function strictly proper hence $deg(num) < deg(den)$. The general compensator formula is shown in Equation (6.6)

$$R(s) = \frac{\omega_{0,i}}{s\, G_{c,i}(s) \prod_{h=1}^{H} \left(\frac{s}{\omega_h} + 1\right)} \tag{6.6}$$

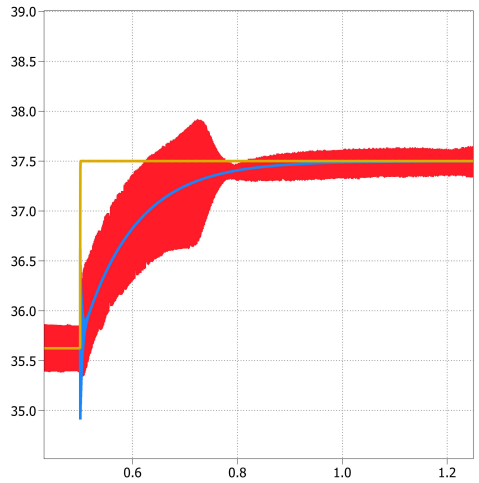
In this case only one high-frequency pole is needed. We can set it at $\omega_{hf} = 0.75\omega_{Ny}$ while the cross-over angular frequency $\omega_{0,i}$ is selected at $2\pi \times 1000$ rad/s. In this example we are using 10 kHz as a Nyquist frequency since the control period T_c is selected at 50 μs (hence 20 kHz). We can easily compute the numerator and denominator of the overall compensator transfer function $R(s)$ as

$$\begin{aligned} N_R &= \omega_{0,i} D_{G_{c,i}} \\ D_R &= \begin{bmatrix} 1 \\ 0 \end{bmatrix}^{\intercal} * N_{G_{c,i}} * \begin{bmatrix} \tau_h \\ 1 \end{bmatrix}^{\intercal} \end{aligned} \tag{6.7}$$

where N_R is the compensator numerator, D_R its denominator, $N_{G_{c,i}}$ and $D_{G_{c,i}}$ are the rectified-current-to-frequency small-signal transfer function numerator and denominator respectively, τ_h is the high-frequency time constant of the HF-pole and $\overrightarrow{v_1} * \overrightarrow{v_2}$ is the linear convolution operator between two vectors $\overrightarrow{v_1}$ and $\overrightarrow{v_2}$. Now, the discrete-time transfer function needs to be evaluated,



(a) Selected bandwidth ∼10 kHz. Control frequency ∼140 kHz (same as the resonance), m_φ of 39.74^o and k_z of 0.06



(b) Selected bandwidth ∼1 kHz. Control frequency of 20 kHz, m_φ of 45^o and k_z of 0.1

Figure 6.12: The red curve is time-domain simulation which (on average) matches with the blue curve representing the analytical model build around the 2^{nd}-order system in [8]. If all the approximations were correct, then both these step-time response shall be similar to the step-response of the yellow curve, that represents a simple 1^{st}-order equivalent system whose -3 dB is selected to be equal to the cross-over frequency. As we can see, in both cases this is not true because the equivalent filter reacts much quicker.

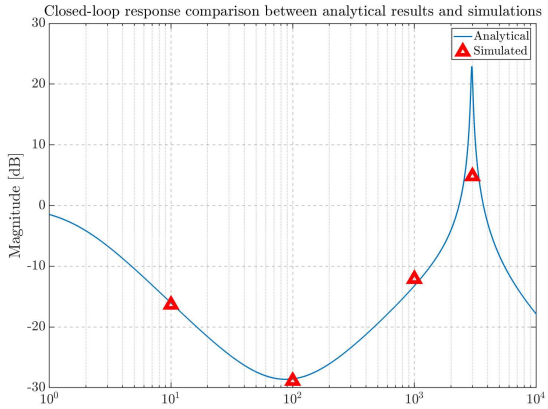
where the most critical point is the resonance of $G_{c,i}(s)$, hence the frequency warping needs to be done at f_{eq}, obtaining in this way a `3p3z` (3-poles-3-zeros) compensator.

$$R(s) \xrightarrow{\text{prewarp } @\omega_{eq}} R(z^{-1})$$

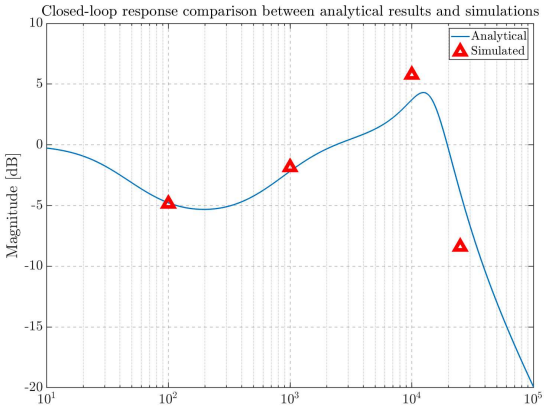
$$N_R(z^{-1}) = -34.2133 + 16.3941z^{-1} + 17.0540z^{-2} - 33.5534z^{-3}$$
$$D_R(z^{-1}) = 1 - 1.87360z^{-1} + 0.771600z^{-2} + 0.1020z^{-3}$$

6.2.1 Difficulties in controlling the output current

As shown in Fig. 6.5, the output current i_o (intended as the rectified current averaged in a switching period) is very difficult to control since the small-signal DC gain changes depending on the load resistance. This poses a big issue in the controllability of this quantity, since the output load is not a parameter which is known *a-priori* and its estimation might be difficult. A much easier task, is controlling the load current since its dynamical behaviour is proportional to the one seen in the case of the load voltage. Configuring the current loop tuned at 1 value of the load resistance and expecting to behave the same in every operating condition is not usually a good idea and might backfire in cases where the gain becomes too big, creating the possibility of making the loop unstable. This is a rather (not strongly, pay attention!) unlikely scenario but the current loop quality shall be kept as high as possible in order to avoid possibly dangerous over-currents. Not only this, but the small-signal model fails to the current response once the resistance load starts getting bigger and bigger (i.e. at lower power levels), as shown in Fig. 6.14.
The inaccuracy in low output current condition is being investigated. One hypothesis is that when the output resistance is big, the first harmonic approximation doesn't hold any more and the converter reaches a "discontinuous mode" operation (DCM). If the FHA approach fails, obviously the small-signal (as is being calculated right now) fails too since the latter is based on its validity.



(a) Closed loop comparison between analytical approximation and TDA simulations. The bandwidth has been selected to be ∼1 kHz with the 20 kHz control frequency solution



(b) Closed loop comparison between analytical approximation and TDA simulations. The bandwidth has been selected to be ∼10 kHz with the ∼140.7 kHz control frequency solution

Figure 6.13: Closed loop comparison between simulation and analytical model in the two operating cases. Only the II-order function is shown for better understanding - as it is possible to see, the approximation is rather good.

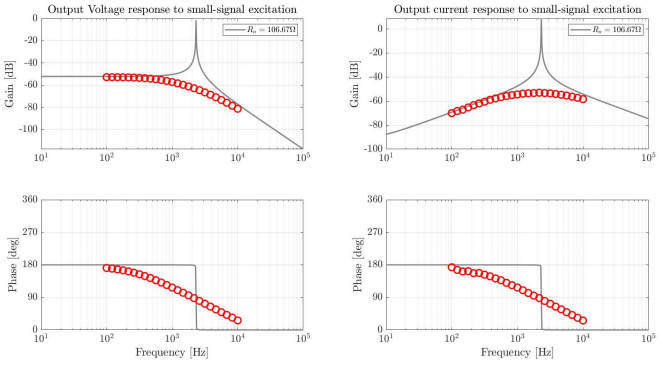


Figure 6.14: Voltage (left) and current (right) responses at 10% power level, hence $R_{Load} = 10R_n$, where R_n is the nominal load resistance necessary for achieving 15 kW output power with the parameters shown in Table 6.2

6.3 An accurate small-signal model

Here I developed a more accurate small-signal model for LLC - actually the previous one was valid only around the resonant frequency while this one is valid kind of everywhere. Let's first write down the LLC non-linear system equations:

$$\frac{di_r}{dt} = \frac{v_{in}}{L_r} - \frac{v_{C_r}}{L_r} - \frac{n}{L_r} sign\left(i_r - i_{Lm}\right) v_o \tag{6.8a}$$

$$\frac{dv_{Cr}}{dt} = \frac{i_r}{C_r} \tag{6.8b}$$

$$\frac{di_{Lm}}{dt} = \frac{n}{L_m} sign\left(i_r - i_{Lm}\right) v_o \tag{6.8c}$$

$$\frac{dv_o}{dt} = \frac{n\ |i_r - i_m|}{C_{out}} - \frac{v_o}{R_o C_{out}} \tag{6.8d}$$

The previous set of equations is not easily worked with, hence the EDF approach (based on the FHA) is used to simplify the equations in (6.8) obtaining (6.9), where the usual definitions of I_s, I_c and I_p

$$f_1 = \frac{4V_{in}}{\pi L_r} - \Omega_s I_{rc} - \frac{V_{cs}}{L_r} - \frac{4nV_oI_s}{\pi L_r I_p} \tag{6.9a}$$

$$f_2 = \Omega_s I_{rs} - \frac{V_{cc}}{L_r} - \frac{4nV_oI_c}{\pi L_r I_p} \tag{6.9b}$$

$$f_3 = -\Omega_s V_{cc} + \frac{I_{rs}}{C_r} \tag{6.9c}$$

$$f_4 = \Omega_s V_{cs} + \frac{I_{rc}}{C_r} \tag{6.9d}$$

$$f_5 = -\Omega_s I_{mc} + \frac{4nV_oI_s}{\pi L_r I_p} \tag{6.9e}$$

$$f_6 = \Omega_s I_{ms} + \frac{4nV_oI_c}{\pi L_r I_p} \tag{6.9f}$$

$$f_7 = \frac{2nI_p}{\pi C_o} - \frac{V_o}{R_L C_o} \tag{6.9g}$$

$$g_1 = \frac{2nI_p}{\pi} \tag{6.9h}$$

$$g_2 = V_o \tag{6.9i}$$

The output function of the system is created in order to observe the output voltage v_o and output current DC value i_o (secondary current after the rectifier and before the capacitive filter) defined as $\frac{2n}{\pi}(i_r - i_{Lm})$.

$$g(x(t), u(t)) = \begin{bmatrix} \frac{2n}{\pi}(i_r - i_{Lm}) \\ v_o \end{bmatrix} \tag{6.10}$$

We define as state-variables the following vector $x(t) = [i_r\, v_{Cr}\, i_{Lm}\, v_o]^\intercal$, while the input vector $u(t)$ is chosen as $u(t) = [V_{in},\, \omega_s]$. Given a system of non-linear equations such as

$$\begin{aligned} \dot{x}(t) &= f(x(t), u(t)) \\ y(t) &= g(x(t), u(t)) \end{aligned} \tag{6.11}$$

that accepts steady-state solution in the form of

$$\begin{aligned} 0 &= f(\overline{x},\, \overline{u}) \\ \overline{y} &= g(\overline{x},\, \overline{u}) \end{aligned} \tag{6.12}$$

It is always possible to find a linearized version of that system around an equilibrium point $(\overline{x},\, \overline{u})$, obtaining

$$\begin{aligned} \dot{x}(t) &\approx Ax(t) + Bu(t) \\ y(t) &\approx Cx(t) + Du(t) \end{aligned} \tag{6.13}$$

where the matrices A, B, C and D are the Jacobians of the functions $f(x, u)$ and $g(x, u)$ defined such as

$$\begin{aligned} A_{ij} &= \left.\frac{\partial f_i}{\partial x_j}\right|_{(\overline{x},\overline{u})} & B_{ij} &= \left.\frac{\partial f_i}{\partial u_j}\right|_{(\overline{x},\overline{u})} \\ C_{ij} &= \left.\frac{\partial g_i}{\partial x_j}\right|_{(\overline{x},\overline{u})} & D_{ij} &= \left.\frac{\partial g_i}{\partial u_j}\right|_{(\overline{x},\overline{u})} \end{aligned} \tag{6.14}$$

By analysing the eigenvalues of the matrix A for different switching frequencies, the poles of the system can be illustrated in different operating conditions $(\overline{x},\, \overline{u})$, as seen in Fig. 6.15.

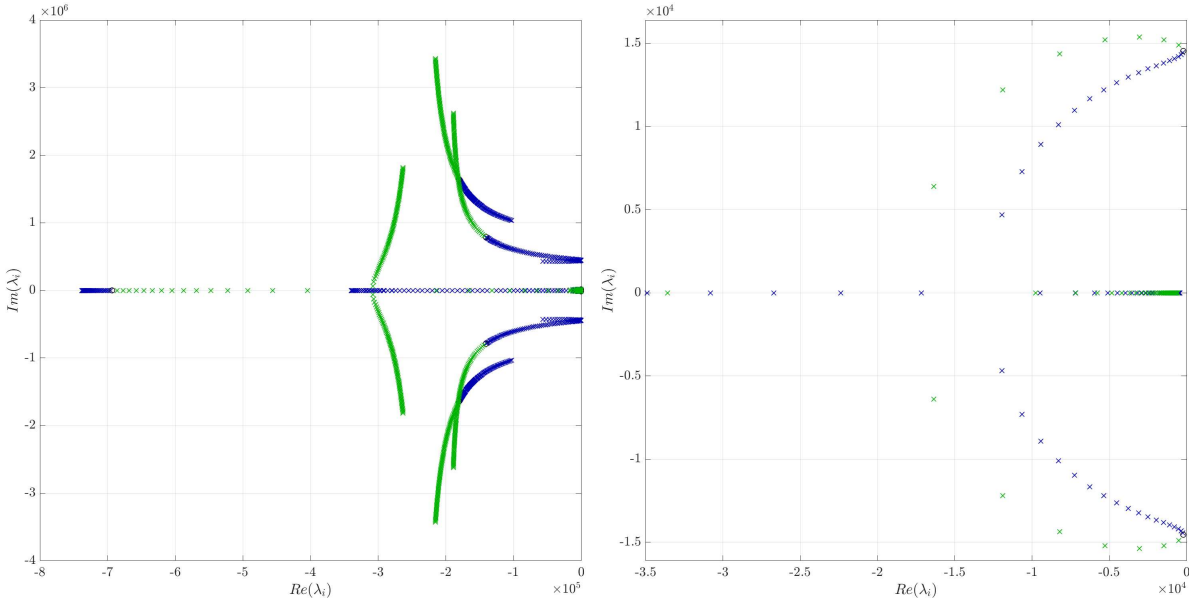


Figure 6.15: Eigenvalues

Literature offers the analytical solutions to this problem already in different forms i.e. [85]. We firstly need to chose the input operating point $\overline{u}$, in the following example $V_{in} = 400$ V and $\omega_s = 2\pi \times f_r$ are chosen. Once $\overline{u}$ is set we can find the steady-state solution of the system $\overline{x}$ by means of different analytical tools (FHA approximation, TDA simulation or else). Once this is done, we can compute the Jacobian linearized matrices (6.14). Applying this procedure, a 2-inputs-2-outputs MIMO system is obtained, where the $\widetilde{\square}$ stands for small-signal interpretation. The inputs are $u(t) = [v_{in}(t),\, \omega_s(t)]^\intercal$ while the outputs are $y(t) = [i_o(t),\, v_o(t)]^\intercal$.

$$\widetilde{G}(s) = \begin{bmatrix} \left.\dfrac{\partial i_o}{\partial v_{in}}\right|_{(\overline{x},\overline{u})} & \left.\dfrac{\partial i_o}{\partial \omega_s}\right|_{(\overline{x},\overline{u})} \\ \left.\dfrac{\partial v_o}{\partial v_{in}}\right|_{(\overline{x},\overline{u})} & \left.\dfrac{\partial v_o}{\partial \omega_s}\right|_{(\overline{x},\overline{u})} \end{bmatrix} \tag{6.15}$$

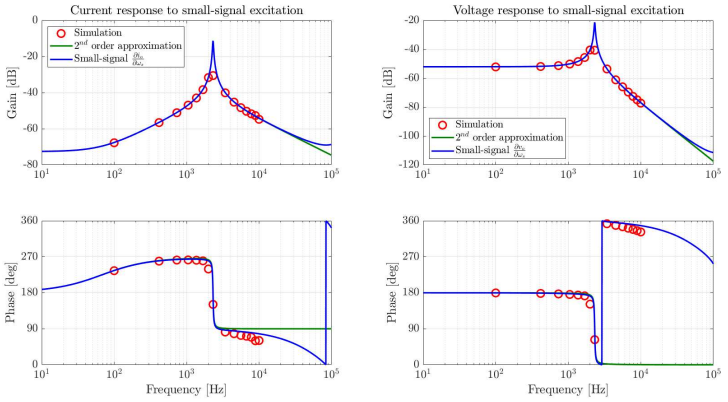


Figure 6.16: Functions $\partial i_o/\partial \omega_s$ and $\partial v_o/\partial \omega_s$ obtained via small-signal analysis, II-order approximation and simulation results.

Once this point is reached, the plant dynamics for both output current and voltage is known for every carrier and modulation frequency - respectively F_s and F_m - is known, as shown in Fig. 6.17.

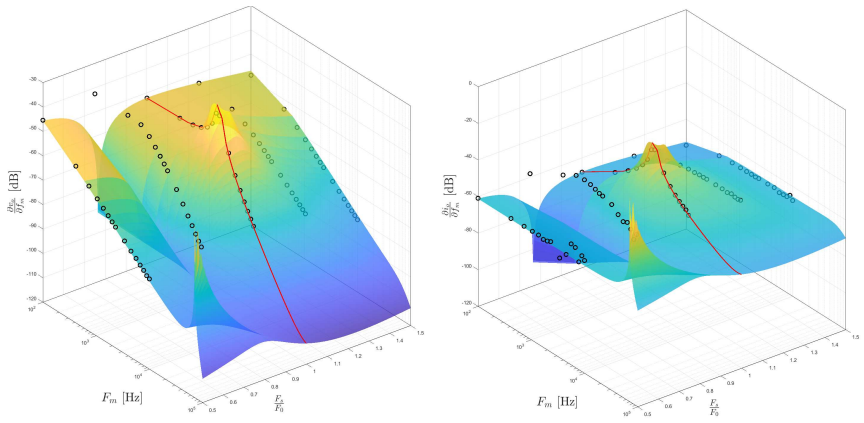
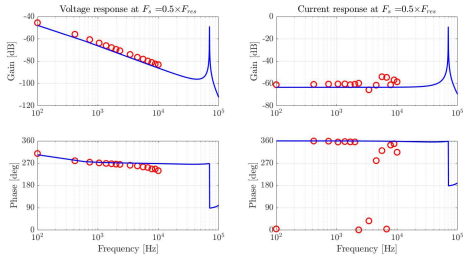


Figure 6.17: 3D frequency-to-output(s) transfer functions depending on the control frequency carrier F_s and modulation F_m. The red lines highlight the behaviour when the carrier matches the resonant point f_r. The black dots represent the circuit simulation results.

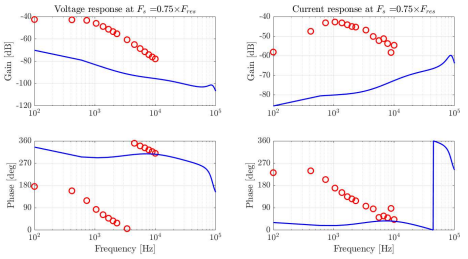
The black dots represent the circuit simulation results, were it is possible to see that for some carrier points (i.e. the one around $0.75F_0$, where there's that sort of "valley") the matching between small-signal analysis and circuit simulation is rather small. This means that the small-signal model as implemented up to this point is not accurate enough to predict the converter behaviour in the whole carrier-frequency range. In the example shown in Figs. 6.17, the carrier range is rather small (0.5 to 1.5 times the resonance), but in many cases much bigger carrier frequencies are requested for enabling an operating range as wide as possible. In Figs. 6.18 the comparison between TDA simulation and small-signal model is shown at different carrier frequencies (namely $f_n = [0.5,\ 0.75,\ 1.25,\ 1.5]$ - note that from now on the ratio between switching frequency and resonant one will be called f_n) The case where $F_s = 0.75\,F_0$ seems critical since the circuit simulation cannot predict the small-signal transfer function. This most likely means that some low order dynamics are being ignored by the ss-model, hence rendering it incomplete. In time-domain analysis the tank excitation is performed via full-bridge inverter in order to simulate the modulating capacity of the real system. For proving the correctness of small-signal analytical analysis via simulation it is better to excite the bridge with a "non-PWM" signal (i.e. an ideal FM-modulated voltage source).

Another problem arising in this analysis is the "DC-bias" operating point which has been indicated before as $(\overline{x},\ \overline{u})$. When linearizing the equation system, we firstly need to find the state variables around the linearization point in order to compute the partial derivatives needed for building the Jacobian matrices around that point. Failure in doing so would result in erroneous results. Right now we're using the EDF (Extended Describing Function) for determining the DC-bias point, which uses the First Harmonic Approximation (FHA) for simplifying the non-linear model dynamical behaviour and makes the output voltage computation extremely easy since a simple matrix inversion is needed as shown in Eq. (**??**) and the algorithm illustrated below, which represent the CL^2C case but applies to the same way to an LLC. As known, this mathematical instrument is accurate only if the quality factor Q of the system is big enough., where

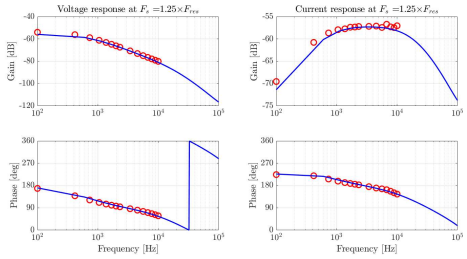
$$\begin{aligned} Q &= \frac{Z_0}{R_{ac}} \\ Z_0 &= \sqrt{\frac{L_r}{C_r}} \\ R_{ac} &= \frac{8n^2}{\pi^2} R_o \end{aligned} \tag{6.16}$$



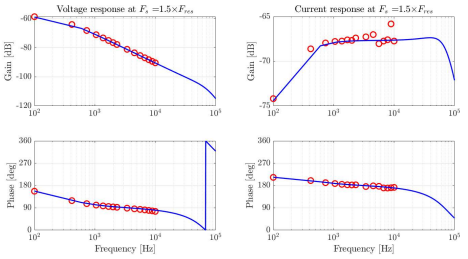
(a) Carrier frequency halved with respect to the resonance



(b) Carrier frequency 75% with respect to the resonance



(c) Carrier frequency 125% with respect to the resonance



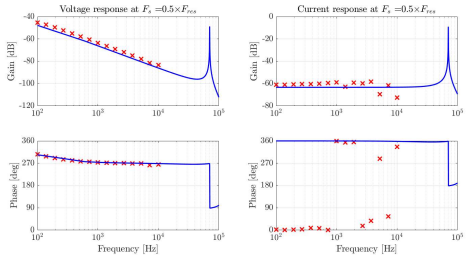
(d) Carrier frequency 150% with respect to the resonance

Figure 6.18: Comparison between small-signal transfer function (blue line) and simulation results (red dots). The tank is excited via full-bridge inverter, hence the voltage is a sinusoidally FM modulated square wave.

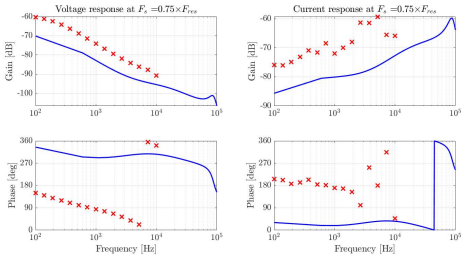
This means that the LLC needs to see a small load resistance, which is equivalent to say that the output current/power needs to be "big enough" (where the definition of "big enough" is not that clear). This effect is shown in Figs. 6.20 where different quality factors are shown in order to show the matching between simulations and analytical approximation.
In Fig. 6.20a the matching is not sufficiently consistent. For $f_n = 0.75$ the actual (simulated) gain differs a lot from the theoretical one, while it is possible to observe some smaller differences at $f_n = 1.25$ and $f_n = 1.5$. In Figs. 6.18 (as well as Fig. 6.19) it is possible to see the mismatch between small-signal analytical transfer function and the ones obtained in simulation. The difference is very noticeable in Fig. 6.18b, as it is the DC-gain around this operating point, further proving the need to develop a system allowing to accurately estimate the DC-gain of such converter at every operating point interdependently from the load condition.

6.3.1 Validation of small-signal model via TDA

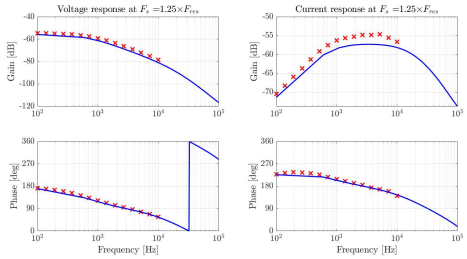
In order to validate the analytical small-signal behaviour, a precise excitation and measuring system is needed. The LLC can be assumed as a frequency to voltage converter, in the sense that once the input full-bridge is driven with a fixed frequency F_s a constant output voltage V_o and average (where the averaging process is done in a switching period $1/F_s$). For example, if $F_s = F_0$ the output voltage V_o would assume a fixed value such that $V_o = V_i/n$ (where n is the transformer primary-to-secondary conversion ratio $n_{primary}/n_{secondary}$). In this condition the average output current I_o would be equal to V_o/R_{Load} (let's assume a resistive load for simplicity sake). This means that the superposition of a modulating function on the carrier frequency, would produce a constant output voltage and average current plus a spectral distribution which depends on how the tank and rectifier respond due to the modulation stimulus. In the small-signal analysis, one is interested in the system output behaviour (in our case v_o and i_o) once the control variable (in our case frequency f_s) moves around a bias point. This *movement* has to be as small as possible in order to achieve linearity around that point. If this condition is matched, the system behaves locally as if it was linear and it is then possible to derive a transfer function to understand the operation around said bias.



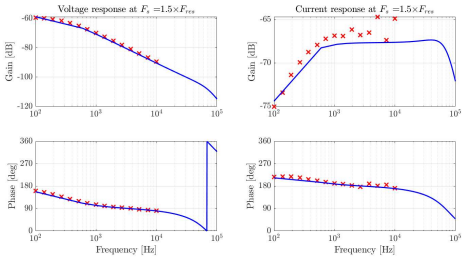
(a) Carrier frequency halved with respect to the resonance



(b) Carrier frequency 75% with respect to the resonance

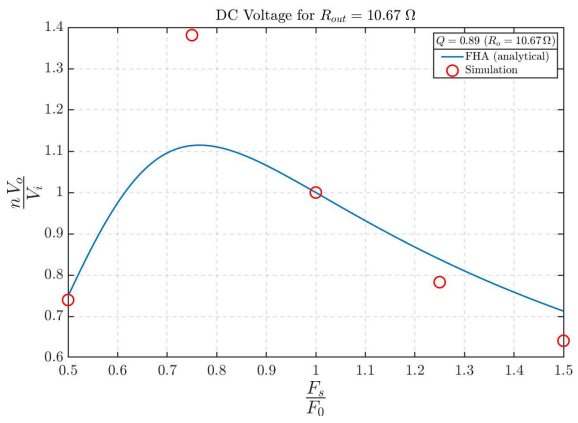


(c) Carrier frequency 125% with respect to the resonance

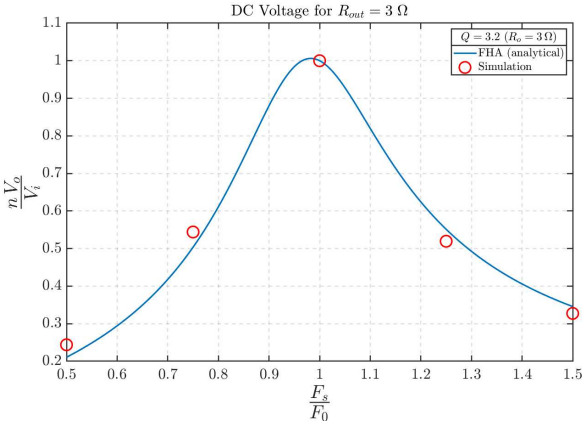


(d) Carrier frequency 150% with respect to the resonance

Figure 6.19: Comparison between small-signal transfer function (blue line) and simulation results (red crosses). In this case the tank is excited via an ideal controlled sinusoidal voltage source, hence we can see how in the case where carrier frequency is $0.75 \times F_0$ the matching is a bit better (still there's a big error, but at least the trend is consistent)



(a) Comparison between DC point simulations and analytical approximation via FHA in *low* Q-factor conditions



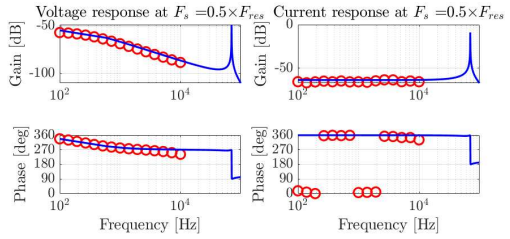
(b) Comparison between DC point simulations and analytical approximation via FHA in *high* Q-factor conditions

Figure 6.20: Comparison between DC point simulations and analytical approximation in different load conditions. In high-load (low resistance) condition, the FHA is a good approximation to the actual DC voltage gain of the converter. This is not true if the load resistance is "big"

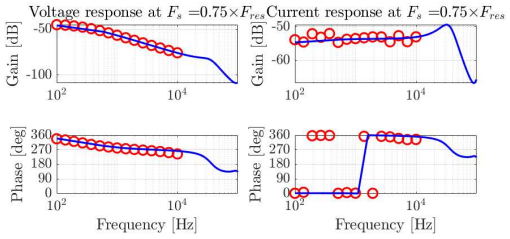
In an LLC, the control variable is the frequency. Let's now call the "polarizing" component of said frequency (the one that allows the achievement of a particular V_o, I_o DC-bias working point) *carrier*, and we'll now indicate at it as F_c. On top of this carrier, we add a *sinusoidal modulation* $x_m(t) = f_\Delta \cos(2\pi f_m t)$.

$$f_s(t) = F_c + f_\Delta \cos(2\pi f_m t) \tag{6.17}$$

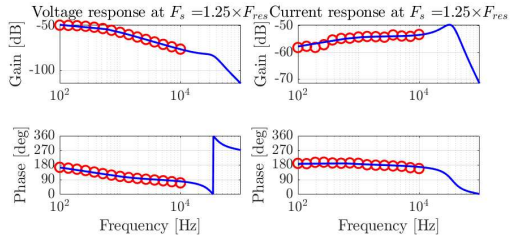
where f_Δ is the maximum frequency variation, while f_m is the modulation frequency. The output voltage (hence the current too), will respond to this excitation with a DC component and a sinusoidal spectral line at frequency f_m. We are interested in measuring this spectral



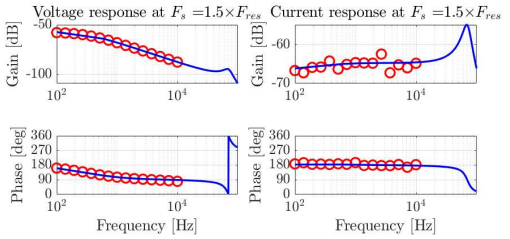
(a) Carrier frequency halved with respect to the resonance



(b) Carrier frequency 75% with respect to the resonance



(c) Carrier frequency 125% with respect to the resonance



(d) Carrier frequency 150% with respect to the resonance

Figure 6.21: In this case we can see how the small-signal analytical model matches very well with TDA simulations since the working condition is such that the DC-gain analytical calculation due to FHA matches very one the simulation cases

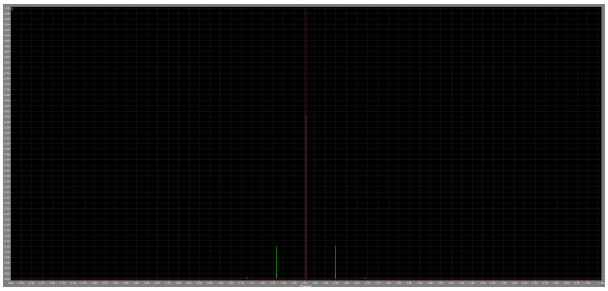
component on the output variables (v_o and i_o). There are some conditions in order for this to happen, which allow the small-signal condition to be respected. The frequency variation needs to be much smaller then the carrier - $f_\Delta \ll F_c$ - and the frequency modulation f_m needs to respect the Nyquist limit $f_m < F_c/2$. After these considerations, we can express the voltage on the bridge as in equation (6.18) which is widely known in literature for the frequency modulation [86]. Note that the spectral analysis which is done right now is for a sinusoidally excited tank (no full-bridge inverter is used).

$$\begin{aligned} v_b(t) &= \frac{4}{\pi} V_{DC} \sin\left(2\pi \int_0^t \left[F_c + x_m(\tau)\right] d\tau\right) \\ &= \frac{4}{\pi} V_{DC} \sin\left(2\pi F_c t + \frac{f_\Delta}{f_m} \sin\left(2\pi f_m t\right)\right) \\ &= \frac{4}{\pi} V_{DC} \sin\left(2\pi F_c t + h_m \sin\left(2\pi f_m t\right)\right) \end{aligned} \tag{6.18}$$

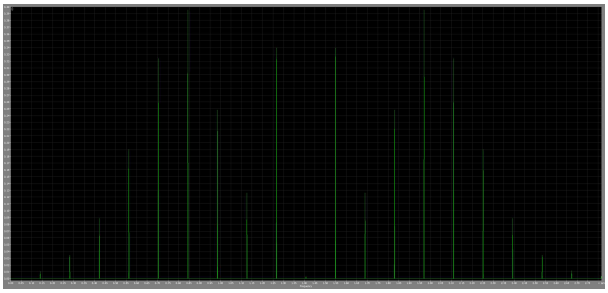
where h_m ($h_m = f_\Delta / f_m$) is defined as the *modulation index* and depending on this value the spectral distribution of v_b can be tailored. In Figs. 6.22 two spectrums with different modulation index are illustrated. Having a narrowband spectrum is advantageous since the LSB (Left Side Band) of the signal might interfere with the frequency component we're interested (which is f_m).
If the carrier function is not a sinusoid (in this case it is a square-wave like voltage excitation on the primary bridge $v_b(t)$), the spectrum behaves equally around every spectral line of the carrier. In Fig. 6.23 this analysis is illustrated.

6.4 Model perturbation for small-signal identification

As seen in previous section, we're now able to define accurately the "large signal behaviour" - or rather the steady-state condition - of the converter once the output voltage is given as a known parameter as well as the operating carrier frequency. This apparently does not look like an improvement but actually puts the basis for a new way of studying the small-signal behaviour of this kind of converters. The main problem we've came across is that in many conditions



(a) Frequency spectrum with modulation index 0.25. The spectrum is very narrow and the sidebands (green) get attenuated very quickly once you move away from the carrier (red) line



(b) Frequency spectrum with modulation index 5.53. The spectrum is wide and the sidebands contain the entirety of power. In this case, the carrier carries no power at all, since it's all spread on the sidebands.

Figure 6.22: Frequency spectrums with two different modulation indexes. The green line is the modulated spectrum, while the red one is the carrier with no modulation. A wide spectrum (seen in the case where $h_m = 5.53$) poses some issues since the LSB (Lower Side Band) spectral lines might interfere with the modulating function which shall be at lower frequencies.

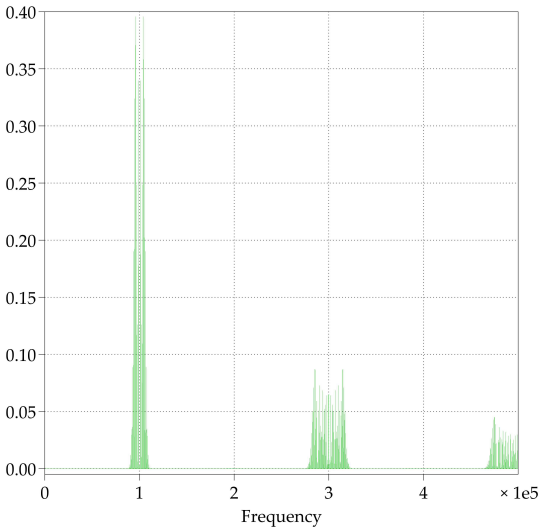


Figure 6.23: Spectrum of sinusoidally modulated square-wave. The carrier is set at 100 kHz and three spectral groups can be observed (around F_c, $3F_c$ and $5F_c$). The modulation index h_m has been set to 5.53, hence only the sidebands contain power.

the usage of the Extended Describing Function (EDF) for perturbing the model around an operating point fails to predict the actual behaviour of the converter (which is double checked via PLECS simulation), likely due to the First Harmonic Approximation (FHA) inaccuracy and this becomes particularly critical when the output power is small or when the equivalent load resistance is big (this has been shown in the previous Chapter). For this new derivation, the LLC and output load are treated as two different entities, where the converter sees an ideal voltage source on its output which is then connected to the load under test as shown in Fig. 6.24.

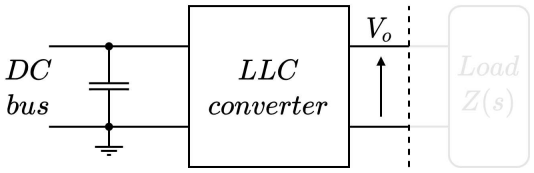


Figure 6.24: Block diagram of LLC converter

In this way it is possible to study the converter small signal current transfer function $\partial i_o/\partial f_m$ separately from the load for different values of conversion ratio M, carrier and modulation frequency (F_c, f_m respectively). This will give an insight on the converter behaviour independently from the load, and we will finally be able to concatenate the LLC and load responses separately. Essentially with this procedure we are studying the output impedance $Z_o(\omega)$ of the converter. In order to do so, a steady-state point (M, F_c) is selected and a small perturbation step ΔF on the control variable (frequency) is applied so that a transient response on the output current i_o can be measured and a system identification procedure is run to match the experimental response with a transfer function.
Said transfer function is discrete in nature because we are interested in the average value of the output current $\overline{i_o}$ which is available after averaging the instantaneous $i_o(t)$ over a switching cycle whose duration T_s is determined by the carrier frequency F_c. By applying the total differential theorem to the output current we obtain:

$$di_o = \frac{\partial i_o}{\partial f_m} df_m + \frac{\partial i_o}{\partial M} \frac{\partial M}{\partial f_m} df_m \tag{6.19}$$

The 2nd term in (6.19) is considered to be zero since M is a parameter hence $\partial M/\partial f_m = 0$ but theoretically it should be taken into account when the output voltage is not fixed (i.e. when the load is a resistor). Might this be the reason why at some point the previous small-signal mathematical model fails? Is the possibility that there comes a point where we cannot consider the 2nd term of the previous equation negligible the mismatch source between analytical model and experimental results?

6.4.1 Identification procedure

Let's select a bias point (M, F_c) and an arbitrary time snap t_0 where the frequency is increased by a fixed step ΔF. In this way the new carrier frequency becomes $F_c\left(t_0^+\right) = F_c + \Delta F$, where we can safely assume that $F_c\left(t_0^+\right) \approx F_c$ since the perturbation ΔF is small

$$\Delta F \ll F_c$$

This will create a change in the average output current $\overline{i_o}$ which is the quantity of interest, computed as

$$\overline{i_o}(t) = \frac{1}{T_s} \int_{t-T_s}^{t} i_o(\tau) d\tau \tag{6.20}$$

The previous is computed at the end of every period whose duration is the reciprocal of the carrier frequency, which means that for $t < t_0$ the integral is computed over a $T_s = 1/F_c$ while for $t > t_0$ the integral is computed on a time window $T_s = 1/(F_c + \Delta F)$. After sampling the current, a tool for system identification can be used to estimate a transfer function $G_{\overline{i_o}|(X_0)}(s)$ where the subscript notation $\overline{i_o}|\,(X_0)$ is intended as the average output current $\overline{i_o}$ at a defined working point $X_0 = (M,\, F_c)$. This step-like analysis will be carried out using PLECS, where the mathematical dissertation discussed in Section 5 for the steady-state will be used to define the initial condition in the TDA simulator on resonant capacitor voltage $v_C(0)$, resonant inductor current $i_L(0)$ and magnetizing current $i_M(0)$. Having the steady-state condition of the system computed via an analytical process (hence very fast) that can be used as initial condition on the circuit simulator is strongly advantageous since it removes the burden of finding the bias point from the simulator, which is usually time consuming and strongly dependent on the operating point.
Let's perform M simulations (do not confuse the number of simulations M with the voltage conversion ratio M!) and for every one, record N time snapshots of the average output current computed as in Eq. (6.20) in order to build matrix $\mathbf{E}$ (which stands for "experiments") as follows

$$\mathbf{E} = \begin{bmatrix} | & | & | & | \\ i_o(1) & i_o(2) & \dots & i_o(N) \\ | & | & | & | \end{bmatrix} \tag{6.21}$$

where the m^{th} row contains the N snapshots of the output current evolution due to a small change in frequency around $F_c(m)$. Depending on how many carrier frequency points and how many time snapshots are taken, this matrix can either be tall and skinny or short and wide.

6.4.2 Regression strategies

Considering that the time response due to a small perturbation in frequency looks very much like a second order, every row of E will be fit by a $2p2z$ discrete-time transfer function by using a Sanathanan-Koerner (SK) iteration [87]. For every row of the matrix E (hence for every carrier), the small-signal discrete time transfer function is now available in the form of

$$G_m\left(z^{-1}\right) = \frac{b_1 z^{-1} + b_2 z^{-2}}{1 + a_1 z^{-1} + a_2 z^{-2}} \tag{6.22}$$

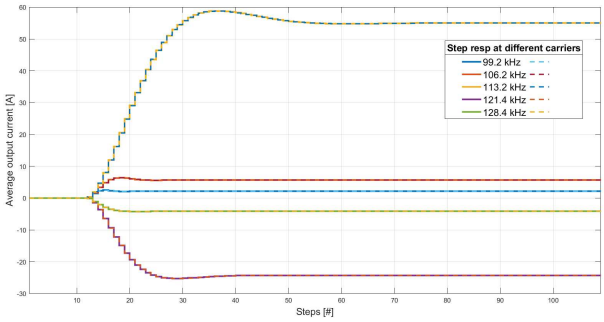


Figure 6.25: Time response to frequency step excitation. The continuous lines are the currents obtained from simulation while the dashed lines represent the time response of the fit $2p2z$ discrete time transfer functions.

The sampling time for the m^{th} transfer function is $T_s(m) = 1/F_c(m)$. Note also that no element b_0 is present on the transfer function numerator, which implies one time step delay between the input and output. In Fig. 6.25 the time response from experimental data are compared to the ones obtained via $2p2z$ transfer functions fitting, while in Fig. 6.26 we show how the 2 complex conjugate poles of the discrete-time small-signal transfer function move when the carrier

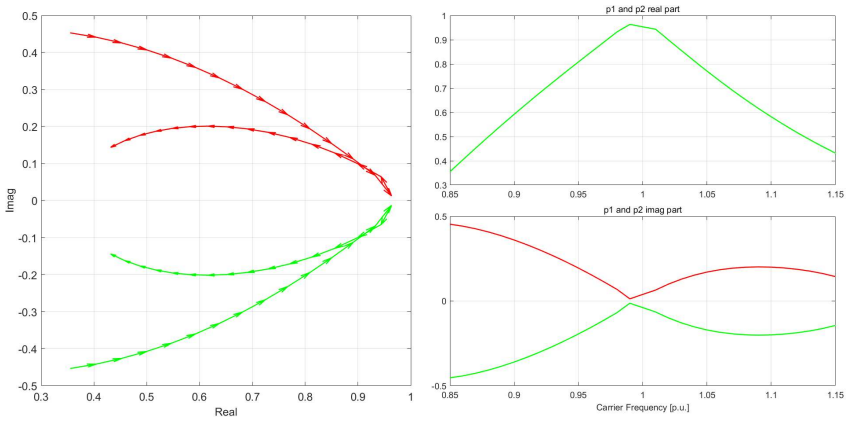


Figure 6.26: Poles of the discrete-time small-signal transfer function $\mathbf{G}\left(z^{-1}\right)$ changing with the carrier frequency.

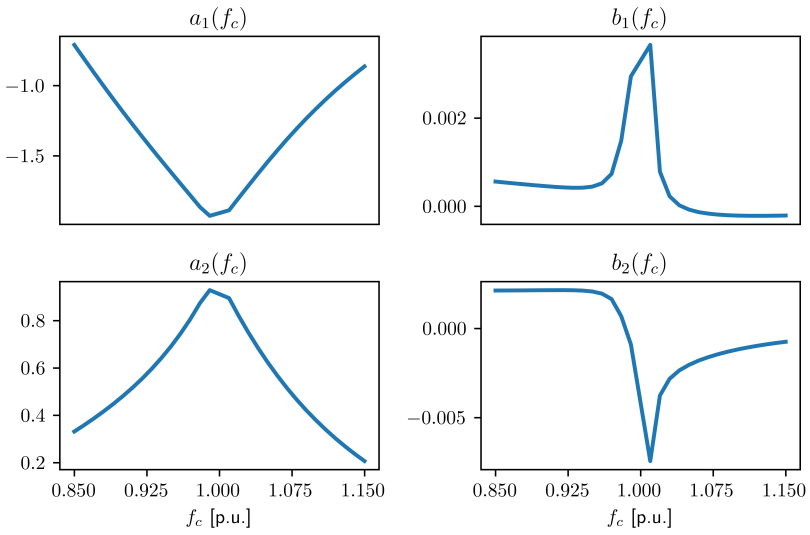


Figure 6.27: Switching frequency dependence of coefficients a_1, b_1, a_2 and b_2 of the small-signal discrete-time transfer function $\mathbf{G}\left(z^{-1}\right)$

frequency changes. In Fig. 6.27 the frequency dependence for the 4 coefficients in $\mathbf{G}\left(z^{-1}\right)$ is shown.
It is now possible to build a matrix whose representation is entirely on the frequency domain by running a Bode analysis for every TF and building a new matrix $\mathbf{E}_f$ as follows

$$\mathbf{E}_f = \left[\begin{array}{cccc} | & | & | & | \\ i_o(f_1) & i_o(f_2) & \dots & i_o(f_N) \\ | & | & | & | \end{array}\right] \Bigg\} \mathrm{M} \tag{6.23}$$

where the $(m,\, n)$-th element of $\mathbf{E}_f$ is the measurement

$$\mathbf{E}_f^{(m,n)} = i_o\left(f_c\left(m\right),\, f_m\left(n\right)\right)$$

In Fig. 6.28 the 3D map representing the matrix $\mathbf{E}_f$ is illustrated. The X-axis represents the normalized carrier switching frequency, with normalization factor f_r (resonant point) while the Y-axis represents the normalized modulation frequency in the range $[0.1,\ 1]$, where 1 is the Nyquist point for that carrier. In Fig. 6.29 the Bode plots for a small number of carriers is shown. The latter figure is a 2D representation of Fig. 6.28.

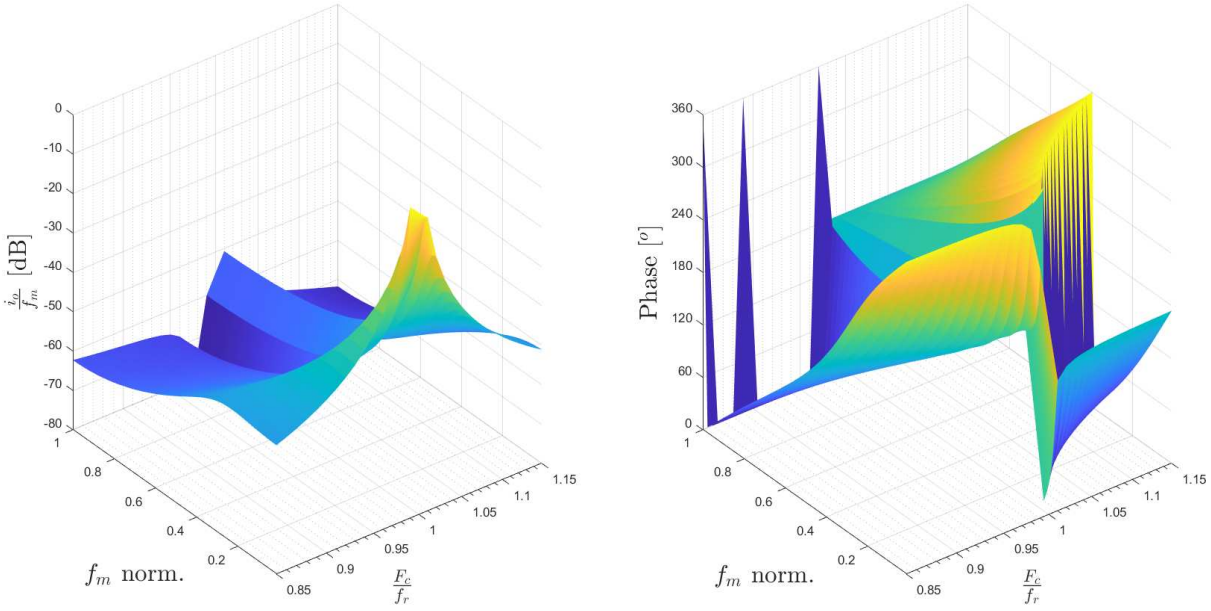


Figure 6.28: Small signal reconstruction maps. The current to frequency gain is shown on the left (computed as $20\log_{10}\left(A/Hz\right)$) while the phase is shown on the right figure.

An idea for utilizing these results would be to use a *multivariate regression* from data in order to build an analytical (scalar) function g in the two variables f_c (normalized carrier) and f_m (normalized modulating frequency)

$$i_o\left(f_c,\, f_m\right) = g\left(f_c,\, f_m\right) \tag{6.24}$$

Let's imagine that the function $g(\cdot\,,\,\cdot)$ can be expressed as a 3^{rd} order polynomial in the variables $\mathbf{x} = (f_c,\, f_m)$, which means that the function can be expressed as in Eq. (6.25).

$$g\left(\mathbf{x}\right) = \sum a_{i_1 i_2 \dots i_d} \prod_{j=1}^{d} x_j^{i_j} \tag{6.25}$$

Analysing the columns of $\mathbf{E}_f$ (6.26) we find that

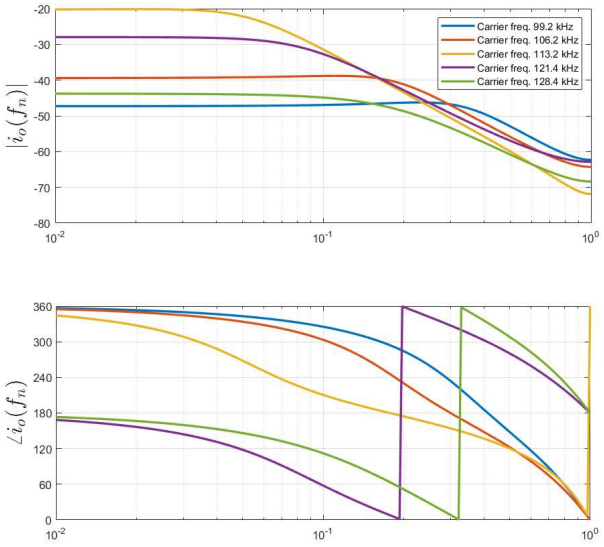


Figure 6.29: Bode representation for different carriers

$$\mathbf{E}_f = \begin{bmatrix} \mathbf{i}_o^T(f_1) \\ \mathbf{i}_o^T(f_2) \\ \vdots \\ \mathbf{i}_o^T(f_M) \end{bmatrix} = \begin{bmatrix} i_1(f_1) & i_2(f_1) & \dots & i_N(f_1) \\ i_1(f_2) & i_2(f_2) & \dots & i_N(f_2) \\ \vdots & \vdots & \dots & \vdots \\ i_1(f_M) & i_2(f_M) & \dots & i_N(f_M) \end{bmatrix} \tag{6.26}$$

It is possible to define $i_n(f_m)$ as the (averaged) output current obtained by the mth carrier in vector $f_c = [f_c(1), f_c(2), \dots, f_c(M)]$ and modulated with the nth frequency in vector $f_m = [f_m(1), f_m(2), \dots, f_m(N)]$. If the 3^{rd} order polynomial solution is sought, then we have that

$$\begin{aligned} \mathbf{E}_f(m,n) \approx & \sum_{j=0}^{3} \sum_{k=0}^{3-j} \boldsymbol{\xi}_{jk}(m,n) f_c^j(m) f_m^k(n) \\ = & \boldsymbol{\xi}_{00}(m,n) + \boldsymbol{\xi}_{10}(m,n) f_c(m) + \boldsymbol{\xi}_{01}(m,n) f_m(n) + \\ & \boldsymbol{\xi}_{20}(m,n) f_c^2(m) + \boldsymbol{\xi}_{02}(m,n) f_m^2(n) + \dots \end{aligned} \tag{6.27}$$

where every coefficient $\boldsymbol{\xi}_{jk}$ is an M-by-N matrix containing the "weights" for the jkth term of the polynomial and $\boldsymbol{\xi}_{jk}(m,n)$ is the $(m,n)^{th}$ entry of said matrix.
Given the observations obtained in $\mathbf{E}_f$, we can build a library matrix $\boldsymbol{\Theta}(\mathbf{X})$ consisting of candidate polynomial functions of the independent variables $\mathbf{x} = (f_c,\, f_m)$.

$$\boldsymbol{\Theta}(\mathbf{X}) = \begin{bmatrix} | & | & | & | \\ \mathbf{1} & \mathbf{X} & \mathbf{X}^{P_2} & \mathbf{X}^{P_3} \\ | & | & | & | \end{bmatrix}^T \tag{6.28}$$

with the final goal to reach a solution where

$$\boldsymbol{\Theta}(\mathbf{X})\, \boldsymbol{\Xi} \approx \mathbf{E}_f \tag{6.29}$$

Note that the previous equation assumes form $\mathbf{A}\mathbf{x} = \mathbf{b}$ where $\mathbf{x}$ is the unknown to be found (coefficients of the polynomial) given an observation data set $\mathbf{b}$ and the function library $\mathbf{A}$. In theory this problem could be solved as $\boldsymbol{\Xi} = \boldsymbol{\Theta}(\mathbf{X})^{\dagger} \mathbf{E}_f$, where the dagger operator $\dagger$ indicates the Moore Penrose pseudoinverse.

$$\boldsymbol{\Xi} = \begin{bmatrix} | & | & | & | \\ \boldsymbol{\xi}_0 & \boldsymbol{\xi}_1 & \boldsymbol{\xi}_2 & \boldsymbol{\xi}_3 \\ | & | & | & | \end{bmatrix} \tag{6.30}$$

Another idea is to fit the time response of the 3^{nd} order degree polynomial $G_m\left(z^{-1}\right)$ and suppose that the parameters a_1, a_2, b_1 and b_2 are a function of the carrier frequency in polynomial fashion. Note that $a_0 = 1$ and $b_0 = 0$ always. The a_1 parameter (and consequently all the others) can be written as

$$a_1 = a_1^{(0)} + a_1^{(1)} f_c + a_1^{(2)} f_c^2 + a_1^{(3)} f_c^3 \tag{6.31}$$

Obviously, we have a column vector containing M of these a_1 coefficient, just as any other coefficient that builds Eq. (6.22), because we have executed M simulations (one for every carrier in vector $[f_c(1), f_c(2), \ldots, f_c(M)]$). Therefore we can build the following regression problem in the form of

$$\mathbf{A}\mathbf{x} = \mathbf{b} \tag{6.32}$$

where

$$\begin{aligned} \mathbf{A} &= \begin{bmatrix} | & | & | & | \\ 1 & f_c(m) & f_c(m)^2 & f_c(m)^3 \\ | & | & | & | \end{bmatrix} \\ \mathbf{x} &= \begin{bmatrix} a_1^{(0)} & a_1^{(1)} & a_1^{(2)} & a_1^{(3)} \\ a_2^{(0)} & a_2^{(1)} & a_2^{(2)} & a_2^{(3)} \\ b_1^{(0)} & b_1^{(1)} & b_1^{(2)} & b_1^{(3)} \\ b_2^{(0)} & b_2^{(1)} & b_2^{(2)} & b_2^{(3)} \end{bmatrix}^T \\ \mathbf{b} &= \begin{bmatrix} | & | & | & | \\ a_1(m) & a_2(m) & b_1(m) & b_2(m) \\ | & | & | & | \end{bmatrix} \end{aligned} \tag{6.33}$$

the solution $\hat{\mathbf{x}}$ is found by solving the problem in (6.34) where every column of the $\hat{\mathbf{x}}$ holds the coefficients in Eq. (6.31).

$$\hat{\mathbf{x}} = \underset{\mathbf{x}}{\operatorname{argmin}} \|\mathbf{A}\mathbf{x} - \mathbf{b}\|_2 \tag{6.34}$$

This can also be easily solved with the dagger operator as $\hat{\mathbf{x}} = \mathbf{A}^{\dagger}\mathbf{b}$. In Fig. 6.30 the difference between actual coefficients and the fit found using the aforementioned idea is illustrated. Apparently, the fit is not good with only 3 terms in the polynomial.

6.4.3 Regression by over-fitting

Since no small order polynomial seem to be well suited for fitting these kind of curves, we try a so called "over-fitting" approach. This means that the library matrix $\mathbf{A}$ is built by a big number of candidate functions, hence the likelihood that some of those functions match the actual model becomes higher. Surely the fitting will hold a better result, hence the mean squared error (MSE) between actual observation and fit data will be very close to zero, but there will be a lot of terms composing the fit results, which is an annoying problem if we want to be able to use these information online on a low-cost DSP. We say that out model prediction *overfits* the data (there are A LOT of functions!).
Other then this, since there seems to be some sort of symmetry around the resonant point (when f_n is 1), a good hint would be to build the matrix $\mathbf{A}$ as a function of $f_n - 1$ rather then

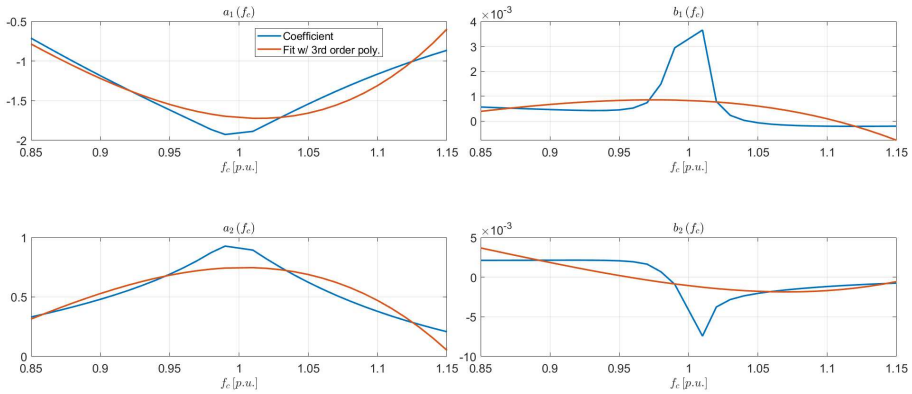


Figure 6.30: Comparison between actual coefficient evolving with carrier frequency (blue line) and 3^{rd} order polynomial fit (orange line)

f_n alone. We define, for simplicity sake, $x = f_n - 1$.
The candidate functions are *Laurent polynomials* (i.e. polynomials that accept both positive and negative exponents), where a Q-degree Laurent polynomial is generally expressed as

$$\mathbf{P_Q}(x) = a_{-Q}x^{-Q} + \cdots + a_{-1}x^{-1} + a_0 + a_1 x + \cdots + a_Q x^Q$$

and *fractional radicals*, which are polynomials whose exponent can be expressed in the form of p/q with $p \in \mathbb{Z}$ and $q \in \mathbb{N}_0$ with $\mathbb{Z}$ being the set of integers $(\dots, -2, -1, 0, 1, 2, \dots)$ and $\mathbb{N}_0$ the set of positive integers without 0 element. This portion of the library is built respecting few constrains

- $p/q \notin \mathbb{N}$ (is non-integer)
- $|p/q| < Q$ (this creates an upper bound on the total function degree uniquely set by Q)
- if q is even and $x < 0$, we don't take into account the value $x^{p/q}$ but rather $\left(x^2\right)^{(p/2q)}$ to avoid complex solutions
- the elements p/q must be unique

Let's update some definitions. From now on we will call $\mathbf{y}$ the observation matrix, which we called $\mathbf{b}$ in Eq. (6.33).

$$\mathbf{y} = \begin{bmatrix} | & | & | & | \\ a_1(m) & a_2(m) & b_1(m) & b_2(m) \\ | & | & | & | \end{bmatrix} \tag{6.35}$$

We call $\mathbf{\Theta}(\mathbf{x})$ the library matrix, where every column is a function of the frequency

$$\mathbf{x} = [f_1 - 1,\ f_2 - 1,\ \dots f_M - 1]^T$$

$$\begin{matrix} & f_1(\mathbf{x}) & f_2(\mathbf{x}) & \dots & \dots & \dots & \dots & \dots & \dots & f_{(P-1)}(\mathbf{x}) & f_P(\mathbf{x}) \\ \mathbf{\Theta}(\mathbf{x}) = \big[& \mathbf{x}^{-Q} & \mathbf{x}^{-(Q-1)} & \dots & \mathbf{x}^{-p/q} & \dots & \mathbf{x}^{p/q} & \dots & \mathbf{x}^{(Q-1)} & \dots & \mathbf{x}^{-Q} \big] \end{matrix} \tag{6.36}$$

and finally we define $\boldsymbol{\beta}$ the matrix containing the unknown coefficients which shall be estimated and we're looking for the best fit $\hat{\boldsymbol{\beta}}$ that solves the following least-squares problem

$$\hat{\boldsymbol{\beta}} = \arg\min_{\boldsymbol{\beta}} \|\mathbf{\Theta}(\mathbf{x})\boldsymbol{\beta} - \mathbf{y}\|_2 \tag{6.37}$$

where the columns of $\hat{\boldsymbol{\beta}}$ hold the coefficients for building a_1, a_2, b_1 and b_2 respectively. What is happening solving this problem, is trying to fit every (coefficient) observation like the following function. The example is expressed for a_1, but every other coefficient will have a similar structure.

$$\begin{aligned} a_1(x) =& \beta_{-Q}x^{-Q} + \beta_{-(Q-1)}x^{-(Q-1)} + \cdots + \beta_{-p/q}x^{-p/q} + \cdots + \beta_{-1}x^{-1} + \\ & \ldots \beta_0 + \beta_1 x + \cdots + \beta_{p/q}x^{p/q} + \cdots + \beta_Q x^Q \end{aligned} \tag{6.38}$$

In Fig. 6.31 we can see how good the matching between actual a_1, a_2, b_1 and b_2 coefficients and fit function from $\boldsymbol{\Theta}(\mathbf{x})$ library is.

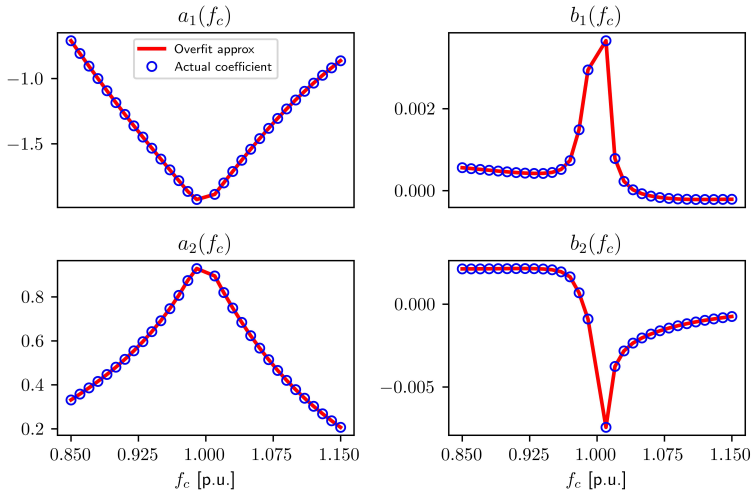


Figure 6.31: The four coefficients after running the above-mentioned procedure. Degree Q is set to 3 in this example. We have the following fitting errors (computed via MSE): $MSE_{a1} = 5.4502e-9$, $MSE_{a2} = 2.5989e-9$, $MSE_{b1} = 1.5433e-12$ and $MSE_{b2} = 1.9451e-12$

As mentioned above, this is not really a good procedure since the number of terms used for approximating every single coefficient can get really big quickly. If $Q = 5$ is selected, 39 total functions must be evaluated for every one of the 4 coefficients building the transfer function.

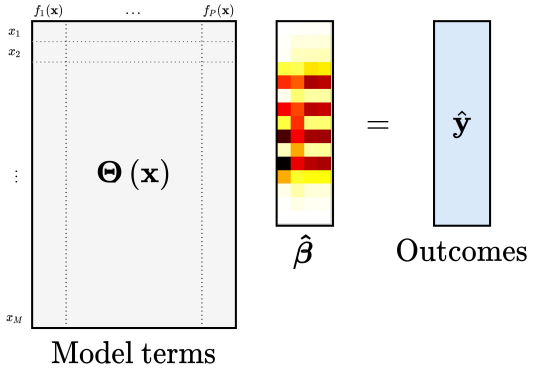


Figure 6.32: Schematic representation of the least-square (over)fitting method.

In Fig. 6.32 the regression result for procedure explained in (6.37) is graphically illustrated. The matrix $\boldsymbol{\Theta}(\mathbf{x})$ contains (in every column) the functions applied to the independent variable $x_j = f_j - 1$ where the subscript j in the previous notation represents the j^{th} element (which in this case is the carrier frequency). The matrix of solutions $\hat{\boldsymbol{\beta}}$ has most elements in every column "lit up", which means that almost all coefficients are important for the accurate regression of the

problem. The outcomes matrix $\hat{\mathbf{y}}$ contains the regressed coefficients as a function of $\mathbf{x} = \mathbf{f} - 1$. We hope (and that is in fact true as it is possible to see from the plots in Fig. 6.31) that the error between measured coefficients $\mathbf{y}$ and regressed ones $\hat{\mathbf{y}}$ is small, where the metric for error computation is the MSE, $\mathbf{y}_\Delta = \|\mathbf{y} - \hat{\mathbf{y}}\|_2$. In this specific case where $Q = 3$ has been selected, 15 total functions are used to try and estimate the tendency of the $\mathbf{G}\left(z^{-1}\right)$ transfer function coefficients. Online computation of 15 terms for every coefficient is obviously not feasible in low cost DSP architectures, that in many automotive application might be required to be smaller then 5$ for applications where these kind of converters are commonly used, like in OBCs and HV-to-LV or HV-to-MV DC/DC converters. This leads to the need of a *solution sparsification*.

6.4.4 Fitting via LASSO

For this purpose, the LASSO [88] method (Least Absolute Shrinkage and Selection Operator) comes in very handy since its goal is trying and sparsify the solution. The LASSO is an ℓ_1 penalized regression that balances model complexity with descriptive ability [89]. The biggest problem of the a least-squares on

$$\boldsymbol{\Theta}(\mathbf{x})\boldsymbol{\beta} = \mathbf{y}$$

is that the solution vector $\boldsymbol{\beta}$ has non-zero coefficients everywhere which means that *all* columns of the library matrix $\boldsymbol{\Theta}(\mathbf{x})$ shall be used to predict the outcome $\mathbf{y}$ even if we believe that the model representing the data shall have fewer elements, hence indicating that $\boldsymbol{\beta}$ should be sparse. Adding an ℓ_1 penalty to the solution allows for regularization of the least-squares regression, ultimately preventing over-fitting:

$$\hat{\boldsymbol{\beta}} = \arg\min_{\boldsymbol{\beta}} \left\{ \|\boldsymbol{\Theta}(\mathbf{x})\boldsymbol{\beta} - \mathbf{y}\|_2 + \lambda_1 \|\boldsymbol{\beta}\|_1 \right\} \tag{6.39}$$

Usually the ℓ_1 penalty term λ_1 is swept through different values and the fit is validated against a test set. Often, a k-fold cross-validation is adopted [90], where the total data is divided in k subsets to perform k rounds of training where on every round $1/k$ of the data set is used for testing. The average test score of the k rounds should be better then a single estimation. For the problem that we need to solve, hence the one in Eq. (6.33), the observation and coefficients matrices $\mathbf{y}$ and $\boldsymbol{\beta}$ respectively, are M×4 sized where M is the number of observations (simulations) and 4 is the number of different data-sets that need to be fit. It is commonly used the term of having a problem made up by 4 *tasks*. Because of this, 4 different runs need to be computed to find the trend for every coefficient since the "standard"-LASSO can only regularize features for single-tasked problems. In case of multi-task solution, the "Multi-task" LASSO [91] needs to be considered, which allows for selecting the same model terms for every task (column).
In Fig. 6.33 we see how it performs against our data set where the sparsification of the solution is undeniable when compared to the optimal one obtained via LSE regression shown in Fig. 6.32. In Fig. 6.34 the fitting and actual data set are compared. Obviously the error is greater then the overfitting solution studied in the previous case, but the number of active coefficients is much smaller. The results are, as expected, much more applicable to DSP implementation.
Decreasing the N_{a_1} and N_{b_2} from 6 to a smaller number shall be considered since these many terms might result in a strongly time consuming task to run real-time. Moreover, the fact that all four functions depend on different model terms contained in the library $\boldsymbol{\Theta}(\mathbf{x})$ might pose a non-trivial challenge in for fast computation requirements. Up to this point, the procedure has been carried out without k-fold cross-validation hence no testing on the results has been done. The input data set is rather small (30 carrier frequencies have been simulated) hence choosing a k of 2 or 3 is the best we can hope for (which is usually considered rather small). In order to force a more aggressive representation of the data set two actions have been taken.

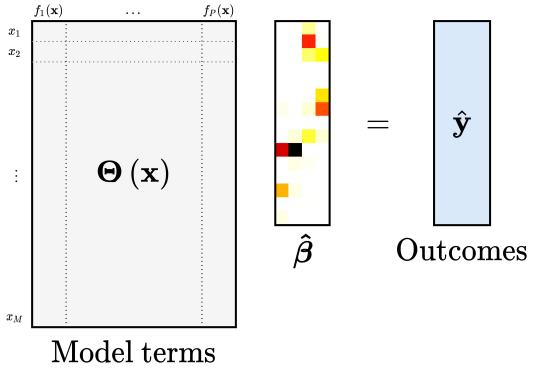


Figure 6.33: Schematic representation of one solution obtained via LASSO fitting. The vector $\hat{\boldsymbol{\beta}}$ is sparse if compared to the one obtained in LSE problem illustrated in Fig. 6.32

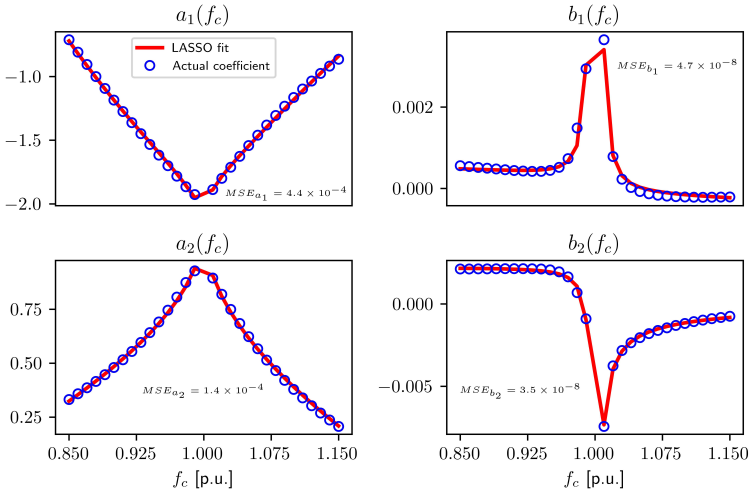


Figure 6.34: LASSO fitting performance. The number of coefficients obtained in this manner is $N_{a_1} = 6$, $N_{a_2} = 5$, $N_{b_1} = 5$ and $N_{b_2} = 6$. Out of all the possible λ_1 values for every function, the ones that allow for minimum MSE have been selected

Increase the available data-set (easily obtainable by increasing the simulation number for the carrier frequency) and selecting a more aggressive λ_1 to promote sparsity.
After some simulations a new data-set is available where M has increased from 30 to 292 points with f_c going from 0.85 to 1.15 with 0.01 spacing (note that some points around the resonance have not been simulated in order to avoid singularities in the solution). We now have a sufficiently large quantity of simulations in order to run a 5-fold or 10-fold cross-validation, which would have proven to be a difficult task beforehand.

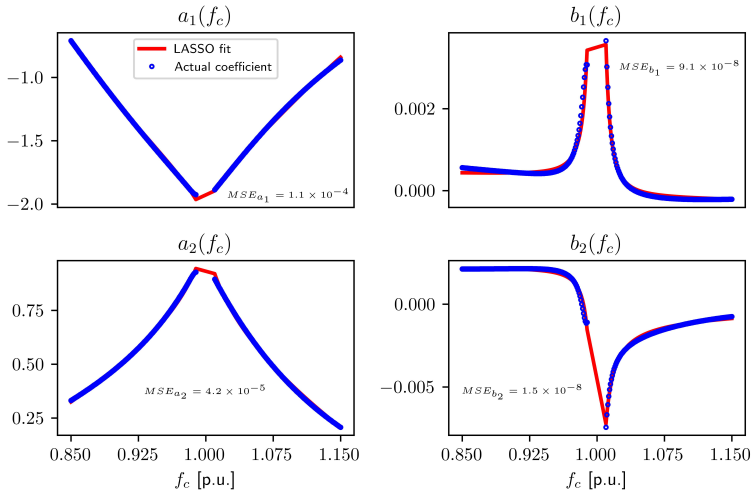


Figure 6.35: Another LASSO fitting performance. The number of coefficients obtained in this manner is $N_{a_1} = 6$, $N_{a_2} = 6$, $N_{b_1} = 5$ and $N_{b_2} = 8$ with lambdas $\lambda_1 = [2e-3,\ 1.4e-3,\ 8e-5,\ 6e-5]$

In Fig. 6.35 the result of latter fitting is shown and some considerations/comparison can be done. First and foremost, differently from the case with 30 points, another metric for choosing the ℓ_1 penalties has been adopted. While before the value that assured the smallest MSE error between fit function and measured point was reached, now a different strategies is chosen which relies on the statistical nature of the regression itself and the cross-validation results. Since a 10-fold cross-validation has been used, the data set has been divided into 10 subsets where each is missing 1/10 of elements which is later used for testing the regression quality done on the 9/10 training set. With this method for every λ_1 we now have 10 possible fits, each with their own average MSE and standard deviation. We can build the **MSE** matrix as in Eq. (6.40) where L is the number of proposed λ_1 and K is the data set division factor (i.e. 10 in case of 10-fold cross-validation).

$$\mathbf{MSE} = k \begin{array}{c} \downarrow \\ \left[\begin{array}{cccc} \mathrm{MSE}_{11} & \mathrm{MSE}_{12} & \dots & \mathrm{MSE}_{1L} \\ \mathrm{MSE}_{21} & \mathrm{MSE}_{22} & \dots & \mathrm{MSE}_{2L} \\ \vdots & \vdots & \dots & \vdots \\ \mathrm{MSE}_{K1} & \mathrm{MSE}_{K2} & \dots & \mathrm{MSE}_{KL} \end{array}\right] \end{array} \begin{array}{c} \overset{\lambda_1}{\longrightarrow} \\ \end{array} \tag{6.40}$$

where for every column of **MSE** there are the 10 solution of the cross-validation. Given an error vector for every fit trial $\mathbf{y}_\Delta$, its mean squared error is computed as

$$\mathrm{MSE} = \frac{1}{P}\,\mathbf{y}_\Delta^T\,\mathbf{y}_\Delta$$

where the error vector is defined as

$$\mathbf{y}_\Delta = \mathbf{y} - \boldsymbol{\Theta}(\mathbf{x})\hat{\boldsymbol{\beta}}$$

Here P is the error vector length hence the size of the function set, as previously defined, $\mathbf{y}$ is the observation vector of length P (for example the measurement $a_1\,(f_c)$ for every frequency simulated), $\hat{\boldsymbol{\beta}}$ is the sparse weights vector that selects the functions in the library $\boldsymbol{\Theta}(\mathbf{x})$. Since we're doing a k-fold repetition, the number of solution vectors $\hat{\boldsymbol{\beta}}$ is $L \times K$. For every column l of **MSE** (hence every value of λ_1) we can define its mean and standard deviation

$$\begin{aligned} \mu_l &= \frac{1}{K}\sum_{k=1}^{K} \mathrm{MSE}_{kl} \\ \sigma_l &= \sqrt{\frac{1}{K}\sum_{k=1}^{K} \left(\mathrm{MSE}_{kl} - \mu_l\right)^2} \end{aligned} \tag{6.41}$$

Out of the columns (lambdas) of **MSE**, there is one value of λ_1 out of those chosen for the possible fittings that shows the smallest value $\boldsymbol{\mu}$. We define for said column (indicate it with an overline $\overline{\square}$) these metrics

$$\begin{aligned} \overline{\mu} &= \min(\boldsymbol{\mu}) \\ \overline{\sigma} &= \sigma \text{ associated with } \overline{\mu} \end{aligned} \tag{6.42}$$

a solution commonly adopted for choosing a good shrinkage parameter for fitting, is to select the biggest λ_1 (call it $\tilde{\lambda}_1$) whose mean MSE (μ) is within 1 standard deviation from $\overline{\mu}$

$$\tilde{\lambda}_1 = \arg\max_{\lambda_1} \left\{\lambda_1 \,|\, \mu(\mathbf{MSE}(\lambda_1)) < \overline{\mu} + \overline{\sigma}\right\} \tag{6.43}$$

This means that solving the problem in Eq. (6.44) should give the sparsest solution while retaining a relatively small error.

$$\tilde{\boldsymbol{\beta}} = \arg\min_{\boldsymbol{\beta}} \left\{ \|\boldsymbol{\Theta}(\mathbf{x})\boldsymbol{\beta} - \mathbf{y}\|_2 + \tilde{\lambda}_1 \|\boldsymbol{\beta}\|_1 \right\} \tag{6.44}$$

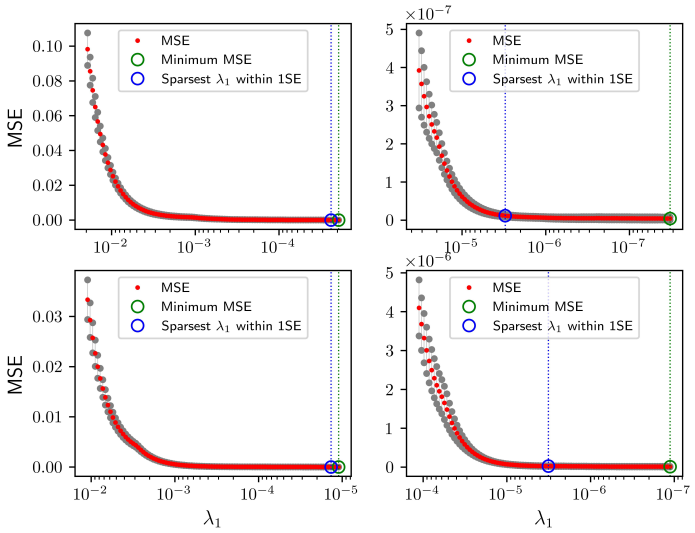


Figure 6.36: Cross-correlation plot of the LASSO's performed for every coefficient in $\mathbf{G}\left(z^{-1}\right)$. The plots are referred to a_1 (top-left), a_2 (bot-left), b_1 (top-right) and b_2 (bot-right)

In Fig. 6.36 the cross-correlation plots are shown for the discrete-time transfer function coefficients, where the λ_1 that produces the minimum MSE and the one that stands within one $\overline{\sigma}$ are highlighted. It is relatively straightforward to think that we can be a little bit more "aggressive"

with the shrinkage parameter selection since the error seems rather flat on all the four graphs up until the point where λ_1 becomes too big and the error starts rising (left-side of the plots). As highlighted in Fig. 6.35, the number of coefficients obtained with the cross-validation strategy on the increased size data-set, gives a bigger non-zero number of coefficients for all the four tasks if compared with the regression adopted on the smaller data-set without cross-validation (see Fig. 6.34). This can be explained by the fact that having a bigger data-set on which the fit needs to be computed, reduces the functional freedom. Said in other words, having more points on which the regression needs to be evaluated, decreases the distance between two data points hence a bigger linear combination of functions needs to be adopted in order to force the error between fit and actual data as small as possible.

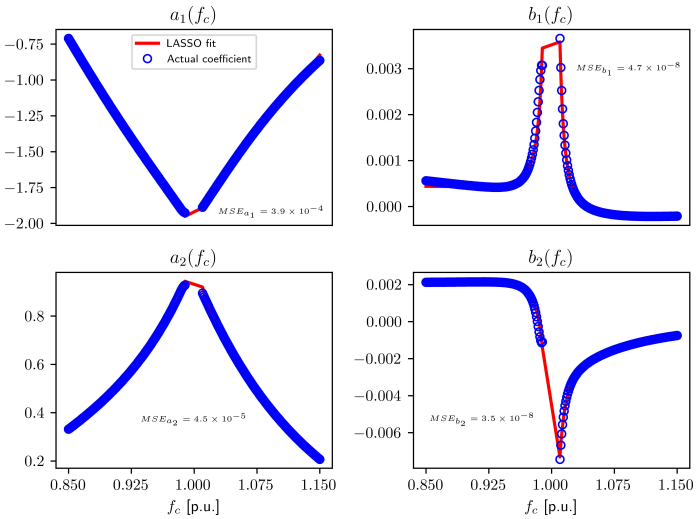


Figure 6.37: LASSO fitting with the newly defined strategy for ℓ_1 penalizer selection

It is possible of think about this issue in the trivial 2 and 3 points data set. In the 2 points data set we only need 2 degrees of freedom to fit perfectly (with no error) the data by using a straight line. Using a straight line in a 3 elements input set surely results in a big error (unless the data points are perfectly aligned hence there's no linear independence between the data-set variables) and, in order to reduce it, we need to add a new degree of freedom (x^2) and interpolate by using a parabola rather then a line.
Another criteria for λ_1 selection is proposed in order to decrease the regression complexity. We select a fixed number of terms B for every task and, out of all shrinkage parameters λ_1 that assures said number of active regressors, the one that allows for smaller MSE is selected.

$$\hat{\lambda}_1 = \arg\min_{\lambda_1} \{\text{MSE}(\lambda_1) \text{ subject to } nnz(\boldsymbol{\beta}) = B\}$$

The results are show in Fig. 6.37 illustrate this very last strategy for the selection of λ_1. Every task is fit with 5 weights, still yielding an acceptable error.

6.5 Parametrization along voltage conversion ratio

When trying to fit the discrete-time average output current transfer function coefficients, either by using an over-fitting approach or the LASSO method explained beforehand, an assumption on the output voltage was made; that is the conversion ratio $\text{M} = nV_o/V_{bus}$ is a fixed quantity. This is not true in two different ways.
The output voltage can increase or decrease over time since it might represents an approximated model for a battery to be charged for example. Not only that, but due to failures or other

reasons, the load voltage might change abruptly (maybe by small quantities). This poses the need to parametrize the behaviour of the converter along this second degree of freedom (DOF). After all, when trying to characterize the behaviour of the converter around an equilibrium point, the definition of equilibrium point is "the state $\overline{\mathbf{x}}$ caused by a constant input $\overline{\mathbf{u}}$". In the LLC cased analysed up to this point, the vector $\mathbf{u}$ is defined as

$$\mathbf{u}(t) = [f_{sw}(t),\, v_o(t)]$$

where the variable $v_o(t)$ is not controlled - since the battery voltage depends on the SoC (State of Charge) - but using it as a "fictitious input" allows to defined the system response to variation of said input in order to understand the behaviour of the converter. Generalizing this concept in a mathematical equation yields the result in Eq. (6.45)

$$di_o = \frac{\partial i_o}{\partial f_{sw}} df_{sw} + \frac{\partial i_o}{\partial v_o} dv_o \tag{6.45}$$

In order to have a complete model of the converter, one should theoretically understand the effect of the small change in output current due to a variation of frequency (when the output voltage is kept constant) and due to a voltage variation (when the frequency is kept constant). These two variational quantities $\partial i_o/\partial f_{sw}$ and $\partial i_o/\partial v_o$ shall be computed for every equilibrium pair $\overline{\mathbf{u}}$.
In the sections before, we identified (via simulation) only the first partial derivative in Eq. (6.45) by sweeping the frequency alone but leaving the output voltage at the same level, which results in the identification of 1-D functions.

6.5.1 Identification of the frequency dependent partial derivative map

Two quantities need to be identified for every working condition pair $\overline{\mathbf{u}} = (F_{sw},\, V_o)$:

1 $\overline{I}_o\,(F_{sw},\, V_o)$ - the DC current level for every bias

2 $\partial i_o/\partial f_{sw}\,(F_{sw},\, V_o)$ - the small signal response to a frequency perturbation df_{sw} for every bias point

The first point has not been done before, but actually comes in for free once the step response simulation is done because at the time instant t_0 where the frequency is step-perturbed, the average output current assumes its bias value $\bar{i}_o(t_0) = I_o\,(F_{sw},\, V_o)$.
In Fig. 6.38 the 3-D map of the average output current depending on switching frequency F_{sw} and output voltage V_o. The red line highlights a "unidimensional" case is illustrated where the voltage conversion ratio is fixed to M = 1.2.
For every quantity we're interested in, we'll now have a 3-D map since the domain in composed by both the frequency and conversion ratio. This means that, the small-signal approximation where we did use the LASSO, actually is to be interpreted with 2 DOF hence a_1, a_2, b_1 and b_2 depend on (f_c, M). This actually poses a big challenge in the implementation of an hypothetical LASSO regularization on the data set.
In Fig. 6.39 the output current as a function of normalized switching frequency (also called *carrier frequency*) and voltage conversion ratio M is shown "from above". All the points where the current exceeds a certain threshold have been eliminated since they represent a physical solution which is not reachable by the converter (i.e. $100\,A$ or above). Note also the presence of a singularity in buck mode ($\mathrm{M} < 1$) around the resonant point ($f_n = 1$). The presence of a singularity around the resonance can be proven analytically by using the equations illustrated in Chapter 5. In boost mode ($\mathrm{M} > 1$) no singularity appears, but a bothersome problem which might cause many issues is seen. At a fixed M there comes a point along the frequency axis

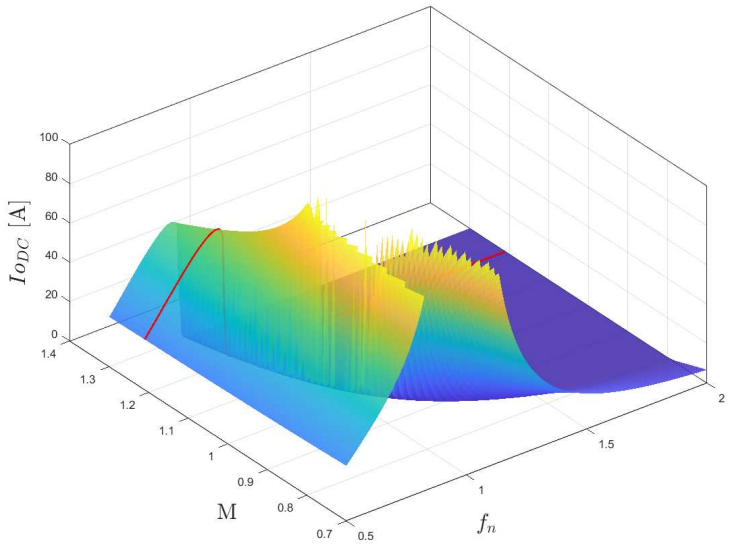


Figure 6.38: Map of average output current $\bar{i}_o$ as a function of (F_{sw}, V_o)

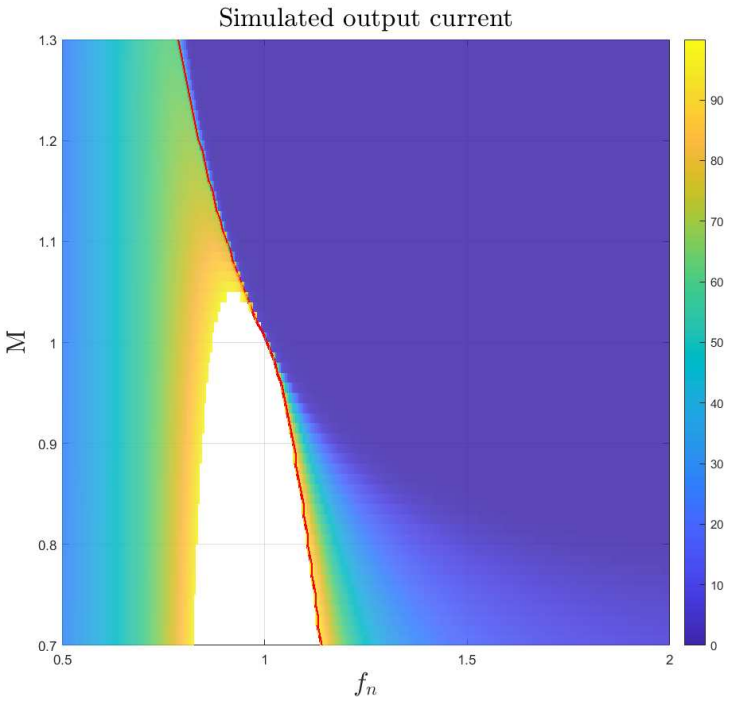


Figure 6.39: i_o as a function of f_n and M (top view)

where the current changes drastically with a small change of frequency. Mathematically, this can be expressed as the presence of a huge partial derivative with respect to frequency

$$\left|\frac{\partial i_o}{\partial f_n}\right| \gg 0$$

This feature is unwanted since the presence of huge derivatives might induce instabilities in the control action because a big change in output current occurs in the face of a small change in frequency. In Fig. 6.39 the red line shows the locus where the maximum current derivative with respect to frequency lies, and it is clearly visible due to colouring that said line separates (along the x-axis) zones where the current is huge by zones where it is small. By moving up in voltage conversion (greater M) the red line tends to move to the left (smaller frequencies), indicating that a possible symmetry of the library functions derived in Section 6.4.3 (i.e. $x = f_n - 1$) would

not produce good results since the symmetry in frequency changes with the output voltage in boost mode.

6.5.2 Difficulty in functional regression for the 2-DOF case

The problems one can think of when trying to come up with a function of 2 variables (2 degrees of freedom, DOF) that can fit the plot in Fig. 6.38 are various. Since we removed some points from the data-set in order to have a more reliable physical representation of the problem, in buck mode ($\mathrm{M} < 1$) there's no clear symmetry around the resonance point because it looks like the "hole" moves to the left (smaller frequencies) as the conversion ratio increases. As pointed out briefly before, in boost mode there seems to be a symmetry along the frequency axis that changes as the conversion ratio increases. Both in buck and boost mode, some sort of symmetry is expected (in buck approximately $f_n = 1$ while in boost around some $f_0(M)$), which might - at first glance - lead to think that a functional description like $I_{o,M}\left(f_n\right) = f(x)$ for $x = f_n - f_0(M)$ (where $f_0(M)$ is a function of M for keeping track of the symmetry) is to be sought. In different words, one might find a solution where it is possible to parametrize a LASSO regularization for every conversion ratio M. In a real world implementation, this means that we need to "slice" the conversion ratio axis in order to have some finite dimensional space, hence

$$\mathrm{M} \in \mathcal{M} \text{ where } \mathcal{M} = \{\mathrm{M}_1, \mathrm{M}_2, \ldots \mathrm{M}_H\}$$

like for example $\mathrm{M}_{1:H} = 0.7 : 0.01 : 1.3$ (written in "MatLAB style"). For every point in $\mathcal{M}$, a LASSO regularization is computed, and for every regression two things need to be saved: the coefficients building up the regression (i.e. $\boldsymbol{\beta}'$) which is a finite dimensional vector (say B-dimensional) and the exponents (same dimension) that associates every element in $\boldsymbol{\beta}'$ to an element in $\mathbf{E}$ in order to perform the regression

$$\tilde{I}_o\left(f_n; \mathrm{M}\right) = \sum_{j=1}^{B} \beta_j x^{e_j}, \, \forall \mathrm{M} \in \mathcal{M} \tag{6.46}$$

where the following definitions have been applied

B	dimension of vector $\boldsymbol{\beta}'$
$\boldsymbol{\beta}'$	LASSO regression coefficient vector $\boldsymbol{\beta}$ deprived of zeros
β_j	j^{th} element of $\boldsymbol{\beta}'$
e_j	j^{th} element of $\mathbf{E}$
$\mathbf{E}$	vector containing an exponent e for every coefficient β
$x = f_n - f_0(\mathrm{M})$	regression variable function of the frequency
$f_0(M)$	symmetry point in frequency dependent on M (H-dim)
$\tilde{I}_o\left(f_n; \mathrm{M}\right)$	regressed current depending on f_n and parametrized on M

The memory requirements for this kind of mapping depend on how thin the voltage conversion ratio axis is sampled. For every element M a vector $\boldsymbol{\beta}'$ and $\mathbf{E}$, both B-dimensional, are stored together with a f_0 element. Hence, the total memory needed for 1 task is $\mathrm{H}(1 + 2B)$ words. The tasks that need to be mapped are the average output current at steady-state and the 4 coefficients for the discrete-time small-signal transfer function, hence a total of 5 tasks. This consideration raises the total memory mapping to

$$\mathrm{Mem} = 5\mathrm{H}(1 + 2B) \text{ Words}$$

If $\mathrm{H} = 70$ and $B = 6$ we have Mem = 4.55 kWords which in a 32-bit floating-point system corresponds to ~ 17.8 kBytes. This might be a difficult requirement to accommodate with low-cost DSP available at the time being. The only possibility for shrinking the memory usage of

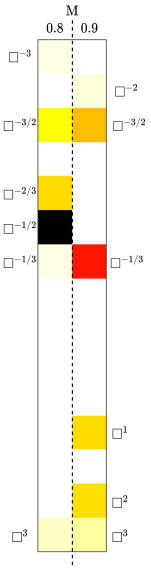


Figure 6.40: Two LASSO threads for different output voltage values: coefficient comparison

this technique is to reduce H (output voltage discretization) which might be a feasible strategy in some cases, but not always.
Other then memory constraints, another rather troublesome issue is to be considered. Imagine that, during online operation, we seek to find the small-signal transfer function for a given operating point $\hat{u} = (\hat{f}_n, \hat{\mathrm{M}})$, and that $\hat{\mathrm{M}} \notin \mathcal{M}$. How are the coefficients β, exponents e and symmetry point f_0 handled? If we pick one of the two M's closest to $\hat{\mathrm{M}}$, which is

$$\mathrm{M} = \arg\min_{\mathrm{M}} \left\{ \left| \hat{\mathrm{M}} - \mathrm{M}_k \right|, \left| \hat{\mathrm{M}} - \mathrm{M}_{k+1} \right| \right\}$$

then the reduction of H in order to accommodate the memory constrains plays against this matter.
The interpolation is the only true solution, but is not possible to implement. Consider a case similar to Fig. 6.40, that depicts two different conversion ratio points ($\mathrm{M} = 0.8$ and $\mathrm{M} = 0.9$) which are both regressed with LASSO regularization but yield different activated coefficients. The lit up cells represent that the coefficient multiplying the corresponding term is non-zero. The darker, the more "important" the coefficient is for the correct regression. In a hypothetical case where $\hat{\mathrm{M}}$ is 0.85 how does one deal with the absence of element $\square^{-3}$ in one of the two cases? Another method needs to be implemented for associating a pair (M, f_n) to the LLC output current and, consequently, to the small-signal transfer function coefficients.

Chapter 7

Dual Active Bridge

The Dual Active Bridge (DAB) topology has gained significant popularity in recent years. This is primarily due to its advantageous features, such as bidirectional operation and galvanic isolation, which make it well-suited for various applications like interfacing with renewable energy sources, battery storage systems, and smart grids. Despite extensive research, analyzing and controlling this type of converter remains challenging due to the numerous control variables that influence its complex behavior.

A comprehensive theoretical model for the single-phase DAB converter is introduced here, based on the work in [36]. This model is highly versatile, capable of accommodating various modulation techniques and operational scenarios. It views the converter as consisting of four legs, each capable of generating voltage across an inductor, and two output legs that can direct the resulting inductor current to the load. The key control inputs considered are the phase-shifts relative to one leg. This approach results in a straightforward yet accurate closed-form algorithm for determining the inductor current waveform.

Furthermore, a novel analytical model for calculating the average output current based on the phase-shift values is presented, independently of the output voltage. It also demonstrates that the average output current can be adjusted on a cycle-by-cycle basis with no additional dynamics. This means that the average output current remains unaffected by the initial inductor current value or any DC offset that may arise during transient conditions.

The proposed models have broad applications throughout the development of a DAB converter, including the design stage for rapid iteration, selecting operating points, and designing control systems. Based on the analytical findings, a novel control loop is proposed, involving a "fictitious" (open-loop) inner current regulation loop. This control scheme can be applied to various modulation schemes, such as Single Phase-Shift and Triple Phase-Shift. The primary advantage of this control approach is that it simplifies the relationship between output voltage dynamics and average output current, decoupling it from the complex interaction between phase-shifts and output current.

Additionally, the paper introduces a Finite Control Set (FCS) method, which selects optimal operating points for different operating conditions and control requirements, ensuring Zero-Voltage Switching (ZVS) in all scenarios. The analytical results and control methods presented are validated through simulations and extensive experimental testing.

The growing demand for electrical power conversion solutions, driven by factors such as the increased use of renewable energy and the electrification of transportation, is fuelling interest in interfacing different systems. These systems include energy storage devices, renewable energy sources, local and wide grids, and specific loads [92, 93]. Within this context, bidirectional isolated DC-DC converters are gaining prominence due to their versatility in various applications [94].

Despite substantial investments and research efforts by both industry and academia, numerous challenges persist in this field. Even small improvements in various aspects, particularly in terms

of efficiency, power density, reliability, and cost, can have a significant impact. Efficiency is a central focus in power electronics applications not only for the sake of energy conservation but also because issues related to thermal power dissipation are critical and ultimately influence the cost and size of converters. Fig. 7.1 illustrates some of the applications where DC-DC converters play a crucial role.

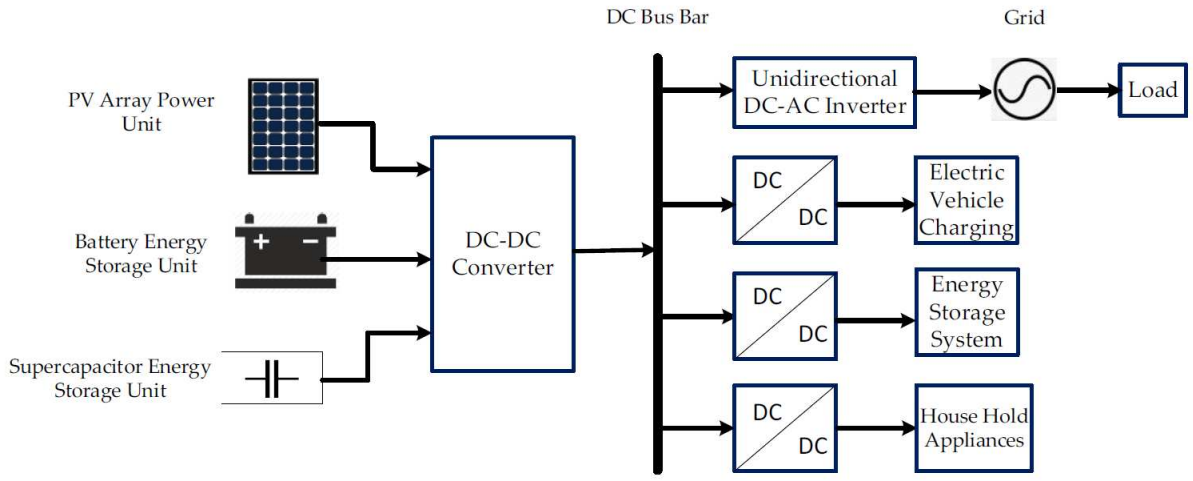
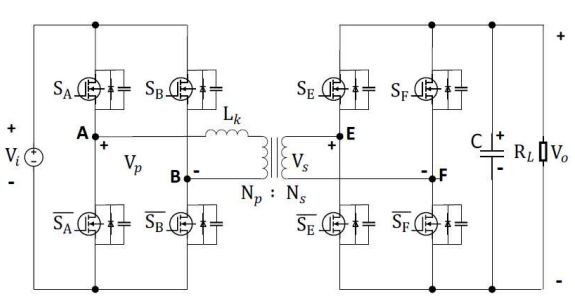
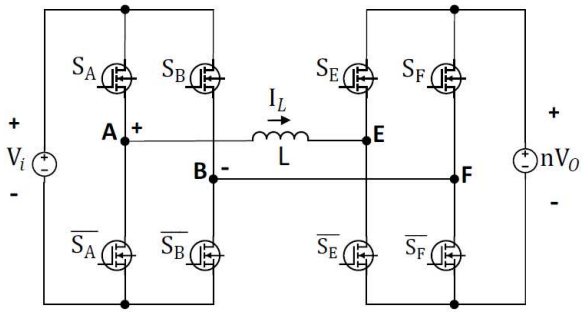


Figure 7.1: Applications example of DC-DC converters [9].

In the coming years, medium and large energy storage systems are anticipated to become increasingly common, particularly in the automotive sector, as electric mobility continues to grow. Converters that serve as interfaces for batteries, for instance, must meet various requirements. These include the need for isolation between input and output, the ability to handle a wide range of input and output voltage and current, and ensuring reliability, efficiency, and smooth operation. One notable application that is gaining traction is Vehicle-to-Grid (V2G) [95], which involves the exchange of energy between electric or hybrid vehicles and the grid through the charging infrastructure. In this context, bidirectional converters operating as interfaces to batteries are poised to play a vital role in enabling this widespread application.
The Dual Active Bridge (DAB) converter has emerged as a popular choice for bidirectional DC-DC power conversion. It comprises two active full-bridges interconnected through a high-frequency transformer (as depicted in Fig. 7.2a), enabling bidirectional power transfer [96, 97].



(a) FFT of compensated and not compensated phase currents.



(b) FFT of compensated and not compensated phase currents in low torque operating condition.

Figure 7.2: Dual Active Bridge DC-DC converter [10]: **(a)** Circuit diagram; **(b)** Simplified equivalent DAB circuit for inductor current behavior analysis.

This particular topology aligns well with the requirements of the aforementioned applications, such as bidirectional power transfer, high efficiency, and the ability to handle a wide range of conversion ratios. In fact, the single-phase DAB converter topology offers several advantages

over competing alternatives [98–100]. These advantages include the potential for high converter efficiency, ease of bidirectional operation, general controllability, a modular structure, and high power density. Despite extensive research into this topology, controlling the DAB converter remains challenging due to the numerous control variables that influence its complex behavior [101–103]. Furthermore, when it comes to hardware and control design, there are multiple objectives to consider. These objectives encompass regulating power flow in both directions and across the entire operating range, achieving soft-switching techniques, primarily Zero-Voltage Switching (ZVS), and minimizing the stress on components [104, 105].

When analyzing the Dual Active Bridge (DAB) converter, as with other converters, it's essential to consider various perspectives and levels of abstraction. These include examining ideal behavior in both steady-state and dynamic scenarios, scrutinizing loss mechanisms, optimizing parameters, and developing effective control strategies [106–108]. While simulation software can simulate parasitic effects of converters, conducting sample-based simulations in the time domain (using iterative numerical solvers) can be computationally demanding, making it challenging for the rapid iteration of design and control decisions [109]. Additionally, a comprehensive analysis of the converter's dynamic properties is crucial to ensure it operates at a defined power level, in the desired power transfer direction, and achieves high efficiency across a wide operating range. Consequently, when evaluating complex topologies like the DAB converter, a detailed analysis of its response across a broad spectrum of parameters is necessary. This process can be time-consuming due to the need for multiple iterations [110, 111].

In response to this necessity, a theoretical model for the Dual Active Bridge (DAB) converter is introduced in [112], and it is substantiated through comprehensive simulations and experimentation in this study. This model, which assumes ideal (non-dissipative) components, is highly versatile and can be applied to any modulation technique. In fact, it can encompass all possible combinations of phase-shifts between the converter legs, essentially all the system's "degrees of freedom," and analyze them using the same model. Existing mathematical models for the DAB in the literature often involve approximations [113], for example, considering only the first harmonic, or they are limited to straightforward modulation modes [93, 114], focusing on just one of the many potential phase-shift variations. Nevertheless, [115] proposes a superposition-based method for highlighting Zero Voltage Switching (ZVS) regions and AC terminal currents (peak and RMS) in DAB for all operating modes and modulation strategies. Independently, a similar approach has been developed by the authors of this paper, yielding similar results.

Furthermore, the study presented here extends the analysis, particularly concerning the response to control input variables in terms of the converter's output current, taking into account the related dynamics. This approach is applied to accurately model the ideal behavior of the DAB. Steady-state waveforms for any operating condition, encompassing any input and output voltage and phase-shift combination, are efficiently obtained using a semi-analytical model.

Moreover, an original fully analytical model with a control-oriented focus is proposed in this paper. This model evaluates the average output current and yields a set of relatively straightforward equations. The novel full analytical modeling of the relationship between phase-shifts and average output current, on a cycle-by-cycle basis, becomes a valuable tool in control development and design. By applying this analysis to a conventional modulation method, such as the Single Phase-Shift, the output current is fully characterized analytically. This results in a single formula for determining the phase-shift value based on the desired output current. This simplifies cycle-by-cycle control of average current, making voltage regulation straightforward, akin to most other converters with an inner current loop.

As a case study, the Single Phase-Shift (SPS) and the proposed optimized control are employed to regulate the output current (average) in an open-loop control by linearizing the control of the DAB's output voltage. The proposed optimized control is based on Finite Control Set (FCS), where control variables are selected from a well-defined set of values, creating a list of values for each phase-shift.

The analytical advancements presented in this work, founded on the superposition principle, enable us to derive closed-form waveforms of inductor and output current through a straightforward and efficient procedure, essentially creating a "semi-analytical" model. This approach can effectively replace dynamic simulations, particularly when examining the steady-state behavior, offering a considerably quicker execution. This, in turn, facilitates the application of optimization techniques for choosing the operating point or during the design phase. For instance, it can aid in the selection of inductance and frequency values. Additionally, a novel and entirely analytical model elucidates the relationship between output current and phase-shifts. The results reveal the average output current on a cycle-by-cycle basis as a function of input voltage and phase-shift values exclusively, regardless of the output voltage. Such a model is highly suited for characterizing the dynamic behavior, particularly for control purposes. This is because it allows us to perceive the converter as a controlled (average) current source, a concept typically applied in the context of other converters.
Building on the analytical findings that establish a connection between the desired output current and the corresponding phase-shifts, a novel control strategy is introduced. This strategy employs a "fictitious" (open-loop) inner current controller. Its primary advantage lies in its ability to separate the straightforward dynamics of the output voltage concerning the average output current, which is predominantly influenced by the output capacitor, from the intricate relationship between the phase-shifts and the output current. This control approach is especially straightforward when applied in the case of Single Phase-Shift (SPS), but it's adaptable to virtually any other modulation technique. In practice, using the DAB behavioral model developed earlier, an optimization procedure is established. This procedure guides the selection of optimal operating points based on input voltage and the desired average output current. The proposed control approach employs a Finite Control Set, which includes a specific number of phase-shift combinations distributed across the entire range, from minimum to maximum phase-shift. The performance is evaluated and compared under both control methods, taking into account variable output voltage. Furthermore, the analytical results obtained are rigorously tested through simulations using PLECS models and confirmed through experimental validation. The subsequent sections of this paper first introduce the DAB and then delve into the analysis of its behavior at each switching period, presenting a cycle-by-cycle model. This study provides a method for describing the current waveforms of the converter using a "semi-analytical" model, which serves the primary purpose of replacing time-consuming simulations for swift iterations in the design phase. Moreover, a fully analytical model is proposed, elucidating the impact of control inputs, specifically phase-shifts, on average output current at each cycle. This outcome, representing a novel contribution, holds particular relevance for designing and implementing the controller. It's essential to note that this model is versatile and can accommodate any combination of phase-shifts, irrespective of the modulation technique used to control the converter.
A practical case example is presented to validate the model's effectiveness through simulations using PLECS Blockset in MATLAB/Simulink initially and subsequently through experimental verification. These experiments primarily focus on assessing the average output current at various operating points. Notably, the experiments under closed-loop SPS control with fictitious current control align well with the theoretical predictions. Further tests with optimized phase-shift triplets validate the proposed optimization method. Finally, an analysis of the converter's performance highlights some intriguing second-order effects linked to dead times, warranting further investigation.

7.1 Cycle-by-cycle model of DAB

The DAB topology comprises two full bridges, denoted as the "primary" and "secondary" (depicted in Fig. 7.2a). These bridges are interconnected through an isolation transformer, which serves to introduce an appropriate voltage ratio and typically includes the necessary

series inductance between the two bridges. Each of the four legs in the DAB topology is conventionally controlled with a 50% duty cycle. The manipulation of power flow is achieved by adjusting the phase-shifts of switch command signals. In this study, all potential modulation schemes, encompassing any phase-shift between the command signals of the legs, are taken into account to leverage variations in phase-shift for effective power flow control.

The primary-side bridge comprises legs A and B, featuring switches S_A, $\overline{S_A}$, S_B, and $\overline{S_B}$. Conversely, the secondary-side bridge incorporates switches S_E, $\overline{S_E}$, S_F, and $\overline{S_F}$. All switching commands follow a 50% duty cycle, which includes complementary high and low states. Each leg is assigned a phase value (φ_A, φ_B, φ_E, φ_F), measured concerning an arbitrary reference time instant and normalized in relation to the switching period (where a phase value of one corresponds to a delay of 1-T_{SW}). The primary-side bridge voltage (V_P) can take on values of $\pm V_i$ or 0, while the secondary-side voltage (V_S) can be $\pm V_o$ or 0. The voltage across the leakage inductance (series inductance) L is the difference between V_P and the V_S reflected at the primary side (i.e., nV_S), resulting in the flow of current. Typically, the inductor current is regulated by adjusting the phase-shift between the primary and secondary commands, with the simplest modulation technique being the single phase-shift [92, 96]. To evaluate the output current, you consider the state of legs E and F. In this context, the inductor current, reflected on the secondary side, can be either short-circuited (when $S_E = S_F$), directly directed to the output (when only S_E is active), or inverted (when only S_F is active).

The proposed theoretical approach for DAB analysis is centered on modeling the inductor current by applying the superposition principle to consider the contribution of each bridge leg. A somewhat similar approach was utilized for a limited number of cases in a previous study. To streamline the analysis, several initial assumptions are made: negligible losses, the four leg commands share the same frequency, and the voltage at both sides of the converter (i.e., "input" and "output") is known and varies gradually. This means that there are no abrupt voltage fluctuations within a switching period. These assumptions are reasonably valid in terms of the inductor current waveform, and losses can be considered as a post-processing step. Through analytical calculations, a systematic closed-form method, hereafter referred to as the semi-analytical method, has been developed to calculate the inductor current waveform by summing the contributions from each transformer leg.

Since the phase-shift is a relative measure, the command S_A is set for leg A with a phase-shift of 0. Therefore, the independent variables (i.e., the "degrees of freedom" available for control inputs) are the phase-shifts of the remaining three switching commands, namely φ_B, φ_E, and φ_F. These phase-shift values are variable and represent the time difference between two rising edges, normalized to the switching period, ranging from -0.5 to $+0.5$.

Assuming no losses (which is typically accepted at this level of abstraction), the inductor current exhibits a piecewise linear waveform. As a result, its shape is entirely defined by the values at the switching points, which are connected by straight-line segments. The approach considers a simplified double-bridge circuit (comprising primary and secondary inductors) with bidirectional behavior, as depicted in Figure 2b. Each bridge consists of two legs with corresponding phase-shifts. An ideal transformer is assumed, negating the presence of magnetizing inductance, which is typical for DAB converters. The analysis takes into account the leakage inductance, which is considered in the series inductor.

The magnitude and direction of power flow or charge transfer during each switching cycle are determined by the phase-shifts between each leg and the reference one, which is leg A. In contrast to previous work, this analysis doesn't impose any restrictions between the four legs, allowing for the consideration of all possible modulation techniques. Each bridge can connect the inductor to a DC voltage source (either input or output). This means that the square wave voltage sources of the primary and secondary bridges in Fig. 7.3a have the same amplitude as the input voltage V_i (for V_A and V_B) or the output voltage V_o (V_E and V_F).

Following the superposition principle, each leg operates on the inductor independently, sim-

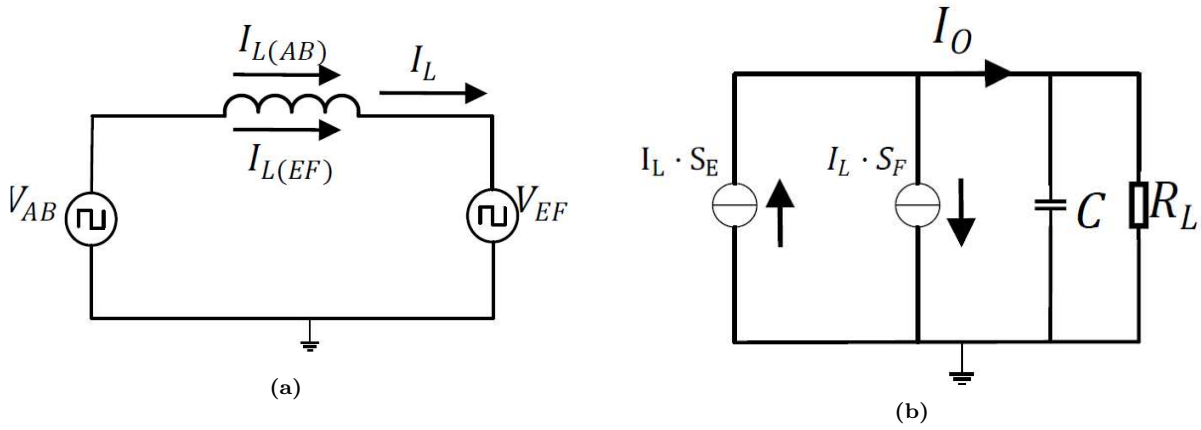


Figure 7.3: Inductor current decomposition: (**a**) equivalent circuit using to the superposition principle; (**b**) equivalent circuit for the analysis of average output current.

plifying the analysis of the inductor current waveform. The total current passing through the inductor is essentially the sum of contributions originating from each individual leg:

$$i_L = i_{LA} - i_{LB} - i_{LE} + i_{LF} \tag{7.1}$$

Within each switching period, the switching times for each leg, accounting for the phase-shifts, are established. At these times, both switching on and switching off, the current is computed for each leg, as illustrated in Fig. 7.4.

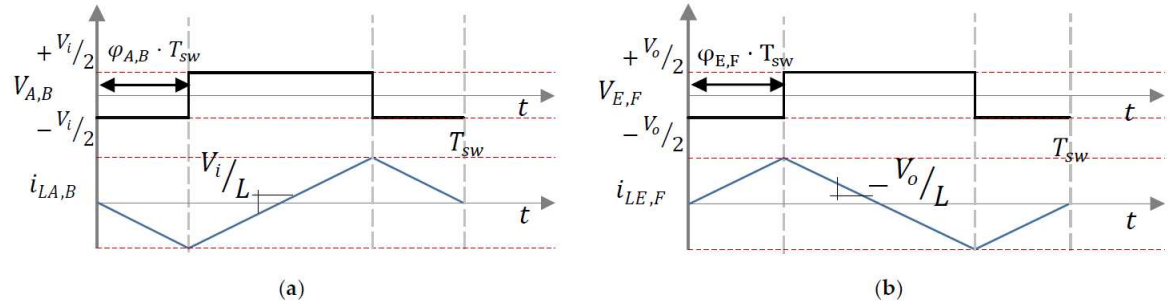


Figure 7.4: Gate signal and inductor current of each leg: (**a**) primary-side legs; (**b**) secondary-side legs.

Notably, the waveform of each component of the inductor current (i.e., i_{LA}, i_{LB}, i_{LE}, i_{LF}) is straightforward. Specifically, the current remains constant when the voltage is zero, which applies both before and after the same voltage pulse. During the voltage pulse, the current exhibits a linear variation. Consequently, to determine the inductor current, it is imperative to differentiate between the instants during the voltage pulse and those outside of it. The calculation of the current slope can be performed as in Eq. (7.2)

$$\begin{aligned} \left.\frac{di_{L\_A,B}}{dt}\right|_{V_{A,F}=0} &= \frac{V_i}{L} \\ \left.\frac{di_{L\_E,F}}{dt}\right|_{V_{B,E}=0} &= \frac{nV_o}{L} \end{aligned} \tag{7.2}$$

The output current, denoted as $i_{o,avg}$, which is delivered to the load, is determined by considering the total inductor current and the switching states of legs E and F, as depicted in Fig. 7.3b. This output current, responsible for powering the load and charging the parallel output capacitor C, is calculated as in Eq. (7.3)

$$i_o = n\, i_L\, (S_E - S_F) \tag{7.3}$$

In this context, "output current" refers to the current supplied from the secondary-side bridge to the output capacitor and the connected load. The model also takes into account the potential presence of unwanted DC current, which might occur during transient conditions or due to non-ideal behavior. By using Eq. (7.1), the total inductor current is rewritten as in (7.4).

$$i_L = i_{DC} + i_{LA} - i_{LB} - i_{LE} + i_{LF} \tag{7.4}$$

The average output current $\overline{i_o}$ is computed as in Eq. (7.5)

$$\overline{i_o} = \frac{n}{T_{sw}} \int_0^{T_{sw}} \left(i_{DC} + i_{LA} - i_{LB} - i_{LE} + i_{LF}\right) \left(S_E - S_F\right) dt \tag{7.5}$$

Based on Eq. (7.5), it's important to note that the impact of DC inductor current on the average output current is nullified. This is because, by definition, i_{DC} is a constant. Additionally, both S_E and S_F are square waves with a 50% duty cycle, and their integrals are identical. Consequently:

$$\frac{n}{T_{sw}} \int_0^{T_{sw}} i_{DC} \left(S_E - S_F\right) dt = \frac{n}{T_{sw}} i_{DC} \left(\int_0^{T_{sw}} S_E dt - \int_0^{T_{sw}} S_F dt \right) = 0 \tag{7.6}$$

Furthermore, Eq. (7.6) underscores that any adjustment in the phase-shifts leads to a corresponding change in the average output current within the same switching period, devoid of any further dynamics. This observation highlights the significance of the obtained results, particularly in the context of implementing converter control. Notably, since the bias inductor current has no impact on the average output current, it can be inferred that the average output current remains unaffected by the initial value of the inductor current, which serves as the sole state variable in the circuit. Therefore, during each switching cycle, the output current is solely determined by the phase-shift values and input voltage, with no influence from prior inputs. Consequently, the average output current can be precisely controlled in a strictly cycle-by-cycle manner, defining the dynamics of current "actuation". It's also crucial to emphasize that the average output current remains independent of the output voltage (assuming negligible variations within a switching cycle), simplifying current control. This allows the converter to be viewed as a controlled current source, supplying the output capacitor and the load, much like other converters.

7.1.1 Semi-analytical model

Here the superposition-based "semi-analytical" model is introduced, which offers a systematic method for obtaining the waveforms of the inductor and output current, average output or input current, as well as their peak values. Due to the straightforward piecewise linear nature of the currents, it's also possible to calculate their RMS values.
However, it's important to note that this model is not condensed into a single set of equations that can directly describe the waveforms as analytical functions of time. Instead, it's presented as a closed-form algorithm, which is why it's termed "semi-analytical". Consequently, the currents in the converter are not directly expressed as analytical functions of time but are calculated at specific breakpoints, corresponding to the switching instants of each leg. This approach yields a comprehensive representation of the waveform. The primary focus of analysis within a switching period is, understandably, the main state variable of the converter, which is the current flowing through the inductor. The use of the semi-analytical model for evaluating converter waveforms involves several key steps:

1. Generate a set of switching instants within the switching period, such as $\varphi_x T_{sw}$ and $(\varphi_x + 0.5)T_{sw}$, arranged in the correct order.

2. Calculate the value of the inductor current caused by each leg at these switching instants, determined by the slope in Equation (2).
3. Compute the total inductor current using Equation (1).
4. Calculate the average of the output current by determining the area under the inductor current waveform and multiplying it by $S_E - S_F$.

The process is indeed analytical and provides a closed-form solution, but performing it manually would be quite laborious. As a result, the model has been translated into an algorithm for practical implementation. The parameters of the DAB prototype, and these parameters are detailed in Tab. 7.1.

Table 7.1: DAB converter parameters

Parameter	Symbol	Value
Switching frequency	f_{sw}	100 kHz
Switching period	T_{sw}	10 μs
Input Voltage	V_i	100 V
Output Voltage	V_o	Variable
Transformer turns ratio	$n = \frac{N_{pri}}{N_{sec}}$	1.6
Duty-cycle	d	50%
Inductance	L	36 μH
Output capacitor	C_{out}	300 μF
Dead-time	T_{dt}	250 ns
Primary SiC output capacitance	C_{oss_pri}	1.1 nF
Secondary SiC output capacitance	C_{oss_sec}	0.6 nF
Primary turn-on resistance	R_{dsON_pri}	16 $m\Omega$
Secondary turn-on resistance	R_{dsON_sec}	30 $m\Omega$
Load resistor	R_{out}	22.8 Ω

7.1.2 Analytical Modeling of Average Output Current vs. Phase-Shifts

In this section, an innovative fully analytical model and a control-oriented approach have been introduced. The model assesses the average output current and yields a series of equations. This newly presented comprehensive analytical model, which elucidates the connection between phase-shifts and average output current, is anticipated to serve as a valuable resource in the development and design of control strategies. Expanding the expression Eq. (7.3) based on Eq. (7.1) leads to:

$$i_o = (i_{oEA} - i_{oEB} - i_{oEE} + i_{oEF}) - (i_{oFA} - i_{oFB} - i_{oFE} - i_{oFF}) \tag{7.7}$$

where $i_{o_{xy}}$ (with $y = E, F$ and $x = A, B, E, F$) represents the interaction between inductor current components Eq. (7.1) and E, F leg states Eq. (7.3):

$$i_{o_{xy}} = n\, i_{L_x}\, S_y \tag{7.8}$$

A model for the average output current (represented by the symbol with a bar, $\overline{i_o}$) is introduced hereinafter. Naturally, the average output current is the summation of the averages of its individual components:

$$\begin{aligned} \overline{i_o} &= \frac{1}{T_{sw}} \int_{t-T_{sw}}^{t} i_o dt = (\bar{i}_{oEA} - \bar{i}_{oEB} - \bar{i}_{oEE} + \bar{i}_{oEF}) - (\bar{i}_{oFA} - \bar{i}_{oFB} - \bar{i}_{oFE} - \bar{i}_{oFF}) \\ &= \bar{i}_{oEA} - \bar{i}_{oEB} - \bar{i}_{oFA} + \bar{i}_{oFB} \end{aligned} \tag{7.9}$$

Some simplifications can be applied, since the terms $\bar{i}_{oEE}$, $\bar{i}_{oFF}$ and $\bar{i}_{oEF}$, $\bar{i}_{oFE}$, cancel each other. Two cases are considered (Fig. 7.5) based on the value of $\phi_{xy} = \varphi_x - \varphi_y$.

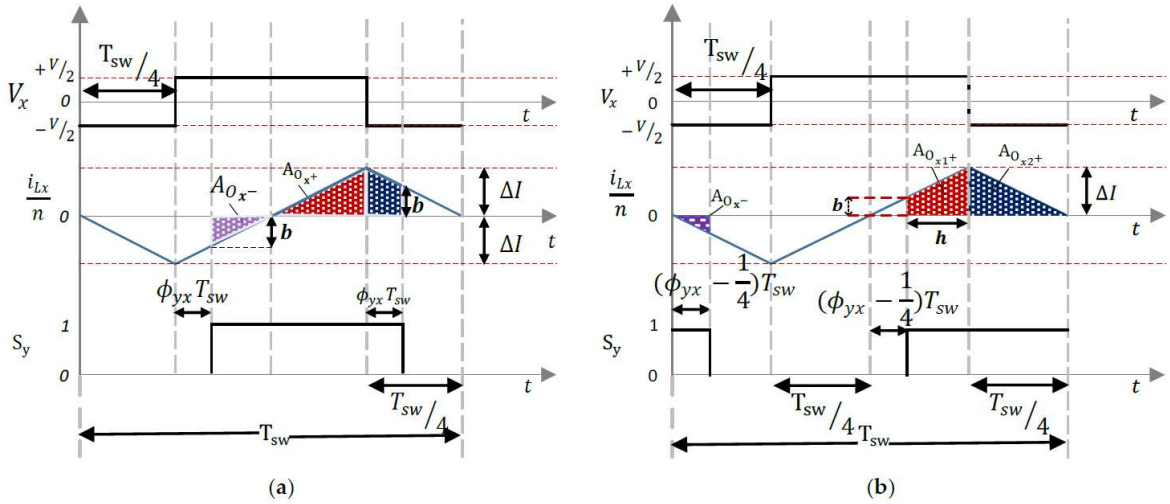


Figure 7.5: Contribution of one primary and secondary leg to the average output current: (**a**) Case 1; (**b**) Case 2.

For each term, the peak inductor current variation (reflected to secondary) is

$$\Delta I = \frac{1}{2} n \frac{V_i}{L} \frac{T_{sw}}{4} \tag{7.10}$$

With small phase-shift ($0 \leq \phi_{xy} < 1/4$), "positive" (triangle and trapezoid, A_{0_x+}) and "negative" (triangle, A_{0_x-}) areas are:

$$\begin{aligned} A_{0_x+} &= \Delta I T_{sw} \left(\frac{1}{8} + \phi_{xy} - 2{\phi_{xy}}^2 \right) \\ A_{0_x-} &= \Delta I T_{sw} \left(\frac{1}{8} + \phi_{xy} + 2{\phi_{xy}}^2 \right) \end{aligned} \tag{7.11}$$

The average output current can be computed as

$$\bar{i}_{o_{xy}} = \frac{A_{0_x+} - A_{0_x-}}{T_{sw}} = 2\Delta I \left(\phi_{xy} - 2{\phi_{xy}}^2 \right) \tag{7.12}$$

When $1/4 \leq \phi_{xy} < 1/2$, areas can still be computed as in Eq. (7.11) and consequently the output current is Eq. (7.12). Including also the generalized phase-shift cases (i.e. $\phi_{xy} \in \{0, 1\}$) we find the generalized output current formula as in

$$\bar{i}_{o_{xy}} = 2\Delta I \left(\phi_{xy} - sign(\phi_{xy}) 2{\phi_{xy}}^2 \right) \tag{7.13}$$

Similarly it would be possible to compute the input current thanks to the symmetry of the two stages.

7.2 Control Methods Based on the Cycle-by-Cycle Model

7.2.1 Operating Point Choice and Optimization

Traditionally, modulation in DAB converters has been carried out using straightforward techniques, such as Single Phase-Shift (SPS) [96]. However, the DAB topology offers three independent variables, or three "degrees of freedom," in the form of phase-shifts that can be harnessed

as control variables. Thanks to the analytical model introduced earlier, it becomes feasible to ascertain the influence of each phase-shift variable on the average output current.
Moreover, the "semi-analytical" model, which significantly accelerates the evaluation process compared to numerical simulations, enables automated optimization for enhancing design decisions. This optimization may focus on crucial aspects like selecting the appropriate inductance, transformer ratio, switching frequency, and the operating point of the converter. Notably, having the capacity to explore various phase-shift combinations among the four legs offers designers considerable flexibility in determining the optimal modulation pattern.
A sensible objective for this optimization process is to minimize conduction losses and mitigate current stress in key components such as switches, inductors, and transformers, while also addressing switching losses, primarily associated with achieving Zero Voltage Switching (ZVS) [113, 116, 117].
Typically, DAB control is primarily directed towards regulating the output voltage. Understanding the converter's response concerning the output current is of significant importance in this context, as it essentially dictates the rate of change in voltage across the output capacitor (C in Fig. 7.2 and Fig. 7.3). When the average output current can be effectively controlled in a rapid and precise manner, it opens the door to implementing a conventional control structure with an inner current control loop and an outer voltage control loop. This approach comes with evident advantages related to tuning, stability, and the capability to limit current.
For controlling the DAB at this level of abstraction, several assumptions are made:

1. Losses can be disregarded, and they are computed subsequently using the derived waveforms.
2. All four leg commands have the same frequency.
3. Phase-shifts remain constant during each switching period.
4. The "input voltage" (V_i) is known and varies slowly, meaning there are negligible variations within a single switching period.
5. The variation of the "output voltage" (V_o) within a single switching period is insignificant. This assumption is usually valid in steady-state conditions.

It's worth reiterating (as observed in the previous section) that any alteration in phase-shift results in a corresponding change in the average output current within the same switching cycle. Essentially, there is minimal dynamic behavior in current control apart from the length of the switching period. Even in situations where there might be an offset in the inductor current, such as during transients when phase-shifts are modified, the DC current does not influence the average output current, as demonstrated in the previous analysis. Additionally, the average output current remains independent of the output voltage (V_o), which is particularly significant for dynamic response and control, as changes in output voltage are, once again, contingent upon the average output current.
Since the roles of input and output can be readily reversed (by considering $1/n$ as the transformer ratio instead of n), either end can be designated as V_i for simplicity when one of the two remains constant.
In the subsequent sections, the analytical results derived from the cycle-by-cycle superposition-based analysis will be employed to propose two distinct control strategies for voltage regulation in the DAB. One utilizes Single Phase-Shift (SPS) modulation, while the other employs a novel optimized modulation pattern.

7.2.2 Single Phase-Shift Control

As an application of the method presented, which is applied to the classical modulation technique known as Single Phase-Shift (SPS), the output current is comprehensively characterized

in an analytical manner. This results in a single formula that enables the calculation of the phase-shift value based on the desired output current. It is important to note that the proposed analytical approach can, in principle, be readily extended to the case of a 3-phase DAB converter.
In the subsequent section, we specifically focus on the SPS case, in which ϕ_E represents the sole control variable. The phase-shift constraints are shown in Eq. (7.14).

$$\begin{aligned} \varphi_A &= 0 \\ \varphi_B &= 0.5 \\ \varphi_F &= \phi_E + 0.5 \end{aligned} \tag{7.14}$$

Utilizing Eq. (7.12) and taking into account both cases for the sign of phase-shifts (ϕ_{xy}), the average output current can be expressed as follows:

$$\overline{i_o} = 8\Delta I \left(\varphi_E - sign(\varphi_E) 2{\varphi_E}^2\right) \tag{7.15}$$

Inverting Eq. (8.15) allows to find the phase-shift as a function of the output current.

$$\varphi_E = sign(\bar{i}_o) \frac{1 - \sqrt{1 - \frac{\bar{i}_o}{\Delta I}}}{4} \tag{7.16}$$

By employing this expression in the voltage controller, it becomes feasible to conduct open-loop control of the average current, enabling the implementation of a linearized voltage control. This approach offers the benefits typically associated with nested current control loops, as illustrated in Fig. 7.6. Since the average output current remains unaffected by the output voltage, the inner "current control" is entirely independent of the outer voltage loop. This decoupling simplifies the design of the voltage regulator, ensuring precise current limitation and overall stability.

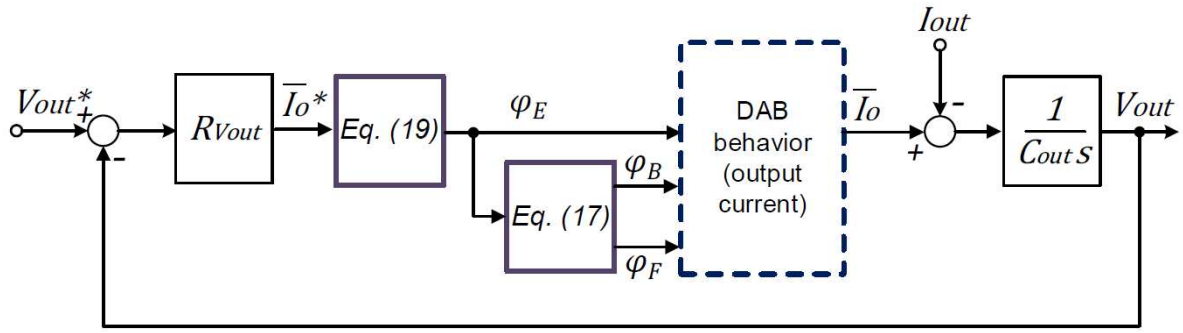


Figure 7.6: Control schematic for the SPS modulation.

7.2.3 Arbitrary Optimized Modulation

The suggested control approach, which integrates an inner open-loop current control within a closed-loop voltage control, can be extended to accommodate any other modulation method. The diagram in Fig. 7.7 illustrates a potential configuration that employs Look Up Tables (LUTs) to derive the three phase-shift values based on the desired output current. Instead of LUTs, alternative functions, whether analytical or empirical, could be employed, and these functions could potentially consider multiple input variables (such as selection based on input or output voltage values).
As mentioned earlier, the semi-analytical approach provides the ability to anticipate the converter's behavior under various operating conditions with reasonable computational effort. This

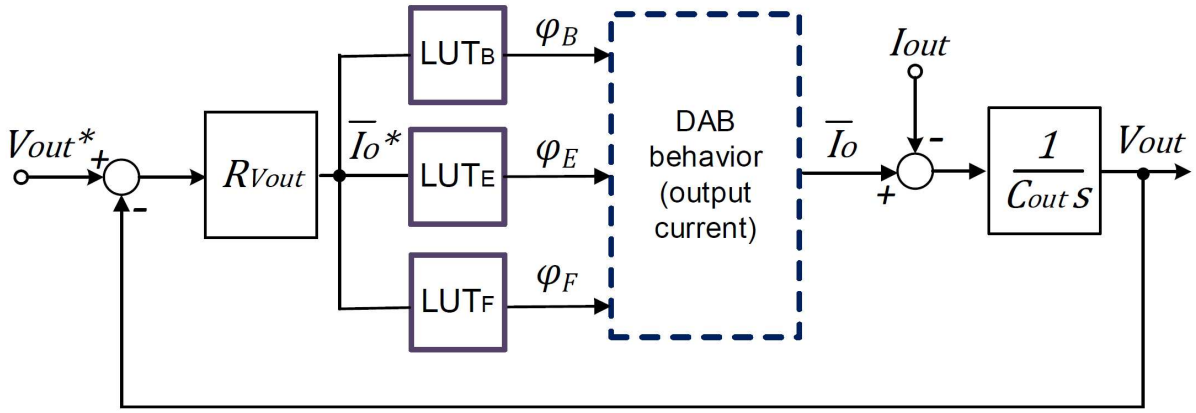


Figure 7.7: Control schematic for an arbitrary modulation (e.g., optimized).

capability can be leveraged to optimize the operating point by combining the desired control outcome (desired output current) with other objectives through a suitable cost function.

In the following, a cost function J is defined (Eq. (7.17)) that takes into account control accuracy in terms of current $(I_o{}^* - \overline{i_o})$, current stress on the switches, conduction losses, and occurrence of soft-switching. The function is the sum of the squared average output current error $((I_o{}^* - \overline{i_o})^2)$, absolute maximum inductor current $(\max\{|i_L|\})$, and zero voltage switching error (ZVS_{error}). The variable "ZVS_{error}" evaluates the soft-switching capability at the specific operating point, being 1 for ZVS achieved in all legs and 0 otherwise. Additionally, it represents the amount of current missing before reaching the ZVS threshold. The constants W_{i_o}, W_{i_L}, and W_{nZVS} are the weighting coefficients for the three components of the cost function, respectively.

$$J\left(\varphi_B,\, \varphi_E,\, \varphi_F,\, V_o, I_o{}^*\right) = W_{i_o}(I_o{}^* - \overline{i_o})^2 + W_{i_L} \max\{|i_L|\} + W_{nZVS}(ZVS_{error}) \tag{7.17}$$

It's important to note that the cost function presented is just one example, and it encompasses the most critical aspects of DAB operation. Different cost function expressions can be proposed, considering various variables, especially if a known relationship exists between each variable in the cost function and the independent variables, such as phase-shifts, output voltage, and desired output current.

To determine the optimal modulation choice, this approach utilizes finite-set optimization, following the Finite Control Set (FCS) approach. The entire range of phase-shift values, spanning from -0.5 to $+0.5$, is systematically evaluated, with small increments of 0.005. For each phase-shift triplet $(\varphi_B,\, \varphi_E,\, \varphi_F)$, all critical converter parameters are calculated using the semi-analytical model. Out of the extensive set of combinations, only those that result in Zero Voltage Switching (ZVS) for all legs are selected.

The optimization process considers a wide range of reference current values within the feasible range, typically within $\pm n/2\, V_i/L\, T_{sw}/4$ of the switching frequency and voltage, with intervals of 0.05 A. The minimum-cost operating point for each reference current value is determined, resulting in three arrays (one for each phase-shift variable, φ_B, φ_E, φ_F), where each value represents the minimum-cost operating point for a specific desired output current $(I_o{}^*)$ value.

The combination of these reference current values and phase-shift values creates a Look-Up Table (LUT), which is employed in the control scheme. This method can be extended to account for different output voltage values, which is particularly important in cases where the output voltage spans a wide range.

7.2.4 Comparison between SPS and Optimized Control with Variable Output Voltage

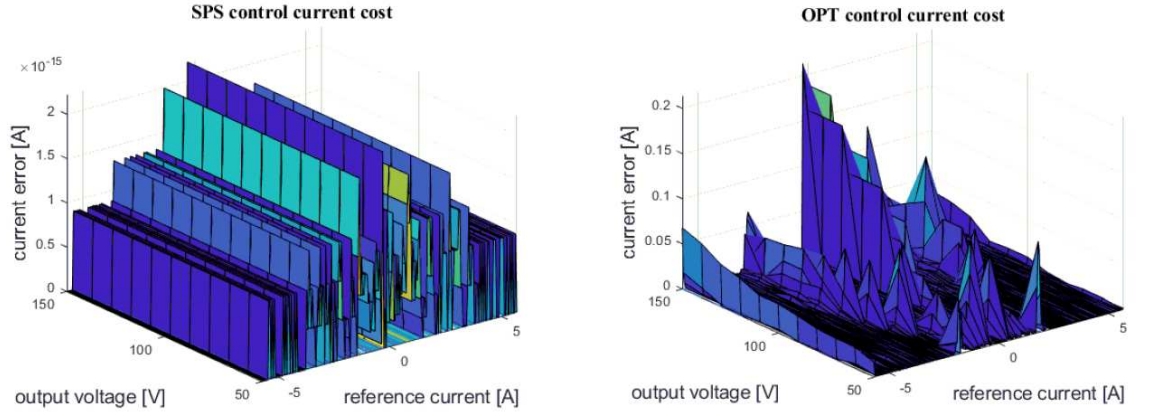
The evaluation of DAB behavior with variable output voltage (V_o) is performed based on the parameters of in Tab. 7.1. To compare Single Phase-Shift (SPS) modulation with optimized modulation, two different procedures are required due to the distinct characteristics of these methods. However, the ultimate objective is to calculate the cost function across the entire range of output current and voltage.
For the case of SPS modulation, the following steps are considered:

- Generate a set of V_o values ranging from 50 V to 150 V with 10 V increments.
- Generate a set of reference average output current values within the range of $\pm\Delta I$ with 0.05 A increments for each V_o.
- Set up phase-shift values for the SPS case using Equation (17).
- Calculate the value of φ_E for each reference average output current (desired current) using Eq. (7.14).
- Calculate all the essential converter parameters for each phase-shift triplet (φ_B, φ_E and φ_F) using the semi-analytical model.
- Calculate the total cost along with its components and store them in the relevant matrices for each reference average output current.
- Evaluate all cost components and save them in their respective matrices for each reference average output current.
- Repeat the procedure for each V_o value and store the results in three Look-Up Tables (LUTs), one for each phase-shift φ_B, φ_E and φ_F), representing the optimal phase-shift choices as functions of output voltage and desired output current.

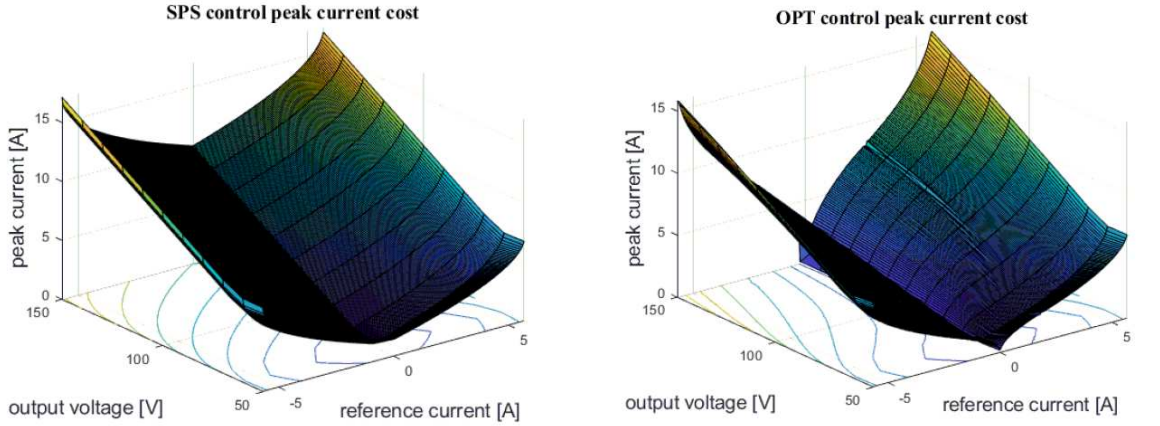
For the case of optimized modulation, the evaluation procedure includes the following steps:

- Generate a set of V_o values ranging from 50 V to 150 V with 10 V increments.
- Evaluate the finite control set, covering the entire range of phase-shift values (from -0.5 to $+0.5$) with small increments of 0.005 for each V_o.
- Calculate all the essential converter parameters for each phase-shift triplet (φ_B, φ_E and φ_F) using the semi-analytical model and save them in the relevant matrices.
- Select only those phase-shift combinations that achieve Zero Voltage Switching (ZVS) in all legs and save the ZVS indexes in the relevant matrices.
- Generate a set of reference average output current values within the range of $\pm\Delta I$, with 0.05 A increments for each V_o.
- Calculate the total cost along with its components using the saved matrices.
- Select the minimum-cost points within the subset of points that achieve ZVS from the total cost matrix for each reference average output current.
- Evaluate all other cost components at the minimum-cost point index and save them in the relevant matrices for each reference average output current.
- Repeat the procedure for each V_o value, and store the results as $3D$ matrices.

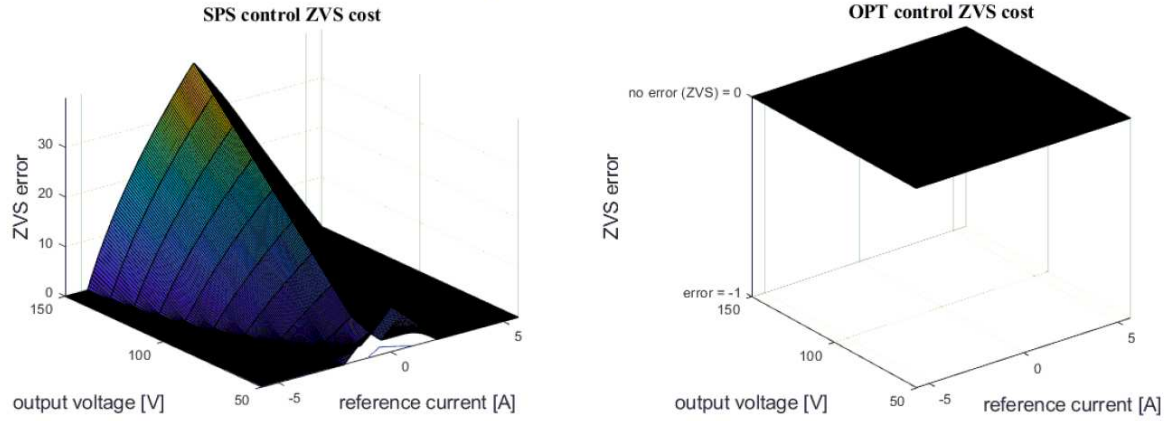
In Fig. 7.9b, the peak current cost is illustrated for both Single Phase-Shift (SPS) and optimized control schemes. The diagrams show that under optimized control, the peak current cost is notably lower, especially at intermediate current levels. This reduction results in decreased conduction losses for the converter and a lower level of stress on its components. In some cases, the reduced peak current may even allow for downsizing of the active switch components.
Fig. 7.9c examines the Zero Voltage Switching (ZVS) cost for both SPS and optimized control. The ZVS cost is zero for the optimized control method since ZVS is consistently achieved. This demonstrates an advantage of optimized control over SPS, as ZVS is maintained across the entire operational range. The resulting Look-Up Tables (LUTs) are constructed by eliminating points where ZVS is unattainable. While this may lead to some cyclic inaccuracies in current control, the control approach can still ensure accurate performance over more extended periods, aligning with the Finite Control Set (FCS) control principle.
Fig. 7.9d, the ZVS range is presented for both SPS and optimized control. This range is expressed as a logical 1 when ZVS is achieved in all legs and 0 otherwise. Optimized control provides a wider ZVS range, which contributes to lower switching losses.
With the optimized control scheme, ZVS is consistently attained, and the peak inductor current is minimized. It's important to note that the soft-switching range is influenced by the value of leakage inductance and the switching frequency. Higher inductance values extend the soft-switching range, even down to very low power levels, such as light loads.
Fig. 7.9e shows the total cost for SPS and optimized control. The total cost under optimized control is lower than that of SPS control, indicating reduced overall losses for the converter.
The essence of optimized control is to move away from rigid modulation schemes that are often based on specific assumptions. Instead, it explores a broader range of potential combinations (all "degrees of freedom") to achieve ZVS and minimize peak current over the widest feasible range. As evident from the 3D surfaces, this approach allows for comprehensive optimization of the converter's operation across the entire operational range based on specific cost functions, in this case, focused on peak current and soft-switching occurrence. A similar analysis can be conducted with other state-of-the-art modulation techniques (e.g., comparing Optimized control with EPS, DPS, and TPS) to assess ZVS ranges and DAB performance.
Furthermore, optimization could be applied during the converter's design phase rather than for specific hardware. It can help enhance or select design decisions, including inductance, transformer ratio, switching frequency, control method, and overall converter performance. The ability to assess various phase-shift combinations enables the search for the most suitable modulation pattern.



(**a**) current control cost

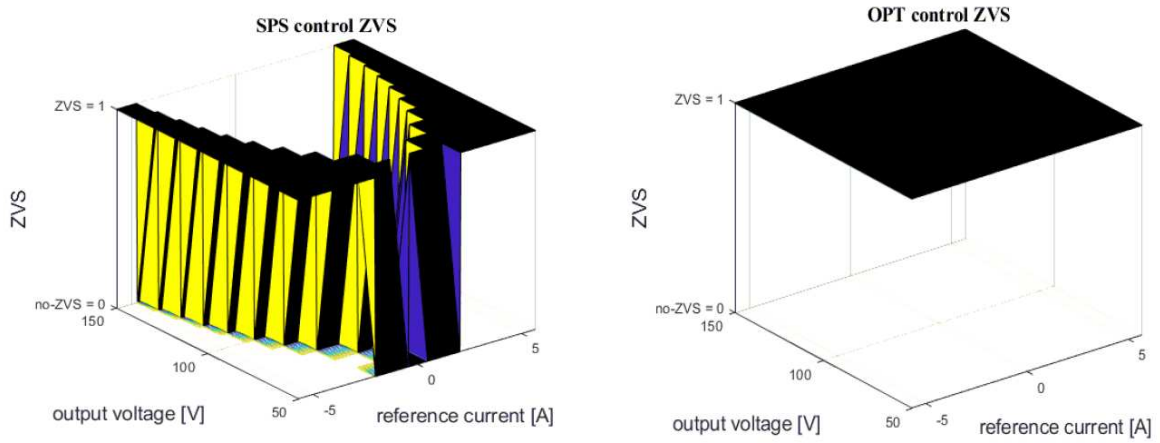


(**b**) peak current cost

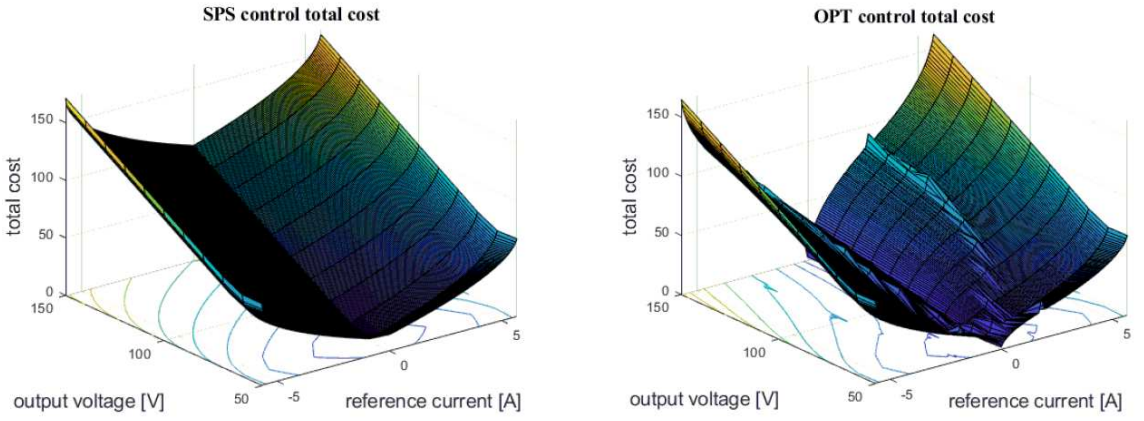


(**c**) ZVS cost

Figure 7.8: Current error, peak current and ZVS error displayed as a function of reference current and output voltage



(d) ZVS



(**e**) Total cost

Figure 7.9: Cost function and its components, 3D surface plots for SPS control and optimized control, with variable voltage.

7.3 Simulation results

The DAB converter was simulated using the Plexim PLECS blockset within the MATLAB/Simulink environment to validate the theoretical and analytical findings. The circuit parameters are detailed in Tab. 7.1. In an initial phase of the simulations, the ideal circuit, which does not incorporate any lossy components, was tested at various phase-shift and output voltage values. These simulations provided confirmation that the results align precisely with the predictions generated by the analytical and semi-analytical models, as outlined in Tab. 7.2.

Table 7.2: Simulation of the ideal converter vs. analytical models: comparison of average output current with different combinations of phase-shift values.

Phase-Shift Values				**Average Output Current**		
Case	$\varphi_{\mathbf{B}}$	$\varphi_{\mathbf{E}}$	$\varphi_{\mathbf{F}}$	**Semi-Analytical Model**	**Analytical Model**	**PLECS Simulation**
1	0.50	0.25	0.75	5.55	5.55	5.55
2	0.50	0.10	0.60	3.55	3.55	3.55
3	0.50	0.35	0.85	4.66	4.66	.66
4	0.20	0.10	0.30	1.33	1.33	1.33
5	0.40	0.25	0.65	5.11	5.11	5.11
6	0.45	0.15	0.75	5.22	5.22	5.22
7	0.50	0.06	0.56	2.48	2.48	2.48

A second model was developed to account for parasitic capacitance and resistive effects, simulating the losses typically present in the real circuit [118]. In the next section, we will examine and discuss the comparison between the average output current results obtained from the analytical model, the PLECS simulation model (which includes losses), and the experimental model under various combinations of phase-shift values, as summarized in Tab. 7.3. To validate the analytical results, simulation outcomes for case 3 and case 5 are presented in Fig. 7.10.
Fig. 7.11 illustrates the response to a change in phase-shifts, which occurs at 40 ms. Specifically, the phase of leg E, φ_E, is varied from an initial value of 0.25 to a final value of 0.30, while φ_B is held at 0.40, and φ_F is set to -0.30. This variation in φ_E leads to an immediate change in the average output current, shifting from 5.15 A to 4.75 A within a single switching period. This confirms that there is no inherent dynamic behavior (apart from the averaging process) in the relationship between phase-shift values and average output current. In essence, the converter can be accurately modeled and controlled on a cycle-by-cycle basis.
Fig. 7.12 displays the primary waveforms over three periods for the case with phase-shift triplet case 1. The waveforms are obtained using the semi-analytical method, PLECS blockset simulation, and the experimental model, showcasing the matching of inductor currents.

Table 7.3: Comparison of average output current with different combinations of phase-shift values.

Phase-Shift Values				**Average Output Current ($\overline{I_o}$)**				**Efficiency (η)**	
Case	$\varphi_{\mathbf{B}}$	$\varphi_{\mathbf{E}}$	$\varphi_{\mathbf{F}}$	**Analytical Model**	**Simulation**	**Experimental**	**Experimental Normalized**	**Simulation**	**Experimental**
1	0.50	0.25	0.75	5.55	5.00	5.00	5.39	89%	93%
2	0.50	0.10	0.60	3.55	3.38	3.15	3.22	97%	98%
3	0.50	0.35	0.85	4.66	4.00	4.00	4.91	80%	81%
4	0.20	0.10	0.30	1.33	1.56	1.40	1.47	92%	95%
5	0.40	0.25	0.65	5.11	4.70	4.60	5.05	90%	91%
6	0.45	0.15	0.75	5.22	4.85	4.80	5.12	92%	94%
7	0.50	0.06	0.56	2.48	2.42	2.36	2.38	97%	98%

It is evident from these waveforms that there is excellent agreement between the three models. While many other cases were successfully tested, they are not presented here due to space

constraints. In addition, the control capability in the case of SPS modulation was assessed. Fig. 7.13a illustrates the top plot with the desired voltage, actual voltage, and low-pass output voltage; the middle plot with φ_B, φ_E and φ_F; and the bottom plot with the desired output current (the output of the voltage regulator) and the actual output current. The proposed control strategy, based on open-loop control of the average output current (as determined analytically), effectively delivers the desired average output current, leading to the linearization of voltage control dynamics. This simplifies the tuning of the voltage regulator. The converter begins with an output voltage of zero and an initial reference value of 100 V, which is gradually reduced by 15 V every 15 ms. The nested open-loop current control is clearly demonstrated by the close match between the reference and actual current.

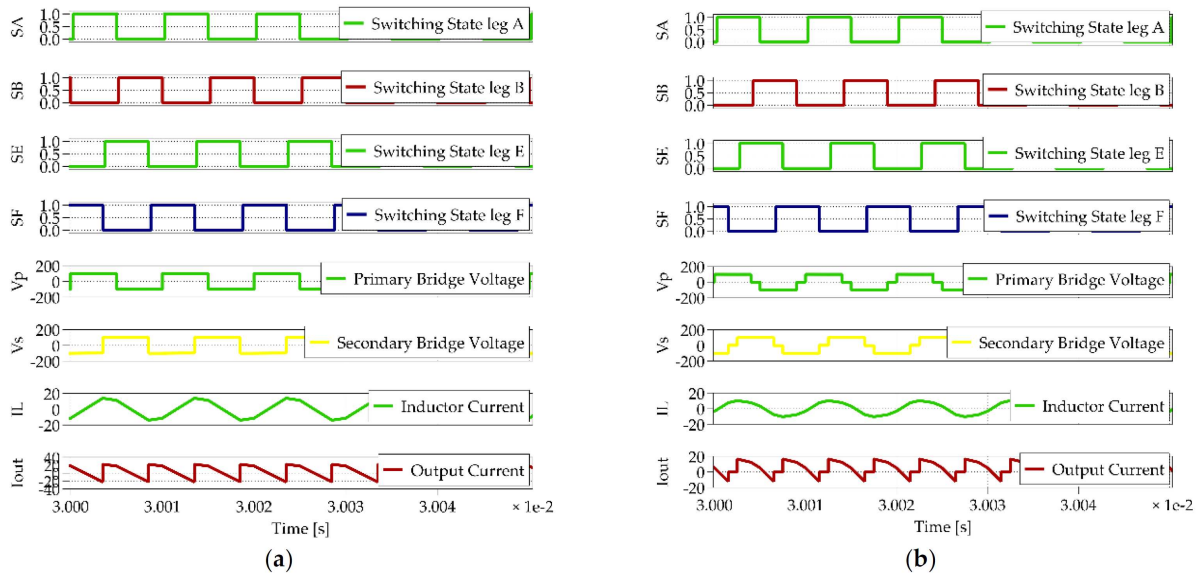


Figure 7.10: Gate control signals, primary and secondary voltage, inductor current and output current (PLECS simulation): (**a**) Case 3; (**b**) Case 5.

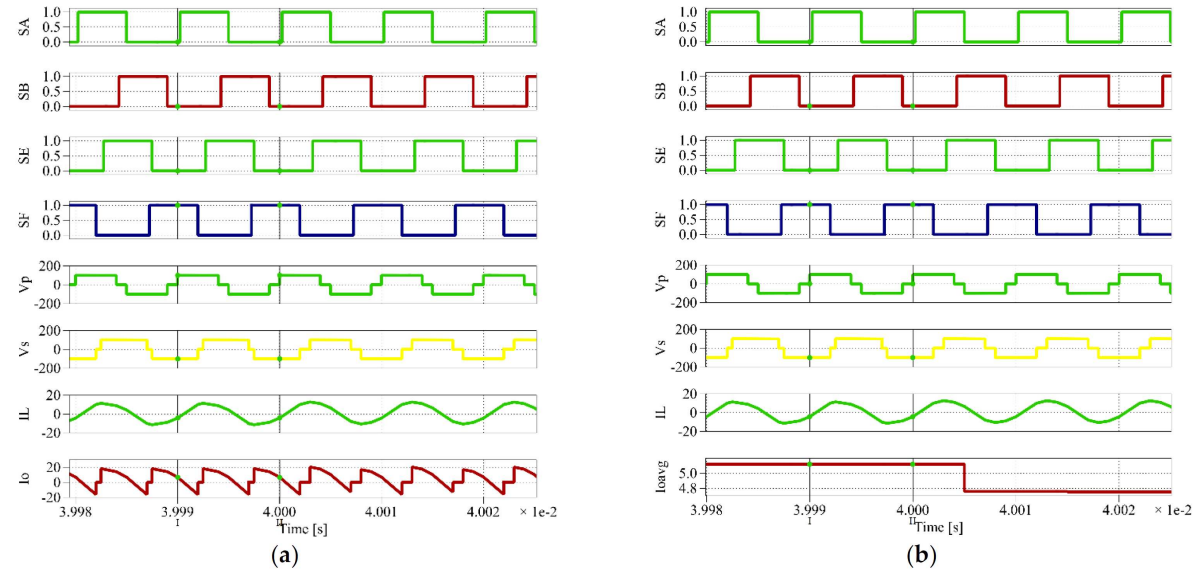


Figure 7.11: Gate control signals, primary and secondary voltage, inductor current and output current (step change, PLECS simulation): (**a**) Output current; (**b**) Average Output current.

The simulation results also validate that any alteration in phase-shift directly impacts the

average output current, leading to a cycle-by-cycle variation without any delay. Although in a real-world converter, the accuracy of current control is somewhat diminished due to non-ideal characteristics, the precision of voltage control remains nearly unaffected, thanks to the feedback control system.

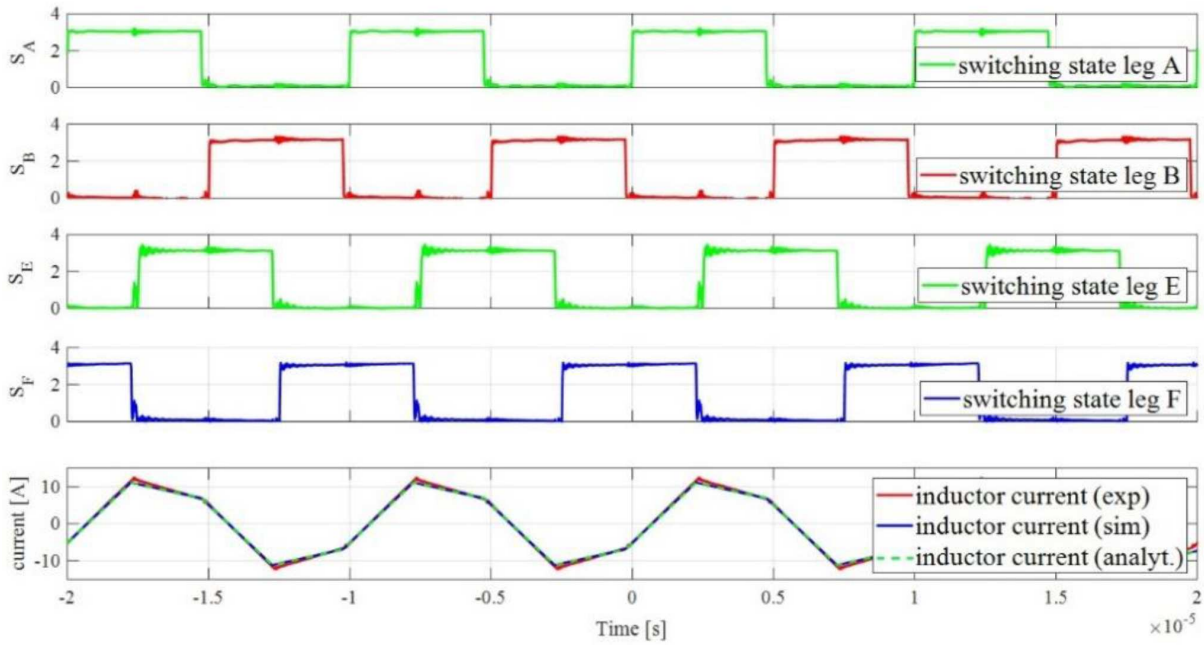


Figure 7.12: Gate control signals and inductor current matching waveforms for semi-analytical, PLECS simulation and experimental model (case 1).

A similar test under identical conditions and reference voltage is conducted with each modulation method resulting from multi-objective optimization. The test results are presented in Fig. 7.13b.
As evident, the control approach's behavior in terms of control accuracy and dynamic range remains similar, demonstrating that it can be adapted to various modulation schemes, provided the correct phase-shift values are associated with the desired average output current. Furthermore, the controller's design minimizes the peak inductor current while preserving the ZVS condition. As mentioned previously, the accuracy of current control is not a critical factor, meaning that it can be traded for other attributes such as efficiency or reduced current load on the switches. At steady state, it can be observed that the output current ripple is reduced compared to SPS control, which is linked to the minimization of the peak inductor current.

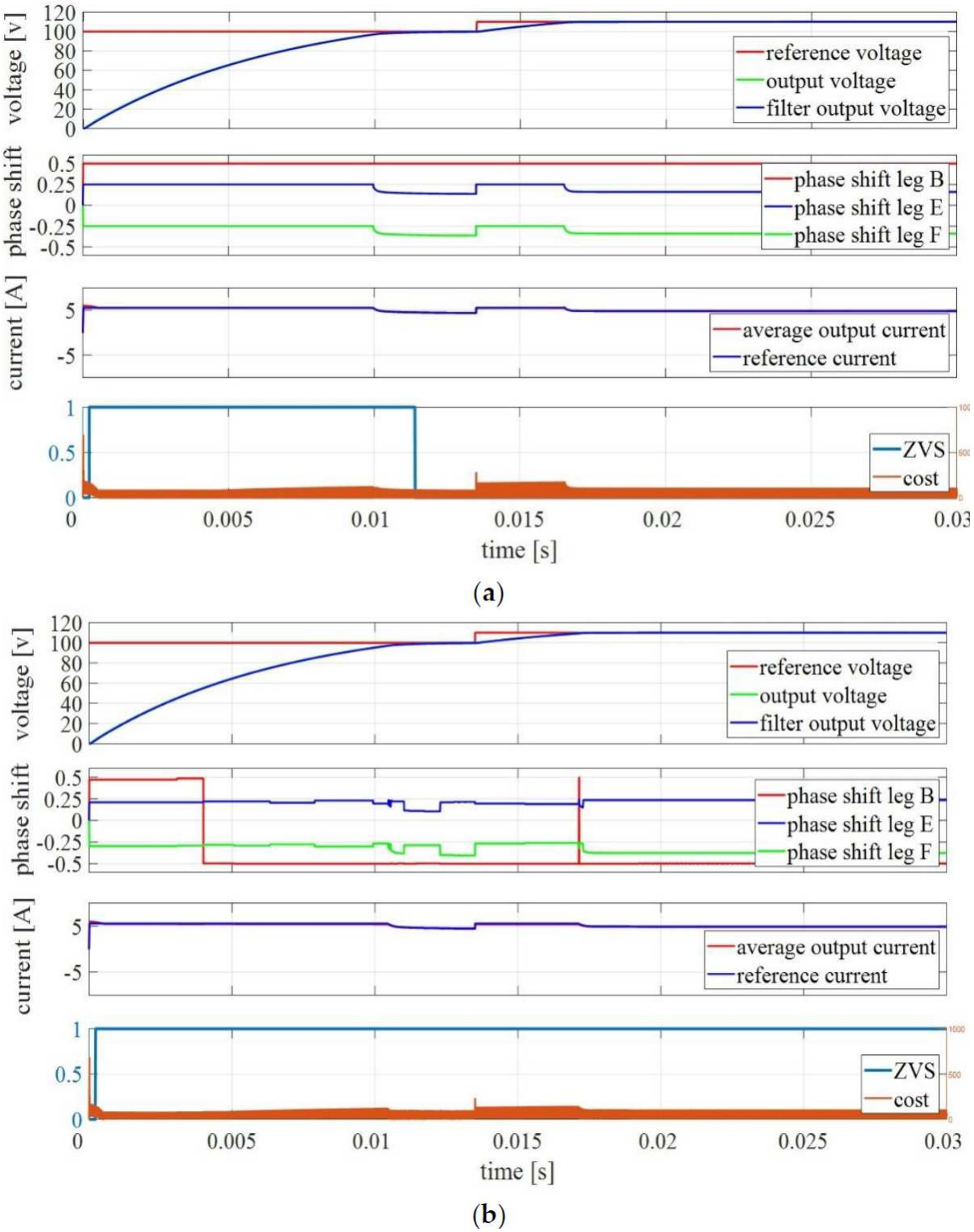


Figure 7.13: Output voltage control with startup from zero and step test (100 to 110 V): (**a**) SPS modulation; (**b**) Optimized modulation.

7.4 Experimental Results

The experimental work is presented here to validate the theoretical and PLECS simulation results and to verify the accuracy of the calculations, with a primary focus on the average output current at various operational points, corresponding to different phase-shift values. The experiments were conducted using a prototype single-phase DAB, featuring essential specifications as listed in Tab. 7.1. The experimental setup, along with the oscilloscope used for measuring key waveforms of the DAB converter, is illustrated in Fig. 7.14.

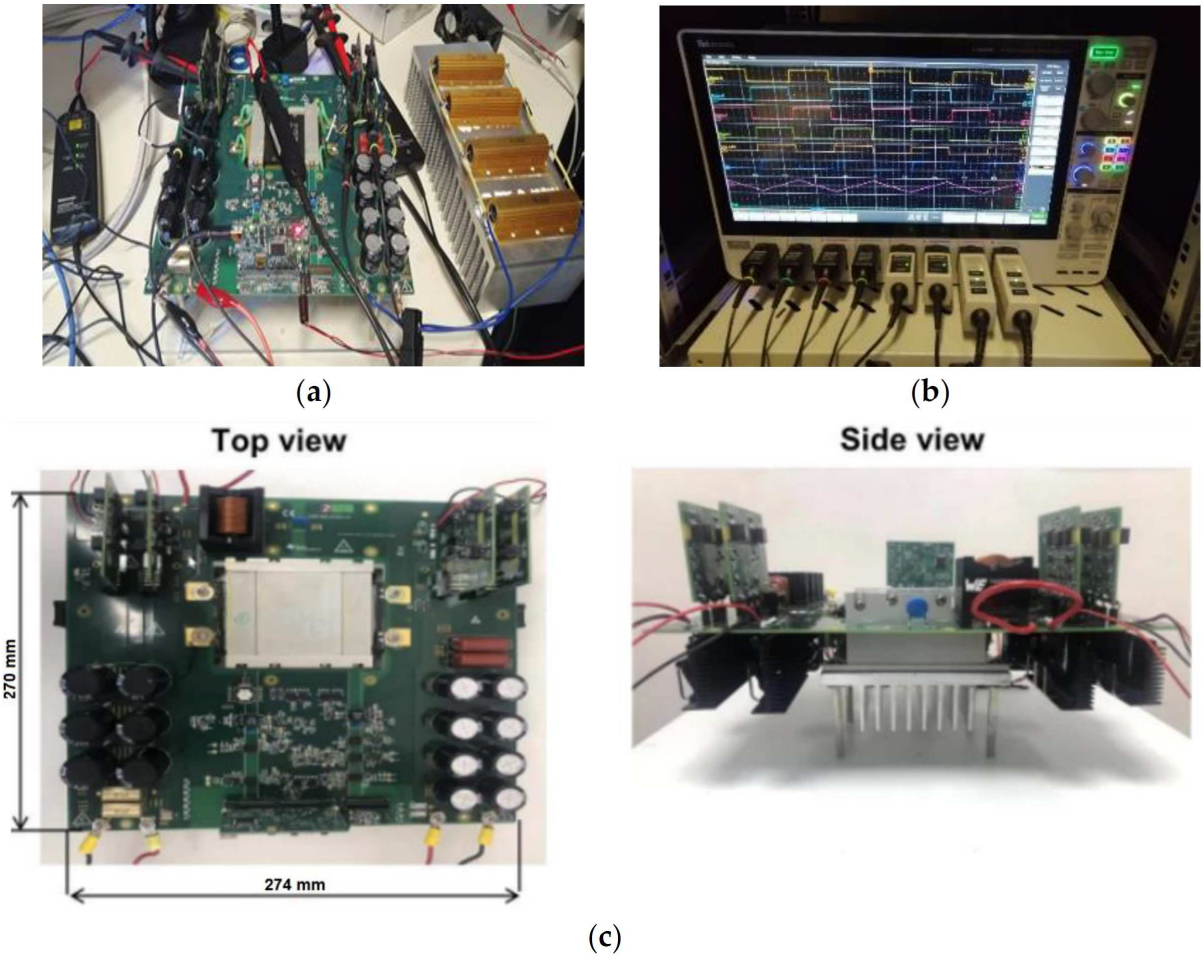
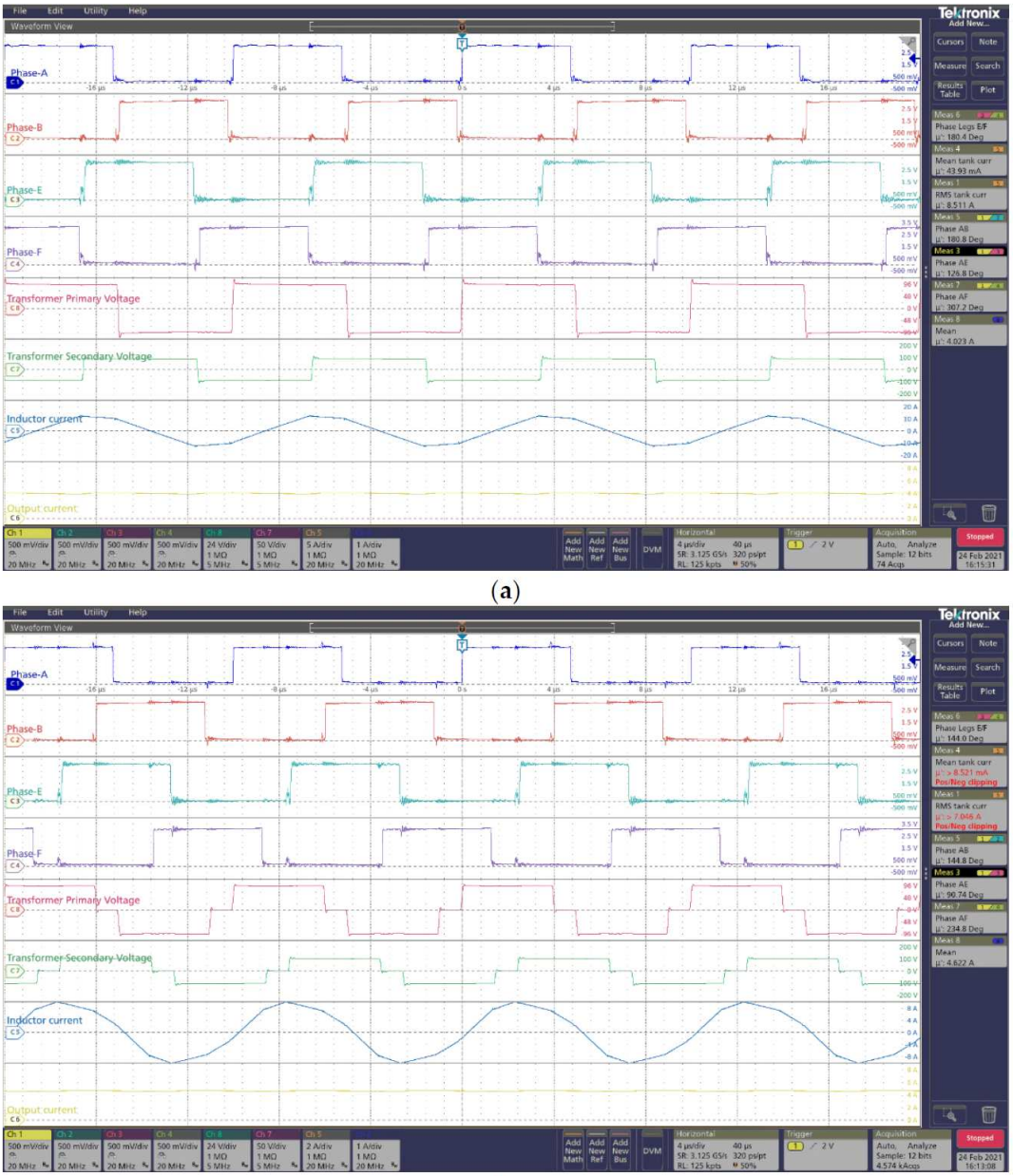


Figure 7.14: DAB Board: (**a**) experimental setup; (**b**) oscilloscope measuring the key wave-forms of the DAB converter; (**c**) top and side view.

7.4.1 Open-Loop Testing with Arbitrary Phase-Shifts

Open-loop tests with various phase-shift triplets were conducted to validate and assess the performance of the DAB DC-DC converter. These tests were carried out using the DAB parameters outlined in Tab. 7.1. Initially, several "random" triplets (φ_B = primary "negative" leg, φ_E = secondary "positive" leg, and φ_F = secondary "negative" leg, as indicated in the schematic) were selected for comparison. Given that the average output current is a key result of this work and is independent of the output voltage (depending solely on input voltage and phase-shifts), the input voltage was maintained at 100 V to facilitate comparisons with various values.
Tab. 7.3 presents a comparison of the average output current obtained from the analytical model, PLECS simulation model, and the experimental model under different phase-shift combinations. The average output current (experimental) reported in the tables has been normalized by the experimental efficiency ($\overline{I_{o\_exp}}/\eta_{exp}$) to align with the analytical results and to understand the

impact of losses (primarily switching and conduction) on the average output current [119–121]. Additionally, Fig. 7.15 displays waveforms of gate control signals, primary and secondary voltages of the transformer, inductor current, and the average output current of the experimental model for case 3 and case 5.



(**a**)

(**b**)

Figure 7.15: Gate control signals, transformer's primary and secondary voltage, inductor current and output current average of the experimental model (open loop): (**a**) Case 3; (**b**) Case 5.

7.4.2 SPS Closed-Loop

To validate the theoretical findings and assess the performance of SPS closed-loop control, steady-state tests were conducted. These tests involved keeping the input voltage fixed at 100 V while varying the output voltage, which corresponds to different values of the phase-shift (φ_E). The switching frequency was also varied in the range of 60–140 kHz to analyze and optimize the ZVS threshold range. This was done to understand its impact on the average

output current and to leverage the switching frequency as an additional degree of freedom for extending the ZVS range. These tests were carried out as an application of the proposed SPS control method and served as an experimental validation of the analytical results obtained with SPS closed-loop control.
The threshold current required for achieving Zero Voltage Switching (ZVS) at each switching event (both turn-on and turn-off) for each leg on the primary and secondary sides is calculated as follows:

$$\begin{aligned} i_{thr\_pri} &= \frac{2C_{oss\_pri}\,V_i}{T_{dt}} \\ i_{thr\_sec} &= \frac{2C_{oss\_sec}\,V_i}{T_{dt}} \end{aligned} \tag{7.18}$$

The threshold current for each leg on the primary side ($i_{thr\_pri} = 0.88\ A$) remains constant since V_i is held constant. However, the threshold current for each leg on the secondary side (i_{thr_sec}) varies for each case as it depends on the output voltage. In Tab. 7.4, you can see the experimental results of the SPS closed-loop control tests at different switching frequencies (f_{sw}) ranging from 60 kHz to 140 kHz. The reference current is normalized by the efficiency (i.e., ${I_o}^*\eta_{exp}$), and the error, which is a normalized measure, represents the difference between the normalized reference current (${I_o}^*$ norm) and the actual measured current. It is assumed that the actual output voltage matches the reference voltage set by the software. For each test, five cases are presented. The first two cases of each f_{sw} exhibit hard switching in the secondary switches, while from case no. 3 onwards, soft-switching is achieved on both the primary and secondary sides, which is highlighted in green.

Table 7.4: SPS closed-loop test with variable switching frequency (60–140 kHz).

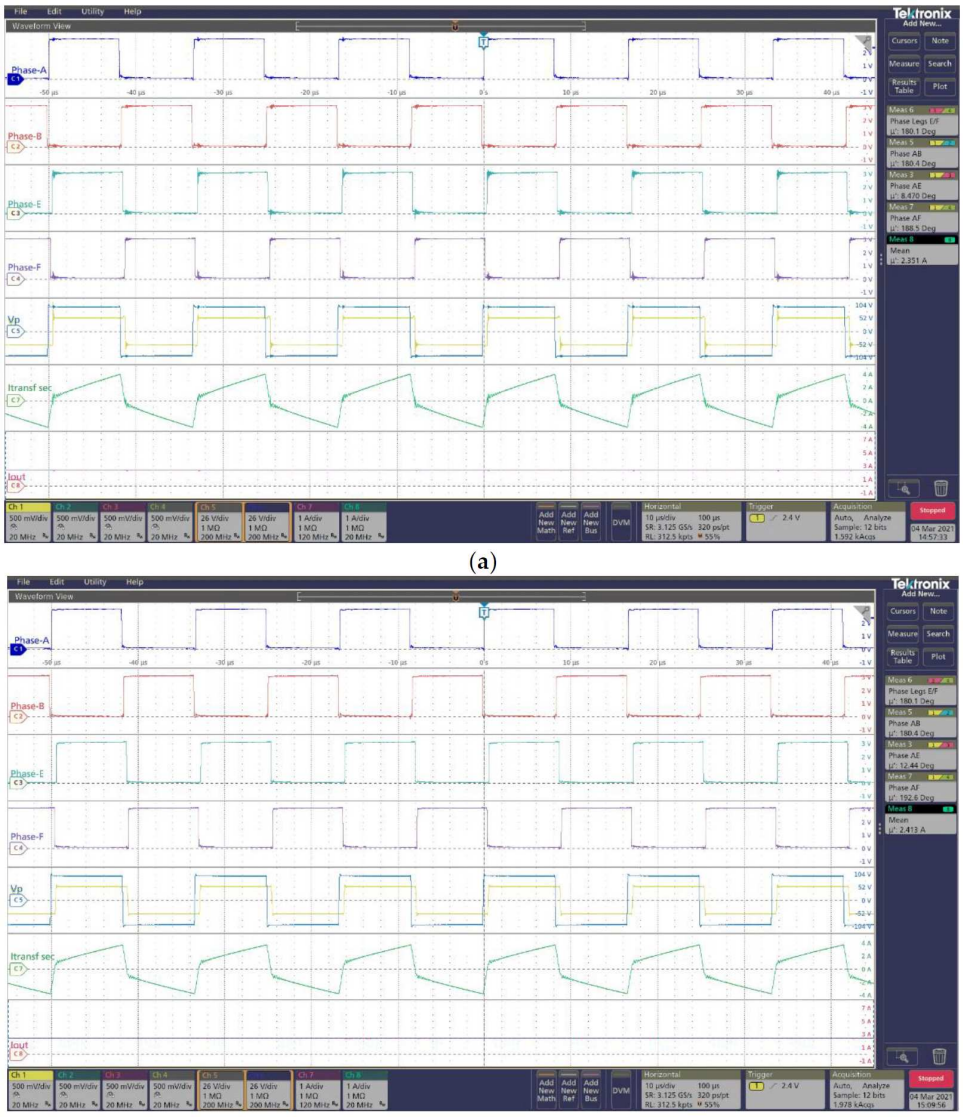
Switching frequency	**Case**	**Phase-Shift Value**	**Experimental (Measured)**			**Ref. $\overline{I_o}^*$ Analytical**	**Normalized ref. $\overline{I_o}^*$**	**Err. Normalized Measured**
kHz	#	φ_E	V_o **(V)**	I_o **(A)**	η_{exp} (%)	$\overline{I_o}^*$	$\overline{I_o}^*$ **(norm.)**	%
60	1	0.020	52	2.28	96	1.48	1.42	−61.1
	2	0.022	53	2.34	97	1.58	1.53	−52.9
	3	0.033	54.85	2.41	97	2.32	2.25	−6.9
	4	0.035	55	2.41	98	2.38	2.32	−3.9
	5	0.046	62	2.72	97	3.14	3.06	11.1
80	1	0.029	51	2.24	96	1.53	1.47	−52.5
	2	0.031	52	2.28	96	1.61	1.55	−46.9
	3	0.047	53.4	2.34	97	2.35	2.28	−2.8
	4	0.051	55	2.41	98	2.56	2.50	3.4
	5	0.06	62	2.72	97	3.10	3.02	10
100	1	0.038	50	2.19	96	1.53	1.47	−46.2
	2	0.040	51	2.24	97	1.61	1.55	−38.6
	3	0.060	52	2.28	97	2.35	2.28	−0.26
	4	0.068	55	2.41	97	2.56	2.50	4.9
	5	0.083	62	2.72	97	3.10	3.02	8.3
120	1	0.030	40	1.75	91	1.05	0.95	−83.3
	2	0.052	49.8	2.19	97	1.7	1.68	−30.4
	3	0.070	50	2.20	96	2.23	2.15	−2.2
	4	0.075	51	2.50	98	2.38	2.57	2.8
	5	0.079	52	2.29	97	2.45	2.37	3.5
140	1	0.038	40	1.76	93	1.13	1.05	−68.1
	2	0.059	48	2.11	96	1.66	1.60	−31.8
	3	0.081	48.3	2.12	97	2.16	2.09	−1.6
	4	0.090	50	2.20	96	2.32	2.24	1.7
	5	0.093	51	2.24	97	2.40	2.32	3.6

In the reported figures (cases 1 and 2 of each test), you can observe hard switching characterized

by noise and ringing in the key waveforms. This hard switching occurs because there isn't sufficient current to discharge the secondary-side MOSFETs' output capacitors. As a result, the device voltage V_{ds} is not zero at the turn-on of leg E and F switches, leading to hard switching on the secondary side.

It's important to note that the error between the measured and analytical average output current is relatively large only in the non-ZVS cases, which demonstrates the effect of hard switching on the output current. On the other hand, this error is smaller in all the ZVS cases. A significant difference in the φ_E value between ZVS and non-ZVS cases is observed, especially between case no. 2 and 3 of each test. This difference is attributed to the impact of dead-times, as discussed in [122].

The key waveforms and transitions between ZVS and non-ZVS cases at switching frequencies of 60 kHz, 100 kHz, and 140 kHz are depicted in Figures 7.16, 7.17 and 7.18.

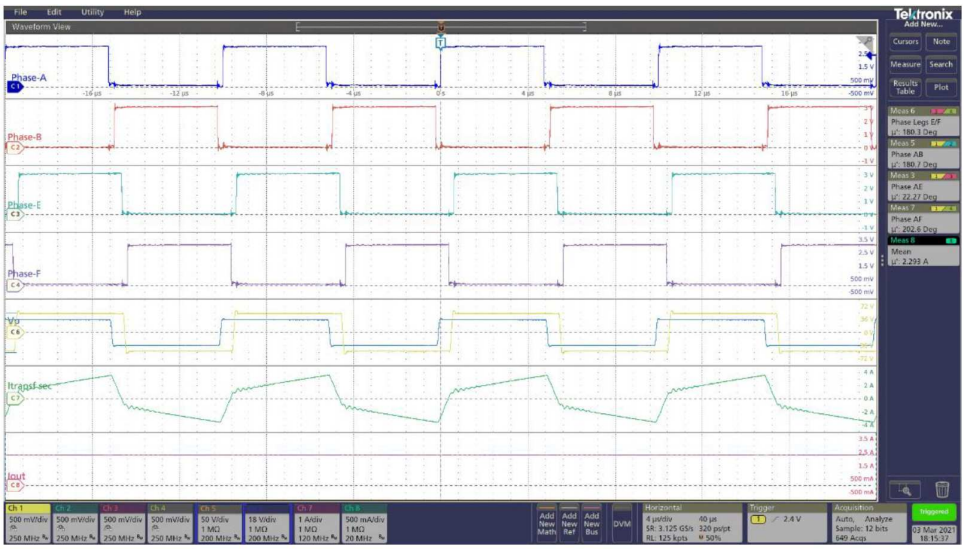


(**a**)

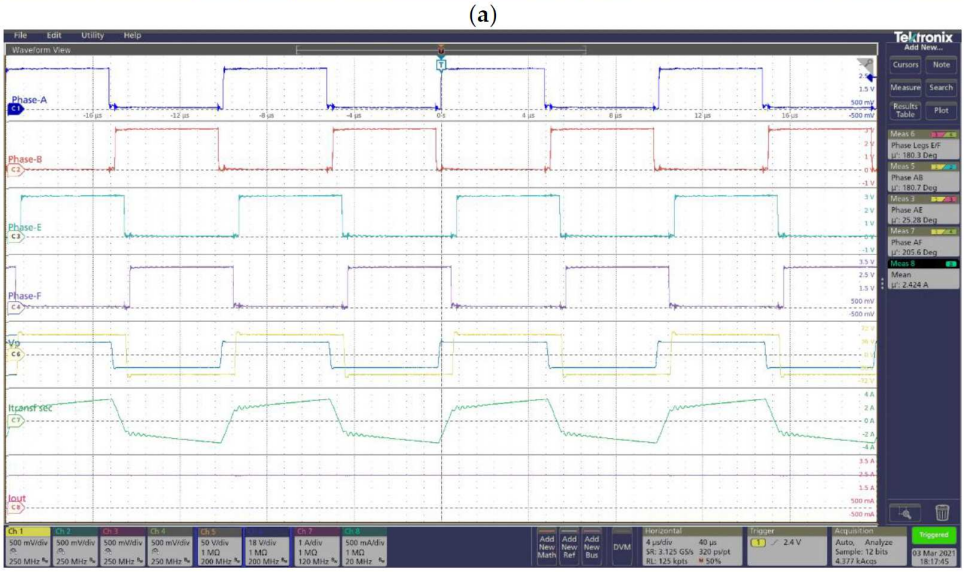
(**b**)

Figure 7.16: Gate control signals, transformer's primary and secondary voltage, inductor current and output current average of the experimental model at 60 kHz: (**a**) Case 2; (**b**) Case 3.

The dynamical behavior of the SPS closed-loop control scheme presented in Figure 6 was put to the test by applying a step change in the output voltage setpoint, transitioning from 0 V to 75 V. The experimental results, as shown in Figure 18, closely align with the corresponding simulation trace. The rise time observed in the experiment is in accordance with the design of



(**a**)

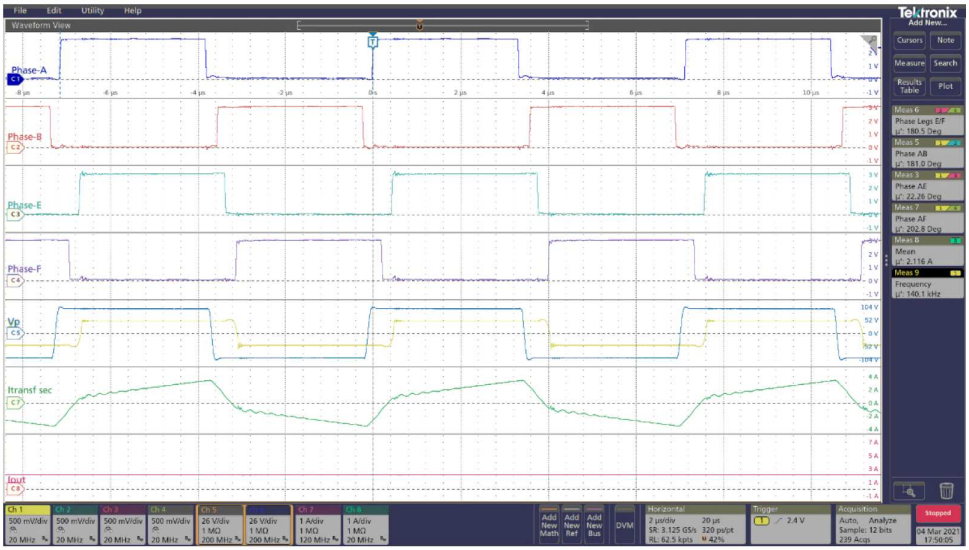


(**b**)

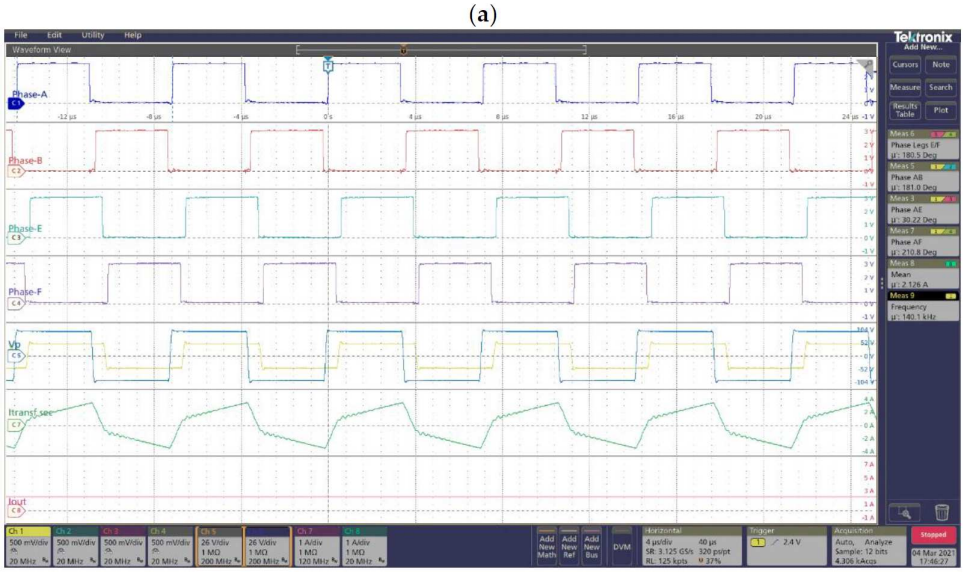
Figure 7.17: Gate control signals, transformer's primary and secondary voltage, inductor current and output current average of the experimental model at 100 kHz: (**a**) Case 2; (**b**) Case 3.

the voltage regulator.

This design leverages the inner section of the schematic (the open-loop current control) to act as a controlled current source. This approach linearizes the controller's behavior, as evident in the performance of the outer voltage regulation loop.



(**a**)



(**b**)

Figure 7.18: Gate control signals, transformer's primary and secondary voltage, inductor current and output current average of the experimental model at 140 kHz: (**a**) Case 2; (**b**) Case 3.

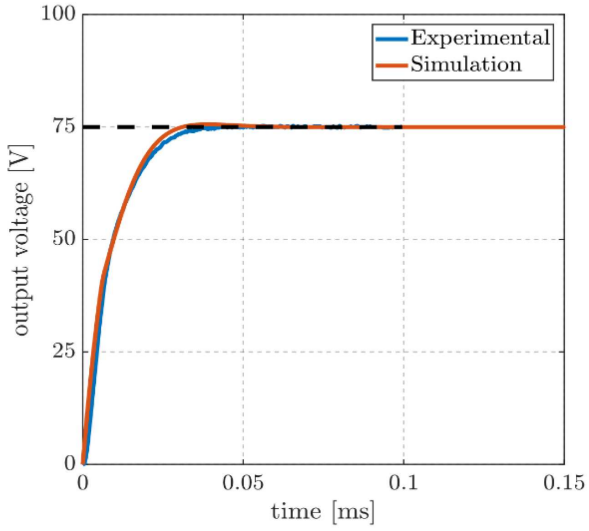


Figure 7.19: Step voltage response of the proposed SPS control, experimental vs. simulation.

7.4.3 Open-Loop Optimized Control Testing

An open-loop test for the optimized control scheme was conducted at an input voltage of 100 V and a switching frequency of 100 kHz. As mentioned earlier, the semi-analytical approach allows for the prediction of the converter's behavior under various operating conditions with reasonable computational effort. This approach can be used to optimize the operating point by considering a cost function that combines the desired output current with other objectives. The test was conducted to apply the proposed optimized control method and to experimentally validate the analytical results.

The results of the open-loop optimized control tests are presented in Tab. 7.5, covering five different cases. All cases involve ZVS on both the primary and secondary sides since the optimization procedure only considers phase-shift triplets where ZVS is achieved in all legs. The analytical optimization results were compared to the experimental results, and they exhibited good agreement. Fig. 7.20 provides key waveforms for the cases with minimum cost and ZVS on both primary and secondary side switches.

Table 7.5: Optimized open loop control at 100 kHz.

Phase-Shift Values				**Experimental (measured)**			**Ref $\overline{I_i}^*$ Analytical**	**Normalized Ref. $\overline{I_o}^*$**	**Normalized error Measured**
Case	φ_B	φ_E	φ_F	V_o **(V)**	I_o **(A)**	η_{exp} **(%)**	$\overline{I_o}^*$	$\overline{I_o}^*$ **(Norm)**	**(%)**
1	0.130	0.025	0.820	24	1.05	81	1.16	0.94	−11.95
2	0.445	0.030	0.530	50	2.20	94	2.19	2.07	−6.29
3	0.555	0.095	0.590	51	2.25	97	2.45	2.37	5.15
4	0.495	0.065	0.585	59	2.60	96	2.90	2.79	6.96
5	0.505	0.065	0.645	71	3.11	97	3.48	3.36	7.57

To validate the optimized control strategy, a comparison with the SPS (Single-Phase Shift) method was conducted under the same operating conditions. The specified conditions included a reference output voltage of 50 V and a load current of 2.2 A. In the case of SPS, as depicted in Figure 20a, it is evident that the secondary legs (E and F) did not achieve the ZVS (Zero Voltage Switching) condition. This is confirmed by observing the 2^{nd} (orange) and 3^{rd} (blue) traces, which represent the high-side drain-to-source voltage of legs E and F, respectively. These traces exhibit significant voltage ringing during the turn-on of the active devices, indicating that they are in a hard-switching condition. Additionally, due to the voltage drop of diodes, the voltage during dead-times either falls below zero or exceeds the output voltage.

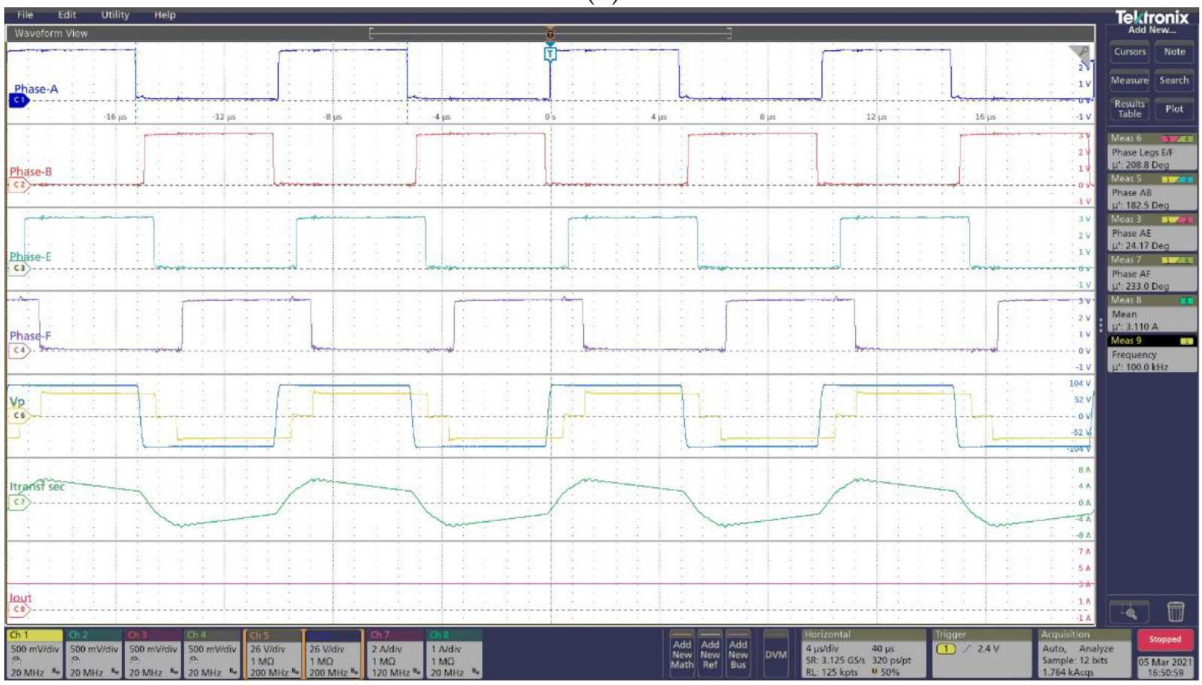
Conversely, in Figure 20b, which illustrates the optimized modulation approach, both legs E and F are in a soft-switching state. The substantial voltage ringing has disappeared, and it is now possible to observe the diode voltage drop, which is depicted as a small overshoot on the drain-to-source voltage as soon as the turn-on phase concludes.

7.4.4 Comments on Experimental Results

In this section, we provide insights into the experimental work, focusing on the validation of calculations, particularly with regard to the average output current at various operating points, corresponding to different phase-shift values.

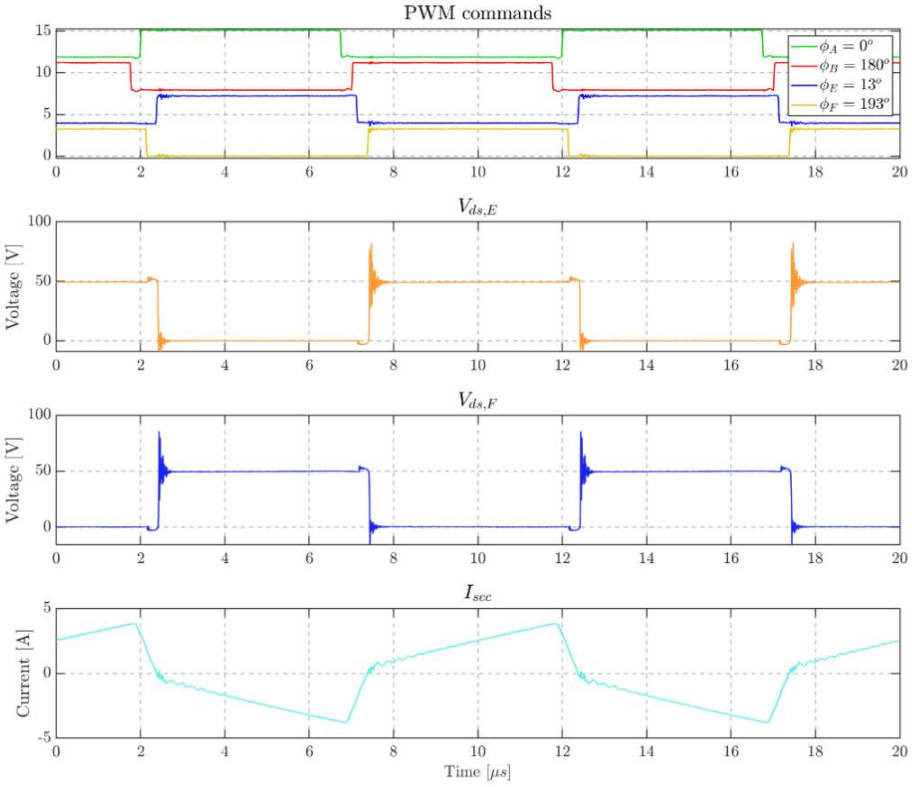
The experimental validation begins with open-loop tests employing arbitrary phase-shift triplets. These tests are conducted to assess and analyze the performance of the DAB DC-DC converter. The average output current results obtained by the analytical model, PLECS simulation model, and the experimental model are compared in five different cases. Notably, the PLECS simulation and experimental results exhibit close alignment, considering that the simulation model accounts for parasitic capacitance and losses. However, a significant discrepancy is observed between the analytical and experimental results, primarily attributed to various stray losses present in the

(**a**)

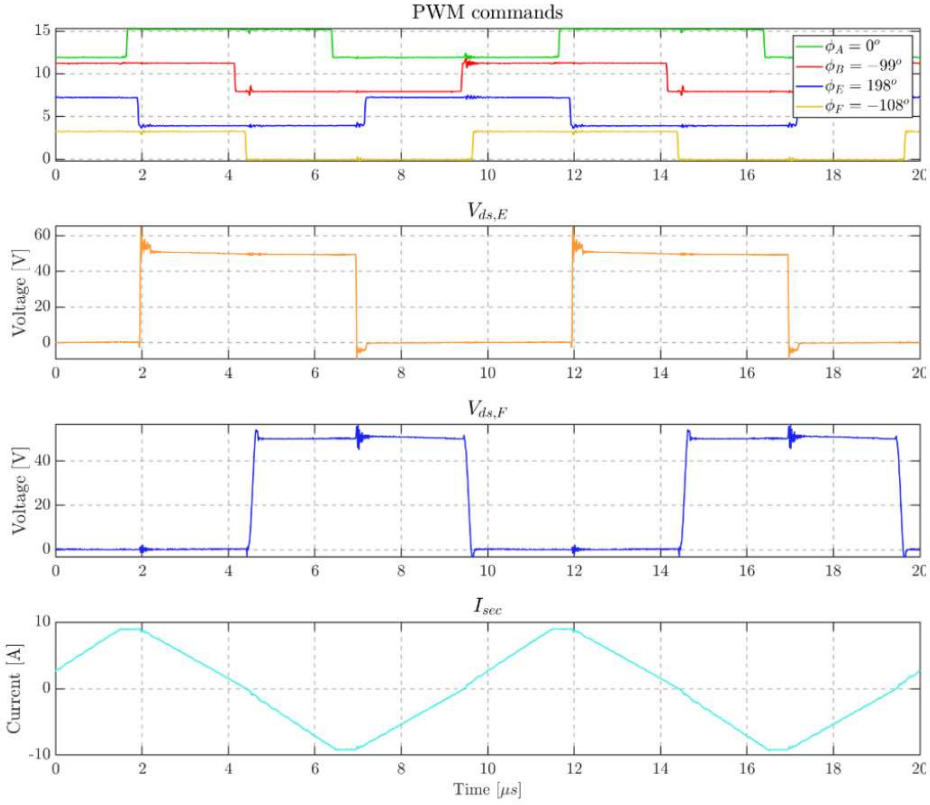


(**b**)

Figure 7.20: Gate control signals, transformer's primary and secondary voltage, inductor current and output current average of the experimental model at 100 kHz (optimized control): (**a**) Case 1; (**b**) Case 5.



(**a**)



(**b**)

Figure 7.21: Comparison between SPS control and optimized modulation; both the controls reach the same operating point: (**a**) SPS control, the secondary switches do not reach the ZVS condition; (**b**) arbitrary (optimized) control, all the legs reach the ZVS condition.

hardware. This underscores the importance of considering efficiency in the power transfer process, with the converter's efficiency assumed to be unity in analytical calculations. As a result, the average output current obtained experimentally is normalized by the estimated efficiency (I_{o_exp}/η_{exp}) to compare it with the analytical results and understand the impact of losses, particularly switching and conduction losses, on the average output current.
Following this, closed-loop Single-Phase Shift (SPS) control tests are performed to experimentally confirm the implementation of the proposed SPS control schematic, which leverages the analytical findings. These closed-loop SPS tests are executed at varying switching frequencies. The tests reveal that the normalized error (factoring in efficiency) between the measured and analytical average output current is relatively large in non-ZVS (Zero Voltage Switching) cases but considerably smaller in all ZVS cases. This discrepancy in non-ZVS cases is attributed to the varying leg voltage levels during dead-times, depending on whether switching occurs in ZVS or not. This behavior is associated with the effects of dead-times and should be further investigated. However, it's important to emphasize that the desired condition is ZVS, and this discrepancy can be avoided by ensuring the desired ZVS condition is met. This is one of the key features of the proposed optimized control method.
It's noteworthy that the average output current and peak inductor current are also influenced by the switching frequency. Therefore, it is expected that this variable should be taken into consideration in optimizing DAB operation. This implies that variable switching frequency can be introduced as an additional degree of freedom in the optimization process, without incurring a substantial increase in computational cost.
Lastly, open-loop optimized control tests are conducted at a 100 kHz switching frequency. The semi-analytical approach, as previously mentioned, provides a means to predict the converter's behavior under various operating conditions efficiently. This capability is harnessed to optimize the operating point. The results of all the reported cases with optimized control demonstrate ZVS on both the primary and secondary sides. The optimization process ensures that only triplets achieving ZVS in all legs are considered. Consequently, the analytical results for the optimized control are experimentally validated.

7.5 Conclusions

In this study, the validation of several critical aspects of Dual Active Bridge (DAB) DC-DC converters have been studied, focusing on modulation methods, control strategies, multi-objective optimization, semi-analytical modeling, and experimental results. The following key conclusions can be drawn from our research:

- The proposed control approach, which integrates an inner open-loop current control into a closed-loop voltage control system, demonstrates remarkable versatility. This adaptability allows for seamless integration with various modulation methods, significantly enhancing the control system's flexibility and applicability.

- By introducing a comprehensive cost function that considers control precision, switch stress, conduction losses, and soft-switching capability, we have successfully achieved multi-objective optimization for DAB converters. This approach provides a practical framework for tailoring converter performance to meet specific requirements. The flexibility of the cost function design allows for the consideration of various control variables and their relationships with independent parameters.

- Our proposed semi-analytical modeling technique offers a computationally efficient means to predict DAB converter behavior across a wide spectrum of operating conditions. This capability is invaluable for optimizing the operating point by considering multiple degrees of freedom, such as phase shifts and switching frequency.

- Experimental validation of our theoretical and simulation results is paramount for assessing the accuracy of calculations and accounting for practical losses. We conducted a series of open-loop tests with arbitrary phase-shift triplets to confirm the alignment between analytical, simulation, and experimental results.

- The experimental demonstration of closed-loop Single-Phase Shift (SPS) control corroborates the real-world application of our proposed SPS control scheme. Our results illustrate the impact of Zero Voltage Switching (ZVS) and non-ZVS scenarios on average output current. We found that control accuracy is consistently maintained during ZVS, whereas variations in non-ZVS scenarios are attributable to the influence of dead times.

- Experimental validation of open-loop optimized control reinforces the efficacy of our analytical model in achieving ZVS throughout an extensive operational range. Our optimized control strategy minimizes peak inductor current while preserving the ZVS condition, ultimately resulting in improved converter efficiency and reduced losses.

In conclusion, this comprehensive study showcases the effectiveness and reliability of DAB converters in various applications. Our proposed control strategies, multi-objective optimization, adaptability to diverse modulation methods, and the integration of analytical modeling and experimental validation make DAB converters a versatile and efficient solution. The results obtained from experimental tests closely align with the theoretical and simulation predictions, underscoring the practical viability of the methods presented. These findings offer valuable insights for the broader application of DAB converters in different scenarios, paving the way for advanced power electronics and control systems.

Part III

Inverters in the automotive industry

Chapter 8

Inverters for traction applications

Within the realm of power electronics for electric mobility applications, energy storage and distribution, it is imperative to address two critical factors that significantly distort the average output voltage in pulse-width modulation (PWM) inverters such as dead-times and switch voltage drops. These distortions are contingent upon the characteristics of the drive system and operating conditions and are often deemed unacceptable in numerous drive applications, necessitating the implementation of an appropriate compensation strategy.

Various techniques have been applied in industrial drives and are documented in contemporary literature to mitigate these issues. However, in contrast to conventional methods, our proposed approach is grounded in a comprehensive physical model of the power converter, which includes the output capacitance and is defined by a concise set of parameters. We introduce an innovative self-commissioning identification process that employs Multiple Linear Regression. This technique is assessed using a commercial drive, and its performance is compared to state-of-the-art techniques.

Additionally, we demonstrate enhancements in back electromotive force (EMF) estimation within a sensorless permanent magnet synchronous motor (PMSM) drive system, offering further validation of our methodology.

Accurate compensation of inverter distortion is very important in many industrial applications of drive systems, e.g. precision servo drives, but becomes also essential in sensorless control, as voltage distortion has strong effects on the performance of the estimation technique, especially at low speed, where the operating voltage of the machine is comparable to the level of distortion. Many techniques have been proposed in the past and also very recently [123, 124].

Given that it can be seen that phase distortion voltage primarily hinges on phase current, the majority of compensation techniques opt for an approximation curve to represent the distortion characteristics. The most basic model for addressing dead time effects solely takes into account diode clamping, leading to a compensation curve contingent upon the direction of current flow [125]. In this scenario, compensation can be implemented, for instance, by introducing suitable adjustments to the pulse width of PWM signals, with the aim of correcting the resultant average voltage [126]. The application of these models leads to a reduction in distortion, but it remains less than optimal, particularly in light of the enhanced capabilities offered by the introduction of increasingly faster digital signal processors. Consequently, in recent years, more intricate models have been embraced, including those that incorporate various correction functions e.g. linear saturated [127], sigmoidal function [128], or exponential [129] while in reference [130] the distortion voltage values relative to the phase current curve have been archived in a lookup table (LUT) for real-time interpolation.

The methodologies mentioned necessitate the identification of parameters for the correction functions or populating the lookup table (LUT). In some instances, this process is executed offline as part of a self-commissioning procedure, as discussed in references [127] and [130]. Typically, the motor is connected to the inverter output, and various values of DC voltage or

current are applied with the objective of assessing the entire current operating range. Subsequently, data is collected and processed to derive the parameters for the distortion curve or values for the LUT.
Other techniques [127, 129, 131, 132], adjust parameters by utilizing real-time measurements of harmonic distortion. Alternatively, a closed-loop compensation is employed to offset specific harmonics, primarily focusing on the 6^{th} harmonic in the rotor reference frame, as indicated in [133]. However, the stability and the impact of other sources of distortion, such as spatial harmonics of the air gap flux, have not been explored in these approaches.
In contrast, certain compensation strategies, as evidenced in reference [134], rely on the real-time measurement of the actual phase voltage at a high sampling rate. This approach aims to estimate the true average value within the switching period and offers a means to pre-distort the reference voltages prior to PWM modulation. What sets these methods apart is their shared absence of a physical model that underlies the compensation curve. Instead, they approximate the actual phenomena occurring within the inverter.
The methodology discussed in this work exploits the comprehensive physical model of the power converter. The distortion voltage is described by a nonlinear function of the current, with its parameters corresponding to the actual dead time interval, switch output capacitance, switching period, and DC bus voltage, similarly to [131]. Compensation according to this model is relatively straightforward once the model's parameters are identified, and the achieved results are exceptionally accurate.
In [135] the authors introduce a new self-commissioning method for identifying voltage distortion in inverters. It relies on a physical model of the power converter, accounting for output parasitic capacitance effects, IGBT and diode voltage drops. The technique simultaneously identifies unknown distortion model parameters and phase resistance at standstill using Multiple Linear Regression fitting. It has demonstrated improved accuracy in identification, leading to enhanced motor control compared to conventional and state-of-the-art methods. The physical model that characterized inverter non-linearities relies on the knowledge of a crucial parameter (threshold current), mandatory if an accurate estimation of interlock behaviour is needed in a self-commissioning scenario. A rough guess of this parameter might lead to wrong estimation of voltage distortion function, hence we propose two new methods that assure minimal error estimation both in evaluating the *threshold current* and subsequently in the quality of the compensation.
Moreover the capacitive behaviour of the switching devices causes a lag in the average value of the current (dependent on the capacitance value and operating point) which is usually neglected. In this work, said effect is analyzed and compensated for the first time.

8.1 Analytical model of the inverter distortion

The characteristics of the inverter's output voltage are subject to the non-ideal aspects of commutation phenomena. These include issues like dead-time effects, commutation delays, voltage drops in power devices, equivalent parasitic resistance, and inductance within the current paths. Furthermore, there are factors like the charging and discharging of the equivalent capacitance within the leg, which can be either parasitic or intrinsic.
To delve into this analysis, we'll primarily focus on the inverter's instantaneous output voltage concerning the reference level of the DC bus (referred to as V_{x0} in Fig. 8.1). We'll then extend our analysis to the average phase voltage for a three-phase load as a natural progression. The inductive behavior of the load allows us to model the leg's output current as relatively constant, particularly during the switching period, and to some extent during the dead-time intervals, as we will clarify shortly.
We'll begin by considering an initial model that accounts for the aforementioned non-ideal conditions but doesn't yet factor in the influence of the output capacitance. Subsequently, we

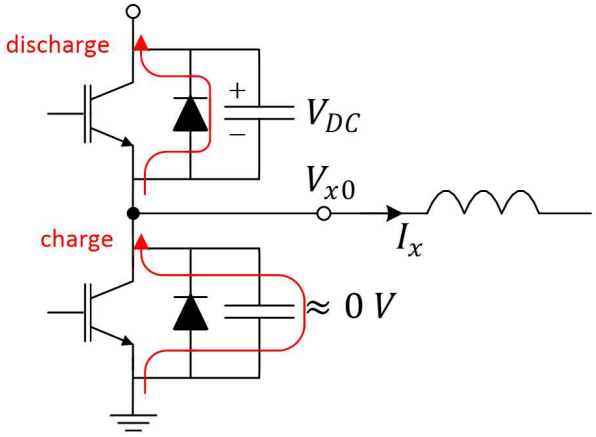


Figure 8.1: Charging and discharging switch capacitance during lower IGBT turn-off

will introduce these effects and develop a comprehensive model. This simplified version of the model serves as the foundation for the self-commissioning and compensation strategy proposed in the following sections.

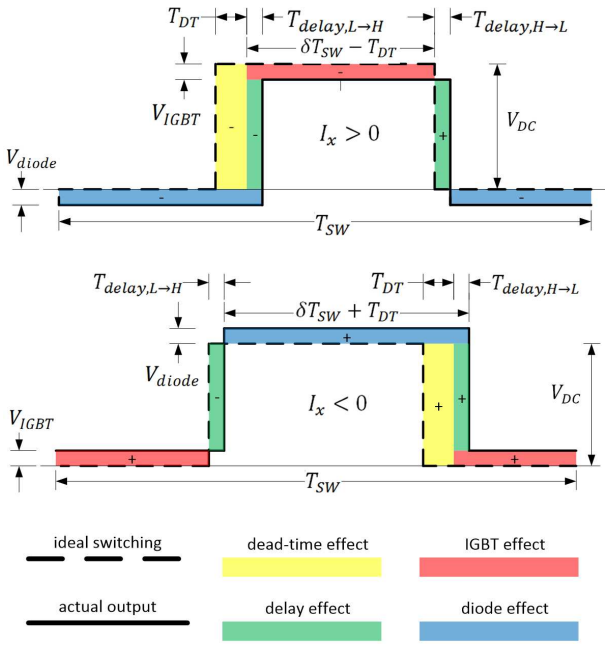


Figure 8.2: Output voltage waveforms during dead time when considering voltage drops and switching delays.

Fig. 8.2 illustrates the output voltage waveforms during the dead-time interval (T_{DT}), taking into account voltage drops (V_{IGBT} and V_{diode}) and switching delays ($T_{delay,H\to L}$ and $T_{delay,L\to H}$). Two distinct cases are presented, depending on the sign of the output current. This sign affects the conduction state of the freewheeling diodes and, consequently, the output voltage.
The voltage disparities (increase or decrease) between the ideal (dashed black lines) and actual switchings (solid black lines) are shaded in color and marked with + and − signs, signifying that they respectively raise or lower the output voltage averaged over the switching period (T_{SW}). In the forthcoming sections, we'll refer to the term $\overline{V}_{x0_{DT}} = \overline{V_{x0}} - \overline{V_{x0}}^*$, which represents distortion in the inverter's output voltage, as the "distortion voltage".
Symmetric commutation delays are depicted in green, with their average contribution typically being zero due to symmetry. Asymmetric commutation delays can be considered as additional dead-time components and are consequently indicated by yellow areas. Additionally, IGBT

and diode contributions are illustrated with red and blue areas. The equivalent on-time of the output voltage can be related to the commanded duty cycle δ_x and the dead-time. Generally speaking, the inverter voltage can be thought as the sum of a resistive component (due to winding resistance) and a non-linear function of the phase currents

$U_x{}^*$	(Avereged)Voltage reference synthesized by current controller
U_x	Ohmic component of the inverter voltage
f_d	Distortion function
i_a, i_b, i_c	Phase current
i_x	Phase-x current
V_{sw}	Diode voltage drop
C_{out}	Output capacitance of the device
R_s	Motor phase resistance

Table 8.1: List of symbols

$$U_x{}^* = U_x + f_d(i_a,\, i_b,\, i_c) = R_s i_x + f_d(i_a,\, i_b,\, i_c) \tag{8.1}$$

In Eq. (8.1) the general equation for the non-linear average voltage imposed by the inverter (in Tab. 8.1 the list of symbols used in this chapter is highlighted). The goal is to measure said distortion function by injecting an increasingly current reference $i_x{}^*$ and measuring the voltage reference generated by the current controller, $U_x{}^*$. It is then assumed that the real current and the real (average) inverter voltages are perfectly matching with their reference in steady-state conditions.
If the average value of the output voltage is assessed within the switching period, the following equations express the distortion voltage as a function of the sign of the output current:

$$U_x{}^* = \begin{cases} \frac{4}{3} V_{sw} sign(i_x) + \left(\frac{{T_{dt}}^2}{4 C_{out} T_{sw}}\right) i_x & \text{if } |i_x| < i_{thr} \\ \frac{2}{3} sign(i_x) \left(U_{dc} \frac{T_{dt}}{T_{sw}} + 2V_{sw}\right) + \left(\frac{1}{3} \frac{{T_{dt}}^2}{4 C_{out} T_{sw} + R_s}\right) i_x - \frac{2}{3} \frac{C_{out} {U_{dc}}^2}{T_{sw}} \frac{1}{i_x} & \text{if } i_{thr} < |i_x| < 2 i_{thr} \\ \frac{4}{3} sign(i_x) \left(U_{dc} \frac{T_{dt}}{T_{sw}} + V_{sw}\right) + R_s i_x - 2 \frac{C_{out} {U_{dc}}^2}{T_{sw}} \frac{1}{i_x} & \text{if } |i_x| > 2 i_{thr} \end{cases} \tag{8.2}$$

The sketches in Fig. 8.3 help understanding the physical meaning of the equations in (8.2), representing the actual averaged inverter phase voltage as a function of the phase current. The term i_{thr} refers to a threshold current level that depend on system (and inverter) parameters such as C_{out}, V_{dc} and T_{dt} [136]. The physical meaning of said quantity is the following: when the phase current i_x assumes exactly this value during the dead-time transition (positive direction as indicated in Fig. 8.1 for simplicity), sufficient charge is moved through the devices capacitance to charge from 0 V to V_{DC} the lower switch, and vice-versa for the upper one.
Now that the analytical V-I relationship is available, exploiting a way to measure it and use said data is imperative. The sampled non-linear V-I characteristic of the inverter is show in Fig. 8.4a and by means of Multi Linear Regression 8.3 for $|i_a| > 2i_{thr}$, the system unknown parameters such as C_{out}, R_s and V_{sw} can be estimated [135]. The switching voltage drop last term is often neglected, but in many applications, this overlook causes errors in the identification of the correct voltage compensation function. The process for estimating these parameters (which will lately be used to build the compensation function) is strongly dependent on the knowledge of the threshold current, whose value cannot be known a-priori since it depends on the output capacitance 8.4, preventing the success of a true self commissioning procedure.
Note how in Fig. 8.4a the measurement of the distortion in actuated on the a-phase (i.e. current injected on a and voltage measured on the same phase), coinciding with the α-phase on the

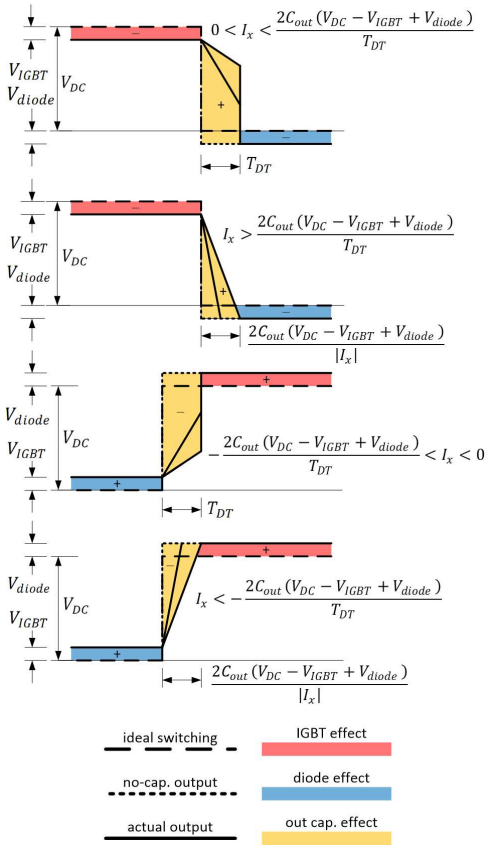


Figure 8.3: Output voltage waveforms during dead time when considering output node capacitance and different current values.

stator reference frame (SSR). Later in the dissertation a different method for the V-I non-linearity measurement will be introduced.
In Eq. (8.4a), x is a $N \times 3$ matrix and y is a $N \times 1$ column vector, assuming N as the number of points used for the identification.

$$\begin{aligned} {U_{regr}}^* &= \chi_0 sign(i_a) + \chi_1 i_a + \frac{\chi_2}{i_a} \\ X &= \begin{bmatrix} \chi_0 \\ \chi_1 \\ \chi_2 \end{bmatrix} = (x^T x)^{-1} x^T y \end{aligned} \tag{8.3}$$

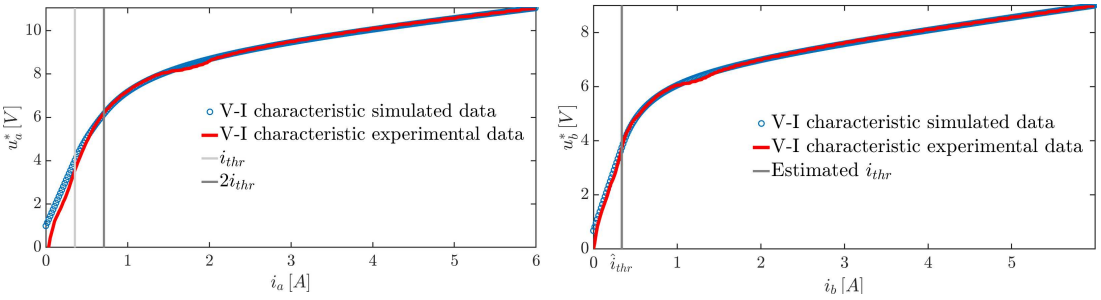
$$i_{thr} = \frac{2C_{out}U_{dc}}{T_{dt}} \tag{8.4}$$

8.1.1 Active space vector and orthogonal vector injection for V-I inverter characteristic sensing

As previously highlighted it is possible to measure the non-linear V-I inverter characteristic in two ways. In Fig. 8.4a, the measurements are correlated to the compensation function, but the data cannot be used directly to adjust the voltage distortion. Injecting a current orthogonal to one of the active space vectors (8), however, allows the measurement of the actual leg distortion voltage caused by dead-time. This function shall be added as a feed-forward term to the reference voltage produced by the current controller in order to compensate the non-linearities. The difference with respect to the previous procedure is that now the measurement can be

directly used for the compensation. Fig. 8.4b shows the experimental measurement and the simulation of the inverter characteristic obtained by injecting a current onto the β-axis.

$$\theta_{me} = \frac{2k\pi}{3} \pm \frac{\pi}{2} \ , \forall k \in \{0,\ 1,\ 2\} \tag{8.5}$$



(a) V-I inverter characteristic in α.

(b) V-I inverter characteristic in β.

Figure 8.4: Inverter non-linearities as seen by using the α-injection (a) and β-injection (b) techniques.

The reference leg voltage Eq. (8.6) is the sum of the phase reference voltage (output of the current regulators) and an injected common mode voltage, such as (for example) 3^{rd} harmonic injection. The difference between the reference and the actual inverter leg voltage Eq. (8.7) is defined as the distortion term $f_d(i_x)$, which is a non-linear function of the phase current.

$$U_{x0}{}^* = U_x{}^* - U_{0N}{}^* \tag{8.6}$$

$$U_{x0}{}^* - U_{x0} = f_d(i_x) \tag{8.7}$$

On the hypothesis of balanced load, the sum of the actual three-phase voltage 8.8 gives 8.9. By substituting 8.6 in 8.7, expression 8.9 can be rewritten as 8.10.

$$U_x = U_{x0} + U_{0N} \tag{8.8}$$

$$U_{0N} = -\frac{1}{3}\left(U_{a0} + U_{b0} + U_{c0}\right) \tag{8.9}$$

$$U_{0N} = -\frac{1}{3}\left(U_a{}^* + U_b{}^* + U_c{}^* - 3U_{0N}{}^* - f_d(i_a) - f_d(i_b) - f_d(i_c)\right) \tag{8.10}$$

Since the sum of the reference phase voltages is zero, 8.10 can be simplified and by substituting in 8.8 the generic reference voltage expression 8.12 is achieved.

$$U_{0N} = U_{0N}{}^* + \frac{1}{3}\left(f_d(i_a) + f_d(i_b) + f_d(i_c)\right) \tag{8.11}$$

$$U_x{}^* = U_x + f_d(i_x) - \frac{1}{3}\left(f_d(i_a) + f_d(i_b) + f_d(i_c)\right) \tag{8.12}$$

By injecting a current in the β-axis ($i_a = 0, i_b = -i_c$) and using 8.12, the reference voltage $U_b{}^*$ can be obtained 8.13. The distortion function $f_d(i_x)$ is odd, and since U_b is the actual voltage drop due to the phase resistance, the expression can be rewritten 8.14. The last equation shows that by knowing the reference phase voltage in the b-axis and its phase current, the distortion function can be estimated if given R_s and vice-versa. This is true only if the injection is applied on an orthogonal axis, such as β.

$$U_b{}^* = U_b + \frac{1}{3}\left(2f_d(i_b) - f_d(-i_b)\right) \tag{8.13}$$

$$U_b{}^* = R_s i_b + f_d(i_b) \tag{8.14}$$

$$f_d(i_x) = \begin{cases} f_d(i_x)^{\Lambda 0} = sign(i_x) V_{sw} + \frac{{T_{dt}}^2}{4 C_{out} T_{sw}} i_x & \text{if } |i_x| < i_{thr} \\ f_d(i_x)^{\Lambda 1} = sign(i_x) \left(V_{sw} + U_{dc} \frac{T_{dt}}{T_{sw}} \right) - \frac{C_{out} {U_{dc}}^2}{T_{sw}} \frac{1}{i_x} & if\ |i_x| > i_{thr} \end{cases} \tag{8.15}$$

Once the identification of the V-I curve is done, by applying a Multi-Linear Regression it is possible to estimate the parameters C_out, V_sw and R_s and finally build a function for dead-time compensation. In Tab. 8.2 the estimated parameters obtained by using both measurement identification procedures is shown. Equation 8.15 holds the same information as 8.2, which are the unknown terms C_{out}, V_{sw} and R_s that can be estimated by means of MLR. The main difference is that the new equation is defined in 2 intervals (for $|i_x|$ bigger or smaller then i_thr) rather than 3, and that the $f_d(i_x)$ can be directly used as a compensation function (even by using a LUT). Given the current references synthesized by the speed regulator, adding the terms f_d expressed in 8.15 for every phase allows compensation for dead-time distortion, as shown in the control scheme of Fig. 8.5.

Table 8.2: Estimated parameters comparison in α and β injection

Estimated parameters	α-**injection**	β-**injection**
$\hat{C}_{out}$ (nF)	1.24	1.15
$\hat{V}_{sw}$ (V)	0.75	0.68
$\hat{R}_s$ (Ω)	0.40	0.42

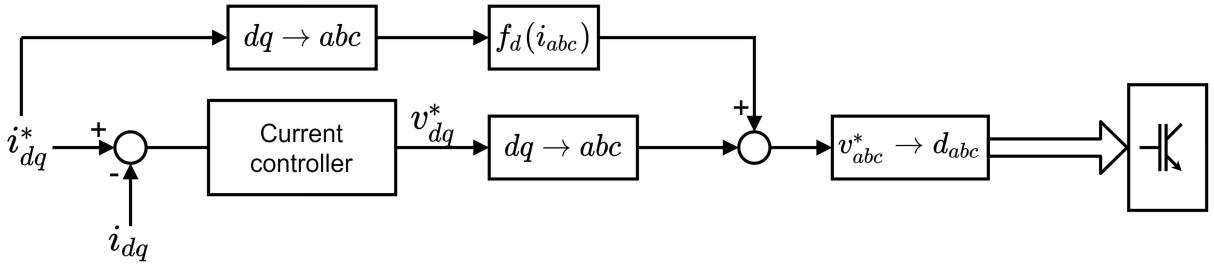


Figure 8.5: Dead-time compensation control scheme.

8.1.2 Additional remarks on current or voltage injection

During the identification procedure, it is very important that the accuracy used for the measurements is as high as possible, especially in the lower current region. This constraint is difficult to maintain due to the capacitive effect of the devices creating a lag in the sampled current. If a current feedback loop is used for current injection (and consequently reference voltage measurement) during the identification phase, the usual assumption that sampling on the period central instant assures the holding of the average value of the current is no longer true as can be seen in Fig. 8.6. This causes a misbehavior of the current controller, which would try to control an average current which differs from the reference one by the quantity named i_{err} in the image.

Since the measurement phase is critical especially for currents below i_{thr} an open-loop voltage injection is proposed, and the current is sampled (rather than the reference voltage produced by the current controller). This does not fully solve the problem of the current sampling inaccuracy but having an open-loop system for the injection procedure might, in some applications, be the best solution.

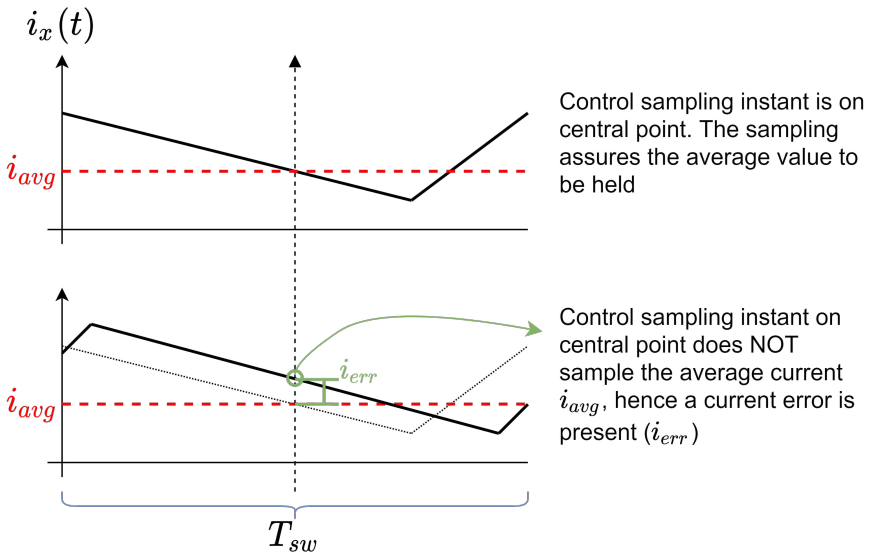


Figure 8.6: Error on average sampling of the current due to capacitive lag

8.2 Current threshold identification techniques

The quality of parameters estimation is strongly related by the correct knowledge of the threshold current that cannot be known *a-priori* and its value is usually roughly guessed. Two methods for identifying the current threshold are presented, the first one is based on an iterative process while the second one seeks the minimum of an error function. Both algorithms converge to same values for the estimated parameters i_{thr}, C_{out}, V_{sw} and R_s even though the latter is more computationally expensive compared to the iterative one.

8.2.1 Iterative method

The threshold current i_{thr} can be computed analytically as in (8.16), but since the capacitance value is not known at first, the regression is iterated in order to find a new value of capacitance and updating the threshold current until convergence is reached.

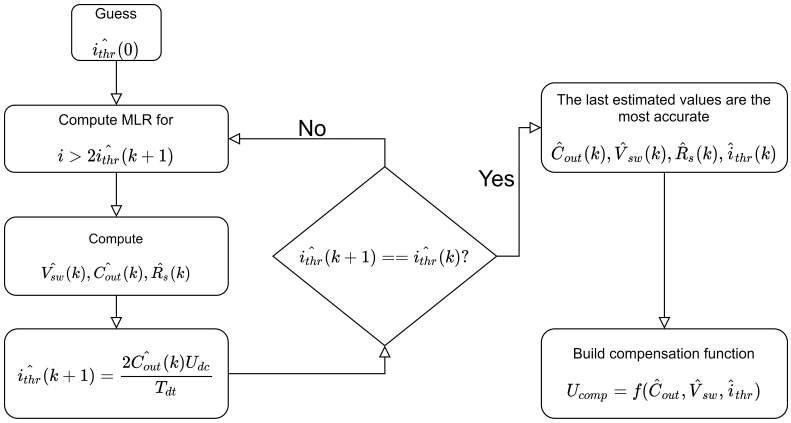
$$i_{thr} = \frac{2C_{out}(U_{dc} - U_{ce0} + U_{f0})}{T_{dt}} \approx \frac{2C_{out}U_{dc}}{T_{dt}} \tag{8.16}$$

Initially, a current threshold guess $i_{thr}(0)$ is chosen in order to let the algorithm begin. The accuracy of said term is not critical for the convergence of the algorithm, but its order of magnitude is easily predictable by assuming that the output capacitance is – in most cases – in the order of the nano Farads. The DC-link voltage and dead-time are system defined parameters, which shall always be known.
Given the first guess, a regression is computed for the current samples such that $i_x > 2i_{thr}$, finding in this way the estimators $C_{out}(k)$, $V_{sw}(k)$ and $R_s(k)$. Given the value $C_{out}(k)$ just computed, it is possible to estimate a new value of the threshold current using (8.17):

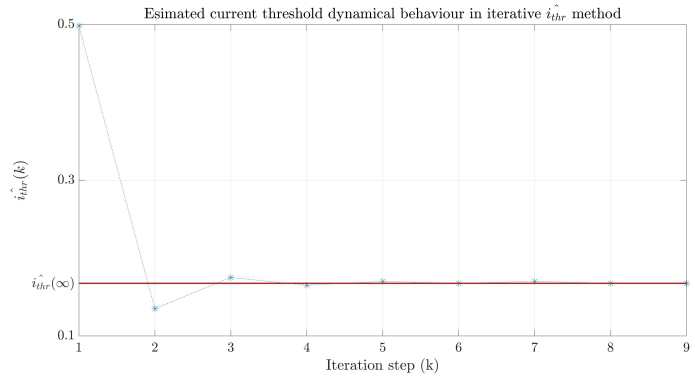
$$\hat{i}_{thr}(k+1) = \frac{2C_{out}(k)U_{dc}}{T_{dt}} \tag{8.17}$$

which will be compared with the previous value. If the difference between two consecutive threshold current estimations is below a certain tolerance, convergence is reached (8.18) and the estimations on $C_{out}(k)$, $V_{sw}(k)$ and $R_s(k)$ are the most accurate values possible.

$$|\hat{i}_{thr}(k+1) - \hat{i}_{thr}(k)| < \varepsilon_{thr} \tag{8.18}$$



(a) Flow-chart showing the iterative method for threshold current identification.



(b) Algorithm dynamical behaviour for reaching convergence.

Figure 8.7: Iterative threshold identification algorithm flowchart (a) and convergence rate (b).

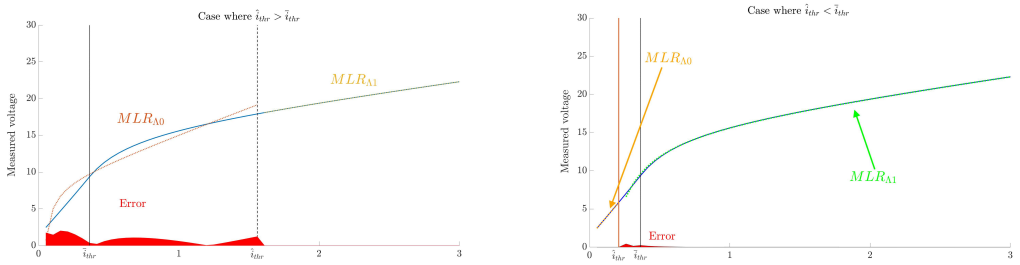
In Fig. 8.7a the flowchart representing the aforementioned algorithm is illustrated, while in Fig. 8.7b the dynamical behaviour is shown. The algorithm converges rather quickly since only 4 iterations are needed in order to reach the actual current threshold value (0.34 A) starting from a guess of 0.5 A.

8.2.2 Minimum error seek method by dual-regression

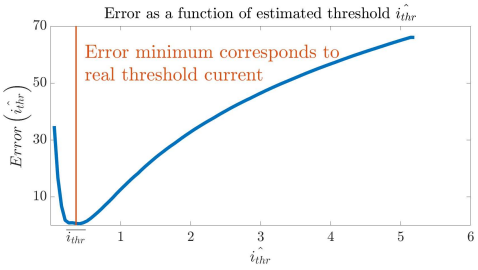
Given the distortion function measured using the orthogonal axis injection as seen previously, it is possible to build an error function whose absolute minimum gives information on the actual threshold current. Since the distortion can be written as a two-interval defined function Eq. (8.15), it is possible to make two regressions using both the analytical representations of the low and high-current threshold intervals. The idea is to compute two MLR functions moving the threshold interval (for low and high-current regions) finding the minimum error between regression function and observation, see Fig. 8.8.
By adopting Equations (8.19) for the two different regressions, the terms λ_{xy} can be used to estimate the parameters in Eq. (8.15), where the terms ${U_x}^{\Lambda 0}$ and ${U_x}^{\Lambda 1}$ are the leg voltages measured in the case of low and high current region, respectively (each with their respective constants λ_{xy}).

$$\hat{U_x} = \begin{cases} {U_x}^{\Lambda 0} = \lambda_{00} sign(i_x) + \lambda_{10} i_x + \frac{\lambda_{20}}{i_x} & if\ |i_x| < i_{thr} \\ {U_x}^{\Lambda 1} = \lambda_{01} sign(i_x) + \lambda_{11} i_x + \frac{\lambda_{21}}{i_x} & if\ |i_x| < i_{thr} \end{cases} \tag{8.19}$$

The terms λ_{xy} are the estimated coefficients of Eq. (8.15), which are reported in (23) and (24). With the notation $\hat{\square}$ indicates the estimated parameter.



(a) $\hat{i}_{thr} > \bar{i}_{thr}$ **(b)** $\hat{i}_{thr} < \bar{i}_{thr}$



(c) Error obtained moving the threshold current from 0 to I_{max}.

Figure 8.8: Simulation showing the results of minimum seeking algorithm. (a) and (b) show the error in two cases where the estimated threshold ($\hat{i}_{thr}$) is greater or smaller than the real one ($\bar{i}_{thr}$) respectively. (c) shows the error value by moving the estimated threshold in the whole current range measurement. The minimum represents the estimated current threshold value $\hat{i}_{thr}$. The result obtained with this method is identical to the one obtained with the iterative algorithm.

$$\begin{cases} \lambda_{00} = \hat{V}_{sw} \\ \lambda_{10} = \hat{R}_s + \frac{{T_{dt}}^2}{4\hat{C}_{out}T_{sw}} \\ \lambda_{20} = 0 \end{cases} \tag{8.20}$$

$$\begin{cases} \lambda_{01} = \hat{V}_{sw} + U_{dc}\frac{T_{dt}}{T_{sw}} \\ \lambda_{11} = \hat{R}_s \\ \lambda_{21} = -\frac{\hat{C}_{out}{U_{dc}}^2}{T_{sw}} \end{cases} \tag{8.21}$$

In Fig. 8.9 the flowchart describing the minimum error seeking algorithm is illustrated.

8.3 Leg voltage lag due to capacitive effects

Accurate compensation of leg voltage distortion allows to match the average voltage within a switching period to the reference one (output of the current controller). However, the capacitive behavior of the leg switching node (mainly due to the switching devices), introduces a phase lag on the actual instantaneous leg voltage. This, in turn, shifts ahead the current waveform (fundamental and ripple) with respect to the ideal symmetry point of the PWM carrier, normally considered as the optimal sampling point for the average phase current. The obtained current samples are no more corresponding to the average values within the switching period. Indeed, a similar issue can be experienced during machine operation at high fundamental-to-switching frequency due to the back-EMF, as reported in (8.22). However, only the first effect has been considered in this work, being closely related to the dead-time, and a proper compensation strategy is proposed. Either the sampling instant or the PWM waveforms can be shifted in a controlled way, based on a proper analytical model, thus allowing to recover a correct measurement of the average value of the phase current.

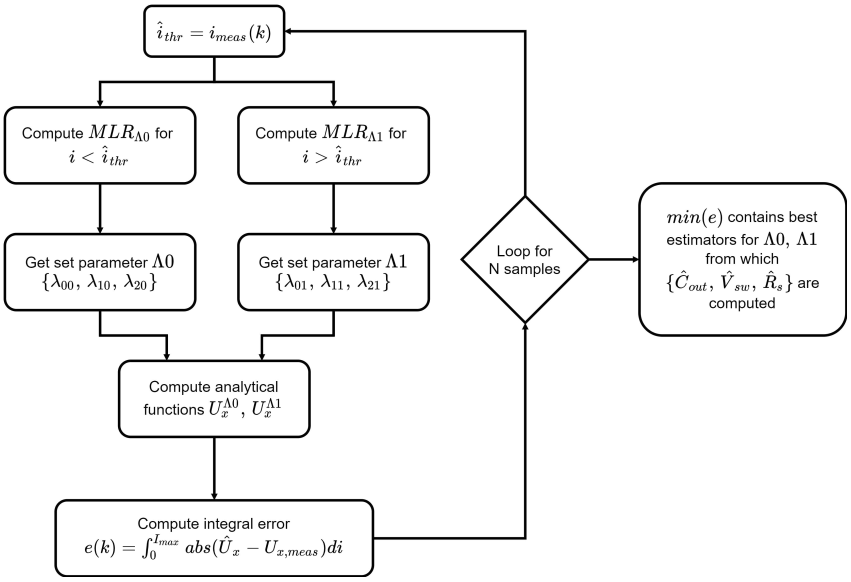


Figure 8.9: Flowchart illustrating the minimum error seek method for current threshold estimation.

The high-side PWM signal and the corresponding shape of the leg voltage in a switching period are depicted in Fig. 8.10, for a certain value of the leg node capacitance and four different current values, namely positive and negative, higher or lower than the threshold value. The dead-time on both semi-periods are shown with green areas, whilst the light blue ones highlight the behavior of the leg voltage due to the capacitive effect, resulting in a modification of both the average leg output voltage and the symmetry point of the waveform. One can notice that, based on the choice of dead-time insertion strategy (e.g. delaying the rising edges, as in this example, or introducing a symmetrical dead-time), the resulting leg voltage is modified (e.g. shifted ahead in this example) and the correct average current value can be obtained by either delaying the sampling point (as shown in the figure) or advancing the PWM signals. If this second case is considered (that provides some additional benefits as briefly discussed hereinafter), the advance time can be analytically calculated by imposing the symmetry condition of the average leg voltage within each PWM switching period, Eq. (8.22).

$$\int_0^{T_s/2} U_{x0}(t)dt = \int_{T_s/2}^{T_s} U_{x0}(t)dt \tag{8.22}$$

The contribution of the light blue areas A_r and A_f can be analytically calculated, leading to (8.23) and (8.24). The switch voltage U_{sw} has been neglected to simplify the calculations (this assumption does not introduce a substantial error). By forcing the symmetry condition (8.22), the time advance (t_{adv}) for each current region can be computed, as reported in (8.25).

$$A_r = \begin{cases} 0 & if\ i_x \geq 0 \\ -\frac{{T_{dt}}^2 i_x}{4C_{out}} & if\ -i_{thr} \leq i_x < 0 \\ T_{dt}U_{dc} + \frac{{U_{dc}}^2 C_{out}}{i_x} & if\ i_x < -i_{thr} \end{cases} \tag{8.23}$$

$$A_f = \begin{cases} \frac{{U_{dc}}^2 C_{out}}{i_x} & if\ i_x \geq i_{thr} \\ T_{dt}U_{dc} - \frac{{T_{dt}}^2 i_x}{4C_{out}} & if\ 0 \leq i_x < i_{thr} \\ T_{dt}U_{dc} & if\ i_x < 0 \end{cases} \tag{8.24}$$

$$t_{adv} = \begin{cases} {t_{adv}}^{\Lambda 0} = \frac{T_{dt}}{2} - \frac{T_{dt}}{4}\frac{|i_x|}{i_{thr}} & \text{if } |i_x| < i_{thr} \\ {t_{adv}}^{\Lambda 1} = \frac{U_{dc}C_{out}}{2|i_x|} & if\ |i_x| > i_{thr} \end{cases} \tag{8.25}$$

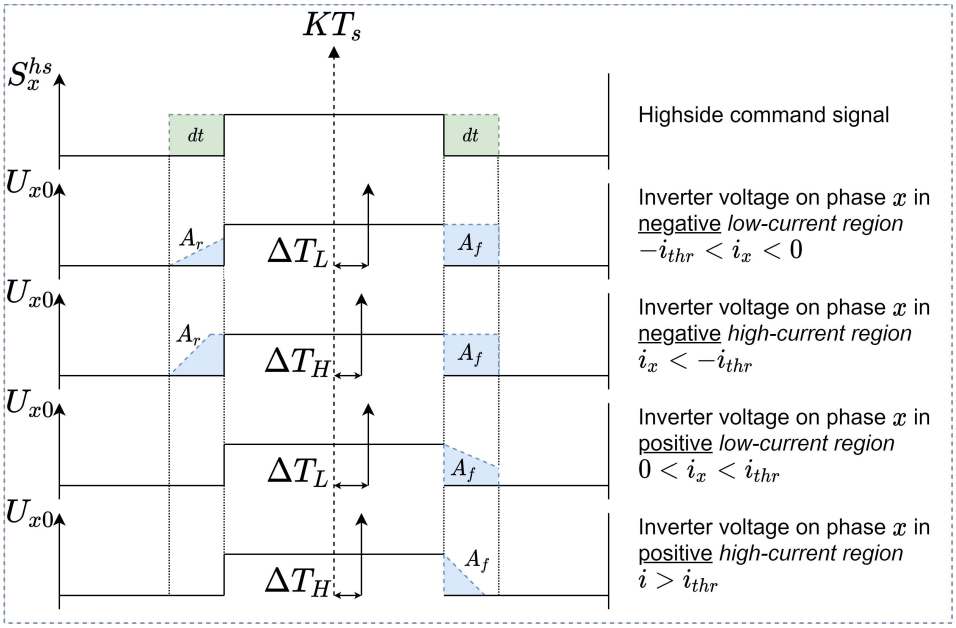


Figure 8.10: Sampling point compensation.

It is worth noticing that delaying or advancing must be applied to each leg current sampling or PWM waveform respectively, as a function of system parameters and the actual current value of each leg, based on model (8.25). It is also important to notice that the latter solution (i.e. advancing of PWM signals) allows to regain symmetrical leg voltages, with additional advantages in terms of current ripple minimization, and it is therefore preferable with respect to the former solution. This compensation becomes particularly important close to the zero-crossings of the currents and with low-inductance loads, since ripple current is high and an incorrect current sample is obtained with respect to the actual average value if no compensation is adopted.Reduction of the current ripple by PWM advancing (especially near zero crossings, as said), definitively allows to improve the quality of the controlled currents.

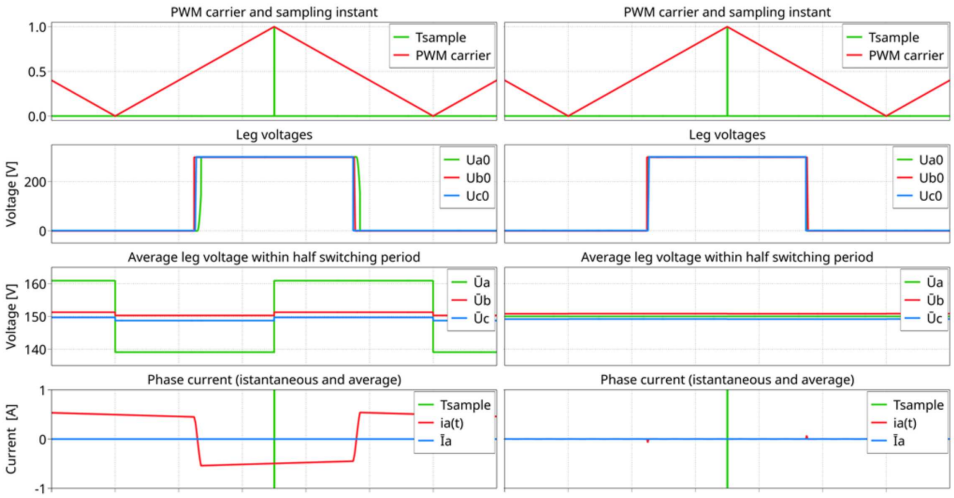


Figure 8.11: Sampling point compensation.

Simulation results are reported in Fig. 8.11 to provide a validation of the proposed current sampling compensation strategy in case of PWM advancing based on (8.25) and a constant capacitance model for the power switches. Triangular carrier and ideal sampling instant (i.e. the peaks of the carrier signal), instantaneous leg voltages, their average values within each half

switching period and one phase current are reported without (left diagram) and with (right diagram) proper advancing on the PWM signals on each leg. The actual average values of the leg output current is also drawn. One can notice how the value of the instantaneous current in the ideal sampling point is quite far from the average values without the PWM advancing strategy. When the advancing is active, a perfect match is obtained, as clearly visible in the right diagram, thus proving that the compensation is effective. Also, the average voltage values are identical within each half switching period, demonstrating that PWM advancing allows to recover the symmetry of the leg voltages, in turn minimizing the current ripple as shown in the bottom subplots.

8.4 Experimental results

Experimental validation of the dead-time compensation strategy was done by a commercial drive feeding both an induction and a permanent magnet synchronous machine, whose parameters are illustrated in Tab. 8.3.

Table 8.3: Motor parameters

Pole pair (p_p)	4
Rated speed (ω_n)	3000 (rpm)
Rated phase current (i_n)	8 (A_{rms})
Rated torque (T_n)	3 (Nm)
Magnet flux linkage (Λ_{mg})	59 (mWb)
Phase resistance (R_s)	0.4 (Ω)
Phase inductance (L_s)	2.5 (mH)

A first set of tests have been performed with the induction machine, fed by a rotating voltage space vector (whose amplitude is comparable to the level of voltage distortion introduced by the dead-time) and a controlled rotating current space vector. The results of the voltage injection are reported in Fig. 8.12, where the comparison between the resulting phase currents is shown without and with the compensation, respectively, leading to a reduction of the total harmonic distortion (THD) from 9.4% to 3.6%. The amplitude of the current in the second case is obviously higher due to a reduced (negligible) effect of dead-time on the actual phase voltages with the compensation active. The results of the controlled rotating current space vector are reported in Fig. 8.13, where the comparison between the resulting reference voltages is shown without and with the compensation, respectively, leading to a reduction of the total harmonic distortion (THD) from 8.2% to 4.2%. The current is closed-loop controlled, therefore its shape is almost sinusoidal in both cases. The amplitude of current and voltage is also very different between with and without compensation.
The last test conditions have also been adopted to analyze the effects of the estimated capacitance value on the effectiveness of the compensation. In the test results of Fig. 8.14 two detuned values are adopted with respect to the nominal (i.e. the value estimated by the regression algorithm), namely -50% and $+100\%$. It is relatively clear that the quality of the compensation decreases in both the situation, as expected, leading to a THD level of 5.8% and 6.9% respectively.
Indeed, compensation of inverter non-linearities has also a beneficial effect on the response of the current control loop, as demonstrated hereinafter in a second set of tests done with the permanent magnet machine at 20 Hz electrical frequency. A standard cascaded speed and current control is considered, with two different values forthe load torque, namely 0.9 and 3.7 Nm The current regulators have been intentionally tuned for a lower bandwidth, in order to emphasize the effects of the dead-time on the current control performance for the sake of a better evaluation of the effectiveness of the compensation strategy. The results are reported

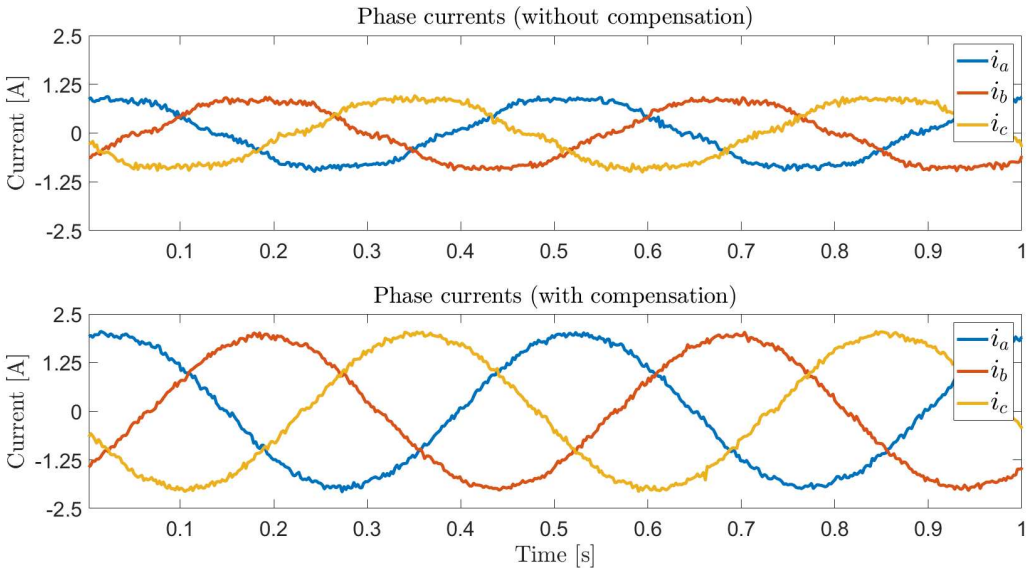


Figure 8.12: Phase currents for open-loop rotating voltage space vector injection (induction machine, $f_s = 2$ Hz, $U_s = 35$ V, $T_{dt} = 4$ μs, $T_{sw} = 100$ μs).

in Fig. 8.15. The current is relatively distorted when compensation is not applied, since the rejection of the (voltage) non-linearity effects on the current control loop is poor due to the the chosen bandwidth. Injection of the compensation voltages allows to improve the shape of the current in both the load conditions. Quantitative comparison is reported in Tab. 8.4, where the THD and the relative amplitude of 5^{th} and 7^{th} harmonic is reported in dBc (i.e. with respect to the fundamental value), showing almost 3 times lower THD with compensation.

Table 8.4: Compensation improvement data

Load torque (Nm)	Compensation	THD	5^{th} harmonic	7^{th} harmonic
3.7 Nm	Yes	3.8 %	-30 dBc	-36 dBc
	No	1.3 %	-43 dBc	-53 dBc
0.9 Nm	Yes	7.5 %	-23 dBc	-50 dBc
	No	2.5 %	-51 dBc	-48 dBc

The motor parameters for the SPM machine used in this work are found in Tab. 8.3

8.5 Conclusions

A recent approach for dead-time compensation adopting an analytical model of the physical behavior of the inverter non-linearities has been considered. Model parameters are derived from a self-commissioning procedure, based on proper voltage injection and processing, both affecting the accuracy of achievable compensation. One of the crucial aspects of this approach is the autonomous selection of the threshold current of the measured voltage-to-current characteristics, a value whose reliable knowledge is mandatory for the accurate identification of the non-linearity model. Two new methods that assure minimal error estimation have been proposed and validated in this paper, allowing the full self-commissioning of the compensation algorithm. Also, a different type of voltage injection has been proposed, allowing a more effective estimation of the voltage-to-current characteristic and direct compensation of each leg voltage as a function of the corresponding current. Finally, the effects of the non-linearities on the accuracy of current sampling and control loops have been analyzed, and an original compensation strategy was proposed and validated. Theoretical analysis and developments have been reported, together

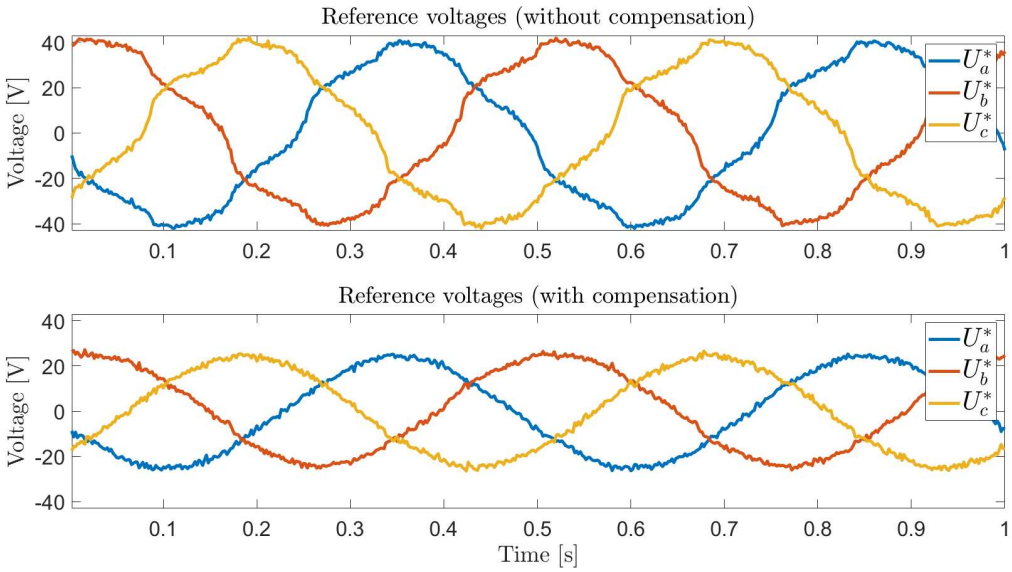


Figure 8.13: Reference voltages for closed-loop rotating current space vector control (induction machine, $f_s = 2$ Hz, $|i| = 2$ A, $T_{dt} = 4$ μs, $T_{sw} = 100$ μs).

with accurate simulations and experimental results based on a commercial drive.

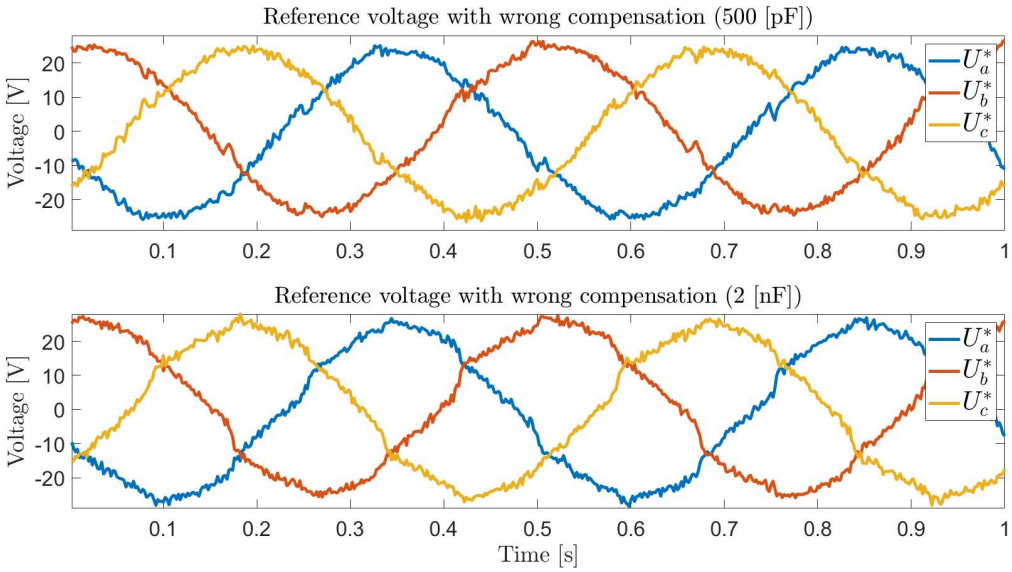
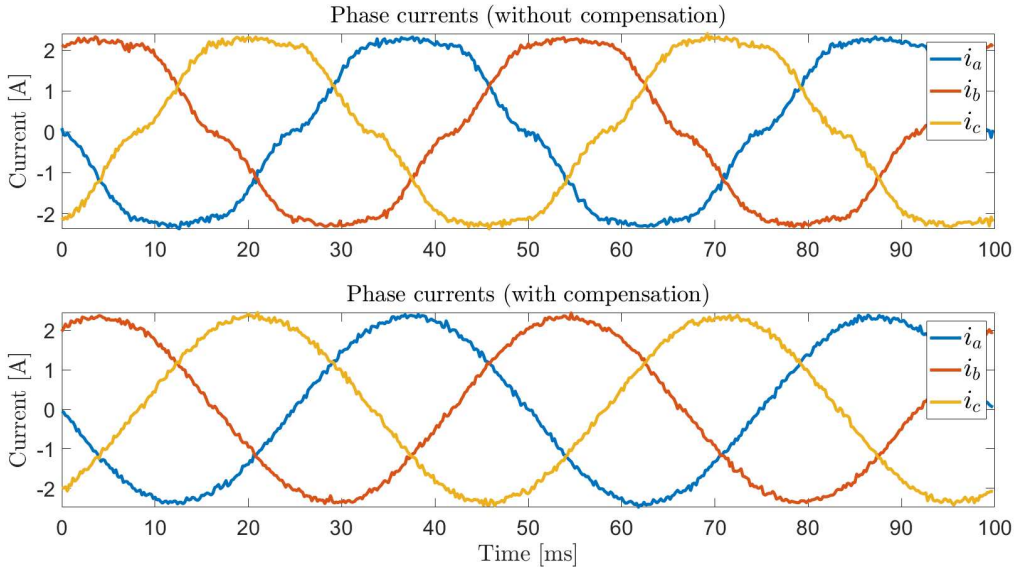
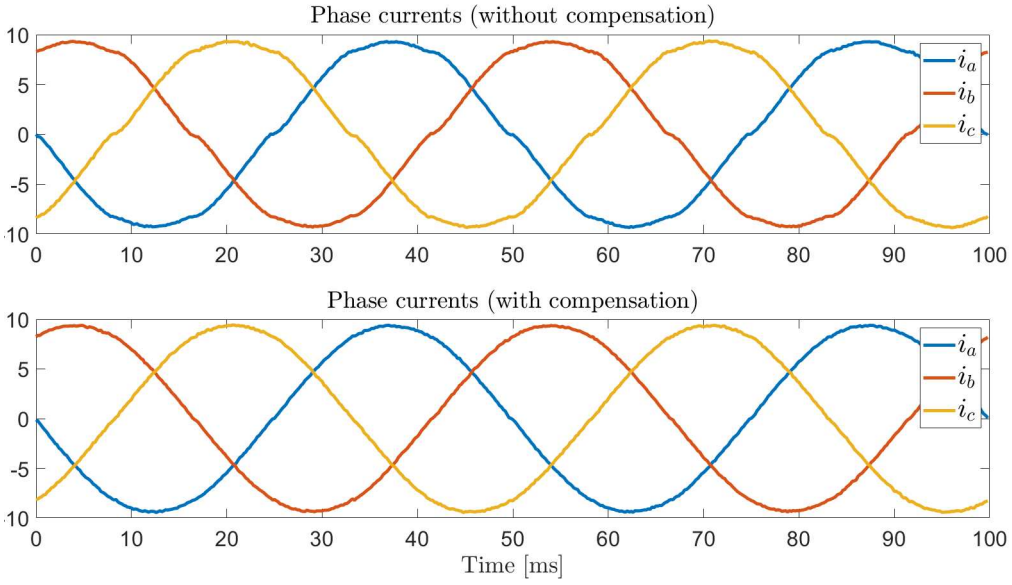


Figure 8.14: Reference voltages for closed-loop rotating current space vector control in case of detuned capacitance value in compensation model.



(a)



(b)

Figure 8.15: Phase currents without and with dead-time compensation under two different load torques. (**a**) $T = 0.9$ Nm, (**b**) $T = 3.7$ Nm

Chapter 9

Range Extender

The main issue limiting electric vehicles as viable partial solution to conventional mobility based on fossil fuels is the reduced range between charges. A possible solution is represented by range extender systems (RES), allowing to charge the main battery of the vehicle when needed, using a dedicated and reduced power internal combustion engine (ICE) coupled with an electric machine (EM) acting as a generator. In this paper a novel system architecture is proposed, based on an integrated multi three-phase PMSM, fed by high-frequency converter modules (HFCMs) employing silicon carbide (SiC) power devices. Magnetic coupling of three-phase modules is managed by a proper decoupling control strategy requiring a real-time communication among modules. Design of the system, including the power and control electronics, and the electric machine, as well as simulation and experimental results are reported to demonstrate the effectiveness of this proposal.

Due to the rapid increase in e-mobility applications, more and more solutions are proposed to increase the overall driving range of electric vehicles which, to this day, is still the bottleneck of this technology. A known system for this purpose is the range extender, a fuel-based auxiliary power unit that extends the range of a battery electric vehicle by driving an electric generator that charges the vehicle's battery, [137]. The automotive and avionic markets impose high power density, fault tolerance and low electromagnetic emissions as requirements. Due to these strict constraints, multi three phase machines are more and more considered for these applications, whose redundancy ensured by the plurality of the windings allows the system to run in the event of a failure of one of the electric motor phases, allows the use of multi drive systems decreasing the volume, [138–141]. Application of multi three phase machines to automotive application has started some years ago and is nowadays one of the most promising trends and a proved viable technology to increase the power density and reliability, [18, 142]. Availability of wide bandgap devices is somehow accelerating this trend, allowing to obtain more effective integration of the power converter into the machine, [143–145].

In this work a novel architecture is proposed for range extender systems, based on an integrated multi three phase PMSM with external rotor, fed by high frequency drive modules employing silicon carbide power devices. Each converter module handles only one third of the rated power of the electric machine, and provides modularity and a certain degree of fault tolerance to the solution. Machine design and finite element analysis are reported, together with a description of adopted control strategy for the startup of the ICE and battery charging operations. Magnetic coupling of three phase modules of the machine is managed by a proper decoupling control strategy requiring a real-time communication among control electronics modules, [18, 143–146]. Design of the system, including the power and control electronics, and the electric machine, as well as simulation and experimental results are reported to demonstrate the effectiveness of this proposal.

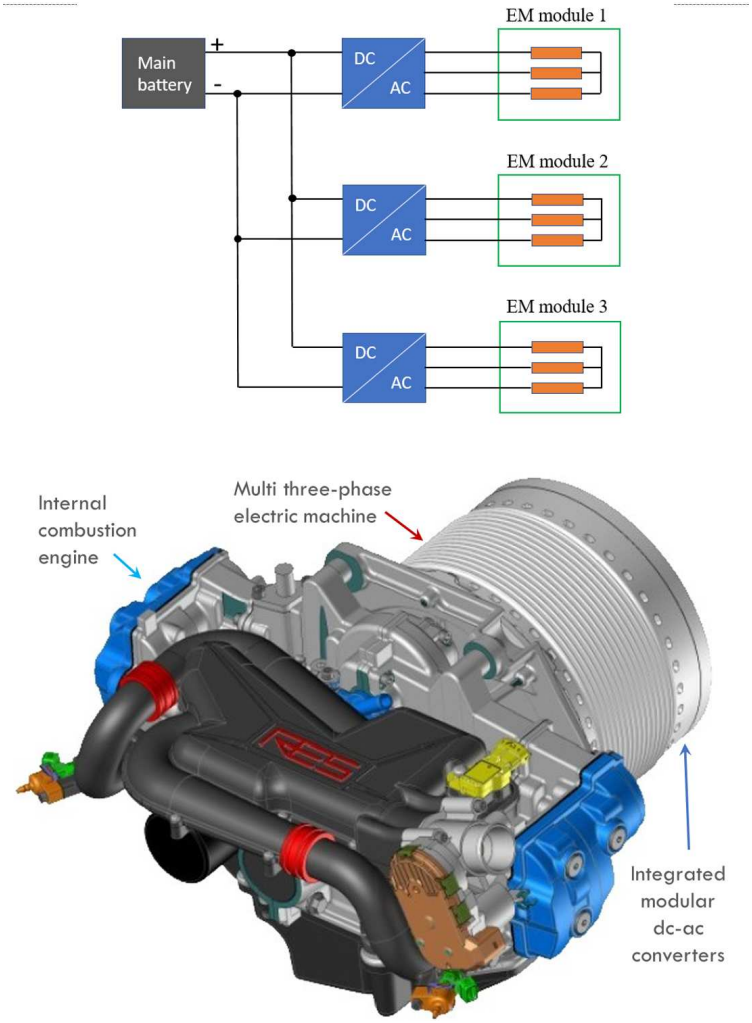


Figure 9.1: Proposed range extender system: schematic block diagram (top) and rendering of the complete solution (bottom).

9.1 Range Extender: concept and components

A schematic block diagram of the proposed system is shown in the top part of Fig. 9.1. The main high-voltage battery is connected to a set of three phase dc ac converters, integrated into the electric machine and each one supplying one of the three-phase modules of machine. The control and power electronics for each converter module handles only one third of the rated power of the electric machine, and allows modularity and a certain degree of fault tolerance of the solution.

An overall concept rendering of the overall system is shown in the bottom part of the same figure, where the three main components of the system are highlighted, namely the ICE, the multi three phase electric machine and the back compartment where the HFCMs are hosted. A detailed view of these last two components is reported in Fig. 9.2. One the left side, the three HFCMs mounted on the back aluminum plate embedding liquid cooling pipes are shown. Input and output connections of the cooling circuit, being shared between the power converters and the electric machine, are also visible on the top right and bottom left side of the external outer periphery of the system. A detailed description of the HFCMs will be reported later. However, one can notice how the battery terminals (three sets of positive and negative) and the electric machine phases (three sets of three phases) are routed on the center part of the assembly, where the connections of the power converters are present. The developed prototype adopts cable connections, but a different solution is foreseen for the final system, i.e. plug in connections, in

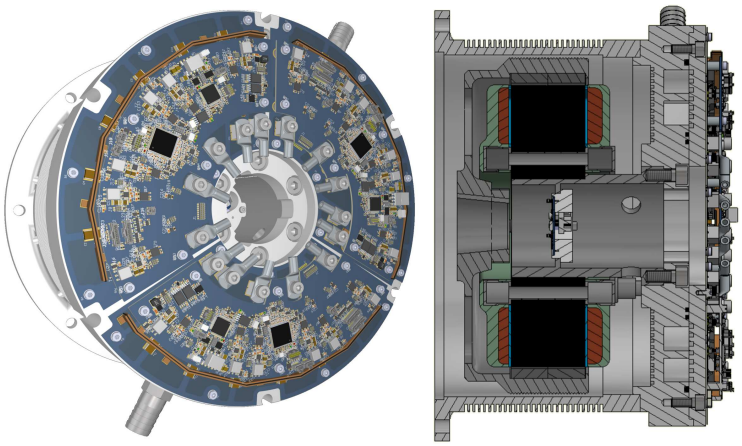


Figure 9.2: The integrated HFCMs mounted on the back side of the electric machine (left), and side section of the electric machine (right).

order to allow a simple and fast assembling of the HFCMs.
The right side of the same figure shows a side section of the assembly, where the external rotor of the electric machine, the stator core and windings and the HFCMs are visible. The shaft of the ICE is directly coupled to the rotor of the electric machine, allowing to satisfy the needed equivalent inertia without any additional rotating mass, and reducing the requirements of additional bearings. Also, an interesting solution for accurate position measurement of the rotor shaft is adopted, based on a magnetic encoder (unless a sensor less approach is adopted). A small magnet is mounted on the shaft termination of the ICE and a custom designed board hosting the encoder electronics is embedded inside the stator cavity, as visible in the figure. This solution allows a low cost contactless and high resolution (12-bit) position measurement, being also compatible with the temperature and vibration ratings of the ICE and easy to manufacture. A cable is routed in the center right cavity of the stator allowing the connection between the encoder board and HFCMs.
The internal combustion engine has been designed and optimized to meet size, weight, efficiency, and limited pollution and noise specifications. A photograph of the prototype is shown in Fig. 9.3 and main parameters are reported in Tab. 9.1.

Figure 9.3: Prototype of the internal combustion engine.

Preliminary power and torque measurements as a function of the speed have been done on a dedicated test bench, leading to the results drawn in Fig. 9.4. The peak power is about 20 kW

Table 9.1: ICE specifications

Architecture	Boxer
Number of cylinders	2
Displacement	500 cm^3
Rated speed	4000 rpm
Rated power	22 kW
Bore	72 mm
Stroke	61 mm
Fuel	Gasoline or methane
Cooling	Liquid

at the rated shaft speed of 4000 rpm in the tested conditions. However, additional tests are on going to optimize the control of the ICE in order to increase the achievable power rating and completely meet the project specifications.

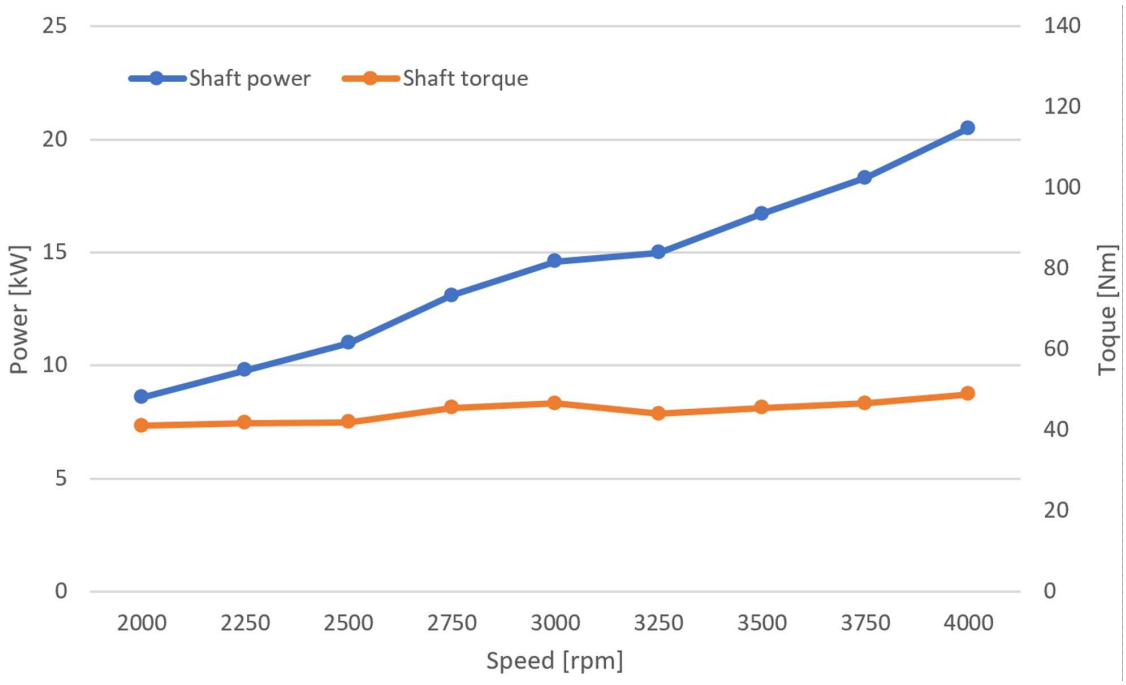


Figure 9.4: ICE power and torque characteristics.

The electric machine is an external rotor PMSM, having three sets of three phase windings (details on the next section), each one contributing with on third of the overall torque. The presence of more than one three phase winding enables the possibility to split the power converter into three smaller units, leading to a reduced volume requirement, each one designed to supply one third of the current of the equivalent single three-phase machine and sharing a common dc bus, i.e. the vehicle battery.

A photograph of the actual prototype of the machine is shown in Fig. 9.5, in a disassembled form. In the top figure the magnetic encoder board is also visible in the internal cavity of the stator. In the bottom figure, the rotor structure is shown. The permanent magnets have been skewed in order to reduce cogging torque that, for the particular choice of the stator slots and rotor poles, is non negligible. The rotor shaft is also visible, with the small magnet needed for the position measurement mounted on its end side. Main parameters of one three phase module of the machine are reported in Tab. 9.2.

The ac dc converter is a three-phase inverter whose rated switching frequency is 40 kHz (this

Table 9.2: SPMSM rated parameters (one module)

Pole pair p_p	4	#
Rated torque T_n	52.3	(Nm)
Rated speed n_m	4000	(rpm)
Rated phase current I_n	21.7	A_{rms}
Phase inductance $L_d = L_q$	1.76	mH
Phase resistance R_s	40	$m\Omega$
PM flux linkage Λ_{mg}	95.5	mWb

value is however depending on the efficiency of the cooling circuit), in order to take advantage of the specific features of SiC power devices and to speed up the control rate allowing to have a more efficient control of the machine currents and to compensate for the higher order back EMF harmonics. Adoption of SiC technology allows also to extend the operating voltage range of the convert to cope with very high voltage levels found in very recent electric vehicles. Main parameters of each HFCM are reported in Tab. 9.3.

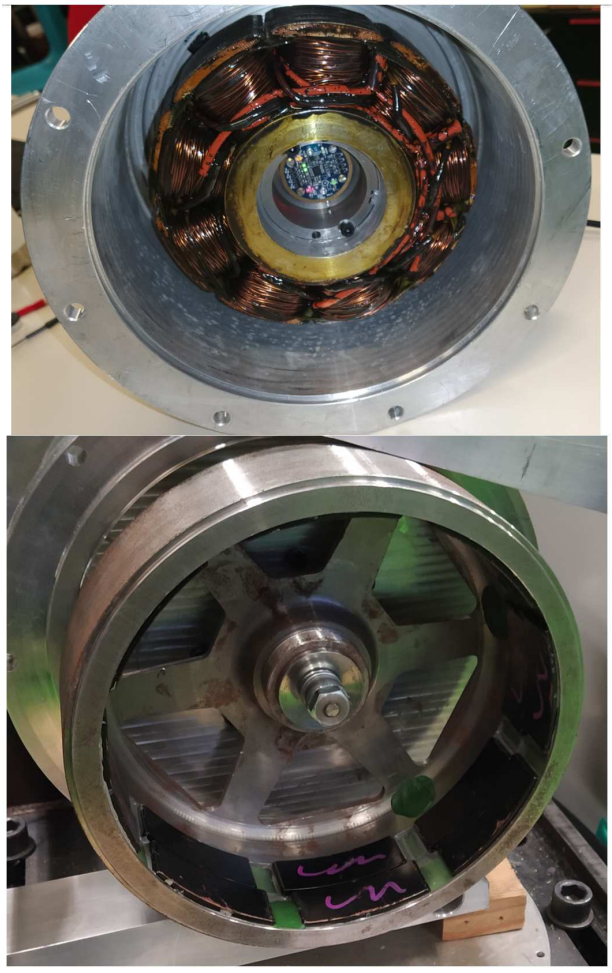


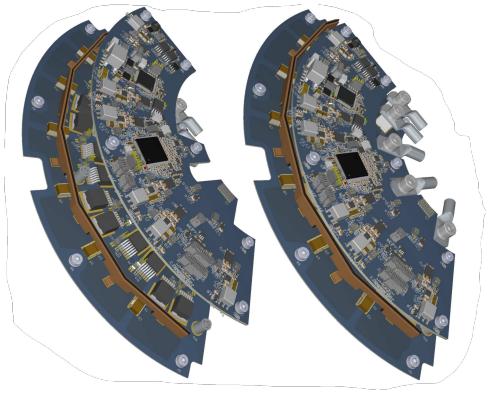
Figure 9.5: Prototype of the electric machine: stator (top) and rotor (bottom).

Each module of the HFCM features a very compact and modular structure and is formed by a stack of a control and a power board, as shown in the renderings of Fig. 9.6a. The configuration on the left is before the plugging in of the two boards, whereas the one on the right is the final assembly. The shape of the boards has been designed in order to have the possibility to mount three identical sets 120 degrees rotated ones another, in order to obtain the required multi three

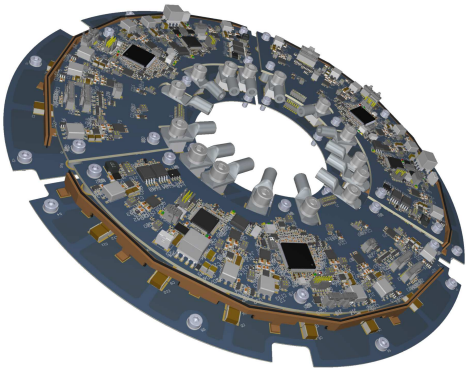
Table 9.3: Power converter module specifications

Rated DC-bus voltage U_{DC_nom}	400	V
Maximum DC-bus voltage U_{DC_max}	1000	V
Maximum DC-bus (battery) current I_{bat}	25	A
Maximum output phase current I_{abc}	50	A
Rated PWM carrier frequency f_{sw}	40	kHz

phase configuration, as visible in Fig. 9.6b. Redundant bottom entry connections have been adopted to reduce the assembling effort and time/costs, and to guarantee a certain level of fault tolerance in the automotive environment.



(a) HFCM: disassembled and assembled power and control boards.



(b) HFCMs: complete assembly three module sets.

Figure 9.6: HFCM 3-D views

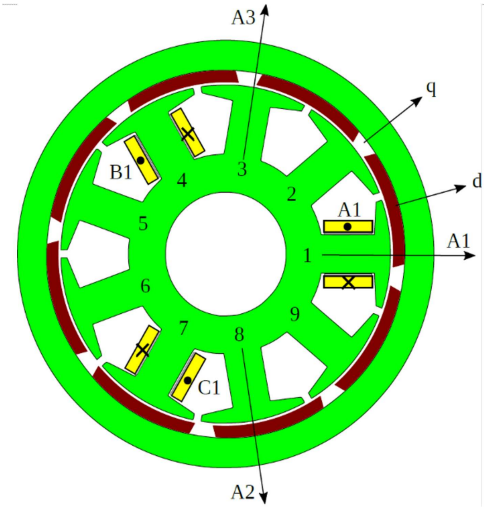
The power board is realized by an insulated metal substrate (IMS), to allow an efficient dissipation of the converter losses through the cooling plate of the machine, and hosts the SiC power MOSFETs, some passive elements and interconnections (for power, gate driving and measurements). A custom designed circular bus bar is adopted to distribute the dc bus to all the three legs of the inverter, allowing a compact solution, and reduction of the parasitic inductance and losses. Only high voltage ceramic capacitors are used, allowing to increase the reliability of the system and reduce the space requirements with respect to a classical solution based on electrolytic technology.

The control board is realized by a standard 4-layers FR4 substrate and host the μCs (both the machine control and communication with the vehicle via CAN bus), the gate drivers and related insulated power supplies, and communication devices. Additional connectors are present for the magnetic encoder, logic power supply and communication.

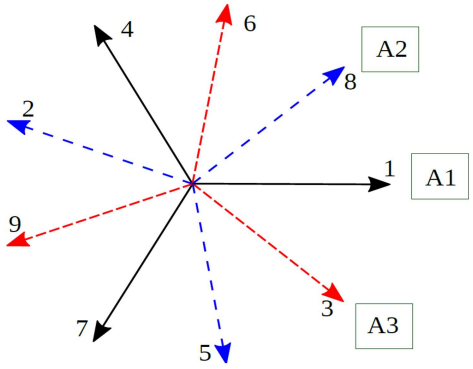
9.2 Design and analysis of the electrical machine

The designed electrical machine is an outer rotor PMSM, featuring 8 rotor poles and 9 stator slots. The outer rotor provides higher torque density and increases the rotor inertia, allowing to meet the value required by the ICE without any additional rotational mass. The three three phase modules of windings will be referred as M1, M2 and M3. Fig. 9.7a shows the coil distribution of the first module, which are labelled as A1, B1 and C1. The A1 axis is considered as the reference axis of the stator. The position of the axis of the phase A2 and the phase A3 are also drawn, as well as the quadrature magnetic axes d and q. Fig. 9.7b represents the star of slots, the slot angle being 40 mechanical degrees and 160 electrical degrees. The star of slot shows the vector of the voltage induced in the different coils of the winding, allowing a rapid analysis of the electrical angular shift of the coils. Starting from the star of slot, the coils of the three systems are chosen:

- the first module is formed by the coils wound around the teeth 1, 4 and 7;
- the second module by the coils wound around the teeth 8, 2 and 5;
- the third module by the coils wound around the teeth 3, 6 and 9.



(a) Electric machine structure and dq reference system for module 1.

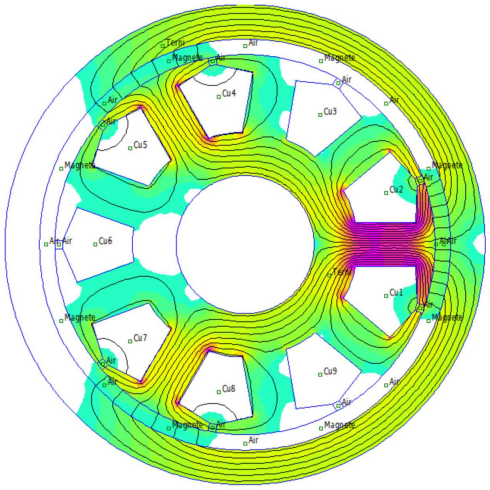


(b) Star of slots.

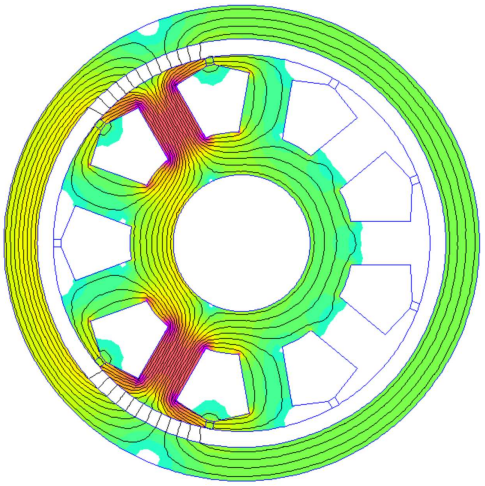
Figure 9.7: Electric machine structure and star of slots

Fig. 10 and Fig. 11 show the flux lines when only a single three-phase module is fed (M1). The magnets have been removed to highlight only the flux due to the currents. Fig. 10 corresponds to the rotor position $\theta_{mech} = 0^o$, with maximum A1-phase current (B1 and C1 opposite and with

half amplitude with respect to A1) while Fig. 11 corresponds to the rotor position $\theta_{mech} = 22.5^o$, with zero A1-phase current and the other two opposite and with half amplitude. From the figures it is possible to evaluate the mutual coupling among the modules. The flux lines are mainly from the stator to the rotor, but there are also lines that pass over the teeth corresponding to the other modules which are the lines of leakage flux between adjacent tooth tips.



(a) M1 fed with 0^o mechanical rotor position.



(b) M1 fed with 22.5^o mechanical rotor position.

Figure 9.8: FEMM simulations of electric machine

9.3 Architecture and limitations

The choice of the most appropriate conversion architecture for the considered application was investigated prior to the design and prototyping phase. The selection was driven by the analysis of a standard electric vehicle power architecture, as sketched in Fig. 12. The high voltage battery is connected to a series of electronic sub systems, aiming at specific conversion functions:

- supply the low voltage network of the vehicle (i.e. 14 V) by means of a dedicated dc dc converter; this solution is normally adopted in order to allow re use of standard auxiliary components on the market and adopted in standard vehicles; in some applications this converter is bi directional to allow power exchange between the two batteries;
- allow vehicle charging from the distribution grid, e.g. the on board charger; also in this

case, bi directional solutions are more and more investigated to allow e.g. vehicle to grid (V2G) operations and integration of the vehicle into microgrid systems;

- feed the traction inverter; this subsystem is normally bi directional to allow regenerative braking;
- allow re charge of the main battery of the vehicle when needed, using the RES.

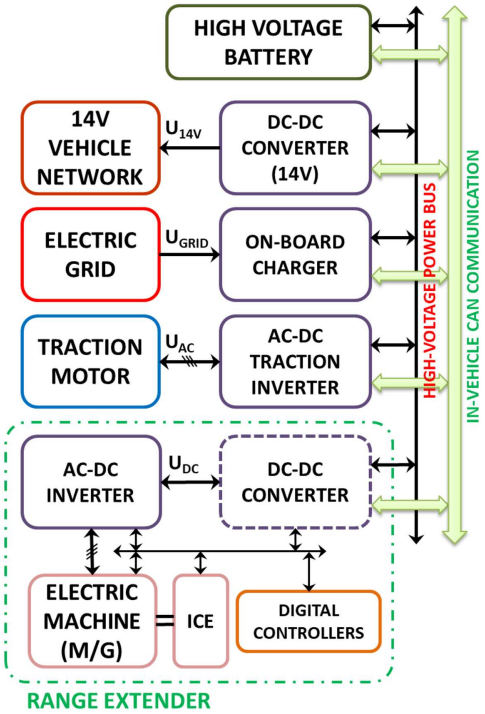


Figure 9.9: Standard electric vehicle power architecture.

The output voltage range of the battery packs of modern electric vehicles can be extremely wide, due to the specific features of adopted chemical technologies and to the possible strong dependence on the state of charge (SOC). A common range for most "standard" vehicles is $250 - 420$ V, increasing up to more than 800 V for very new vehicles. All the subsystems included in the block diagram of Fig. 9.9 are specified and must guarantee correct operations within actual voltage operating range of the battery pack of the specific vehicle, i.e. they must cope with possible very wide range. In some cases galvanic isolation is requested, thus introducing additional constraints and pushing for very high power density designs.
The depicted scenario highlights how the actual battery voltage range and the adopted activation policy of the RES as a function of the SOC have a strong impact on its architecture and the adopted power conversion topologies. This is true also in the opposite direction, i.e. the adopted architecture and power conversion topologies may have a strong impact on the possible activation strategies of RES, leading to the need of a careful evaluation of the different aspects and constraints. The most simple solution is limiting the activation of the RES when the battery is almost empty, i.e. its output voltage is very low and close to the minimum value. Alternative and more complex activation strategies may be considered, e.g. taking into account an accurate planning of the residual trip of the vehicle and a proper coordination of the RES based on traffic limitations in specific areas included in the trip route. In this second scenario, the battery state of charge at the time of RES activation may be far from the minimum one and the corresponding battery voltage even relatively high. The RE sub system block diagram reported in Fig. 9.9 (dashed box) highlights that one or two power converters may be adopted for interfacing the electric machine of the RES with the high voltage battery. Bi-directional operation is normally

required when the electric machine is also asked to start up the ICE. The two stage solution allows an almost complete decoupling between the electric machine design (and ICE operating speed) and the level of the high voltage battery, thus allowing a simple implementation of whatever activation policy. The intermediate dc bus at the output of the ac dc converter (e.g. a simple inverter) may be designed as high as to handle every level of the battery voltage with buck operation of the dc dc converter. This solution exhibit three major drawbacks with respect to the single stage solution due to the presence of two series power converters, i.e. a possible limited efficiency, the need of quite big passive components for the dc dc stage and higher complexity and cost. An alternative design option is to consider a low voltage intermediate dc bus at the output of the ac dc converter, thus requiring a boost topology for the dc dc stage. Similar drawbacks may be highlighted, as in the previous case, with the additional remark that a low voltage machine needs to be considered now with a possible strong impact on the efficiency of the dc ac stage due to the higher ac currents. Therefore the two stage solutions was not considered for the design of the RES reported in this paper. On the other hand, the adoption of a single ac dc converter introduces a strong constraint on the design of the RES electric machine and the converter itself, and a proper control strategy, possibly involving the ICE, needs to be introduced. A first simplifying hypothesis is considered, i.e. ICE is operated at constant speed (this leads to a number of advantages, i.e. limited pollution, vibration and noise, and higher efficiency). The main issue is that the dc voltage level (corresponding to the battery voltage, in this case), should be enough high to allow a proper control of the machine currents (i.e. to control the braking torque), meaning that the ac dc converter is always operated in boost conditions. The design of the electric machine windings (i.e. the phase voltage) should be done to allow the boost operation whatever the level of the battery voltage. Designing a machine with low phase voltage would assure a proper operation of the ac dc converter even at very low state of charge of the battery, at the cost of increasing losses in the converter due to higher currents. On the other hand, designing a machine with a high phase voltage would reduce the phase currents, but a higher battery voltage must be guaranteed for a proper converter operation. Therefore, a trade off is present between actual machine design, and ICE speed and battery voltage, preventing RES activation in certain operating conditions unless additional control strategies are considered. In this second scenario, two possible remedial strategies can be adopted to preserve RES operation, i.e. controlling (specifically reducing) the ICE speed when battery voltage is enough high (even modulating the speed as a function of the battery voltage), or implementing a flux weakening strategy for the machine, in order to keep the phase voltage enough low even at rated ICE speed. Each solution is featuring specific advantages and limitations. Controlling the ICE speed below the optimal design condition would increase noise and pollution, possibly introducing undesired vibrations and reducing the efficiency and the output power, exhibiting a relatively low implementation effort. A proper design of the machine may allow a certain flux weakening range with a limited implementation effort, but reduces the power factor and the available output power (unless a certain oversizing is considered, with an impact on the ac dc converter too). The validity of the discussed strategies rely on the analysis of the voltage to SOC characteristic of a common battery, i.e. the voltage in the first part of the charging profile (i.e. at very low SOC) is very steep and the required energy is relatively low. Therefore, the remedial strategies need to be applied for a limited amount of time and should be preferably assisted by a proper limitation of the traction power for the vehicle in that period. An analysis has been done in this paper to identify the actual allowed steady state operating range of the electric machine (in terms of shaft power) for a variable speed and battery voltage level, starting from the calculation of the electrical speed limit expression Eq. (9.1)

$$\omega_{me} = \frac{-\Lambda_{mg} R_s I_q + \sqrt{\Lambda_{mg} R_s {I_q}^2 - \left[{\Lambda_{mg}}^2 + (L_q I_q)\right]^2 \left({R_s}^2 {I_q}^2 - \frac{{V_{bus}}^2}{3}\right)}}{{\Lambda_{mg}}^2 + (L_q I_q))^2} \tag{9.1}$$

where R_s, Λ_{mg} and L_q are the machine phase resistance, q-axis inductance and permanent magnet flux linkage amplitude respectively, V_{bus} is the converter input voltage (battery voltage) and I_q is the steady state current, under the hypothesis that the machine is isotropic and maximum torque to Ampère (MTPA) control is considered. Flux weakening operations are not considered in this analysis.

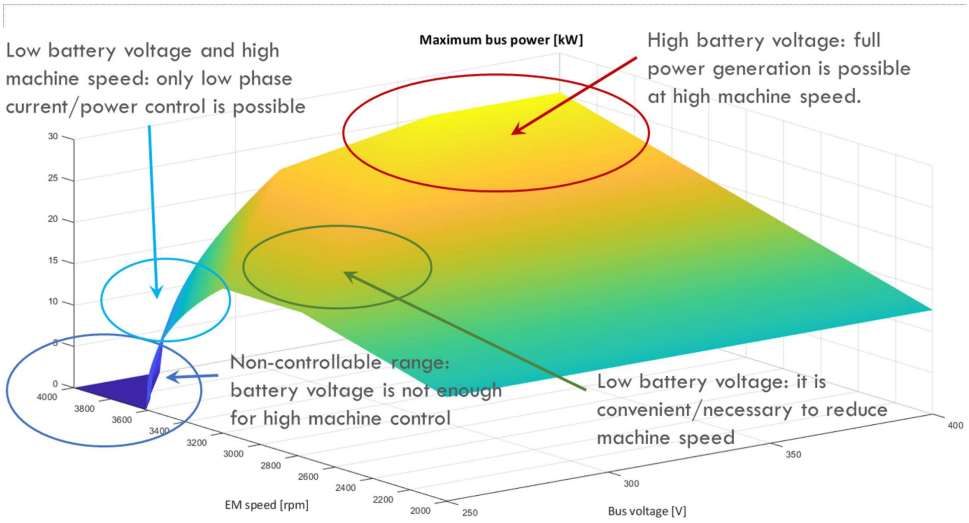


Figure 9.10: Electric machine maximum shaft power as a function of speed and battery voltage.

The results are shown in Fig. 13 for the actual design parameters of the system. Three main zones can be identified.

High battery voltage ICE speed can be controlled to the rated value and full power can be delivered to the battery.

Low battery voltage It is convenient/necessary to reduce the ICE speed or to apply a flux weakening strategy to allow proper control of the machine currents; delivered power is progressively reduced; a strong reduction is obtained if the speed is kept enough high.

Non controllable range Battery voltage is not enough and ICE speed is too high.

9.4 Simulation results

A complete model of the range extender system has been implemented to verify the effectiveness of the proposed solution, both in the ICE startup phase and in the battery charging operation. An accurate dynamical model of the ICE was built for simulating the actual pulsating torque shape as a function of the rotor position and speed. The model has been fine-tuned based on accurate mechanical simulations of the engine, verified by measurements on the actual prototype. The shaft torque as a function of the crank angle is shown in Fig. 14 for two different values of the shaft speed, i.e. at standstill (to simulate the ICE startup phase) and at rated speed. The implemented model allows to simulate all the different speed conditions in between dynamically. It is easy to verify that the peak starting torque is below the rated torque of the machine.
A limited number of simulation results are reported in Fig. 9.12, aiming at showing system behavior under different speed and battery voltage conditions, to verify the discussed operation limits and identify relevant control variables, e.g. the phase current amplitude and shaft power. In the figure, the following configurations are illustrated: 400 V at 4000 rpm; 300 V at 4000 rpm; 300 V at 3500 rpm; 260 V at 3200 rpm. Electric machine torque, ICE torque and ICE speed are reported in the left diagrams, whilst reference and actual phase current amplitude, and electromagnetic torque are reported in the right diagrams. The ICE startup, acceleration towards the

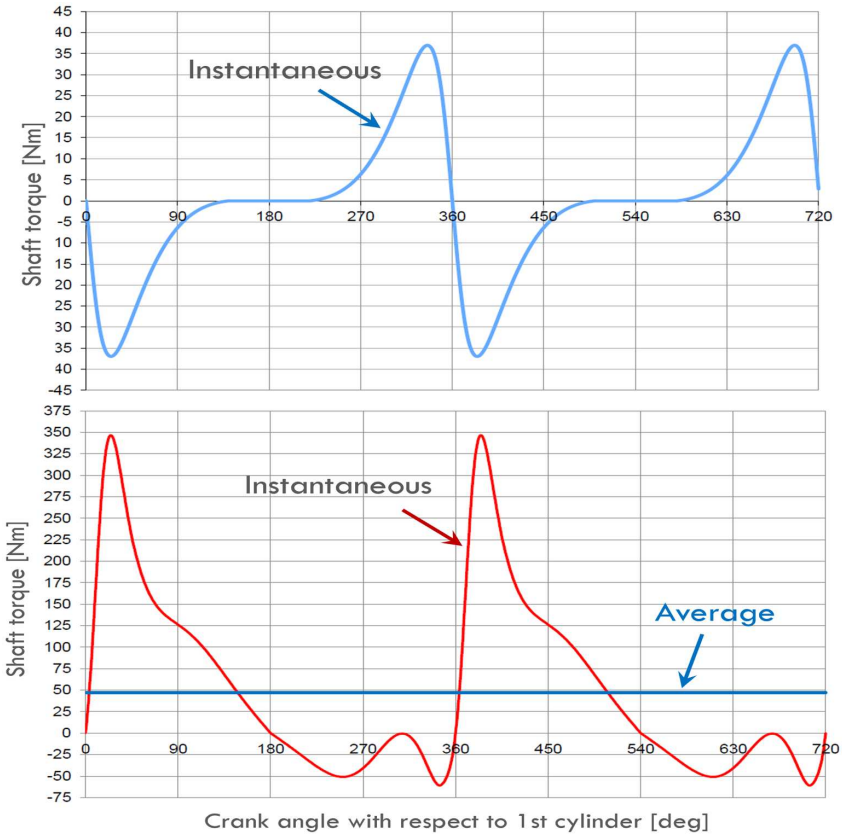


Figure 9.11: Torque characteristic of the ICE as a function of the crank angle: standstill (top) and rated speed (bottom).

speed setpoint and charging operations are identified with vertical bars. Limit operating current and torque conditions are also highlighted with red and green crosses respectively. Speed control is lost when the machine voltage reaches the inverter limitations.

9.5 Control of multi-three phase machines and related simulation results

Since the machine sets are magnetically coupled with one another, flux current on one three-phase set leads to flux-linkage on the others. For this reason, a standard control strategy, where each module is independently controlled with a conventional vector control, could lead to interference between the control action on different modules, resulting in non-optimal torque transients and to an unbalanced operation of the three modules when the parameters are slightly different. A recently proposed technique allows to overcome this issue, introducing the requirement of real-time communication between the control modules [140, 141]. The two control strategies will be referred to as independent control and coupled control in the next subsections.

9.5.1 Independent (coupled) control

In this case, one of the three controllers (designated as "master") receives the reference speed from a higher-level control unit (i.e., via CAN communication) and synthesizes the current (or torque) reference, which in turn will be sent to the other two control units so that each controller can impose their respective torque. There are mainly two ways to do so, here explained.

- the master controller sends equal torque reference values to each module (one third of

the total), which in turn computes phase voltages independently. This technique ensures balanced current sharing equally split among the three magnetic sets.

- the master controller computes the reference voltage as a result of its local current loop, then sends the reference voltage to the slaves, which will be applied by means of each PWM modulator. This solution gets rid of computational burden (only one unit will compute speed and current loop) but does not ensure equal current sharing among them.

The independent control technique is not optimal in case of magnetically coupled machine, since the different current loops interact one another due to the inherent characteristic of the motor, unless the centralized speed and current control is considered, which has the problem of not guaranteeing the current sharing.

9.5.2 Decoupled control

The currents in every set are used to compute a common-mode (average) and $N-1$ differential modes (in this case, 2 differential modes, being N equal to the number of three-phase sets, hence 3). This transformation allows to obtain a set of three linearly independent equations; hence three independent controllers can be adopted in order to control the reference torque, [18, 146].
In the simulation results of Fig. 9.13 and Fig. 9.14 two different scenarios are proposed in the case the inductance of one M1 is reduced, with and without differential mode control, respectively. In the first case (Fig. 9.13), the currents flowing in the three sets are not equally shared due to the unbalance and the torque provided by each module is not the same, eventually introducing magnetic pull in the machine. The same condition has been considered in Fig. 9.14, where the differential mode controller has been enabled, and all the currents in the three modules are now balanced.
In the simulation results of Fig. 9.15 and Fig. 9.16 the independent control (option a) has been considered, also in the case the inductance of one M1 is reduced. The results of Fig. 9.15 are showing how, in steady state conditions, the phase currents of the three modules are correctly split among the modules, as independent current control assures that each module is controlled by the same current reference. Nevertheless, when speed and torque transient conditions are considered (Fig. 9.16), the decoupled control exhibits better dynamical performances and faster response. The highly pulsating load torque of the ICE will have a detrimental effect on the current control of the machine unless decoupled control is adopted.

9.6 Experimental setup and results

The effectiveness and operation of the developed drive system has been verified in a laboratory test bench. It is equipped with a high accuracy torque meter and an auxiliary machine/drive is adopted to emulate the behavior of the ICE during the start up as well as the generation phases. The RES electric machine was hosted in a proper structure to allow connection to the test bench through a standard shaft. A 15 kW bi-directional power supply was used to emulate the battery and a chiller was adopted to keep a controlled temperature of the coolant in the cooling circuit during the tests. The RES system is controlled via CAN bus through a specifically developed human machine interface. Selected photographs of the overall system are shown in Fig. 9.19.
Preliminary tests of the RES in the single three phase as well as multi three phase configuration have been done up to 2200 rpm, due to a limitation of the mechanical structure hosting the electric machine. Therefore, the maximum generated electrical output power that was possible to test was limited to about 8 kW, as visible in the screenshot of the power supply interface in Fig. 9.20. The shaft power in that condition was about 1 kW more, due to non-negligible losses of the mechanical structure hosting the machine. Correct start up of the emulated ICE

controlled at nominal load torque and transition to generation mode was also tested, confirming a proper operation of the system. Installation of the system on the ICE and preliminary tests are on going.

9.7 Conclusions

A novel architecture has been proposed for range extender systems, based on an integrated multi three phase PMSM and high frequency drive modules employing SiC power devices. System architecture and concept, design of relevant elements, including the power and control electronics, and the electric machine machine, have been discussed, and the actual prototype was shown. A proper decoupling control strategy has been introduced to cope with magnetic coupling of the machine, requiring a real-time communication among control modules, and relevant simulation results have been reported demonstrating the feasibility and effectiveness of the proposal. Extensive simulations and experimental results of the complete system on a laboratory test bench were reported. Installation and testing on the ICE is on going.

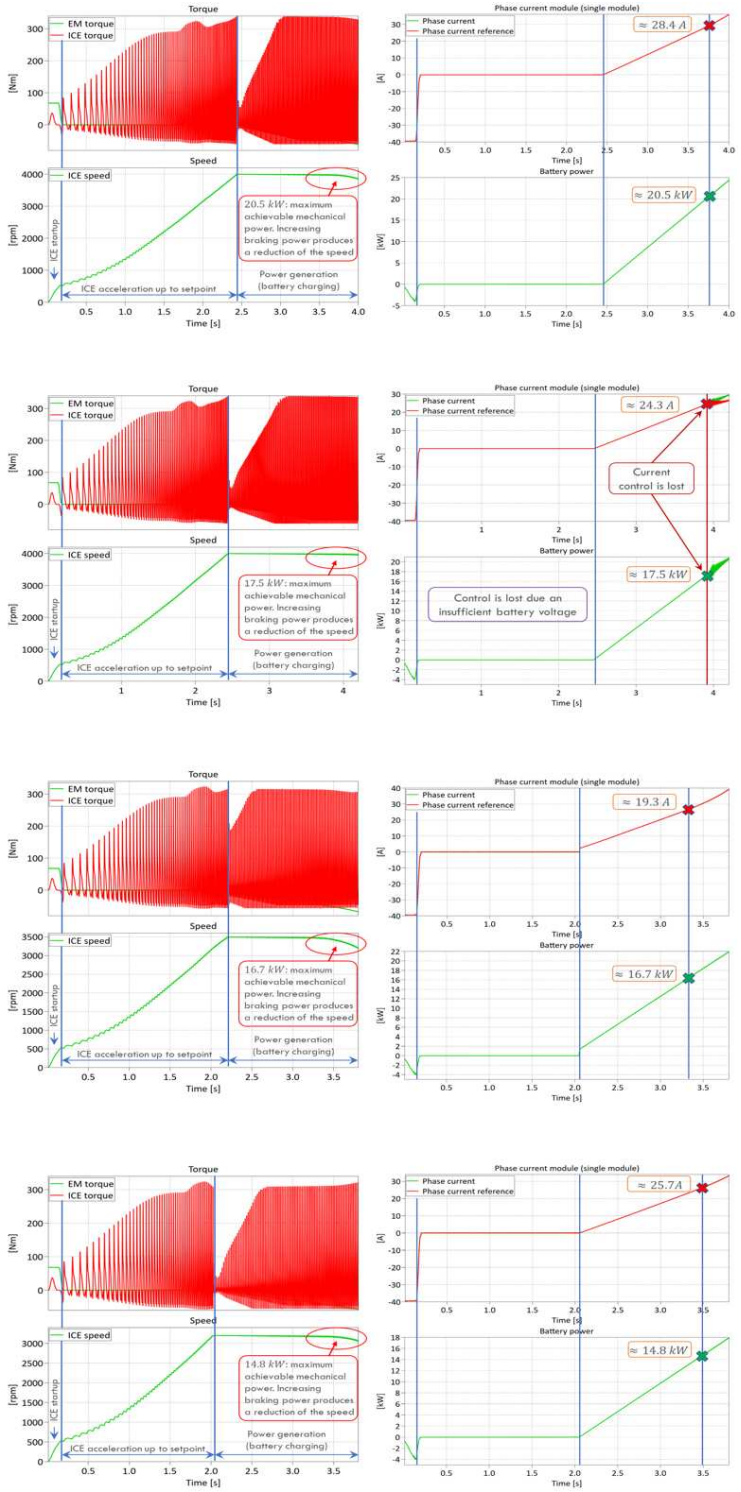


Figure 9.12: Startup and battery charging at different speed and battery voltage.

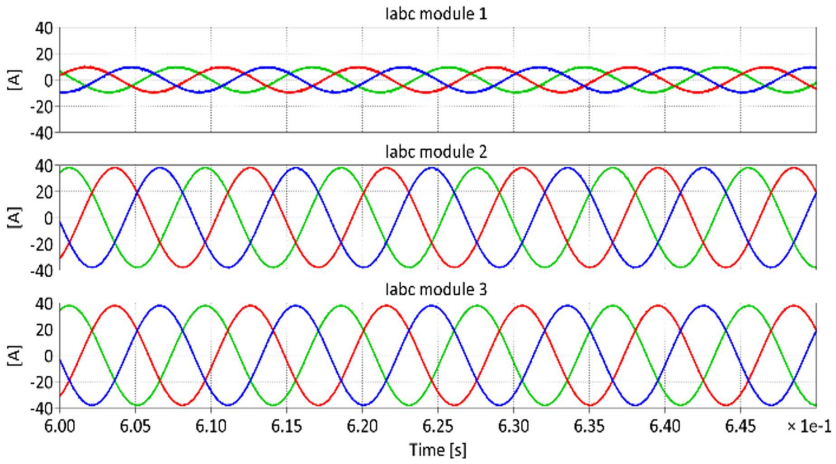


Figure 9.13: Decoupled current control when the differential mode(s) control is disabled.

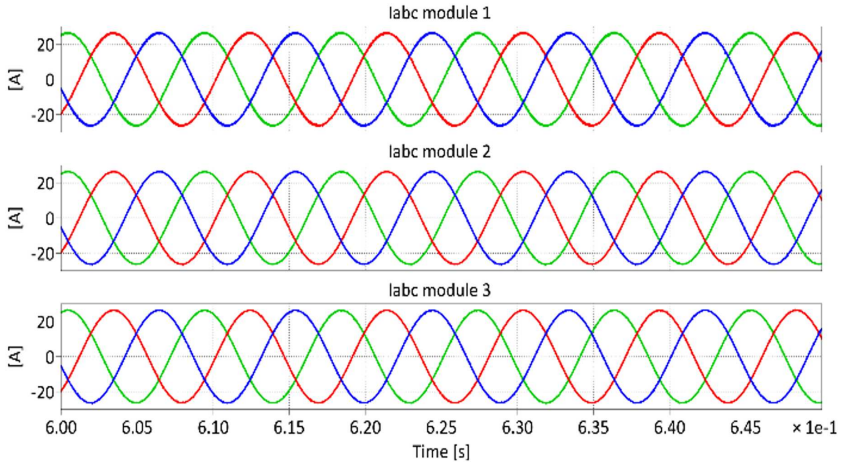


Figure 9.14: Decoupled current control when the differential mode(s) control is enabled.

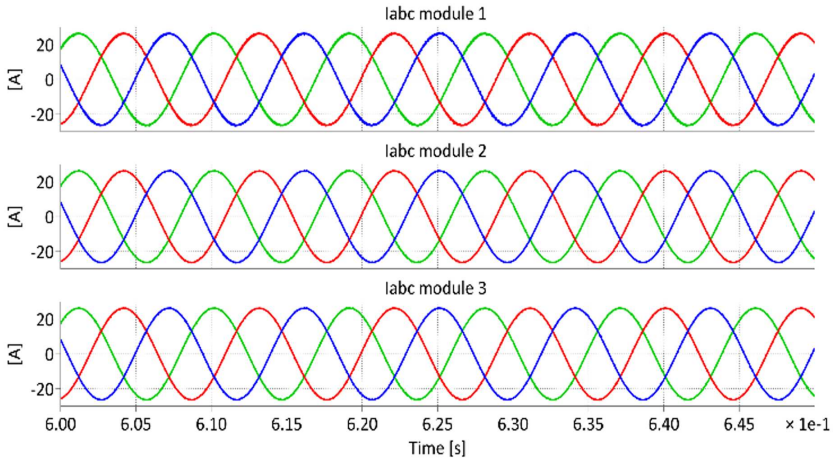


Figure 9.15: Independent (coupled) current control under unbalanced conditions.

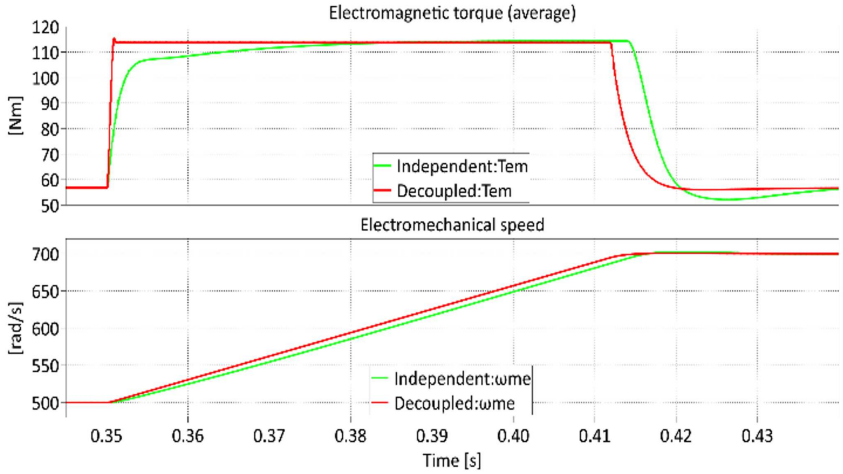


Figure 9.16: Speed and torque transient for independent (coupled) current control under unbalanced conditions.

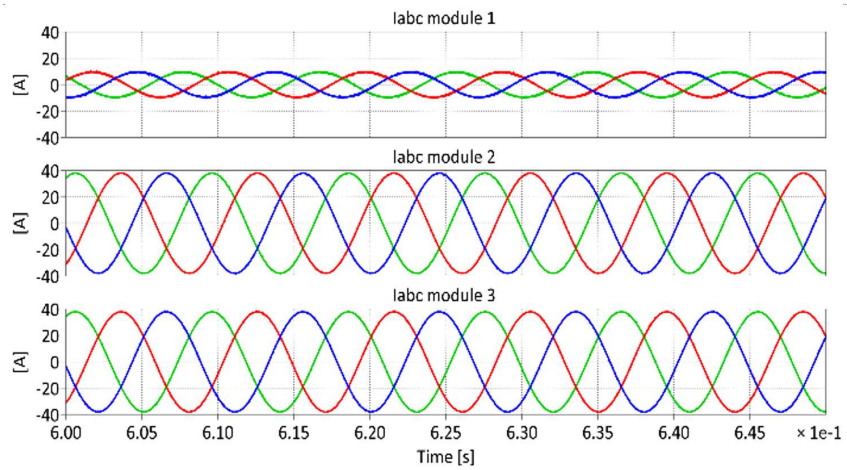


Figure 9.17: Decoupled current control when the differential mode(s) control is disabled.

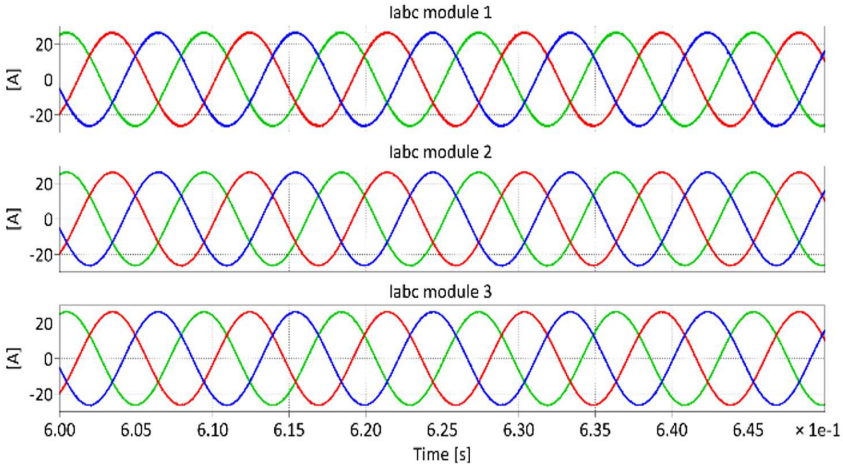


Figure 9.18: Decoupled current control when the differential mode(s) control is enabled .

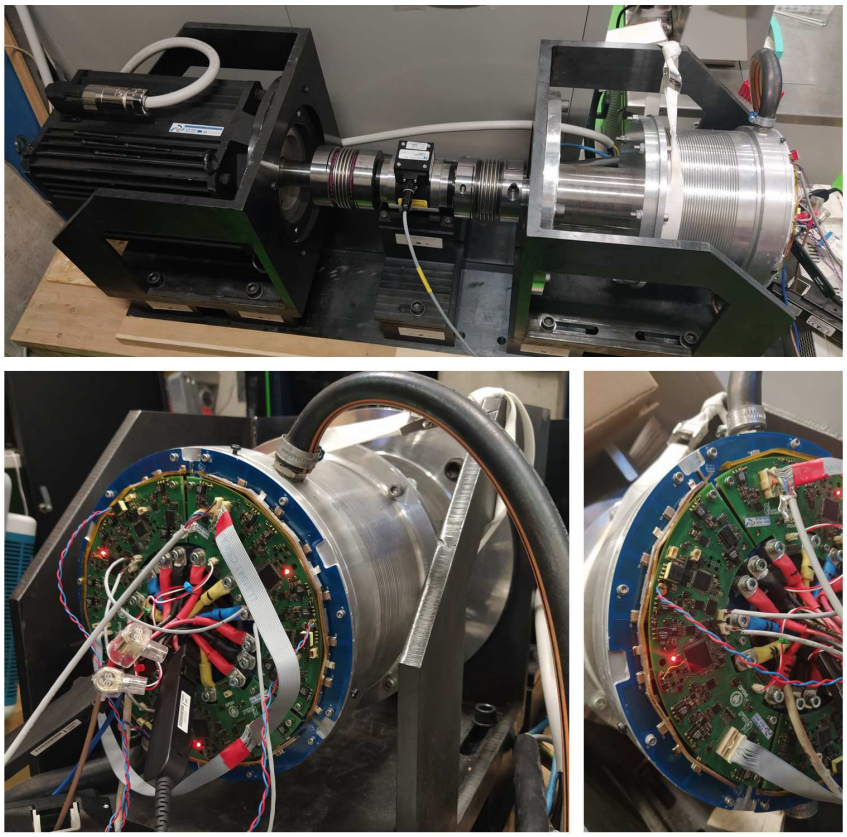


Figure 9.19: Photographs of the laboratory test bench.

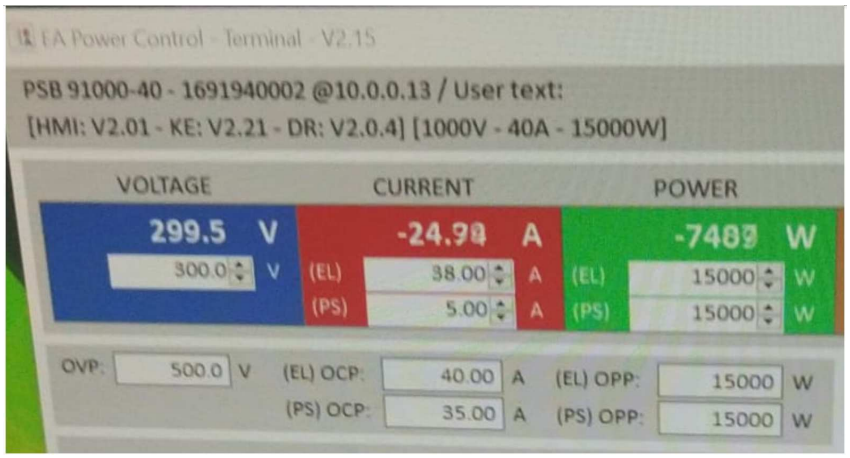


Figure 9.20: Screenshot of the power supply interface emulating the battery during the tests.

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