

# Revisiting Piezoelectric FETs with Sub-Thermal Swing

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A subthreshold swing ( $SS$ ) below 60 mV/decade at room temperature is a critical requirement in CMOS transistors for ultralow power electronics. In the past decade, tremendous efforts have been made to explore new switching mechanisms overcoming the Boltzmann thermal limitation of traditional MOSFETs [1]. Examples include tunnel FETs utilizing band-to-band tunneling (BTBT) and the corresponding energy filtering action [2], and the negative capacitance FETs (NC-FETs) based on ferroelectric materials [3]. While TFETs have shown performance below expectations for a number of fundamental as well as design challenges [4-7], and the potentials of NC-FETs are still under intense scrutiny, additional device concepts are being proposed and investigated.

The piezoelectric FETs (Piezo-FET) is an intriguing device concept that exploits a piezo-layer in the gate stack in order to produce a strain in the transistor controlled by the gate voltage,  $V_G$ . If the strain modifies the conduction band edge (for an  $n$ -FET) so that the electron affinity increases with increasing  $V_G$ , then an  $SS$  smaller than 60 mV/decade can be achieved [8-9]. In this paper, we revisit the Piezo-FET by both providing a set of analytical, insightful expressions for the  $SS$  dependence on several material and design parameters, and reporting numerical simulations of strain distribution and IV calculations in technologically relevant device structures.

The schematic of Piezo-FET with a FinFET structure considered in this work is shown in Fig. 1, where the piezo-layer is placed between the metal gate and a second metal shorted to the source, so that the voltage drop across the piezo is  $V_G$ . The piezo material is assumed to be PZT-5H, whose parameters are reported in Table 1 [8,10-11], and the thickness  $W_{\text{pie}}$  of the piezo-layer is varied from 3 nm to 10 nm. Upon application of a positive  $V_G$ , the piezo-layer expands along  $z$  direction, thus the semiconductor in the channel is compressed, as it is shown in Fig. 2(a), reporting the numerically calculated strain distribution obtained with the COMSOL simulator [12]. The 1D analytical model utilized to calculate the stress and strain is illustrated in Fig. 2(b), where it is assumed that the  $x$  and  $y$  directions are unconstrained, so that  $T_{xx}$ ,  $T_{yy}$  components are negligible as compared to the stress,  $T_{zz}$ , along  $z$  direction. Because the device structure is assumed to repeat periodically in the  $z$  direction, the sum of the displacements along  $z$  direction for each device must be zero (see equation  $E1$  in Fig. 2). Considering the relationship between stress and strain for the metal gate, oxide, semiconductor and the piezo-layer and combining with  $E1$ , the analytical expressions for the stress and strain are obtained as shown in Fig. 2(b), which are consistent with [8]. Figs. 3(a), (b) show the stress and strain profiles as a function of  $W_{\text{pie}}$  calculated using either the analytical model in Fig. 2 or the 3D numerical simulations for (001)-oriented silicon with channel thickness  $W_{\text{fin}}$  of 5 nm at a  $V_G$  of 0.3V. It can be observed that the analytical model is in fair agreement with the numerical simulations, but, overestimates the strain for very thin piezo-layers. Maximum  $V_G=0.3V$  for minimum  $W_{\text{pie}}=3\text{nm}$  is compliant with the critical electric field  $E_{\text{cr}}=100$  MV/m for the PZT-5H. For the  $\Delta$  valleys in silicon, the strain induced modulation of the conduction band is [13]

$$\Delta E_{C,k} = \Xi_d \cdot (\epsilon_{xx} + \epsilon_{yy} + \epsilon_{zz}) + \Xi_u \cdot \epsilon_{kk} \quad (1)$$

where  $k=x, y$  or  $z$  is the longitudinal direction of  $\Delta$  valley, while  $\Xi_d$  and  $\Xi_u$  are the dilation and uniaxial deformation potentials, respectively. For silicon,  $\Xi_d$  and  $\Xi_u$  are 1.1 and 9.29 eV, respectively.

Fig. 3(c) shows the  $\Delta E_{C,k}$  calculated based on the strain shown in Fig. 3(b): a  $\Delta E_{C,z}$  of -0.126eV is obtained for the device with 3nm piezo-layer. The gate voltage controlled  $\Delta E_{C,z}$  can be included in a self-consistent top of the barrier model [14] to get the transfer characteristics for the devices with and without piezo-layer shown in Fig. 4. A steep  $SS$  of 41.9 mV/decade is achieved for the thinnest piezo-layer  $W_{\text{pie}}=3\text{nm}$ .

In order to develop an intuitive insight in the device operation, we now derive an analytical expression for  $SS$ . To

this purpose we consider an  $n$ -type, ultra-thin-body (UTB) FET (or a FinFET), assume that the inversion density  $n_{inv}$  in sub-threshold regime is carried by the lowest subband (i.e. quantum limit approximation), and thus write  $n_{inv}$  as [13]

$$n_{inv} \approx \frac{\mu_0 m_{d,0} (K_B T)}{\pi \hbar^2} \exp\left[\frac{-\varepsilon_0}{K_B T}\right] \quad (2)$$

where,  $m_{d,0}$  is the density of state mass,  $\mu_0$  is valley degeneracy,  $\varepsilon_0$  is the energy of the lowest subband. In Eq. 2 the electron gas is assumed to be non-degenerate (which is fully appropriate for the sub-threshold region) and the Fermi level is taken as the reference energy, namely  $E_F=0$ . We now recall that the electrostatic potential,  $\phi_G$ , at the interface between the metal gate and the oxide in an UTB-FET, can be written as [13]

$$q\phi_G = qV_G - (\Phi_M - \chi_{SCT}) \quad (3)$$

where  $\Phi_M$ ,  $\chi_{SCT}$  are respectively the metal work function and semiconductor electron affinity (with  $q$  being the electron charge). We further assume that  $\varepsilon_0$  in Eq. 2 moves rigidly with  $\phi_G$ , so that we finally obtain

$$\frac{\partial \varepsilon_0}{\partial V_G} \approx -\frac{\partial(q\phi_G)}{\partial V_G} \approx q \left[ 1 + \frac{\partial \chi_{SCT}}{\partial(qV_G)} \right] \quad (4)$$

where  $\Phi_M$  has been taken independent of  $V_G$ . If we now suppose that, in sub-threshold region, the current  $I_D$  changes with  $V_G$  just as  $n_{inv}$ , we finally obtain

$$\frac{\partial(\log_{10}(I_D))}{\partial V_G} \approx \frac{\partial(\log_{10}(n))}{\partial V_G} = \frac{\partial(\log_{10}(n))}{\partial \varepsilon_0} \frac{\partial \varepsilon_0}{\partial V_G} \approx \frac{q}{\ln(10)K_B T} \left[ 1 + \frac{\partial(\chi_{SCT})}{\partial(qV_G)} \right] \quad (5)$$

and consequently

$$SS \approx \frac{\ln(10)K_B T}{q} \left[ 1 + \frac{\partial \chi_{SCT}}{\partial(qV_G)} \right]^{-1} \quad (6)$$

As it can be seen, an  $n$ -type Piezo-FET can have an  $SS$  below 60mV/decade if  $V_G$  induces a strain such that  $\chi_{SCT}$  increases with  $V_G$ . Fig. 5 shows that the  $SS$  values given by the analytical model and those extracted from the numerical simulations in Fig. 4 agree well.

In conclusion, the  $n$ -type FinFET device with piezo-layer in the gate stack is investigated in this paper. The gate voltage controlled stress, strain, conduction band edge shift, and the subthreshold swing are analytical modeled. The values of  $SS$  demonstrate a strong dependence on the thickness of piezo-layer. A steep  $SS$  of 41.9 mV/decade is achieved for the device with the thinnest  $W_{pie}$  of 3 nm.

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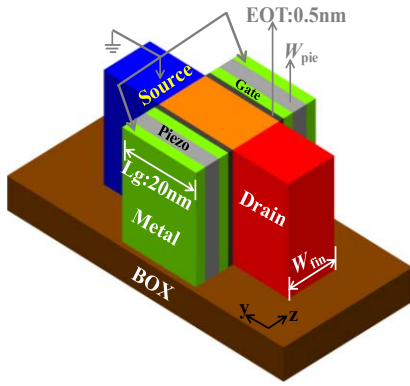


Fig.1 The schematic of Piezo-FET with a FinFET structure.

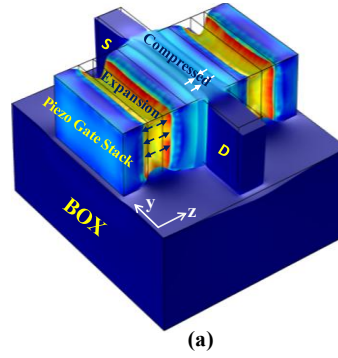


Fig. 2 (a) Numerically simulated strain distribution for the device at  $V_G=0.3V$ . The semiconductor in the channel is compressed due to the expansion of the piezo-layer. (b) Analytical model for stress and strain calculation.

The sum displacement along z direction is zero. Hence, the boundary condition:

$$E1: W_s \varepsilon_{s,zz} + 2W_{ox} \varepsilon_{ox,zz} + 2W_g \varepsilon_{g,zz} + 2W_{pie} \varepsilon_{pie,zz} = 0$$

Considering the relation between stress and strain for piezo-layer and the MOS-layer:

$$E2: \begin{cases} \varepsilon_{pie,33} = S_{33} T_{zz} + d_{33} E_z \\ \varepsilon_{M33} = S_M T_{zz} \end{cases}$$

The electric field along Z direction:

$$E3: E_z = V_G / W_{pie}$$

Combining E1, E2 and E3:

$$T_{zz} = \frac{-d_{33} V_G}{0.5W_s S_{s,11} + W_{ox} S_{ox,11} + W_g S_{g,11} + W_{pie} S_{pie,33}}$$

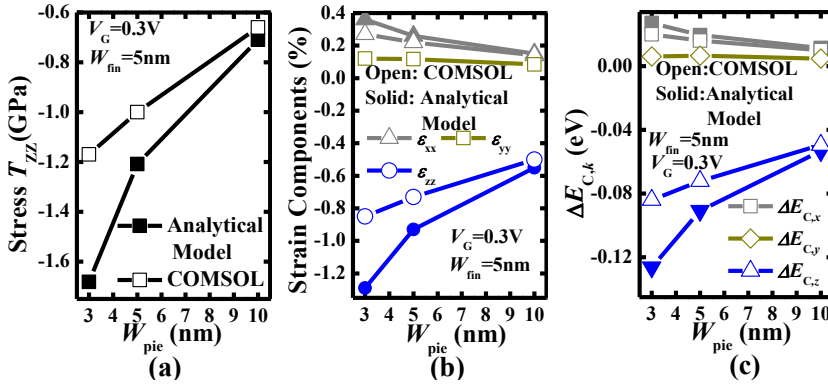


Fig. 3 Analytically modeled (solid) and numerically simulated (open) (a) stress, (b) strain, and (c) the conduction band edge shift for (001)-oriented Si as a function of the  $W_{pie}$  at  $V_G$  of 0.3V.

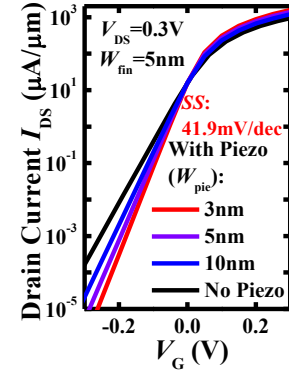


Fig. 4 The transfer characteristics for the devices with and without piezo-layer obtained with a numerical, self-consistent top-of-the-barrier current model.

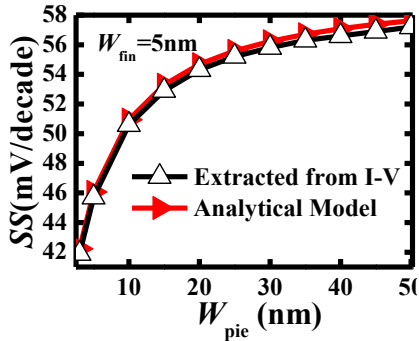


Fig. 5 The SS obtained from Eq. 6 and extracted from the  $I_{DS}-V_{GS}$  curves of Fig. 4.

Material	Parameters for stress and strain calculation							
	Elastic compliance constant, $S_{ij}$					Piezoelectric strain constants, $d_{ij}$ [ $10^{-12}C/N$ ]		
	[ $10^{-12}m^2/N$ ]					$d_{x5}$	$d_{z1}$	$d_{z3}$
PZT-5H <sup>[8]</sup>	$S_{11}$	$S_{12}$	$S_{13}$	$S_{33}$	$S_{44}$	741	-274	593
Silicon <sup>[8]</sup>	16.5	-4.78	-84.5	20.7	43.5	NA	NA	NA
HfO <sub>2</sub> <sup>[10]</sup>	7.68	-2.14	NA	NA	12.5	NA	NA	NA
TiN <sup>[11]</sup>	5.27	-1.21	NA	NA	11.4	NA	NA	NA
	1.73	-0.34	NA	NA	5.88	NA	NA	NA

Table 1. The elastic compliance constants  $S_{ij}$  and the piezoelectric strain constants  $d_{ij}$  of the materials for the strain and stress calculation.