UNIVERSITÀ DEGLI STUDI DI UDINE

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TESI DI DOTTORATO DI RICERCA

POWER DISTRIBUTION ANALYSIS IN COMPLEX SYSTEMS

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Abstract

Electronic systems are continuously growing nowadays in every ambit and application; concepts like mobile systems, domotic, wireless monitoring are becoming very common, and the reason is the continuous reduction of the energy and time needed to collect, process and send information and data to the end user.
The energy management complexity of these systems is increasing in parallel both in terms of efficiency and reliability, in order to increase the lifetime of the application and try to make it energy-autonomous, thus also the power management should not be seen only as an efficient energy conversion stage, but as a complex system which can now manage different energy sources, and ensure an uninterrupted power supply to the application.
The problems that must be overcome increase as the number of scenarios where the end applications have to be used: this thesis aims to present some complex power distribution systems and provide a detailed analysis of the strategies necessary to make the solution reliable and efficient.

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Introduction

Electronic systems are spreading increasingly in everyday applications; the developments made in all the fields of electronics, allow to several devices to efficiently and quickly interface with the user and communicate a lot of data. Also the processing and the speed at which the informations are sent, are greatly increased, this has enabled the spread of concepts like wireless networks, where different devices communicate and share data to each other. Wireless Sensor Networks (WSN), in the specific, are widely used in many areas such as health monitoring, temperature sensing, and numerous information gathering applications.
If the cost of these systems is always an issue to the mass distribution, the bottle neck, after several years from their birth, remains the energy amount needed to supply these systems, because where the grid is not available, a battery or another energy storage have to be used. This problem pushes the research in different ways:

- Realizing batteries with more energy densities, in order to store more energy in less space, but, in the same time, reducing the time needed to recharge them. The lifetime of the batteries have to be also increased, and, as explained in this thesis, due to the chemistry of the storages, the recharge process require specific current and voltage profiles that the power stage have to comply.

- Try to efficiently recharge the battery with environment energy, if possible, this can avoid the need of disconnect and recharge batteries; this concept is also known as *Energy Harvesting* or *Energy Scavenging*, and is based on the optimization of the extraction of environment energy (light, heat, wind, kinetic energy) and stored for small, wireless autonomous devices, like those used in wearable electronics and wireless sensor networks.

- Reduce the energy needed to supply the systems, and this can be done by realizing more efficient devices and optimizing the operating time of peripheral; in some cases, for instance in mobile applications, the processor communicate directly with the power management unit, in order to change its own supply voltage depending on the required speed: this can save a lot of energy. Moving towards smaller process nodes, leakage power reduction

> also becomes more significant; to stop leakage losses of an unused block, power gating puts into practice the idea of disconnecting that block from the supply rail. Modern processors are equipped with a global power grid, unused blocks can be cut off by the power management unit from the global supply, zeroing out leakage.

It is clear that the power management has not to be considered just as a simple conversion stage, but as a complex and intelligent system, which aims to optimize the overall efficiency of the devices, manage in some cases different energy sources and optimize the charge/discharge of the energy storages.

The concept of *Complex Power Distribution* is not only intended as complex system architectures, but should be extended also in scenarios out of our common environment, WSNs for example are attractive also in applications outside the typical industrial operating temperature range and conditions, in order to monitor and send data such as temperature, operating conditions of machines or motors and so on; also in these cases a fault tolerant power management system is required.

This thesis aims to provide some examples of Complex Power Distribution Systems, in order to highlight issues due to energy sources, storages and environment, and find optimal solutions for provide efficient and reliable power management systems. The work is divided in two main chapters, coherently with what introduced so far: Power Distribution Systems in Harsh Environments and Power Distribution Systems in Remote Applications.

In the first chapter an update of the LHC, which is the world's largest and highest-energy particle accelerator, is presented, and can be considered a very hard environment for electronic devices due to its temperature range, size and the presence of ionizing radiation sources. Another big problem of this environment is the presence of a huge magnetic field which can saturate all the commercial ferromagnetic inductors; all these problems leads to use air inductors and obliges to develop dedicated integrated circuit.

In the second chapter an overview of remote applications power supplies with some examples using different energy sources is presented; this kind applications, when are required to supply small energy systems, are usually known as *energy harvesting*, as previously explained. The choice of the adequate energy source and energy storage have to be made considering not also the energy requirements of the system to supply, but also environment problems such as temperature, presence during the day of the natural source to harvest and so on.

Chapter 1

Power Distribution Systems in Harsh Environments

A lot of applications need electronics able to operate outside typical industrial temperature range and conditions. Typical harsh environments are oil and gas exploration and production, undersea cabling, heavy industrial sensors, medical or jet engine sensors.

A lot of companies offer a wide range of semiconductors for use in harsh environments; these applications have special requirements for qualification, packaging and reliability, but still exist some applications where these components are even not enough reliable. One on these is the CERN Large Hadron Collider, which is the largest particle physics laboratory in the world: in the experiments the magnetic flux density is about 8 T (Tesla), the collision of the particles generates an high radiation level and the temperature variation can be from -20 to $+150$ $°C$. All the electronic components in the experiments must be tolerant to this conditions, and must also satisfy other requirements such ah the cooling capacity and the limited material budget, in order of do not interfere with the particle's experiments.

In this chapter the design strategies of an Application Specific Integrated Circuit (ASIC) DC-DC Converter for the LHC experiments upgrade are presented, in order to meet the above reliability requirements.

1.1 Large Hadron Collider upgrades

CERN is the world largest particle physics laboratory, its goal is to study the basic constituents of matter and their reciprocal interaction. The instruments needed for particle physics experiments are particle accelerators and detectors; accelerators are used to accelerate beams of charged particles up to a speed close to the speed of light, and when they have reached the desired energy, they collide with another cluster of particles coming from the opposite direction. The detector

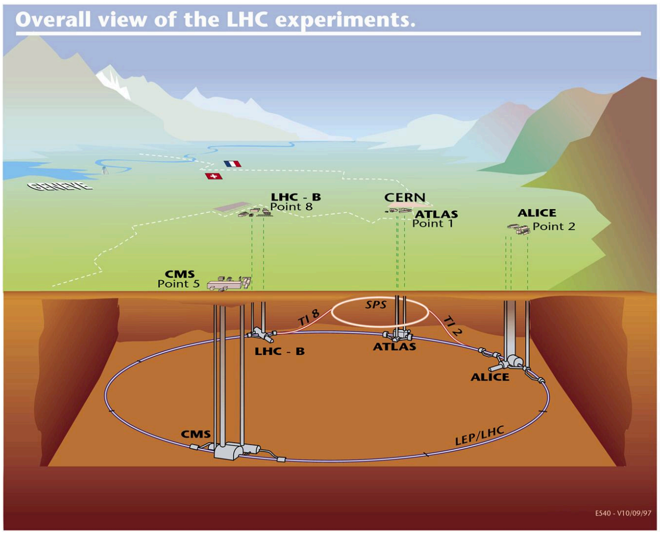


Figure 1.1: LHC experiments.

is built around the point of collision, in order to study the effects of the collision. Every detector is called experiment.
Since 2008 a new accelerator and five experiments are working and providing very important results to the High Energy Physics (HEP) community. The tunnel is burried at about 100 m underground, between the Swiss and French borders, in the outskirts of Geneva.
High energy beams are moved around the LHC ring inside a continuous vacuum, guided by superconducting magnets, which are cooled by a huge cryogenic system. Proton beams are prepared by CERN's existing accelerator chain before being injected into the LHC. Five experiments are present in the LHC (Figure 1.1):

- ALICE: A Large Ion Collider Experiment
- ATLAS: A large Toroidal LHC ApparatuS
- CMS: The Compact Muon Solenioid (Figure 1.2)
- LHCb: Large Hadron Collider beauty experiment
- TOTEM: TOTal cross section, Elastic scattering and diffraction dissociation

In the experiments two counter-rotating particles bunches enter the detectors from two opposite sides and collide head-to-head in its center, where le detector is located.
A detector is a complex system composed by several sub-detectors, organized in a cylindrical part called barrel, closed at the two ends by two end-caps. In the end-caps other detectors are present, which grants the coverage of as much solid

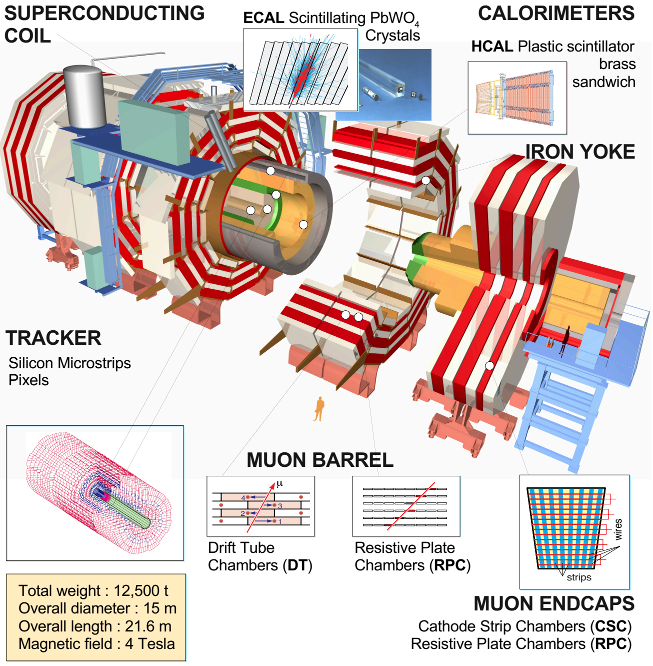


Figure 1.2: Cross section of CMS experiment.

angles seen from the interaction point as possible.

Every sub-detector has a specific task: the tracker reconstructs the trajectory of the generated particles, the calorimeters measure the energy and the muon chambers detect the muons. A part of the detector is surrounded by an electromagnet which generates a very strong magnetic flux density (up to 4 T), in order to bend the generated particle's trajectory. From the curvature angle, is possible to know the momentum and the charge sign (polarity) of the particles.

In the actual experiments, front-end circuits are reached with long cables ($> 100\ m$) that do not guarantee a stable input voltage ($2 - 4\ V$) and dissipate power in heat, increasing the cooling system's load, also because linear regulators are placed on patch panels (PP) to stabilize the input voltage.

In the future upgrades of the trackers for HLLHC (High Luminosity LHC), the HEP community will strive to further reduce the material budget and, at the same time, increase the number of the detector readout channels. Since cables and cooling are amongst the main contributors to the material budget, and they are both dependent on the amount of power burnt in the tracker, on- detector power management is necessary. It is important to both decreasing the power per function ratio of Front-End (FE) electronics, and to distribute the power efficiently.

The first objective can be reached decreasing the supply voltage, but this is not possible for the analog readout circuitry, whose design will already be challenging in the low-voltage CMOS processes in the 130 nm node or below (typical

Table 1.1: Comparison of the power requirements for the current ATLAS SCT barrel tracker and the Short Strip barrel layers of the HLLHC ATLAS tracker in the present strawman design. For the HLLHC two scenarios are compared: same voltage (1.2 V) or different voltages distributed to analog and digital circuitry in the FE ASICs

	SCT barrel	HLLHC SS barrel
N of layers	4	3
Min and Max R [cm]	30.51	38.60
Barrel length [cm]	153	200
N of FE ASICs	25000	173000
Active Power [kW]	11.6	16.2 (1.2 and 0.9 V), 20.3 (1.2 V only)
Load Current [kA]	2.75	17.2

maximum Vdd around 1.2 V), and it's also not possible in the optoelectronics components, where the minimum required voltage is 2.5 V; this can be done only in the digital circuitry, where the supply voltage can be decreased below 1.2 V.
The above considerations lead to separate analog and digital power supplies to be provided to HLLHC trackers: a 2.5 V line for the I/O and 1.2 V or less for the core; on the other hand the presence of two voltages on-chip is a normal feature of the advanced commercial digital circuits and is commonly supported by CMOS technologies.

The number of power domains is not sufficient to draw a specification for the power distribution system without an estimation of the required current. Although the design of FE readout circuits for HLLHC trackers is still in a very preliminary phase, a projection based on available estimates can be very useful. The following projection refers to the ATLAS tracker, for which an estimation for both analog and digital power consumptions exist [1]. In Table 1.1, the projected needs for a portion of the tracker, the Short Strips barrel detector, is compared to the barrel SCT detector which is currently installed at comparable radius. In the table, we call active power the total power actually consumed by the electronics. The basic assumptions for the projection are:

- Current for the analog readout circuit: 130 μA/channel
- Total current for the on-chip digital circuitry: 80 mA
- 128 channels in each FE ASIC
- 20 FE ASICs per hybrid
- Only FE readout ASICs are considered

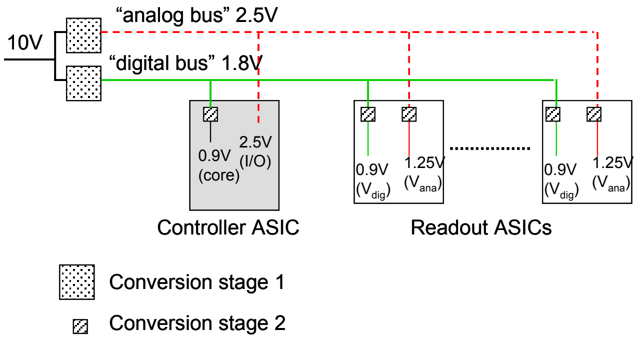


Figure 1.3: Power distribution scheme provides multiple voltages to the controller and readout ASICs from a single 10 V bus.

As can be seen, the current to be provided to the load increases by a factor of 6; since the power lost in a cable is proportional to the square of the current, this implies a 36-fold increase in losses if the power distribution system remains the same as today. Second, a large amount of power is wasted (about 4 kW out of 16 kW, or 25%) if the distribution system is unable to provide different voltage domains for analog and digital circuitry. It is clear that, to be efficient, the new distribution system has to reduce the current in the cables from the power supplies (off-detector) to the hybrids, and has to support the distribution of two different voltages.

In applications such computing and networking, power is generally distributed using AC-DC and DC-DC converters. A first AC-DC stage, converts power from the main grid, to an intermediate bus voltage, where Point of Load (PoL) converters finally supply the circuitry. The low voltage required by the load is hence produced close to it, the required power being distributed at higher voltage ($P = V \cdot I$).

A similar approach could be used to distribute energy in HLLHC trackers, such scheme is also capable of locally providing different voltage levels through the integration of different converters on the hybrid.

Figure 1.3 shows the power distribution scheme, where two DC-DC converters are used: a conversion stage 1 on stave or hybrid provides two intermediate bus voltages: an "analog" 2.5 V and a "digital" 1.8 V. These buses locally run across one hybrid or a few neighbour hybrids. A second conversion stage, integrated on-chip, acts as a divider by 2 to supply the required voltage to the analog and digital circuitry on both the controller and readout ASICs. The overall conversion ratio achieved is closed to 10, for a comparable decrease in the current on the 10 V line coming from the off-detector power supplies.

A possible implementation of the proposed solution is shown in Figure 1.4, where a full stave is powered through a single 10 V line. At the left of the stave a stage 1 converter supplies the 2.5 V line for the optoelectronics and the controller,

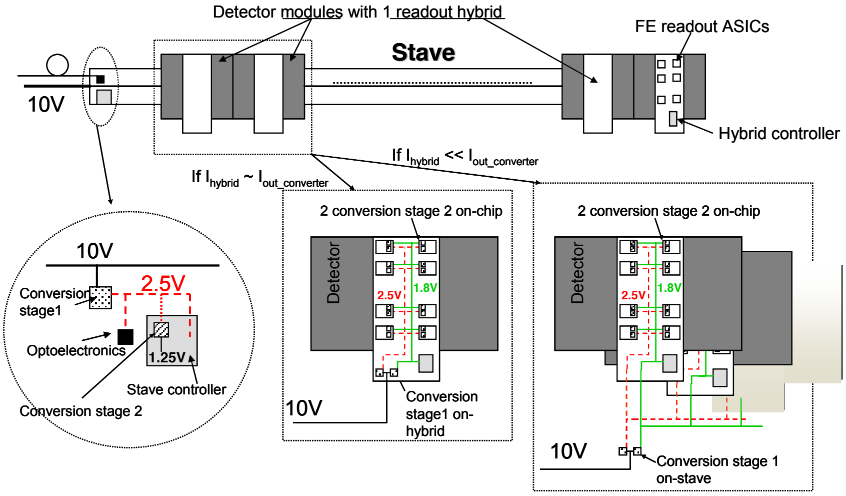


Figure 1.4: Possible implementation of the proposed distribution scheme. The choice of whether to have the conversion stage 1 depends on the power rating of the converter and hybrid and on the available space.

and the 1.2 V is generated on-chip by the conversion stage 2 just by dividing the 2.5 V.
The main features of the proposed solution can be summarized as follows:

- The current on the main supply line is reduced by a factor of about 10: power losses are drastically reduced.

- High modularity in the distribution of power allows the individual or grouped turning on/off of ASICs, facilitating the system start-up. In case of ASIC failures, only individual groups can be turned off without loosing full hybrids.

- All the supplies are generated from a unique 10 V line: FE analog and digital circuitry can be efficiently powered at the desired Vdd.

All these features require some fundamental problems to be solved for a successful implementation. In the first place each converter needs to be tolerant to the radiation and the high magnetic field present in the tracker. Commercial step-down converters are designed to use ferromagnetic inductors that would saturate in the $2 - 4$ T magnetic field, and are not engineered to reliably tolerate high levels of radiation, so they are not suitable for this application. Another aspect to be considered is the long length of the supply cables, that can affect the stability of the converters, therefore a dedicate development is needed (ASIC). In this chapter the design strategies of an ASIC CMOS DC-DC Converter for the conversion stage 1 are presented.

1.2 Radiation Tolerance

The main effects of radiation on matter can be grouped in two main classes: ionization effects and nuclear displacement. This effects can be caused directly by the incident particles or from secondary phenomena induced by it, and represents the majority of the events that happen in the irradiated matter. Whether neutrons give origin mainly to nuclear displacement (neighbouring interstitial atom and vacancy) that has a limited importance in this case [3], photons and electrons are responsible for ionization effects: ionization in a semiconductor or insulating material creates electron-hole pairs; the number of the created pairs is proportional to the quantity of energy deposited in the material, which is expressed through the total absorbed dose.

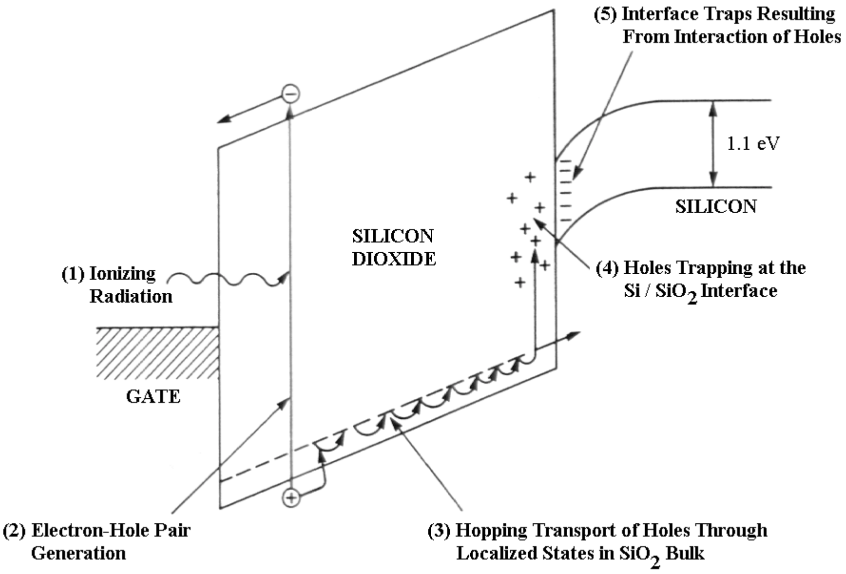


Figure 1.5: Schematic illustration of the effects induced by the ionizing radiation in a MOSFET, where the gate is positively biased.

1.2.1 Electrical Parameters Effects

Effects in MOSFETs

When a ionizing particle goes through a MOS transistor, electron-hole pairs are generated; in the gate (metal or polysilicon) and in the substrate, the pairs quickly disappear, however in the oxide, electron and holes have different behaviours, as their mobility differs from five to twelve orders of magnitude. The electron-hole pairs that are not recombined are separated in the oxide by the electric field and coherently with the polarity of the voltage applied to the gate, electrons or holes drift to the gate and to the $SiO_2 - Si$ interface as in Figure 1.5 with a very different transport phenomenon.

If a positive voltage is applied to the gate, some holes may be trapped in the oxide very close to the interface with the silicon, creating a fixed positive charge, that also induces the creation of traps at the $SiO_2 - Si$ interface (in the silicon side); the first phenomenon gives origin to a shift of the flat-band voltage, and therefore in the threshold voltage of the transistor, the second one introduces defect states that work as acceptor or donor traps, intensifying the threshold-voltage shifting.

The interface states increase slower that the positive charge in the oxide, this explains why the threshold voltage shift in an n-channel MOSFET as a function of the total dose can be negative at the beginning and becomes finally positive after a certain time.

Another effect of the irradiation, is the increase of the off-state current of the transistor; this is due by two main factors: the first one is the increase of the threshold voltage (in p-channel transistors) which causes an increase of the subthreshold current, and the second one is the creation of two parasitic paths, one under the region called bird's beak or, further away from the device, underneath the thick oxide; the second one is the dominant effect in all the measured technologies from 0.7 μm to 0.25 μm. If the thick oxide is present also in a interconnection between a biased well of a p-channel and the grounded well of an n-channel, a leakage current can be present: also this problem had been considered in the design of the layout.

The last effect is the mobility degradation, which is caused by the increase of the interface traps, since the conduction in a MOSFET is due to the carrier motion close to the $SiO_2 - Si$ interface.

Effects in DIODEs

Like in the MOSFETs, also diodes are subject to leakage currents, sometimes higher than 1 μA; since diodes are generally used in bandgaps, the minimum current used in the voltage reference diodes should be higher than 10 μA, in order to avoid voltage shifts.

To further increase the tolerance to radiation, diodes should be designed with a square shape, this maximizes the ration Area/Perimeter, decreasing the fraction of the leakage perimeter current compared to the useful current.

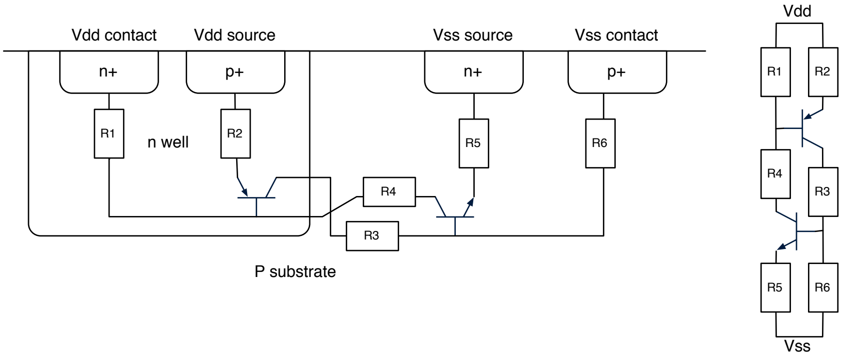


Figure 1.6: PNPN Thyristor present in a common CMOS process.

1.2.2 Single Event Effects

Single Event Effects (SEE) are caused by an high energy particle, such as an heavy ion, passing through an integrated circuit. They are divided in two categories:

- Soft Errors: when the generated errors are reversible and do not damage the device.
- Hard Errors: when the errors are destructive and can damage the device.

Single Event Upset

Single Event Upset (SEU) is a soft error that occurs when a ionizing particle crossed the drain or the source of a logic cell transistor. The collected charge can modify the voltage stored in the source or in the drain, possibly corrupting the stored information. This effect can be simulated: the amount of energy deposited by a charged particle per unit of length can be expressed in terms of Linear Energy Transfer (LET) in units of $MeVcm^2mg^{-1}$, which is the energy loss dE/dx divided by the density of the traversed material, in our case Si, and depends obviously from the energy of the incident particle. The maximum LET considered in the LHC experiment upgrades is the worst event generated by nuclear interaction, which is the fission of the tungsten, present in tiny parts in the metallization stack in the ASIC. This event is very rare but can generate LETs up to 40 $MeVcm^2mg^{-1}$.

Single Event Latch-Up

Latch-Up is well know phenomenon present in CMOS technology (p substrate CMOS technologies, SOI technologies are latch-up free), and consists in the turning on of the parasitic PNPN thyristor present in a normal CMOS structure,(Figure 1.6) and can short the power lines, destroying the whole IC. Two conditions for turning on the thyristor are required

- The product of gains of the two involved transistors ($\beta_{npn} \cdot \beta_{pnp}$) must be higher than 1.
- The power supply must be able to provide the required current required by the transistors.

Generally latch-up is caused by electrical transients on input/output lines, high temperature or improper turn on of the supply biasing, but in this case can be also initiated also by an ionizing particle. The only procedure to avoid the destruction is to turn off the supply as fast as possible.

Single Event Burn-Out

Single Event Burn-Out (SEB) is present in bipolar transistors and power MOSFETs, since these devices contain a parasitic bipolar transistor. In some biasing conditions there is a possibility than a ionizing particle turns on the transistor, which can conducts enough current to melt the MOSFET. This phenomenon needs to be taken in account during the tests of the suitable technology.

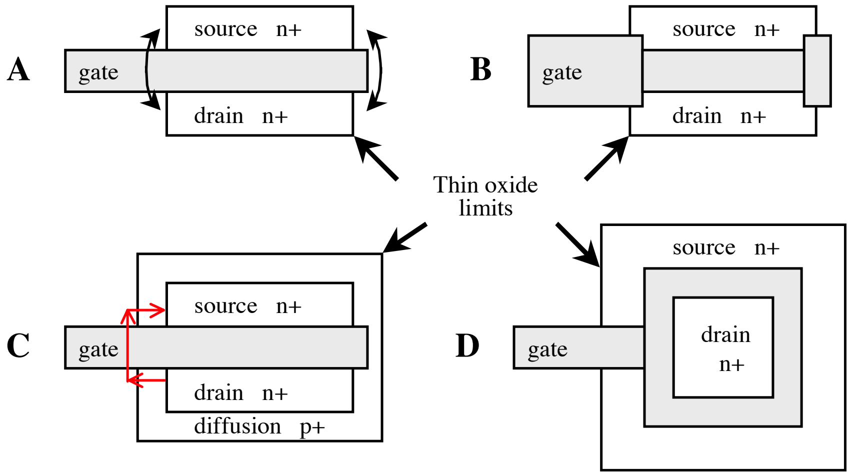


Figure 1.7: Layout of a standard NMOS (A) and three possible alternatives (B,C,D) to avoide leakage paths.

1.2.3 Techniques to Achieve Radiation Tolerance

There are three possible levels on which the radiation tolerance of a CMOS IC can be improved:

- Hardening by process (HBP): acting on the process, modifying some technological parameters or process steps in order to reduce the sensitivity to radiation-induced problems; this technique cannot be implemented with commercial technology and in particular in Multi Project Wafer run, where process modification is not allowed.
- Hardening by design (HBD): using special layouts stratagems, solving problems of radiation-induced leakage currents; this technique will be used in the presented work.
- Hardening by circuit and system architecture: using special circuit architectures that are less sensitive to the changes in the device parameters.

In the HBD the first issue that has to be solved is the leakage inside the n-channel MOSFET after the irradiation, which is shown in Figure 1.7-A. Solution B consists of increasing the length of the leaky area, this is the least intrusive but also the least effective. With solution C allows to keep the transistor dimensions very close to the original one but generally is not applicable in commercial processes since it violates some design rules. Solution D is the one adopted in this work, as it is the safest from the radiation hardness point of view: in this case the leaky path is removed, in fact these type of layout is mandatory if high total dose radiation tolerance has to be achieved. However it has some drawbacks:

- Higher area.

- Difficulties in modelling W/L ratio of the transistor.
- Limitations in the choice of W/L ratio.
- Increase of the gate and drain capacitance.
- Lack of symmetry.

For what concerns the leakage currents between different devices, the solution is to surround each nmos with a p+ guard ring, which cuts any possible path; this method has been verified to be very effective. Again the drawback is an increased space required in the IC.

New "radiation" model libraries have been created and all the designed circuits have been simulated with 300 Montecarlo runs with normal and "radiation" parameters. The worst-case 550 mV PMOS V_{th} variation drastically limits the input and output swing of amplifiers, restricting the choice of architecture to only those leading to large input/output ranges (no more than two PMOS in series).

Regarding the circuit and system architecture, the designer should focus on the nets of the device that are more vulnerable for the reliability. For instance a single event can charge a net with positive or negative charges, increasing the capacity of that node, can avoid fluctuations of its voltage; an example of a vulnerable net is the main reset net.

Table 1.2: Properties of high-voltage transistors in the studied technologies.

Tech.	Tech. node	Transistor Type	Max $V_{ds}[V]$	Max $V_{gs}[V]$
A	0.35 μm	Vertical N	80	3.3
		LDMOS N	14	3.3
		LDMOS P	80	3.3
B	0.25 μm	LDMOS N	22	2.5
		LDMOS P	15	2.5
C	0.18 μm	LDMOS N & P	20	5.5
D	0.18 μm	LDMOS N & P	20	1.8
		LDMOS N & P	50	1.8
		LDMOS N & P	25	5
E	0.13 μm	LDMOS N & P	20	4.5

1.2.4 Selection of the Suitable Technology

The successful development of a radiation-tolerant converter ASIC requires an adequate semiconductor technology capable of integrating both the conventional low-voltage CMOS devices (transistors, capacitors, resistors) and additional transistors with higher voltage capability, up to $14 - 20\ V$ for a converter rated at $10\ V$ of input voltage. These transistors are often constructed as Lateral Diffusion transistors, LDMOS.

Several commercial technologies (Table 1.2) offering the above feature have been studied to assess their response radiation in terms of Total Ionizing Dose (TID) and displacement damage effects [4]; radiation tests are made with X-rays at energy of $10 - 20\ keV$, as commonly done for radiation effects studies on semiconductors. Some results are shown in Figure 1.8 and Figure 1.9

Wide variability in TID response is observed. Threshold voltage shifts generally correlate with the gate voltage ratings of each device, hence with gate oxide thickness. On the contrary, no systematic correlation is observed for the source-drain leakage currents in n-channel transistors. The leakage increase seems hence to be determined mainly by details in the construction of the device that are not necessarily linked to voltage ratings or technology node.

Two technologies appear to provide adequate radiation performance, in different CMOS technology nodes (0.25 and 0.35 μm) [5]. Several prototypes were realized in both technologies, in order to evaluate the reliability and the real behaviour under radiation conditions. Figure 1.10 shows the evolution of a realized 0.35 μm DC-DC step down converter's efficiency as a function of TID [6]. The initial efficiency drop and subsequent recovery at higher TID correlate well with the leakage current of the LDMOS as measured on individual evaluation transistors.

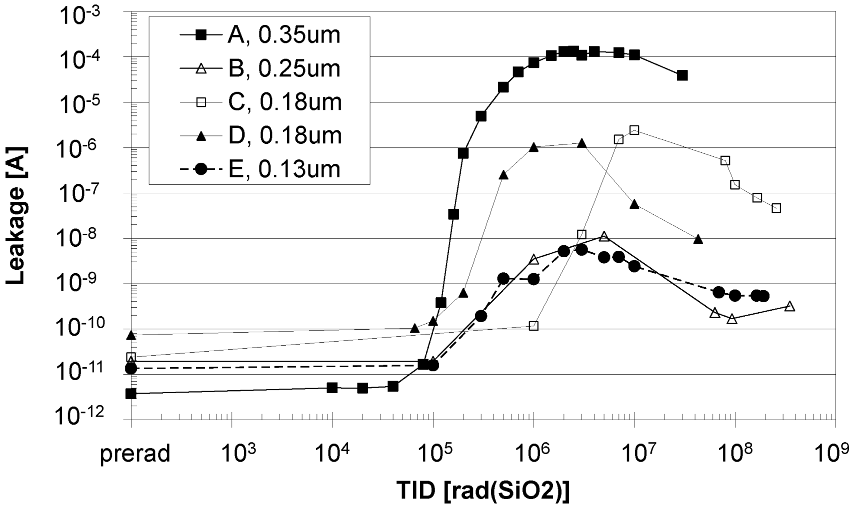


Figure 1.8: Evolution of the leakage current with TID for standard (not HBD) n-channel LDMOS in all technologies. Irradiation was performed at room T under worst case bias. For technology D, data refers to the device rated at 1.8 V.

The antagonist contribution of charges trapped in the oxide and of interface states explains this evolution.

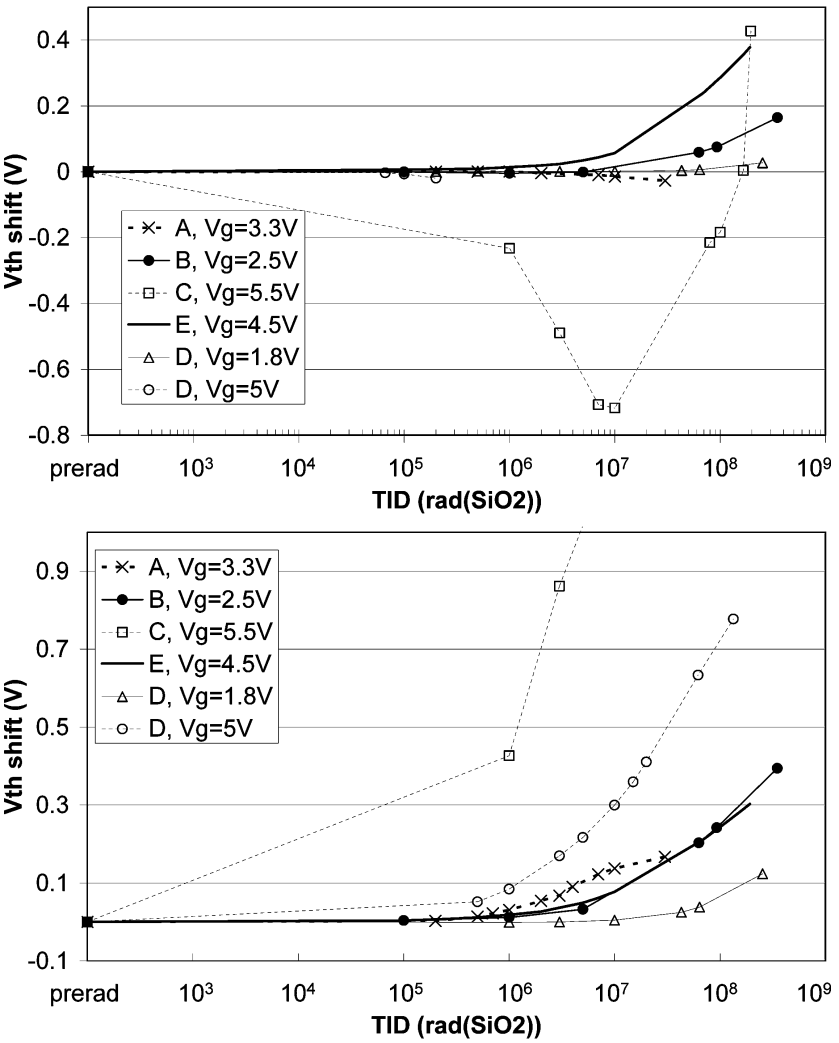


Figure 1.9: Threshold voltage shift induced by TID on n-channel (top) and p-channel (bottom) LDMOS transistors biased in the WC condition at room temperature. For the n-channel, technology D, $V_g = 5\ V$, the leakage current was too large after 200 krd (SiO_2) to enable extraction of V_{th} in the linear regime.

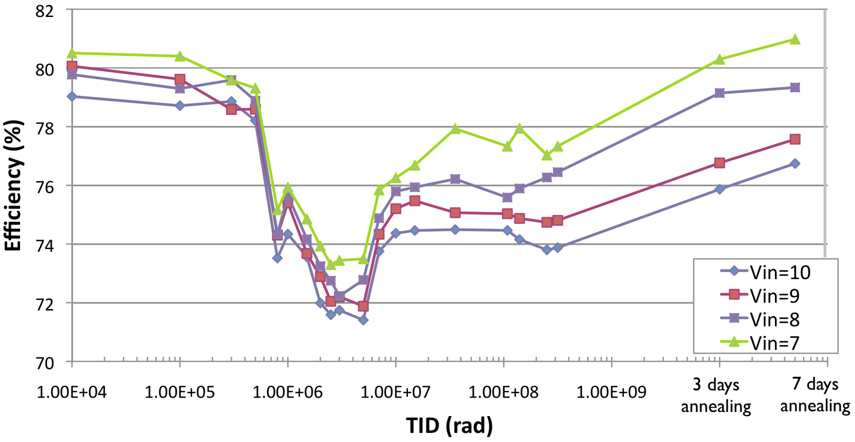


Figure 1.10: Evolution of the efficiency of a realized 0.35 μm DC-DC step down converter ASIC with TID during X-ray irradiation.

1.3 High Magnetic Field Tolerance

Whenever a current flows into a wire, a magnetic field is radially produced; this phenomenon is characterized by Ampère's law:

$$\oint_C B \cdot dl = \mu \iint_S J \cdot dS = \mu I, \qquad B = \mu H \tag{1.1}$$

If a wire is wrapped forming a solenoid, B becomes:

$$B_{int} = \mu \frac{NI}{l} \tag{1.2}$$

Where I is the current flowing into the wire, N is the number of turns, l the length of the solenoid and μ is the permeability of the core. When this is combined with the definition of inductance $L = N\phi/I$, we obtain that

$$L = \mu \frac{N^2 A}{l} \tag{1.3}$$

Generally solenoid inductors are very common, and are made with ferromagnetic cores, in order to have an higher permeability and consequently an higher ratio inductance/volume. Permeability is the measure of the ability of a material to support the formation of a magnetic field within itself. In other words, it is the degree of magnetization that a material obtains in response to an applied magnetic field. Ferromagnetic materials like iron are composed of microscopic regions called magnetic domains that act like tiny permanent magnets that can change their direction of magnetization. Before an external magnetic field is applied to the material, the domains are oriented in random directions. Their

Table 1.3: Permeability and saturation flux density of magnetic materials.

Material	μ at $B = 20\ G$	Max. μ	Sat B (G)
Cold rolled steel	180	2,000	21,000
Iron	200	5,000	21,500
Purified iron	5,000	180,000	21,500
45 Permalloy	2,500	25,000	16,000
Hipernik	4,500	70,000	16,000
Monimax	2,000	35,000	15,000
Permendur	800	4,500	24,000
Hiperco	650	10,000	24,200

tiny magnetic fields point in random directions and cancel each other, so the material has no overall net magnetic field. When an external magnetizing field H is applied to the material, it penetrates the material and aligns the domains, causing their tiny magnetic fields to turn and align parallel to the external field, adding together to create a large magnetic field B which extends out from the material. This is called magnetization. The stronger the external magnetic field, the more the domains align. Saturation occurs when practically all the domains are lined up, so further increase in applied field can't cause further alignment of the domains. Considering for instance the solenoid, if the flux density B reaches B_{max}, the permeability will decrease and will become about the vacuum permeability μ_0 ($\mu_0 = 4\pi 10^{-7}\ N/A^2$), this will cause a drastic reduction of the inductance.

As shown in Table 1.3, the highest value of saturation of flux density of a material is 24.500 G (Gauss), but as mentioned, the permanent magnetic flux density in the experiments is up to 40 kG; it's clear that the use of an air inductor is almost mandatory to avoid saturation problems.

This type of inductors however there's a strong limitation for what concerns the value of the inductance and the physical dimensions: without an high permeability an higher length of wire is required to increase the inductance, increasing consequently the volume and the copper losses of the DC-DC converter. This also limits the choice of the topology of the converters: without a ferromagnetic core, a transformer would have excessive losses.

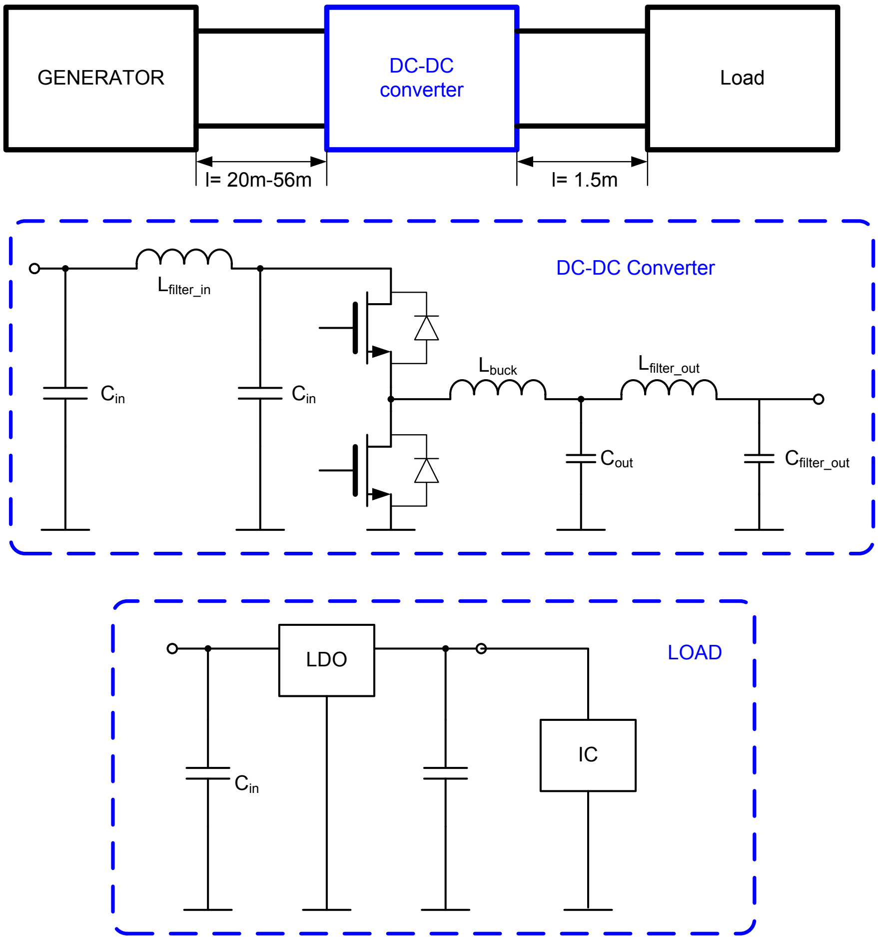


Figure 1.11: Representation of the whole power distribution system.

1.4 Long Cables Tolerance

As explained, a possible implementation of the power management for the HLLHC upgrade is shown in Figure 1.4, where a full stave is powered through a single 10 V line; the 10 V line will be supplied by a huge generator which will be placed outside the experiment, and connected through very long cables ($20-56$ m long). Finally the complete distribution system can be summarized with the represented scheme in Figure 1.11. The load can be constituted by a multiplicity of different elements connected in parallel. This power distribution architecture will be analysed in the detail to understand the convenient solution in terms of voltage control loop. Figure 1.12 is a representation of the system analysed with the State Space Averaging method; impedances Z_s and Z_L contain respectively the impedances of the input filter with the contributions of the power supply cables and the output filter with the eventual remote connection cables. An example of the values of all the impedances are reported in the Table 1.4.

In Figure 1.13 is represented the input impedance Z_s of the converter with

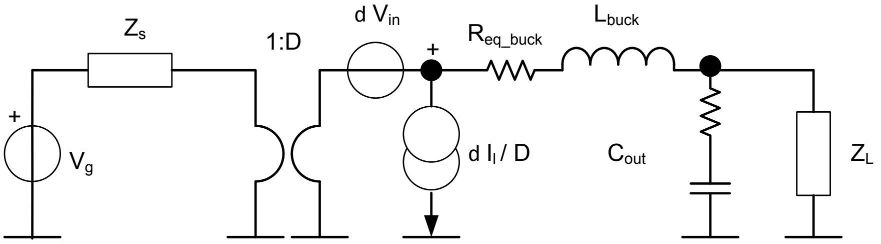


Figure 1.12: Representation of the converter with the input and output filter.

Table 1.4: Power distribution system parameters.

Component	Value	Corresponding impedance
L_{in}	Inductor=25 μH, DCR=0.1 Ω	Contribution in Z_s
C_{in_buck1}	Capacitor=21 μF, ESR=0.5 $m\Omega$	Contribution in Z_s
C_{in_buck2}	Capacitor=21 μF, ESR=0.5 $m\Omega$	Contribution in Z_s
L_{filter_in}	Inductor=120 nH, DCR=8 $m\Omega$	Contribution in Z_s
L_{filter_out}	Inductor=120 nH, DCR=8 $m\Omega$	Contribution in Z_L
C_{filter_out}	Capacitor=21 μF, ESR=0.5 $m\Omega$	Contribution in Z_L
$L_{connection}$	Inductor=1 μH, DCR=10 $m\Omega$	Contribution in Z_L
C_{in_load}	Capacitor=6.7 μF, ESR=0.5 $m\Omega$	Contribution in Z_L

the data reported in Table 1.4. At low frequencies the impedance is dominated by the resistive value of the filter connected in series with the resistance of the cable as reported in Equation 1.4.

$$Z_s(0) = DCR_{cable} + DCR_{filter} \tag{1.4}$$

For higher frequencies the value of the impedance increases because the more important contribution in the cable is the equivalent inductor, until there is the resonance of the input inductor of the cable with the total input capacitance of the converter, that occurs at the frequency reported in 1.5. Because the impedance of the EMI inductor is negligible respect to the impedance of the cable inductor, the impedance Z_s can be considered as a parallel LC impedance.

$$\omega_{ppc1} \cong \frac{1}{\sqrt{L_{cable}(C_{in\_buck1} + C_{in\_buck2})}} \tag{1.5}$$

The maximum value of this impedance depends on the value of the total resistance present in the system. By considering the resistance of the cable inductor and the impedance of the equivalent capacitor, the maximum impedance can be calculated

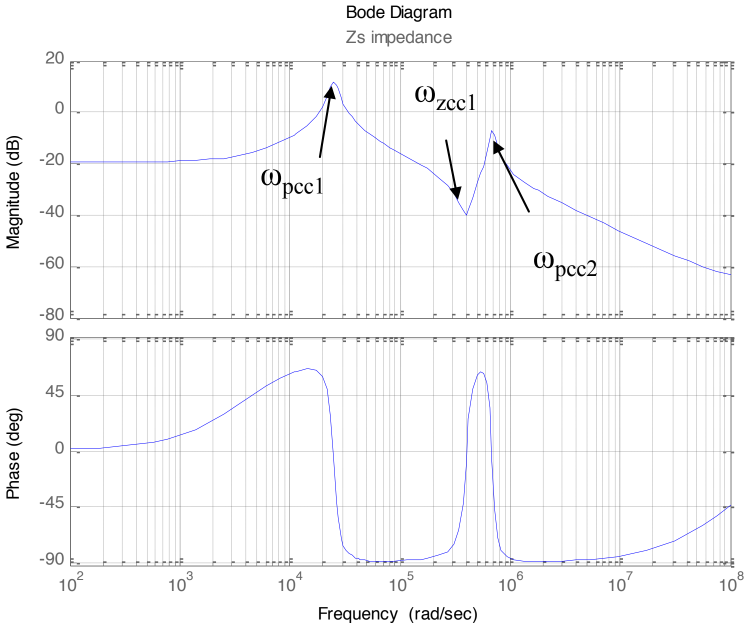


Figure 1.13: Impedance at the input of the converter.

as reported in 1.6.

$$|Z_s(\omega_{ppc1})| \cong \sqrt{\frac{L_{cable}}{C_{in\_buck1} + C_{in\_buck2}}} \sqrt{1 + \frac{L_{cable}}{(C_{in\_buck1} + C_{in\_buck2})R_{cable}^2}} \tag{1.6}$$

After the first resonance the impedance is approximately capacitive dominated by the parallel of the all input capacitor, until the series resonance due to the EMI filter inductor occurs and for higher frequencies there is the last parallel resonance. Approximated values for these resonance frequencies are reported in 1.7 and 1.8.

$$\omega_{zcc1} \cong \frac{1}{\sqrt{L_{filter} C_{in\_buck1}}} \tag{1.7}$$

$$\omega_{pcc2} \cong \frac{1}{\sqrt{L_{filter} C_{in\_buck2}}} \tag{1.8}$$

In this case these two approximations give the same results and the two singularity are close as reported in bode diagram of Figure 1.13. As described in the precedent case, the maximum value of impedance can be calculated by Equation 1.9.

$$|Z_s(\omega_{ppc2})| \cong \sqrt{\frac{L_{filter}}{C_{in\_buck2}}} \sqrt{1 + \frac{L_{filter}}{C_{in\_buck2} R_{filter}^2}} \tag{1.9}$$

The necessary condition to obtain the stability of the system constituted by the Z_s with the input impedance of the converter Z_{in}, can be expressed in terms of

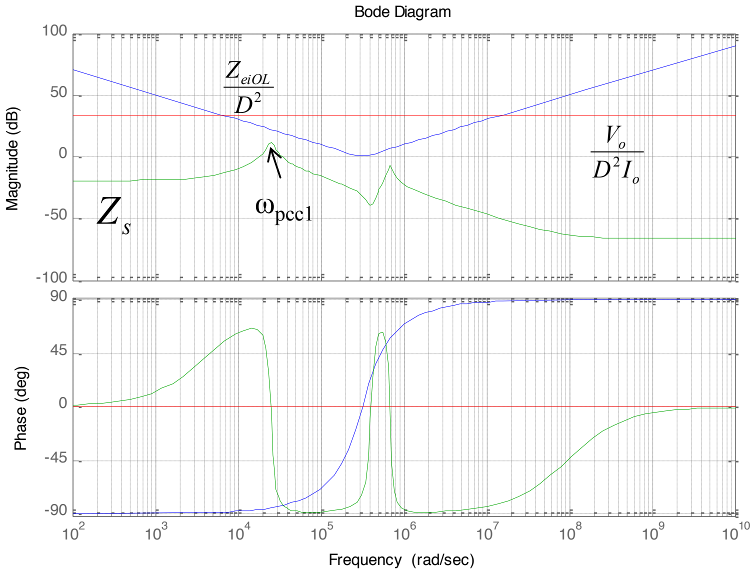


Figure 1.14: Z_S compared with transfer functions of relations 1.11.

the stability condition on the transfer function T_n in close loop as reported in 1.10:

$$\begin{aligned} Z_{eq} &= \frac{Z_i Z_s}{Z_i + Z_s} = \frac{Z_s}{1 + T_n} \\ T_n &= \frac{Z_s}{Z_i} = -\frac{T}{1+T}\frac{D^2 Z_s I_o}{V_o} + \frac{1}{1+T}\frac{D^2 Z_s}{Z_{eiOL}} \end{aligned} \tag{1.10}$$

where the D represents the duty cycle, T the open loop transfer function of the converter and Z_{eiOL} represent the impedance of the buck output filter connected with the load and V_o and I_o are respectively the output voltage and current. As can be observed on the second equation of relation 1.10, the impedance of the converter Z_i is negative when it's control loop transfer function $T >> 1$ and depends on the output power level. In general a sufficient condition is:

$$\begin{aligned} \left|\frac{D^2 I_o Z_s}{V_o}\right| &<< 1 \\ \left|\frac{D^2 Z_s}{Z_{eiOL}}\right| &<< 1 \end{aligned} \tag{1.11}$$

These conditions are satisfied as reported in Figure 1.14, but with a very low margin on the impedance value. Applying the Nyquist criterion of stability on the transfer function T_n, we can express the next relation:

$$\left|\frac{D^2 Z_s I_o}{V_o}\right| < 1 \rightarrow |Z_s(\omega_{pcc1})| \frac{D^2 I_o}{V_o} < 1 \tag{1.12}$$

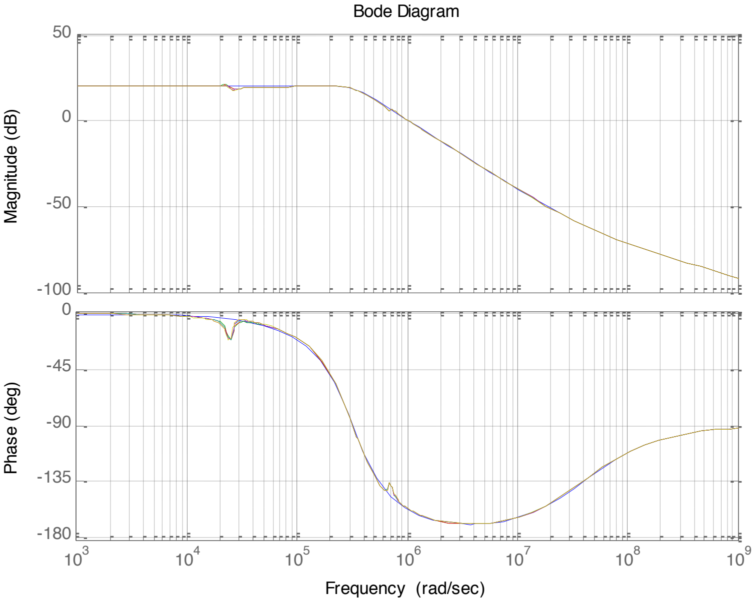


Figure 1.15: Transfer function of the converter (blue) and the transfer function of the converter with the input filter and the cable impedance (green).

For the Equation 1.6 the ratio between the impedances is very close to 1, so the stability can't be assured in all the conditions. The transfer function of the DC-DC converter considering the effect of the input filter is reported on the relation 1.13.

$$T' = T\frac{1-\frac{D^2 I_o Z_s}{V_o}}{1+\frac{D^2 Z_s}{Z_{eiOL}}} \tag{1.13}$$

If the 1.11 conditions are satisfied, the transfer function is approximately the same of the transfer function of the converter. In our case of study the transfer function is reported in Figure 1.15 and the effect of the input filter is a small reduction of phase of the transfer function. This phase reduction depends on the value of the parasitic resistance of the cable connection that is related to the temperature. Lower is the resistance for each meter, higher is the phase reduction. If the phase reduction is high, a solution to the stability problem in all condition is a reduction of the bandwidth at a frequency less than the resonance frequency of the input network:

$$\omega_T < \omega_{ppc1} \tag{1.14}$$

The limitation of the bandwidth imposed by the Equation 1.14, causes a reduction of the audio susceptibility of the converter so the output can be affected by low frequency oscillations present on the power bus. In the example we are considering a converter connected to the bus by the cable with the parameters reported in the Table 1.4, the frequency of the complex poles is about seven times the crossover

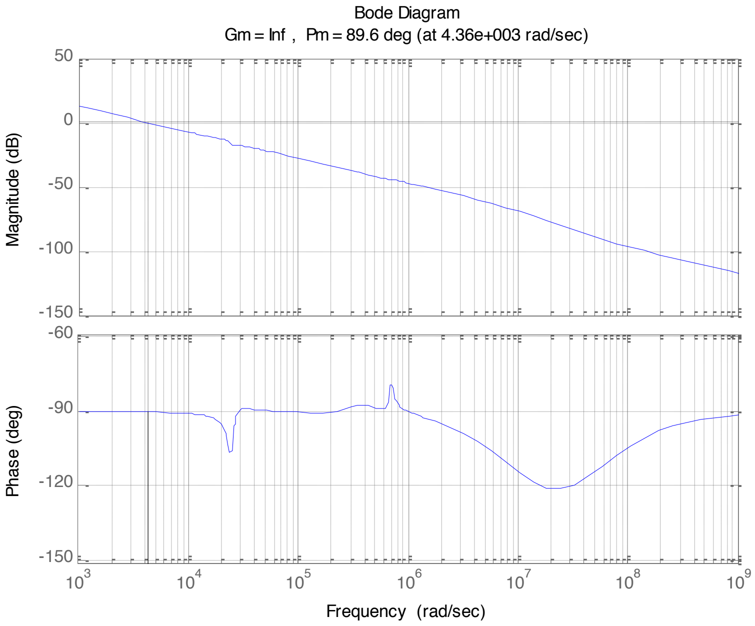


Figure 1.16: Transfer function of the control loop.

frequency of the controller. The loop transfer function is reported in Figure 1.16. In Figure 1.17 is reported the load transient effect in the output voltage and in the input voltage of the converter. The oscillation present in the output voltage are due to the input voltage variation because the bandwidth of the controller is less than the oscillation frequency on the bus. To overcame this limitation a higher bandwidth can be utilized for the controller. In the following example the bandwidth is about ten times higher than the oscillation frequency of the complex poles. As can be seen in Figure 1.19 the bus voltage is approximately the same of Figure 1.17 but the oscillations on the output voltage are lower. Another solution

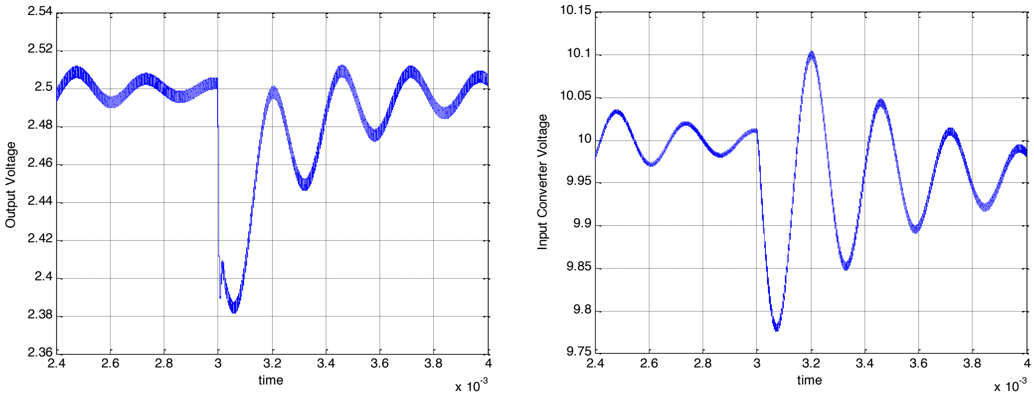


Figure 1.17: Output voltage swing and input voltage of the converter during a load transient.

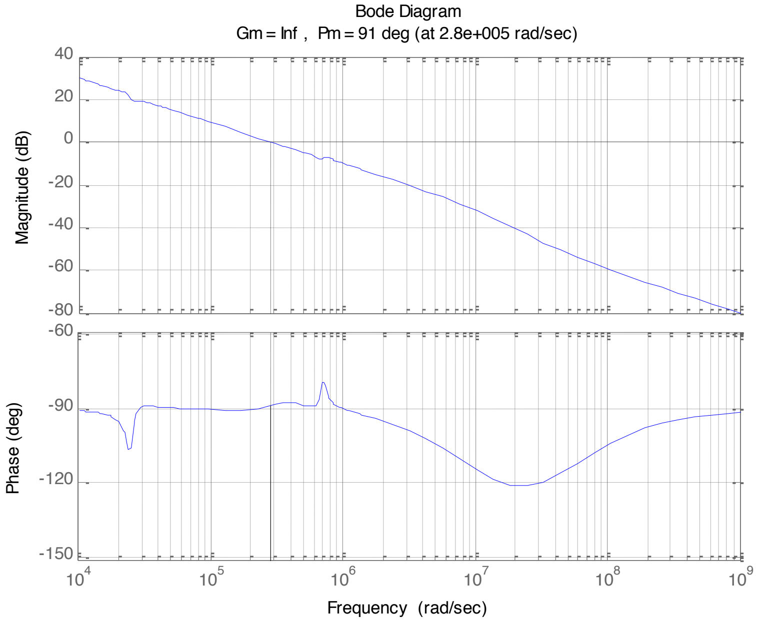


Figure 1.18: Transfer function of the control loop.

for the rejection of the bus voltage oscillation especially when many converters utilize the same power bus is the feed forward compensation. In this case the slope of the modulation ramp of the converter depends on the input voltage. This compensation introduces another block on the transfer function of the converter as reported in Figure 1.20. Obviously to obtain the total cancellation of the input contribution on the output voltage the signal must be different and the relation 1.15 must be satisfied.

$$FF = \frac{D}{V_{in}} \tag{1.15}$$

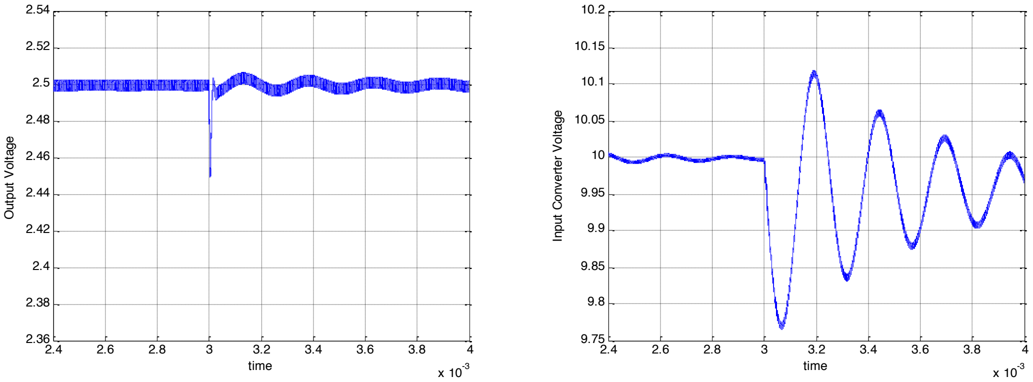


Figure 1.19: Output voltage swing and input voltage of the converter during a load transient.

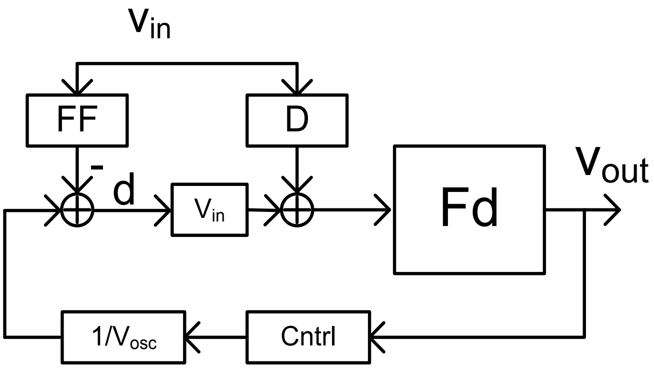


Figure 1.20: Basic FF scheme.

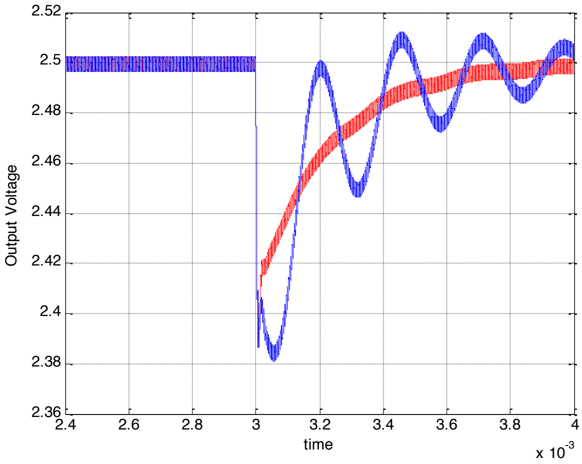


Figure 1.21: Transient response with (red) and without (blue) a Feed Forward compensation.

By this contribution the transient has a better behaviour even if there is a small control bandwidth. In Figure 1.21 is shown a transient response with and without feed forward compensation utilizing the same controller transfer function.

Another solution of the 1.14 to obtain a better stability of the power bus can be addressed on the compensation of the impedance by introducing a resistance in series to the capacitors of the *CLC* filter in order to obtain a damped *LC* filter. By this system the input capacitor or the two capacitors of the network can be substituted by two capacitor connected in parallel as reported in Figure 1.22.

By this solution is possible to reduce the maximum peak of the Z_s impedance by reducing the resonance of the L_{in} cable inductor with the capacitors of the network. By changing the value of the R_d resistance starting from 0 to infinite, the peak of the impedance is high when the R_d is 0 at the resonance frequency of the two capacitors connected in parallel with the input inductor, when the value

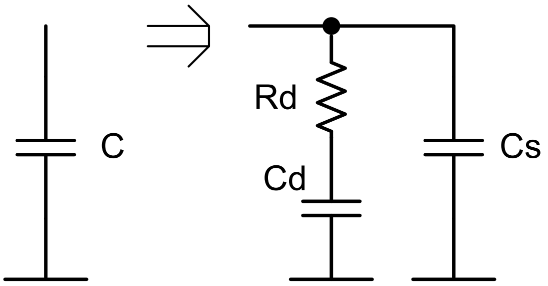


Figure 1.22: Substitution of the capacitor of the CLC filter with an anti damping network.

of R_d is very high the impedance has a peak at the resonance frequency of the input inductor L_{in} with the C_s capacitor. The capacitor C_s can be chosen in order to maintain the same impedance at the switching frequency by considering the parasitic elements (ESR, ESL) of a capacitor.

$$\frac{1}{\omega_{sw} C_s} < |ESR + j\omega_{sw} ESL| \tag{1.16}$$

By defining "n" the ratio between the two capacitors C_d and C_s ($C_d = nC_s$), there is a best value of R_d for which the Z_s impedance peak is minimum. The value of the impedance is:

$$|Z_{s\_peak\_min}| = \sqrt{\frac{L}{C_s}} \sqrt{\frac{2(2+n)}{n^2}} \tag{1.17}$$

So the value of n must be chosen in order to reach the condition 1.11, the other parts of the filter can be calculated by this relation.

$$Rd = \sqrt{\frac{L}{C_s}} \sqrt{\frac{(4+3n)(2+n)}{2n^2(4+n)}} \tag{1.18}$$

When there are two ore more modules connected to the same cable, the stability condition 1.11 can be satisfied as reported in Figure 1.23, where are reported the same graphs of Figure 1.14 in case of connection of a number of N modules that start form 1 to 10.
The sufficient condition for the stability is satisfied for many modules connected in parallel because the reduction of the value of the transfer function Z_{eiOL} and R_{OUT} are compensated by the reduction of Z_s.

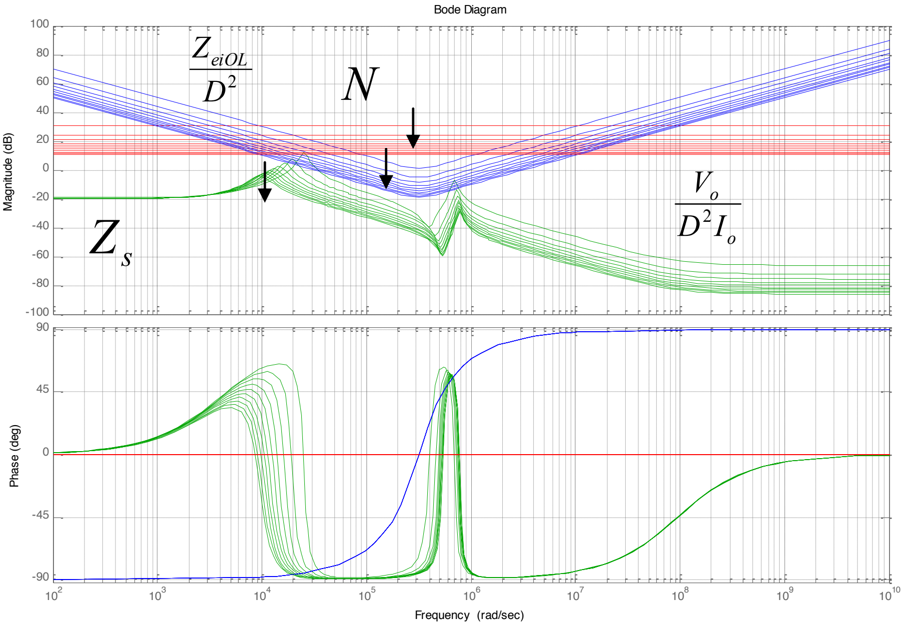


Figure 1.23: Z_s compared with the transfer functions of the relations 1.11 for a number of module connections N that starts from 1 to 10.

Chapter 2

Power Distribution Systems in Remote Applications

With the recent advances in wireless sensor networks (WSNs), the realization of low-cost embedded industrial remote systems have become feasible [7]. In these systems, wireless tiny sensor nodes are installed on industrial equipment and monitor parameters critical to each equipment's efficiency or are directly used to monitor environmental parameters such as vibration, temperature, pressure and light. These data are then wirelessly transmitted to a sink node that analyses the data from each sensor or are shared with the other neighbouring nodes. Ideally each node should be energy autonomous and without the need of battery replacement and disposal [8]. In WSNs, the use of batteries as power source for the sensor nodes can be troublesome due to their limited lifetime, making periodic replacements unavoidable. In this respect, energy-harvesting (also referred to as energy scavenging) techniques, which extract energy from the environment where the sensor itself lives, offer another important way to prolong the lifetime of sensor devices.

An overview of different energy harvesting techniques in WSNs is reported in Table 2.1 [7], which gives a rough idea of the obtainable energy from different environmental sources.

Two choices are available for energy storage [9]: batteries and electrochemical double layer capacitors, also known as supercapacitors; batteries are a relatively mature technology and have a higher energy density (more capacity for a given volume, weight, and cost) than supercapacitors; however, supercapacitors have a higher power density than batteries, and are more efficient and offer higher lifetime in terms of charge-discharge cycles. The main disadvantage of supercapacitors in energy harvesting applications is the high leakage current.

Four types of rechargeable batteries are commonly used: nickel cadmium (NiCD), nickel metal hydride (NiMH), lithium based (Li+), and sealed lead acid (SLA). Of these, SLA and NiCD batteries are less used because the former has a rel-

Table 2.1: Overview of different energy harvesting techniques in WSNs present in literature [7].

Energy Source	Performance	Commercially Available
Primary Battery	2880 J/cm^3	Yes
Secondary Battery	1080 J/cm^3	Yes
Light (indoor)	$10-100\ \mu W/cm^2$	Yes
Light (outdoor)	$10-23\ mW/cm^2$	Yes
Airflow	$0.4-1\ mW/cm^3$	No
Vibrations	$200-380\ \mu W/cm^3$	Yes
Thermoelectric	$40-60\ \mu W/cm^2$	Yes
Electromagnetic Radiation	$0.2-1\ mW/cm^2$	Yes
Piezoelectric	$100-330\ \mu W/cm^3$	Yes

atively low energy density and weight, and the latter suffers from capacity loss caused by shallow discharge cycles, termed as the memory effect. Li+ batteries are more efficient than NiMH, have a longer cycle lifetime, involve a lower rate of self-discharge, and its cycle-life is independent of the Depth of Discharge (DoD) problem that is present also in SLA and NiCD batteries. However as can be seen from Tables 2.2 and 2.3, also other parameters are involved in the choice of a battery, such as temperature range, charging simplicity and obviously the cost.
It is clear that every remote application requires an analysis of the adequate energy source and energy storage, and is not possible to say from the outset, which is the best battery for every application.

Table 2.2: Properties of various commercial battery technologies [11, 12].

Technology	Specific Energy[Wh/kg]	Energy Density[W/kg]	Cicle Life(cycles) at 80% DoD	Temp.[$°C$]	Cost
Lead-Acid	20-50	200-400	400-700	-20 +60	Inexpensive.
NiCd	22-60	50-150	800-1200	-20 +45	Inexpensive.
NiMh	35-95	140-300	500-1000	-20 +60	Inexpensive.
Li-ion	80-250	250-600	1000-6000	0 +60	Expensive.

Table 2.3: Advantages and disadvantages of different battery technologies [13].

Technology	Advantages	Disadvantages
Lead-Acid	• Inexpensive and simple to manufacture • Low self-discharge • High specific power and capable of high discharge currents • Good low and high temperature performance • No memory	• Low specific energy • Slow charge • Must be stored in charged condition to prevent sulfation • Repeated deep-cycling reduces battery life • Flooded version requires watering • Not environmentally friendly
NiCd	• High number of charge/discharge cycles • Good load performance, rugged and forgiving if abused • Can be stored in a discharged state • Good low-temperature performance • NiCd is the lowest in terms of cost per cycle	• Relatively low specific energy compared with newer systems • Memory effect: needs periodic full discharges • Environmentally unfriendly • High self-discharge
NiMh	• Less prone to memory than NiCd • Simple storage and transportation • Environmentally friendly • Nickel content makes recycling profitable	• Deep discharge reduces service life • Requires complex charge algorithm • Does not absorb overcharge well • Generates heat during fast-charge and high-load discharge • High self-discharge • Degrades if stored at high temperatures
Li-ion	• High energy density • Relatively low self-discharge • No memory	• Requires protection circuit to limit voltage and current • Subject to ageing, even if not in use

2.1 Photovoltaic-Based Wireless Sensor Networks

While a wide variety of harvesting modalities are now feasible, solar energy harvesting through photovoltaic (PV) conversion provides the highest power density, which makes it the preferred choice to power an embedded system that consumes several milliwatt using a reasonably small harvesting module for outdoor applications [9].

Solar cells exhibit a strong non-linear electrical characteristic and the extraction of energy is even more difficult in non- stationary environments. Variable operating conditions can be associated with the weather change (e.g., cloudy and non optimally radiating solar power environments) and ageing effects or efficiency degradation in the solar panel (e.g. dust or rust in the cell surface). Moreover, the energy transfer mechanism is strongly influenced by the illumination condition such as the angle of incidence of the sunlight which varies along the day especially if the sensor node is in a mobile system, besides shadow that depend on the instantaneous position of the sensor. The general approach for low power solar energy harvesting solutions consists on a simple on/off-threshold charge mechanism relying on a diode connecting the cell with the rechargeable battery [9]. Unfortunately, a diode-based solution is extremely low cost, but the working point of the cell is set by the battery voltage and cannot be adjusted to maximize the energy transfer iwn changing environment. This problem can be address by substituting the diode based solution with a Maximum Power Point Tracker system. Such design method requires the development of adaptive system to transfer the energy generated by the solar cell into a storage element, such as a battery or a super capacitor, while maintaining the working point of the cell around the optimal one (for which the transferred power is maximized).

Figure 2.1: Sensor used for the vibration monitoring.

2.1.1 Project M.I.A.R.I.A.

The M.I.A.R.I.A. project aims at developing an integrated monitoring approach for real time monitoring of alpine scenarios subject to hydro-geological risks. The project addresses the development of a robust, distributed monitoring infrastructure highly reusable in diversified application scenarios with a high resolution in space and time.

One of the applications of this project was the monitoring of a land slide near Lecco (Italy). A cabled sensor network has been installed onto a rock, the aim is to monitor the seismic activity in order to try to predict a possible landslide; for the measurement of the vibrations, MEMS sensors have been used, installed in a shaker directly into the rock, as shown in Figure 2.1.

All the sensors are connected to a main station located at the top of the mountain, where a wireless transmission system is located, and therefore is possible to send the seismic informations in a server in Lecco. The overall system should:

- Withstand cold temperatures in winter and worm temperatures during the summer
- Be reliable over the years. Every maintenance would be expensive and time consuming
- Be efficient
- Ensure high percentages of operating time

Since there weren't space problems, Lead-Acid batteries were chosen, especially for their tolerance to a wide range of temperatures, and because they do not require particular charge profiles.

Power Budget

The first issue to solve is the sizing of the storage and of the solar source. In order to do that, is necessary to analyse the consumption of the overall system:

- The sensors are 10, their consumption is about 30 mA for each module, which are powered with a voltage of 3.3 V.
- The mainboard power consumption is about 250 mW in normal operation
- The wireless module power consumption is about 6.3 W during transmission, but it will be used only once a day for few seconds, in order to transmit the seismic data to the server, located in Lecco.

The average consumption in the end is about 1.25 W.
The nominal power of a solar panel is measured is STC (Standard Test Conditions), or rather at a temperature of 25 $°C$ and a radiation of 1000 W/m^2; observing the historic radiation of Lecco from [17], the month with less sun radiation is December, with a daily average of 4.1 MJ/m^2, and are equivalent to about 47 W/m^2. From the trends of current and voltage of a solar cell shown in Figure 2.2, is possible to observe that the current is basically proportional to the radiation, and the voltage follows a logarithmic behaviour, but basically is constant; with this assumptions it possible to roughly assume that the power is basically proportional to the radiation, and allows to calculate the size of the panel:

$$\frac{P_{PV}\,[W]}{1000\ W/m^2} \cdot 47\ W/m^2 = 1.25\ W \Rightarrow P_{PV} = 27\ W$$

As precaution, two panels of 20 W nominal power had been used.

For ensure high percentages of operating time an adequate size of the energy storage have to be chosen; a lead acid battery of 60 Ah had been chosen: considering its voltage of 12 V, it means that it will be possible to supply the system in absence of sun for about 24 days. So far the system is working continuously since about 2 years.

Power Solution

By a 20 W solar source, with a nominal voltage of 18 V, a 12 V lead battery has to be recharged, in order to collect all the possible energy from the solar module; the battery itself will be the unique source for the sensor network and the main station. The proposed power architecture consists on a DC-DC converter connected directly from the photovoltaic panel to the battery. As shown in Figure 2.3, the DC-DC converter has an inner input voltage control. The MPPT algorithm imposes the input voltage reference $V_{ref_{MPPT}}$ and the converter switching frequency based on the optimization of the battery current $I_{Battery}$, being equivalent to the

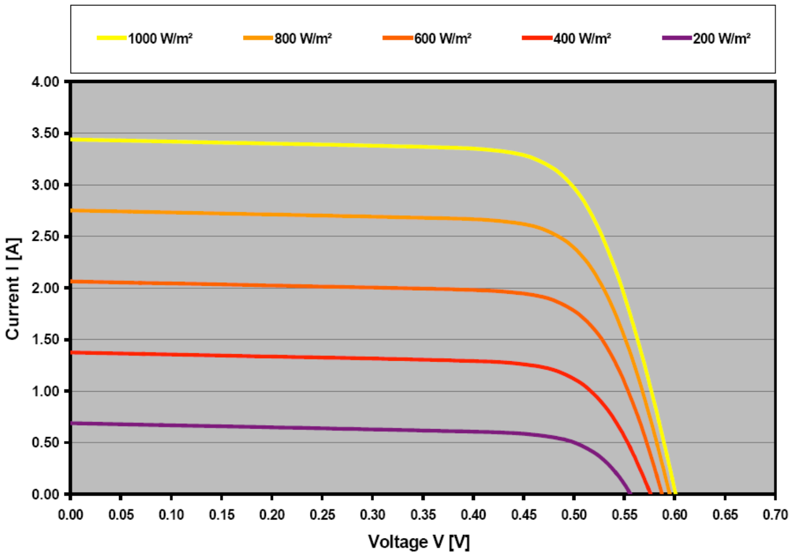


Figure 2.2: Current and voltage behaviour of a commercial solar cell at different radiation levels.

optimization of the output power delivered to the battery under the assumption that the battery voltage variation is negligible during the MPPT perturbation. If this is not verified, the converter output power is measured based on both output voltage and output current sensing. In either case, the output power on the battery is the product of the input power source and of the converter efficiency:

$$\begin{aligned} &P_{OUT}(V_{IN}, V_{Battery}, I_{Battery}, f_{SW}, ..) = \\ &\eta(V_{IN}, V_{Battery}, I_{Battery}, f_{SW}, ..) \cdot P_{IN}(V_{IN}) \end{aligned} \tag{2.1}$$

and it is a function of several parameters and operating conditions. For a given converter, the only two parameters, which are under the control of the DC-DC converter, are the input voltage and the switching frequency and both are used for the delivery of the maximum power to the battery. As far as the DC-DC converter topology, its choice depends on several factors, such as the reduction of the input ripple current, the step-down and step-up capability, etc. and although there are several options available, a SEPIC converter as shown in Figure 2.3, is used. In fact, the SEPIC topology guarantees small input current ripple and it is compatible with the voltage levels of the photovoltaic panel (around 18 V at MPP) and of the battery (between 10 and 17 V) without the need of galvanic isolation. Regarding the conversion ratio, we recall here that, in Continuous Conduction Mode (CCM) operation, the input voltage can be stepped down or up to the bus voltage:

$$\frac{V_{Battery}}{V_{PV}} = \frac{D}{1-D} \tag{2.2}$$

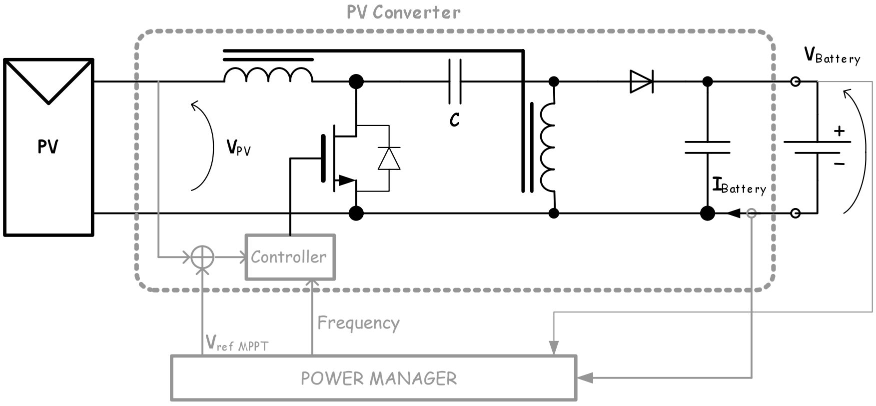


Figure 2.3: SEPIC converter utilized for the photovoltaic conversion with input voltage controller

Furthermore, this converter, by using a coupled inductor, requires only a magnetic element, possibly reducing the board area and the magnetics cost. In order to investigate the effect of converter efficiency as function of the switching frequency, a detailed analysis of converter losses is needed. Instead of performing a detailed loss model, a preliminary converter prototype has been designed and built and the efficiency versus switching frequency trade-off at different power conditions established experimentally. Several approaches for the converter design can be used; in our investigation we have followed the procedure reported in [14, 15], that proposes the design of the power components starting from the maximum output power value, input and output voltages and desired switching frequency, then it is possible to calculate the optimal inductor value and select the appropriate switch and driver. The ripple current in inductors $L1$ and $L2$ is given by:

$$\begin{aligned} \Delta I_L &= I_{IN} \cdot 0.4 = I_{OUT} \cdot \frac{V_{OUT}}{V_{IN(min)}} \cdot 0.4 \\ I_{L1(peak)} &= I_{OUT} \cdot \frac{V_{OUT}+V_D}{V_{IN(min)}} \cdot \left(1+\frac{0.4}{2}\right) \end{aligned} \tag{2.3}$$

where the peak-to-peak ripple current is assumed to be 40% of the maximum input current at the minimum input voltage. If $L1$ and $L2$ are wound on the same core and the leakage effects are negligible, the value of inductance can be calculated by:

$$L1 = L2 = \frac{L}{2} = \frac{V_{IN(min)}}{2 \cdot \Delta I_L \cdot f_{SW}} \cdot D_{MAX} \tag{2.4}$$

Based on this design procedure, a converter prototype with the following parameters is realized: $V_{IN(min)} = 10\ V$, $V_{OUT} = 12\ V$, $f_{SW} = 150\ kHz$ and

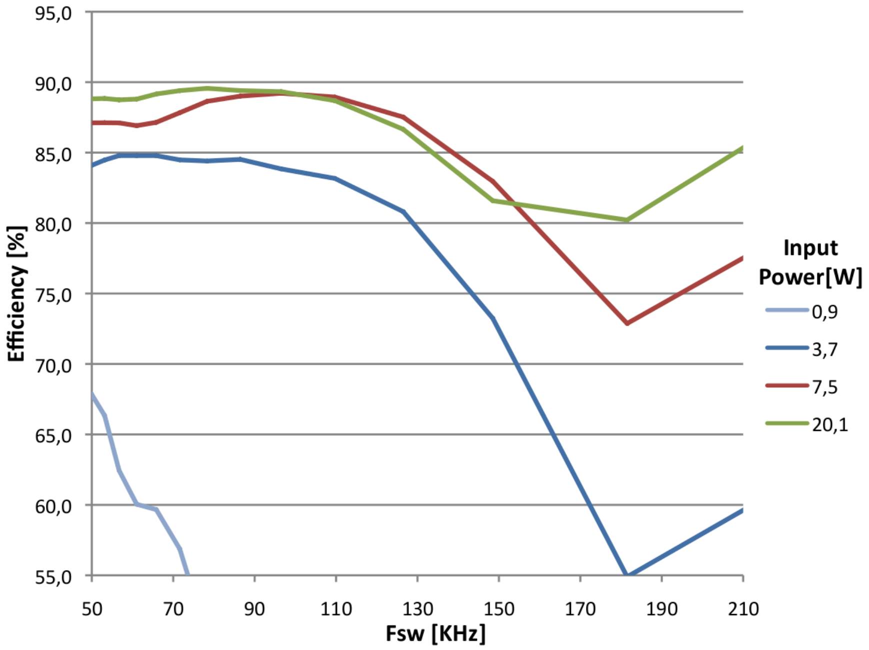


Figure 2.4: Measured efficiency over switching frequency of the realized SEPIC converter at different input power levels, with $V_{IN} = 10\ V$ and $V_{OUT} = 12\ V$.

$\Delta I_L = 0.8\ A$, obtaining an inductor value of about $20\ \mu H$.

The converter efficiency under different input power conditions has been measured, with an input voltage of $10\ V$ and an output voltage of $12\ V$, the results are reported in Figure 2.4. As can be seen, the efficiency strongly depends on the operating frequency and, more importantly, the switching frequency at the maximum efficiency point significantly changes with the input power. Thus, independently on the specific design adopted and the results here reported, the switching frequency should be adapted to maintain the efficiency at the maximum level. Although in principle it is possible to establish a priori the relationship between η and f_{SW} and store it in a look-up table, the accurate model is very complex and it should include several parameters (such as the operating temperature, thermal feedback, converter parasitics, etc.); thus, an on-line optimization is preferred.

One of the main issues of the proposed approach is the possible presence of multiple maximum points. As shown in Figure 2.4, this efficiency is increasing again for $f_{SW} > 180\ kHz$ for some input power levels. While this issue is still under investigation, hereafter the switching frequency has been limited in an interval closer to the originally designed value ($150\ kHz$), thus avoiding the presence of multiple maxima in the efficiency curve.

The two-dimensional optimization method utilized is also known as Nelder-Mead method or downhill simplex method or amoeba method [16]. This method guarantees a simple optimization technique that can be easily implemented in a microcontroller based platform. The method uses the concept of a simplex, which

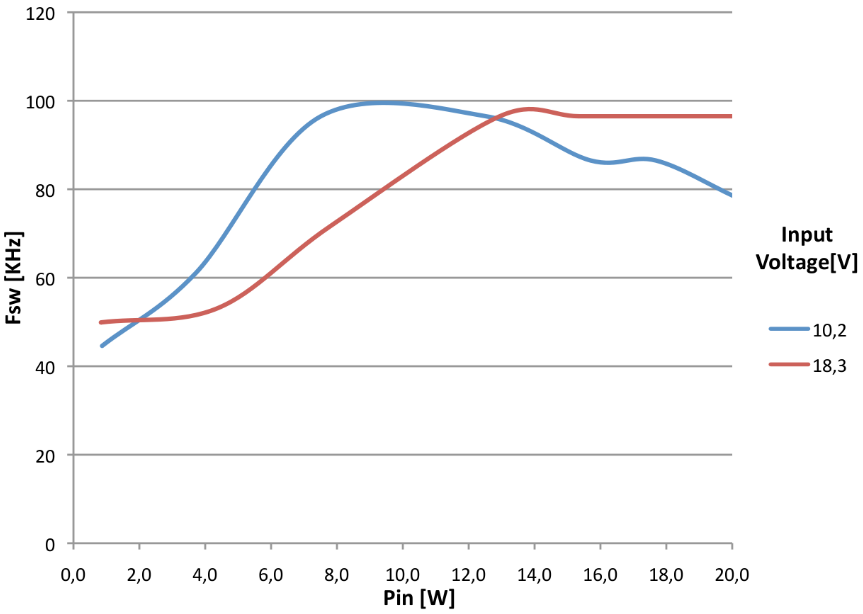


Figure 2.5: Optimal switching frequency value over input power level, at different input voltages.

is a polytope (i.e. a two-dimensional polygon) of three vertices in two dimensions (or, in general, of $N+1$ vertices in N dimensions). The method approximately finds a locally optimal solution to a problem with N variables when the objective function varies smoothly. Nelder-Mead algorithm generates a new test position by extrapolating the behaviour of the objective function measured at each test point arranged as a simplex. The algorithm then chooses to replace one of these test points with the new test point and so the algorithm progresses. The simplest step is to replace the worst point (i.e. the point with the lower cost function) with a point reflected respect to the line identified by the remaining points (*Reflection*). If this point is better than the best current point (i.e. the cost function at this point is higher that the cost function of the other points), then is tried stretching exponentially out along this line (*Expansion*). On the other hand, if this new point is not better than the previous value, the algorithm shrink the simplex towards the best point (*Contraction*). In order to understand the algorithm, let's consider a simple example shown in Figure 2.6. The converter efficiency (i.e. the cost function) is measured in three different points, being each point a vector $\vec{P_i} = [f_{SWref_i} \quad V_{INref_i}]$; the first step is to identify the point with the minimum efficiency and, for the purpose of explanation, let's assume that:

$$\eta(\vec{a}) < \eta(\vec{b}) < \eta(\vec{c}) \tag{2.5}$$

The lowest point $\vec{a}$ is then moved to the opposite side (point $\vec{d}$) of the original

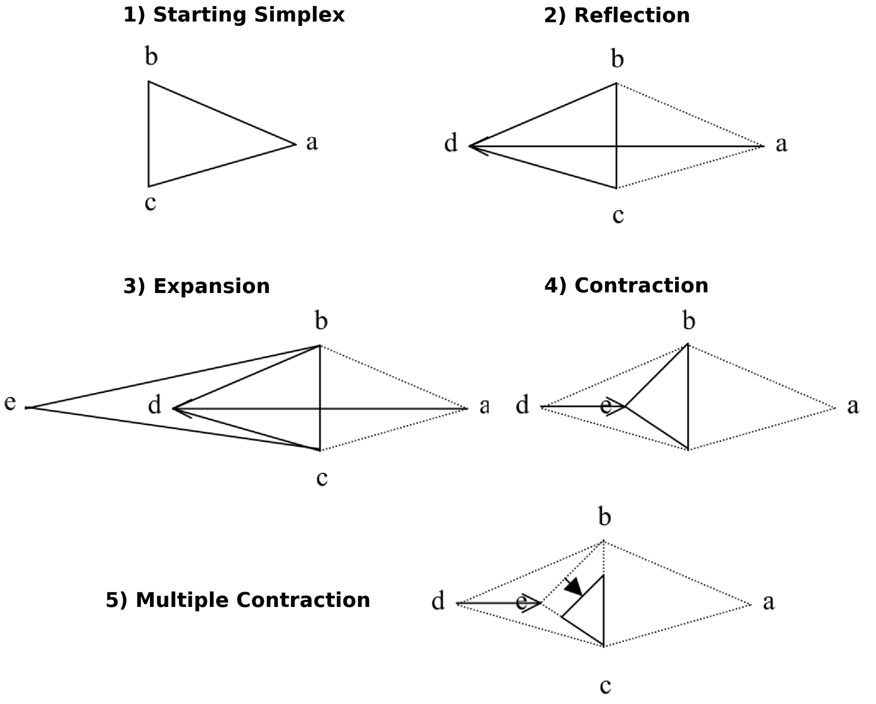


Figure 2.6: Downhill simplex algorithm: 1) Reflection of the lowest point. 2) Reflection and expansion. 3) Contraction toward the best point. 5) Multiple contraction toward the best point.

simplex, as seen in Figure 2.6-2, thus reflecting point a along the line $\vec{b} - \vec{c}$:

$$\vec{d} = \vec{b} + \vec{c} - \vec{a} \tag{2.6}$$

If the new point $\vec{d}$ has an higher efficiency than the previous highest $\vec{c}$, the new point is expanded, as in Figure 2.6-3:

$$\vec{e} = 2 \cdot \vec{d} - \frac{(\vec{b} + \vec{c})}{2} \tag{2.7}$$

If the new point $\vec{d}$ has an lower efficiency than the point $\vec{b}$, $\vec{d}$ is contracted as in Figure 2.6-4 in:

$$\vec{e} = \vec{d} - \frac{\vec{d} - \frac{\vec{b}+\vec{c}}{2}}{2} \tag{2.8}$$

If the new point $\vec{e}$ is still the lowest among $\vec{b}, \vec{c}, \vec{e}$, points $\vec{b}$ and $\vec{e}$ are contracted around the highest point $\vec{c}$ as in Figure 2.6-5:

$$\begin{aligned} \vec{e} &= \vec{e} - \frac{\vec{e} - \vec{c}}{4} \\ \vec{b} &= \vec{b} - \frac{\vec{b} - \vec{c}}{4} \end{aligned} \tag{2.9}$$

In all of the other cases we start the algorithm again with the updated points of the simplex.

In the algorithm if we avoid the points to collapse in a single one or align between themselves we obtain a sort of bidimensional perturb and observe algorithm that allows adjusting the maximum efficiency point.

The coupled inductor is sized using Equation (2.4), obtaining a value of 20 μH, the drivers and mosfets used are respectively UCC27322 and IRF1902. The controller utilized for this converter is a commercial controller Si9145 working from 45 kHz to 250 kHz, limited by the microcontroller at 180 kHz to avoid multiple maxima points: the switching frequency is determined by a capacitor and a resistance, and it was adjusted by a 100 $k\Omega$ digital potentiometer, CAT5114, controlled by the PIC device. The input voltage reference is still generated by the controller using a filtered PWM signal. The experimental results are shown in Figure 2.7 and 2.8 [17]. In order to test the 2-D MPPT algorithm under controlled operating conditions, the photovoltaic module for simplicity is emulated with a constant voltage generator of 20 V with a series resistance of 5 Ω, such the maximum obtainable power is 20 W at 10 V. Moreover, the output voltage is fixed by an active load emulating the load battery. The switching frequency is shown as a voltage reference realized by a PWM channel of the microcontroller, at 0 V the switching frequency is 45 kHz and at 5 V is 180 kHz: it is possible to see that the algorithm reaches the optimal points, which are [100 kHz 10 V] for the

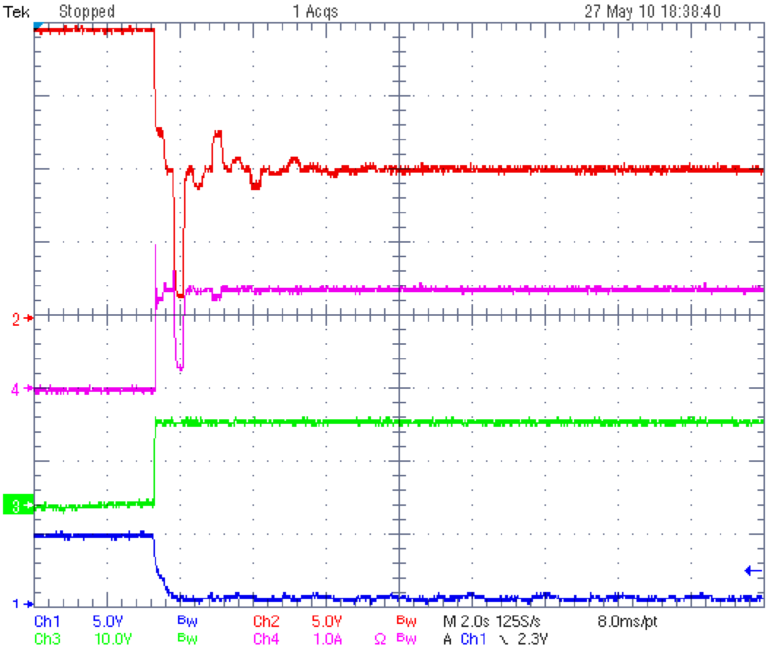


Figure 2.7: System main waveforms during the start-up transient with an input power of 20 W. Channel 1) is the frequency reference f_{SWref}, 2) is the input controlled voltage V_{PV}, 3) is the output voltage channel $V_{Battery}$ or V_{OUT}, which is connected to the active load, 4) is the input current I_{IN}.

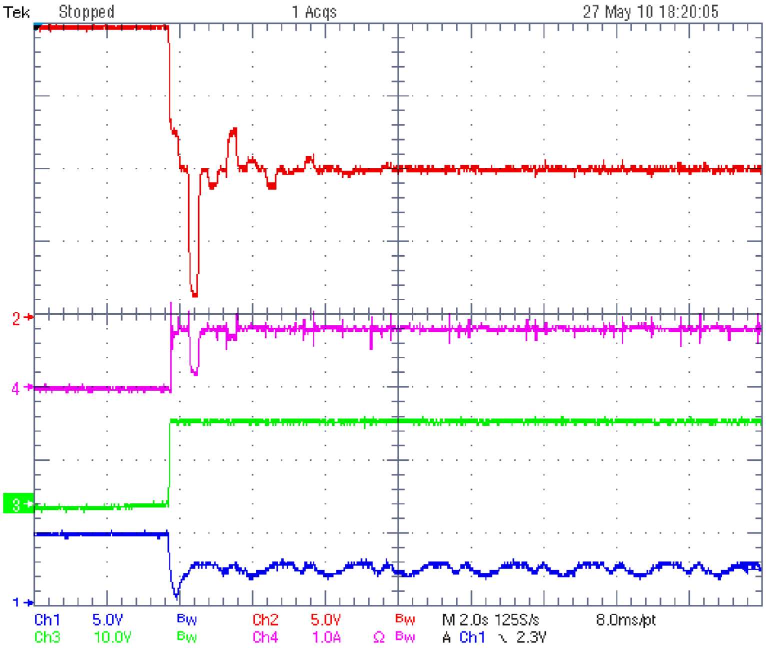


Figure 2.8: System main waveforms during the start-up transient with an input power of 9 W. Channel 1) is the frequency reference f_{SWref}, 2) is the input controlled voltage V_{PV}, 3) is the output voltage channel $V_{Battery}$ or V_{OUT}, which is connected to the active load, 4) is the input current I_{IN}.

Figure 2.9: Main station of the project M.I.A.R.I.A.

configuration of Figure 2.8, and [78 kHz 10 V] for the configuration of Figure 2.7.

The main drawback of this solution is a frequency fluctuation at low power levels, due to the presence of a flat maximum and a low resolution current sensing; in fact, the simple, low cost current sense, and the low-resolution ADC of the microcontroller do not have the accuracy needed for changing the state with very small current variations: in the example of Figure 2.8 the current variation from 86 kHz to 126 kHz is only 8 mA, that causes a voltage variation of 8 mV on the 10 bits microcontroller's ADC, which has a resolution of 4.8 mV. This issue can be solved either with additional gain of the current sensing or reducing the quantization level of the current ADC.

The main station with the solar panels and the wireless antenna is shown in its location in Figure 2.9, the power converters, the main board and the battery are isolated in the protected box.

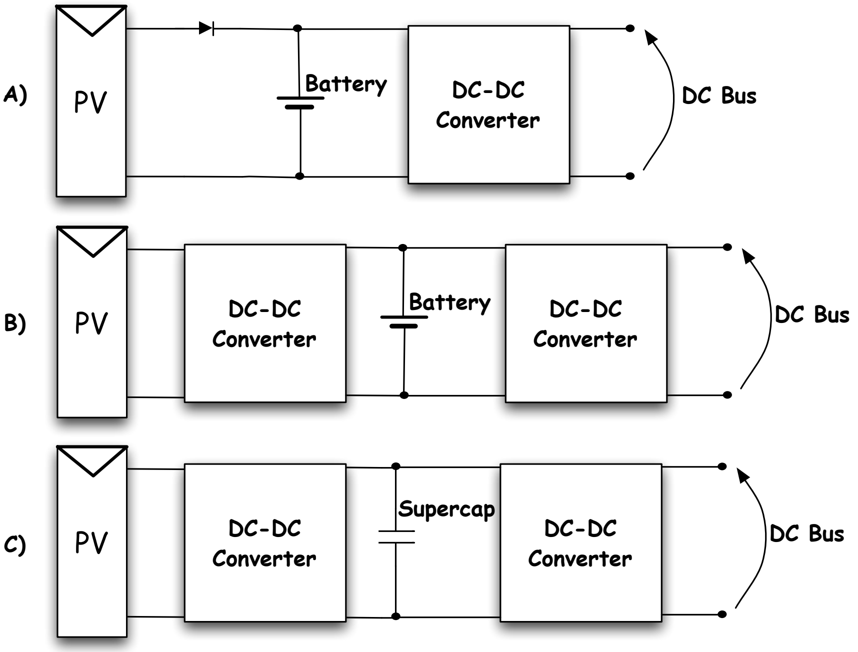


Figure 2.10: Standard solutions for solar energy harvesting.

2.1.2 Wireless Distributed Nodes

As explained a wireless sensor network consists on a large number of micro-sensors distributed in an area of interest, however is not always possible to directly connect all the sensors as in the previous example, but it is desirable to have a wireless connection between sensors and a main station, and ideally each node should be energy autonomous, compact, and without the need of battery replacement and disposal.

A simple and low cost way to extract and store energy from a photovoltaic source is to connect the solar panel directly to a battery with a diode [18], as shown in Figure 2.10-A. The main disadvantage of this solution is that the system does not always work in the optimal condition to convert the available solar energy. To improve the system performance, a controller can be added between the PV panel and the battery [9, 18, 19], as shown in Figure 2.10-B. The controller is usually a DC-DC converter and controls the input voltage or current so that the extracted energy is maximized, and the output voltage is fixed by another DC-DC converter; in the case of using a supercap as energy storage [20], the scheme is shown in Figure 2.10-C and generally the output converter is a step-up converter because of the low voltage of the supercapacitors. Maximum power point tracking (MPPT) circuits differentiate themselves in the design of the power converting electronics and/or in the control strategy, but the charging of batteries in presence of fluctuating power sources remains an open issue. For example, Figure 2.11

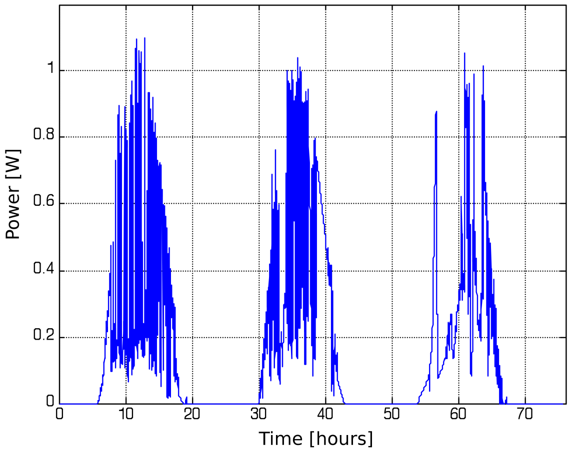


Figure 2.11: Power obtainable by a PV of 2 W nominal power in a mobile system constituted by a buoy on the sea.

reports the power obtainable by a solar panel of 2 W nominal power, in a mobile system constituted by a buoy on the sea; as can be observed, even if the weather condition is good, the irradiation is in tropical condition, and the temperature is maintained stable by the sea water, the available power has a large fluctuation due to the wave motion that changes the instantaneous orientation. This situation is incompatible with the charging of high-density accumulators, like the lithium batteries, where a precise charge mechanism is required to preserve the lifetime of the battery [9, 21–26] which is generally composed by a constant current phase and a constant voltage phase.

The following solution proposes an hybrid accumulator architecture that combines the advantages of the supercapacitors in terms of lifetime and charge/discharge cycles (10 years and millions of charge-discharge cycles [27]) and the lithium batteries for their highest energy density and costs; the power management is addressed to increase the lifetime of the storages, especially the lifetime of the Li-Ion battery, which is typically the bottleneck of endurance in energy autonomous sensor nodes.

Degradation Mechanisms in Li-Ion ($LiCoO_2$) batteries

For better understanding the charge strategy used in the proposed architecture, it is useful to explain the mechanism that affects the lifetime of the Li-Ion batteries. Chemistry, performance, cost, and safety characteristics vary across Li-Ion Battery (LIB) types. Handheld electronics mostly use LIBs based on lithium cobalt oxide, which offers high energy density, but have well-known safety concerns, especially when damaged. Lithium iron phosphate, lithium manganese oxide and lithium nickel manganese cobalt oxide offer lower energy density, but longer lives and inherent safety. These chemistries are being widely used for electric tools, medical equipment and other roles. Lithium nickel manganese cobalt oxide in particular is a leading contender for automotive applications. Lithium nickel cobalt aluminium oxide and lithium titanate are specially designs aimed at particular niche roles. Below lithium cobalt oxide $LiCoO_2$ batteries are considered, which are, as explained, the chemistry which has one of the the highest energy density and are very common on the market.

In general terms, the charge procedure consists in two phases: a constant current phase and a constant voltage phase; the charge current in expressed as a rate of the nominal capacitance, for example charging a battery of 1000 mAh with a current of 1 A, means charging at 1 C; this phase requires the 20-30% of the charging time and allows the 70-80% of the total charge [25]. This state ends when the maximum cell voltage is reached (generally 4.2 V), and the second phase starts. In this last phase (constant voltage phase), the cell voltage is maintained until the current drops under the minimum current, that depends on the C rating of the battery or for a certain period of time. This last stage requires the 70-80% of the total time and allows the 20-30% of the total charge, but a long float-charge period at 4.2 V or above is one of the causes of the lifetime reduction of the cell [21], as shown in Figure 2.12, whose values are obtained from real experiments made by [21] on a $LiCoO_2$ cell.

Another factor of degradation in Li-Ion batteries is the high charge rate, i.e. > 0.5 C, this can be shown in Figure 2.13 (results from [21]). At low charge rates < 0.5 C the degradation generally is independent of the charge rate.

The worst degradation factor is the overvoltage condition: as can be seen in Figure 2.14 (results from [21]), charging the battery at a voltage above the nominal voltage, causes a rapid decrease of the overall capacity.

From this consideration, it is possible to obtain some guidelines for the optimal solar battery charger for increasing the lifetime of the Li-Ion cells:

- The constant current phase, or CC, should be done at a low current rating (< 0.5 C), condition not always guaranteed in a solar battery charger, it depends on the nominal power of the photovoltaic module and on the instantaneous irradiation.
- The CC stage should stop if the nominal voltage is exceeded.
- The constant voltage stage should be avoided. The drawback of this choice is loosing a part of the capacity of the battery (20-30%).
- The number of charge/discharge cycles should be as low as possible. As previously explained the current coming directly from a photovoltaic cell

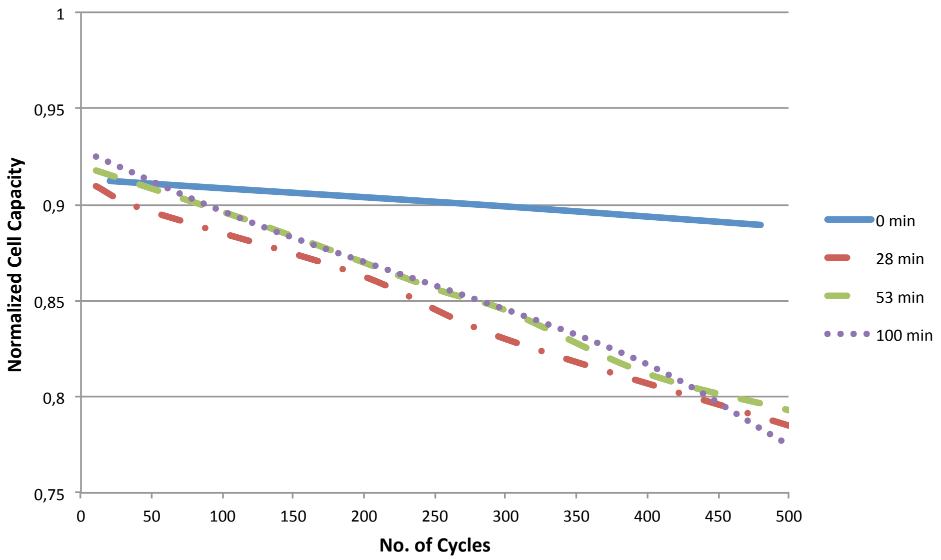


Figure 2.12: Effect of CV charge period at 4.2 V on cycle performance (data extracted from [21]). Test cells charged at constant current at 1 C rate to 4.2 V followed by the CV float charging at this voltage for various periods and then discharged to 2.75 V at 1 C rate.

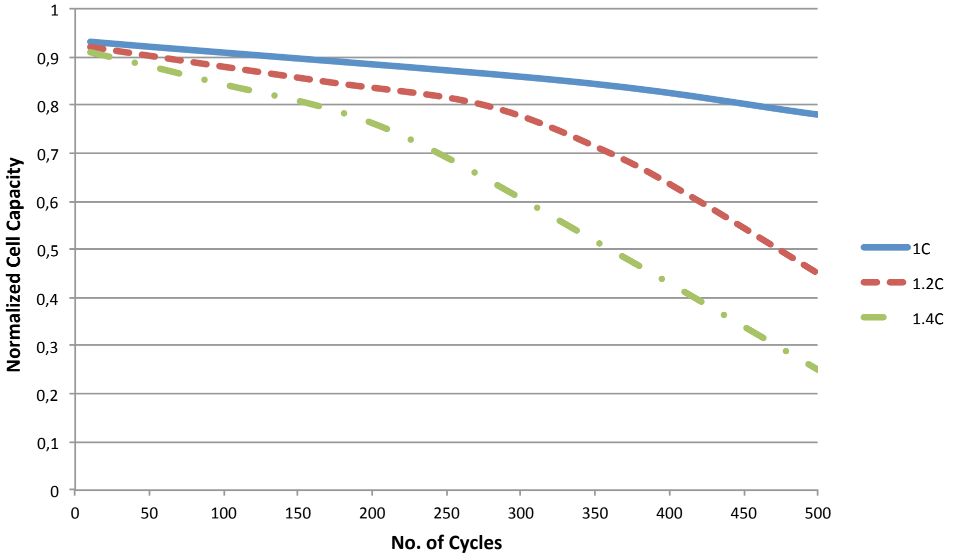


Figure 2.13: Effect of charge rate on cycle performance (data extracted from [21]). Test cells charged at constant current at various rates to 4.2 V followed by CV float charging at 4.2 V for 2.5 h and then discharged to 2.75 V at 1 C rate.

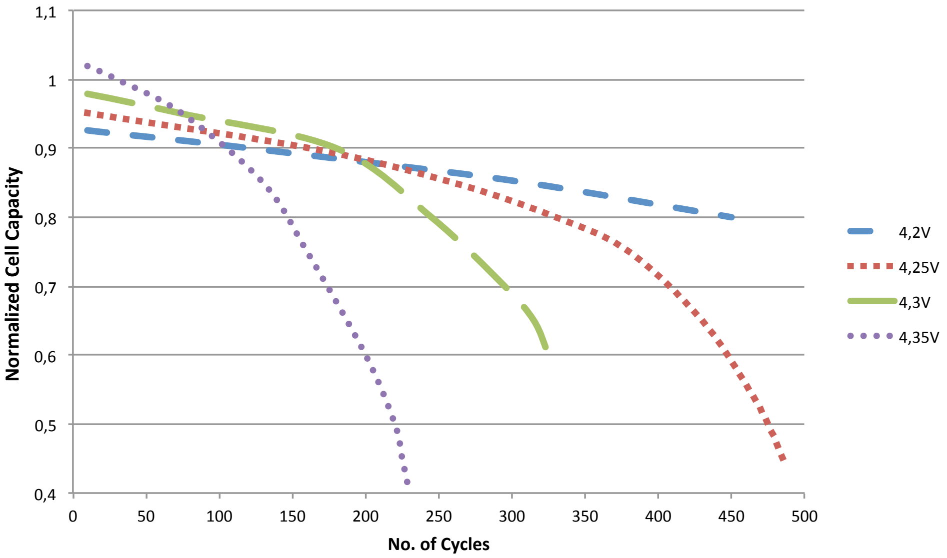


Figure 2.14: Effect of CV charge voltage on cycle performance (data extracted from [24]). Test cells charged at constant current at 1 C rate to cut-off voltage followed by CV float charging at this voltage for 2.5 h and then discharged to 2.75 V at 1 C rate.

due to the weather conditions is not constant. Quite often as a result of cloud formations passing in front of the sun, the current will be fluctuating. The result of this fluctuating input current is a recharging sequence that is quite often interrupted. The battery is charged for a while but before it is fully charged it is already partially used or discharged. Whether this is causing capacity fading is not clear. Note, however, that these cycles are shallow discharge cycles and small discharges and pulsed charging are sometimes claimed to enhance battery lifetime [26]. In this work only complete charge/discharge cycles are considered: the total charge stored in the battery is integrated and then divided for the nominal energy of the battery:

$$n_{cycles} = \frac{\int E_{charge}(t)\, \mathrm{d}t}{E_{battery}} \tag{2.10}$$

Power Management Architecture and Control

The proposed power management architecture is reported in Figure 2.15, where three DC-DC converters are connected in parallel to the DC power bus. The first converter, denoted DC-DC PV interfaces the PV panel to the DC power bus, the second, denoted DC-DC battery connects the DC bus to the battery and the third, denoted DC-DC Supercap connects the DC bus to the supercapacitors. The internal power bus is the main power supply of the electronic systems utilized by sensor node.

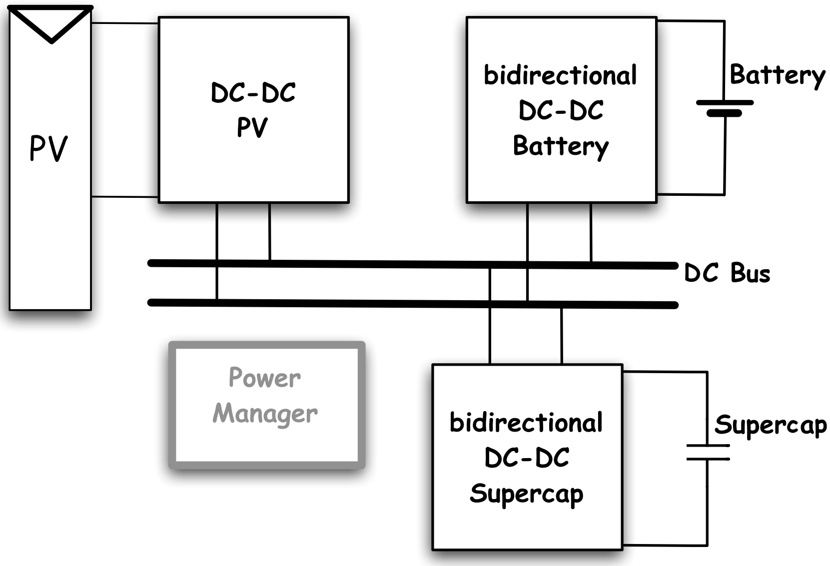


Figure 2.15: Architecture of the proposed power management

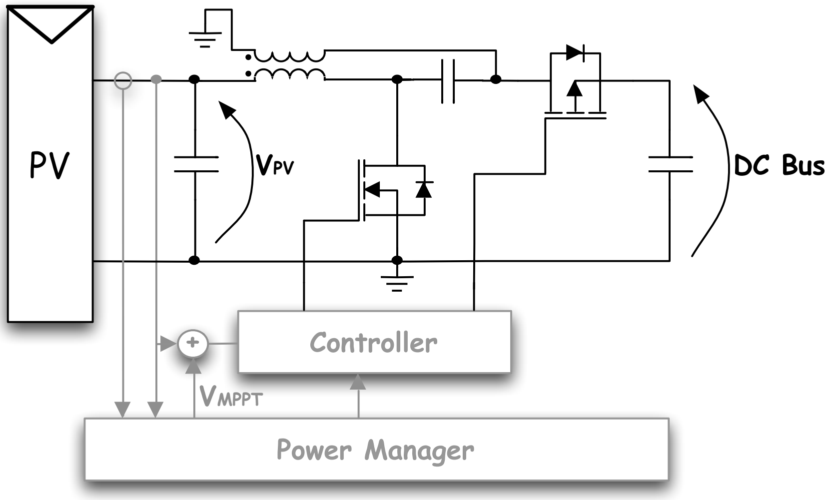


Figure 2.16: Sepic converter utilized for Photovoltaic conversion with input voltage controller

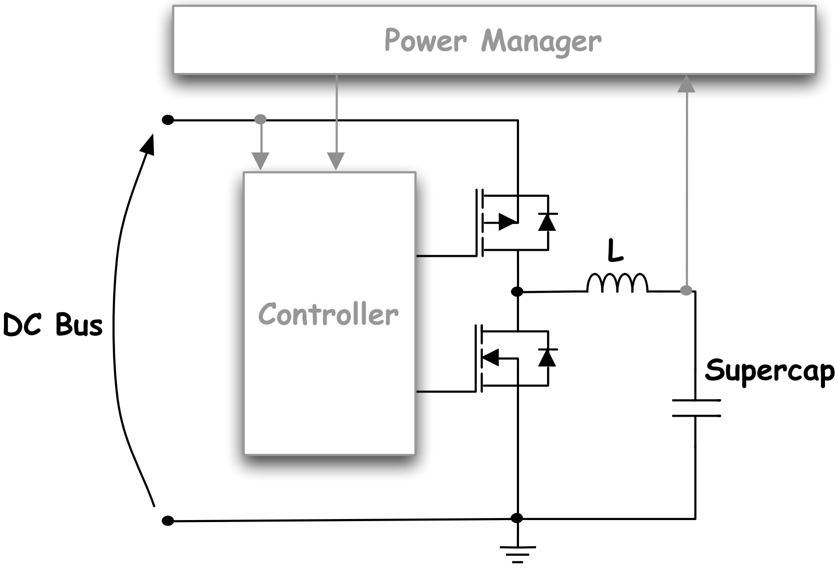


Figure 2.17: Bidirectional Buck converter connected to the supercapacitor

The DC-DC PV converter realizes the MPPT of the photovoltaic module: the input voltage of the converter is controlled by a feedback loop and the reference is determined either by the source MPPT or by the control on the supercapacitor voltage, depending on the state of the power management algorithm. The DC-DC PV converter is based on a synchronous Sepic topology as reported in Figure 2.16; this solution guarantees small input current ripple and it is compatible with the voltage of our photovoltaic cell (about 5 V) because, in CCM operation, the conversion ratio can be stepped down to the bus voltage as explained in Equation 2.2.

The DC-DC Supercap converter is a bidirectional converter synchronous buck converter reported in Figure 2.17; several bidirectional, high efficiency converters are present in literature, also specifically for battery applications [28–31], but for cell balancing in high energy battery packs, or for interface supercaps and batteries to an high voltage (tens of V), high power (hundreds of W) DC bus, they require several switches, magnetic components or complex controls, that don't easily enable high efficiencies at low loads (mW) like in our application. For this reason a simple buck converter has been chosen. The converter operates in step-down mode when the current flows to the supercapacitor, and in step-up mode when energy from the supercapacitor is needed, being the typical maximum voltage of a supercap about 2.7/2.5 V [27]. This converter controls the DC bus voltage operating as a sink or a source depending on the instantaneous power budget of the system as explained in next section.
The proposed architecture presents a direct power conversion from the solar panel

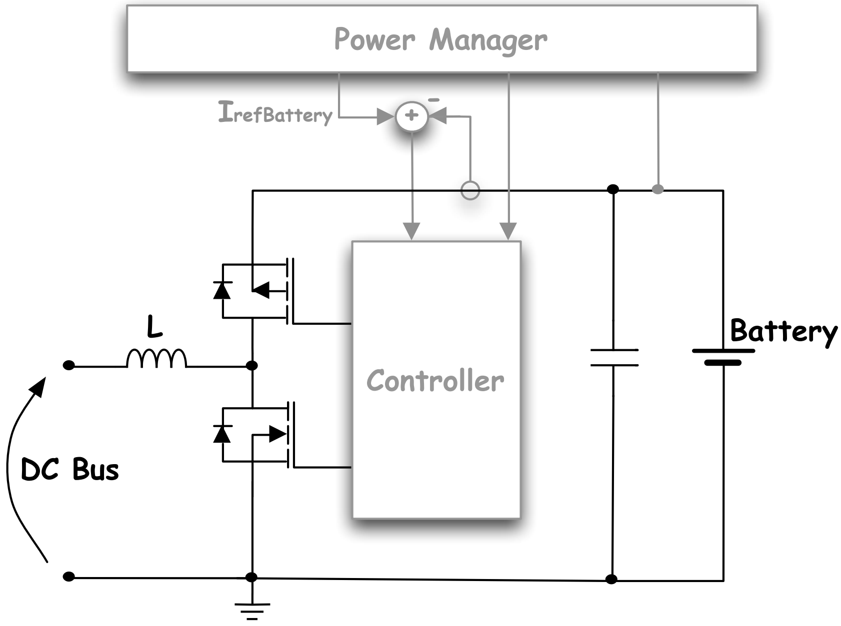


Figure 2.18: Bidirectional Boost converter connected to the Battery

to the load bus. The extra power available on the bus, due the difference between the source and load power, is stored in the supercapacitor and can be utilized by the conversion system when a reduction of the available power on the source is present. The stored energy can be designed to manage the variation of the instantaneous power guaranteeing the power to the load in portable system, to supply the system for many hours without irradiation or provide the energy necessary for charging the battery in case of fluctuation of the input power.
By utilizing the bidirectional DC-DC converter, the supercapacitors are connected in parallel without requiring an over voltage protection system on each element that is needed in the serial connection as in [32].
The DC-DC battery converter is a bidirectional boost converter, as shown in Figure 2.18, to charge and to utilize the battery at the same time depending on the working conditions. This choice is dictated by the required voltage level of the battery, respect to the DC power bus, in fact the lithium battery has a nominal voltage of 4.2 V and the DC bus voltage is 3.3 V. This converter operates like the DC-DC Supercap converter, but has a current controlled loop, and the power management algorithm decides the current reference based on the charging/discharging state of the battery.

The power management algorithm is basically based on six different states. In the first stage, the "Off" stage, all the storages are discharged, the controller is in sleep state and all the converters are disabled; when the energy provided from the solar module is sufficient for power the controllers, a start-up procedure

occurs. If the input power is sufficient the algorithm moves to the "Soft Start" stage; the "DC-DC PV" converter starts to control the input voltage and the controller provides the voltage reference for realize the MPPT, the "DC-DC Supercap" controls the voltage of main DC bus and the energy difference between the input solar panel and the load is stored in the supercap, the "DC-DC Battery" converter is still disabled. This stage lasts until the capacitor reaches 1.9 V, when a sufficient energy is stored for start charging the battery: in fact if there are input power fluctuations the energy stored in the supercap should help the system to provide a constant current for the battery charging. In the "Battery Charge" stage, the input stage is still working, and MPPT implemented, but now the "DC-DC Battery" converter is enabled if the battery voltage is less than the maximum voltage: the battery can be charged with a constant current. If the voltage across the supercap is greater than the maximum voltage (2.5 V), which means that the input power is grater than the load power and the power needed for recharge the battery, the algorithm moves to the "Overvoltage" stage, where the input stage is disabled to avoid the damage of the supercap, and the battery is still in charge mode. If the supercap voltage drops below 0.9 V, means that the input power is not sufficient for recharge the battery and the control moves to the "Supercap Charge" stage: the battery converter is disabled; the grey stages are the only two where the battery charging can be done, this is decided according to the battery voltage: if it's low the charging phase can starts, otherwise if the voltage is near the maximum voltage the "DC-DC Battery" converter is disabled. It is preferable that the battery is fully charged in the "Overvoltage" stage so that the system will be with both storages fully recharged. The last stage is the "Battery Discharge" stage, this occurs when the supercap voltage drops below 0.8 V, and means that the input power is not enough to supply the load and the supercap is exhaust; in this phase the battery is discharged in the DC bus at a constant current and consequently the supercap recharged until its voltage reaches 2 V or is present enough power at the input stage. If, for example, there is no input power for a long time, the systems alternates between the "Battery Discharge" stage and "Supercap Charge" until the battery and the supercap are both without energy and the system goes to "Off".
With this type of architecture and control strategy the guidelines described in the previous paragraph for the optimal solar battery charger for increasing the lifetime of the Li-Ion cells are implemented.

Storage and Source Sizing

In this type of remote applications, it is difficult to evaluate the size of the sources and storages. In some places, it is common to have several weeks without sufficient sunlight to provide energy to the remote sensor node; for this reason the sizing should be done with a statistical approach, to ensure a certain percentage of

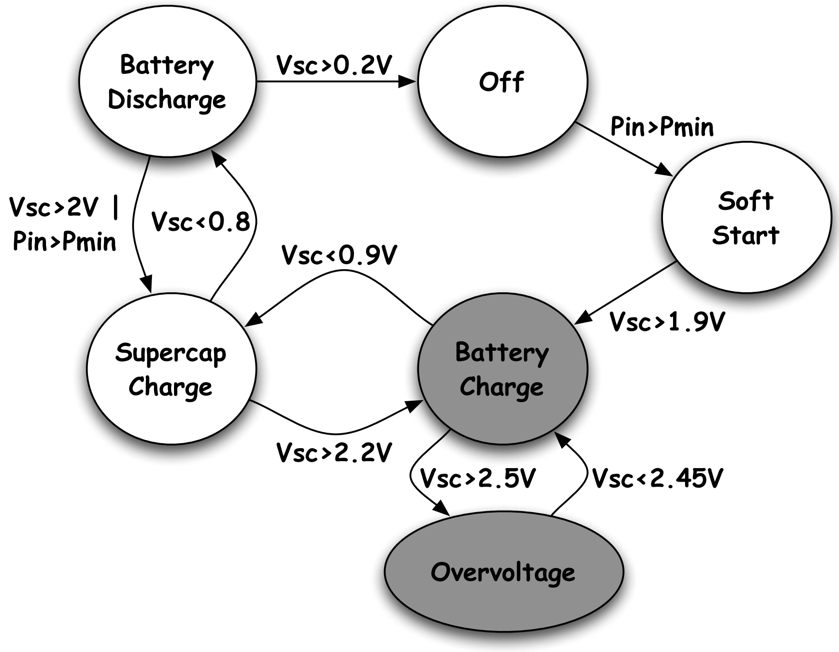
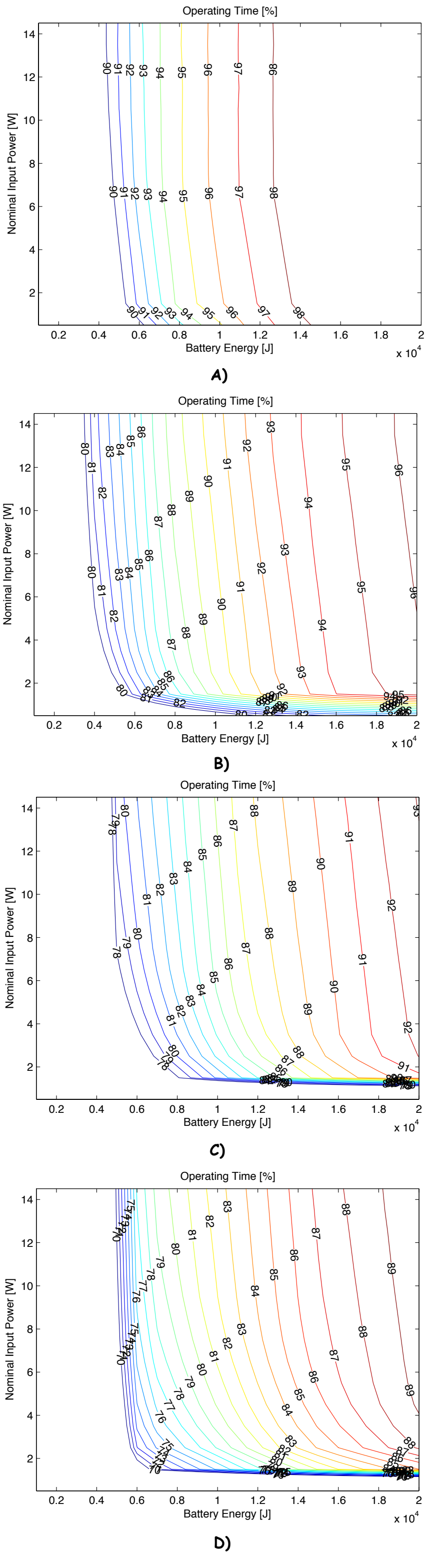


Figure 2.19: Power management block diagram of the proposed solution.

working time of the remote system during the year.
As the penetration of photovoltaic systems is increasing, it is not difficult to obtain the historic values of their generated power; with these data it is possible to obtain an estimation of the average power that can be generated from a certain nominal photovoltaic source in a certain place, and to simulate the behaviour of a solar storage system. This solution proposes a sizing strategy based on a historical of power values of 238 days, from 8 July 2010 to 4 March 2011 of the M.I.A.R.I.A. station.
The proposed design procedure starts from the power source and the stored energy necessary to achieve a specified operating time, then it is possible to size the supercapacitor for reduce the number of charge/discharge cycles of the battery. With a Matlab-Simulink model of the architecture of Figure 2.10-B,the behaviour of the circuit with different loads was simulated using the historical power values mentioned earlier, and the charts in Figure 2.20 were obtained; the simulated control algorithm is very simple: it charges the battery with the input power recorded data, and, if the battery voltage exceeds the maximum, the input power is switched off.

This result is very interesting and shows that at low power loads, the operating time depends almost uniquely by the size of the storages; in our case the consumption of the wireless sensor is 0.3 W with a duty cycle of 5 min/hour, which is equivalent to an average power of 0.025 W, but the consumption of the two bidirectional converters has to be added; the overall load is estimated to be



A)

B)

C)

D)

Figure 2.20: Simulated operating time of the circuit in Figure 2.10-B, in function of the photovoltaic nominal input power and battery energy, with a constant load of 0.025 W (A), 0.05 W (B), 0.075 W (C) and 0.1 W (D).

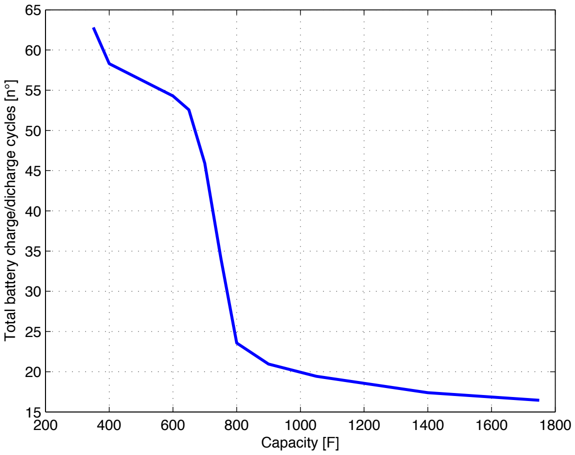


Figure 2.21: Number of equivalent charge/discharge cycles, as defined in Equation (2.10), in function of the capacity of the supercap.

about 0.05 W.

In our application an operating time of 88-90% is sufficient so a 5 W solar pannel ad a 10 kJ storage is sufficient to supply the sensor, which is equivalent to a Li-Ion battery of about 700 mAh; a commercial battery for mobiles of 680 mAh has been chosen, the photovoltaic module instead has a nominal power of 5 W, a open circuit voltage of 6.6 V and a short circuit current of 904 mA. Note that the same amount of energy stored can be obtained with a supercap of about 3000 F, but this solution would be very expensive and cumbersome.

The next step is to size the supercapacitor; a detailed Simulink model of our architecture has been developed, and controlled by a state machine that implements the control algorithm explained in the previous paragraph in order to simulate the entire system and estimate the charge/discharge cycles saved. To make the model as real as possible, several factors were considered: first, the converter efficiency was set at 80%, the internal resistance of the battery which dissipates energy, the supercap leakage current, set at 1 mA, and the auto-consumption of each converter was estimated to be about of 0.07 W with the real components used in the prototype, consumption that obviously was considered only when the converter is active. The supercap converter is the only one that works for all the time, and is designed to operate in light load conditions with a pulsed frequency modulation, to reduce the auto consumption and increment the efficiency; this feature is implemented in the model. Another non-ideal factor considered is the absence of the constant voltage phase during the charge process; thus, as previously discussed, a 15% of the available capacity of the battery has not been used; the charge current instead is set at 300 mA (less than half the C rating), and the discharge current at 150 mA.

With this model it has been possible to simulate the number of charge/discharge cycles of the battery, as defined in (2.10), varying the capacity of the supercap, obtaining the Figure 2.21. In our application a capacity of 1050 F has been chosen (three caps of 350 F), obtaining in the simulation an equivalent average load of about $37mW$ (neglecting che auto discharge of the supercapacitors), a simulated operating time of 89.28% and an equivalent number of charge/discharge cycles of 18; the waveforms of the 238 day's simulation are reported in Figure 2.22: the first image represents the overall load of the circuit and includes all the losses and the auto consumption of the converters, as previously explained, note that the consumption of the wireless sensor is 0.3W with a duty cycle of 5min/hour; the second image represents the instantaneous input power of the solar panel, the third image is the supercap voltage, the fourth image is the status of the control state machine, for simplicity the states are numbered: 0 is the Off state, 1 is the Soft Start state, 2 the Battery Charge state, 3 the Over Voltage state, 4 the Supercap Charge state, and 5 is the Battery Discharge state, coherent with Figure 2.19; the last figure is the total instantaneous energy of the battery. Considering the same average load in the Simulink model of Figure 2.10-B, used for sizing the battery, the number of charge/discharge cycles applied to the battery with the traditional architecture were estimated to be about 87 cycles, that means almost 4.8 times the cycles required by our architecture. The different slopes in Figure 2.21 can be interpreted as follows: the greatest increase of saved charge cycles is obtained using a supercap that can supply the circuit for all the night without using the battery (as visible from the voltage battery and energy in the simulation of Figure 2.22); then the saved cycles becomes less, because the only benefit is to increase the overall storage energy and so the operating time, operation that can be made using an higher capacity battery.

The power manager is implemented by a microcontroller of the Microchip family (PIC18F2620), and it works with a quartz crystal oscillator of 4 MHz for reduce the consumption. The controller utilized for each of the tree converters is a TPS43000; the sepic converter is realized with a coupled inductor from Coilcraft MSD1278, of 10 μH, the two mosfets are a FDS9934C and operates at a switching frequency of 250 kHz.

The two bidirectional converters works at the same frequency, which is 490 kHz and the inductors are SER1360 of 10 μH each, produced by Coilcraft: this choices were made to reduce the current ripple and the switching losses at low loads ; the high side mosfets are IRF7433 and the low sides mosfets are IRF1902, both driven directly from the internal driver of the TPS43000; infact mosfets with a low total gate charge (Q_g) are chosen to reduce the driving losses. Two current senses are needed to implement the algorithm previously described, one on the input source for measure the instantaneous power of the solar module, and one to measure the battery current, both realized with an INA213. The supercaps are

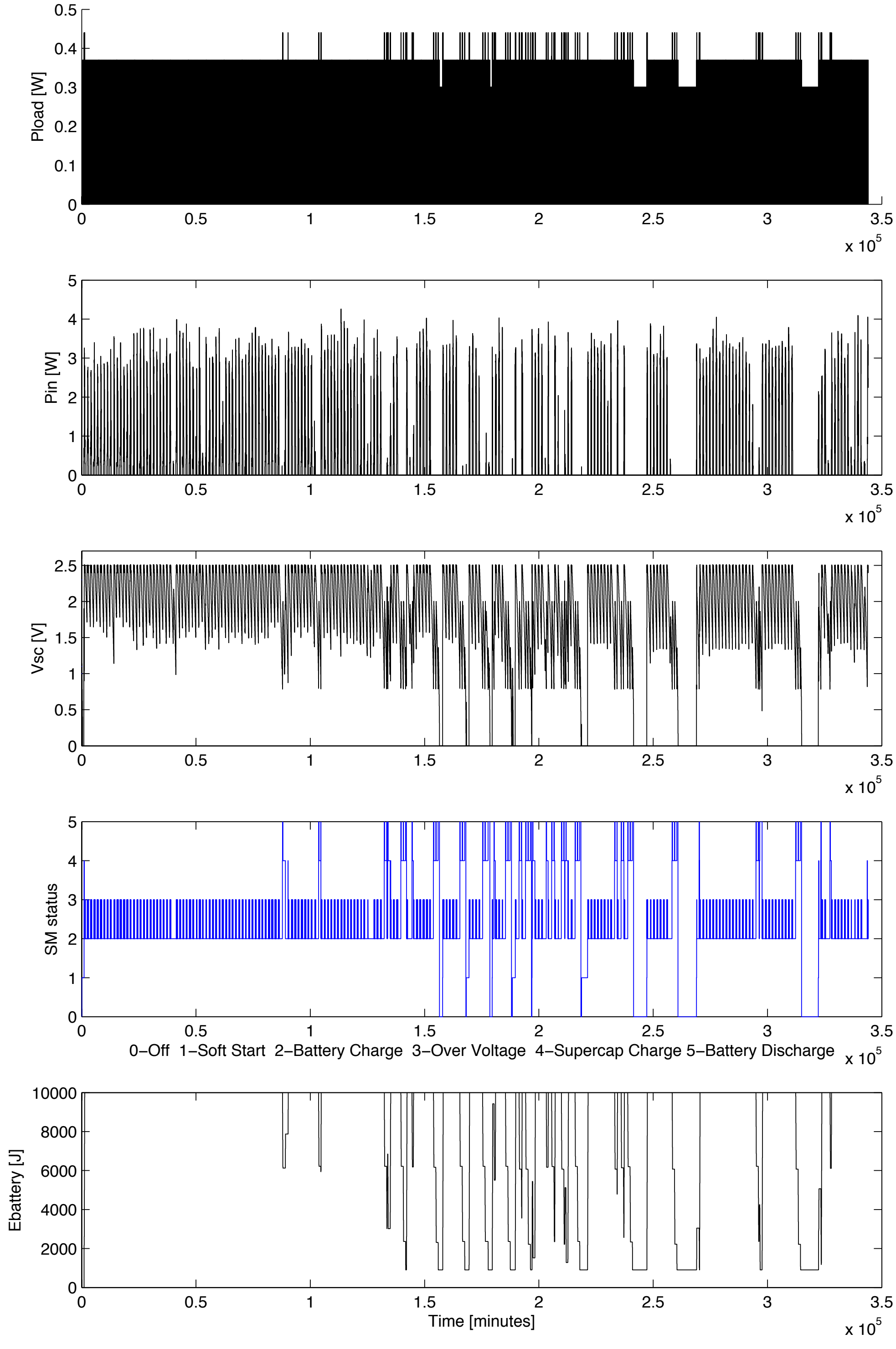


Figure 2.22: Simulation of 238 days of the proposed architecture, with a solar source of 5 W, a supercap of 1050 F and a Li-Ion battery of 680 mAh.

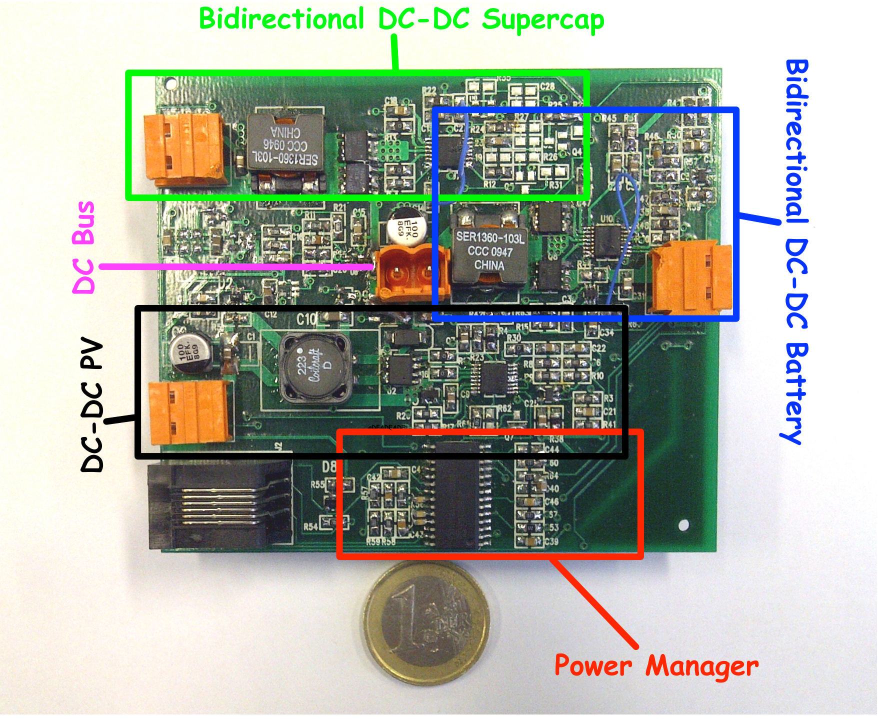


Figure 2.23: Prototype of the proposed power management system.

three Maxwell Boostcap CCAP0350, of 350 F and the battery is a simple Li-Ion battery for mobiles, a Cellular Line BSIV3, 3.7 V, 680 mAh.

The efficiencies of the three main converters are reported in Figure 2.24: A) is the measured efficiency of the bidirectional DC-DC Supercap converter in Buck mode, at different supercap voltages B) is the measured efficiency of the bidirectional DC-DC Battery and C) is the measured efficiency of the DC-DC PV converter.

In order to verify the correct operation of the circuit, an SPI interface has been connected to the power manager; this communication enables the monitor of currents and voltages in the circuit and of the state of the power manager, as well as the verification of the validity of the Simulink model and the proposed design procedure. The sampled values are reported in Figure 2.25: the first image represents the solar panel voltage, the second image represents the instantaneous input current of the solar panel, the third image is the instantaneous input power, the fourth image is the voltage across supercap, the fifth image is the status of the control state machine, for simplicity the states are numbered: 0 is the Off state, 1 is the Soft Start state, 2 the Battery Charge state, 3 the Over Voltage state, 4 the Supercap Charge state, and 5 is the Battery Discharge state, coherently with Figure 2.19; the last figure is the voltage of the battery.
To verify the operating time of the circuit, several months of measures in the wireless sensor network's position are required, measures that are not available;

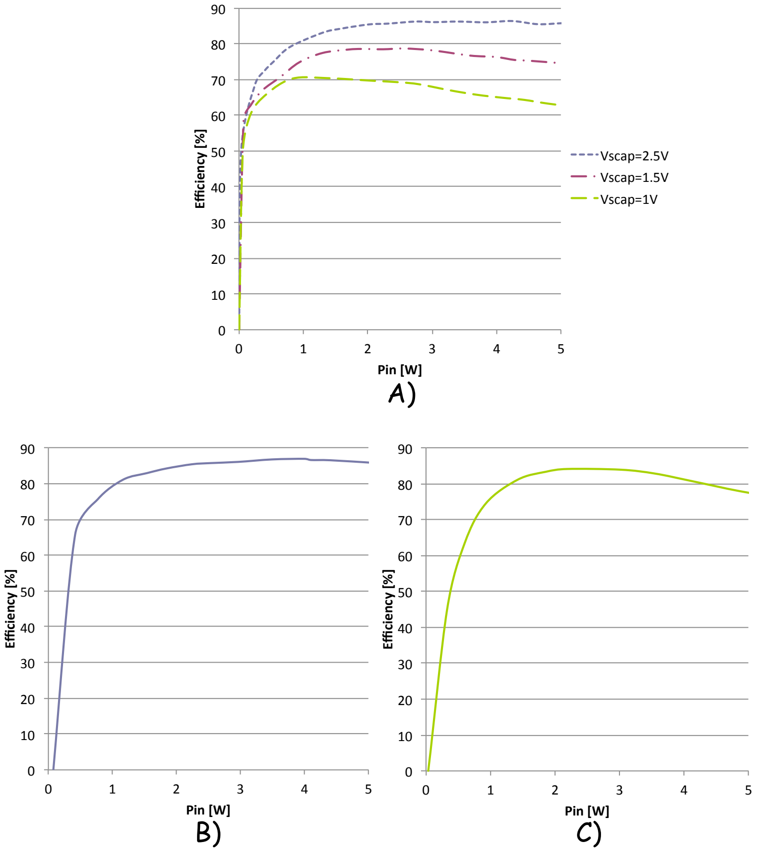


Figure 2.24: Efficiencies of the three main converters: A) is the measured efficiency of the bidirectional DC-DC Supercap converter in Buck mode, at different supercap voltages B) is the measured efficiency of the bidirectional DC-DC Battery and C) is the measured efficiency of the DC-DC PV converter.

to verify our model, however, it is sufficient evaluate the voltage ripple of the supercap during several nights: if during the day the supercap is fully charged, in the night the voltage should drop at values similar to those obtained using the simulation model. From the simulation of Figure 2.22, the voltage of the supercap during the night drops to about 1.5/1.8 V, as in the measured values of Figure 2.25: this confirms the accuracy of the simulation model and the validity of the proposed design procedure.

The major limitation of this system is the auto consumption of the supercap converter, which is 37 mW and 25 mW is the one required by the sensor. A controller that implements a pulsed frequency modulation is almost necessary, and using an high value of inductance can increase the efficiency at light loads.

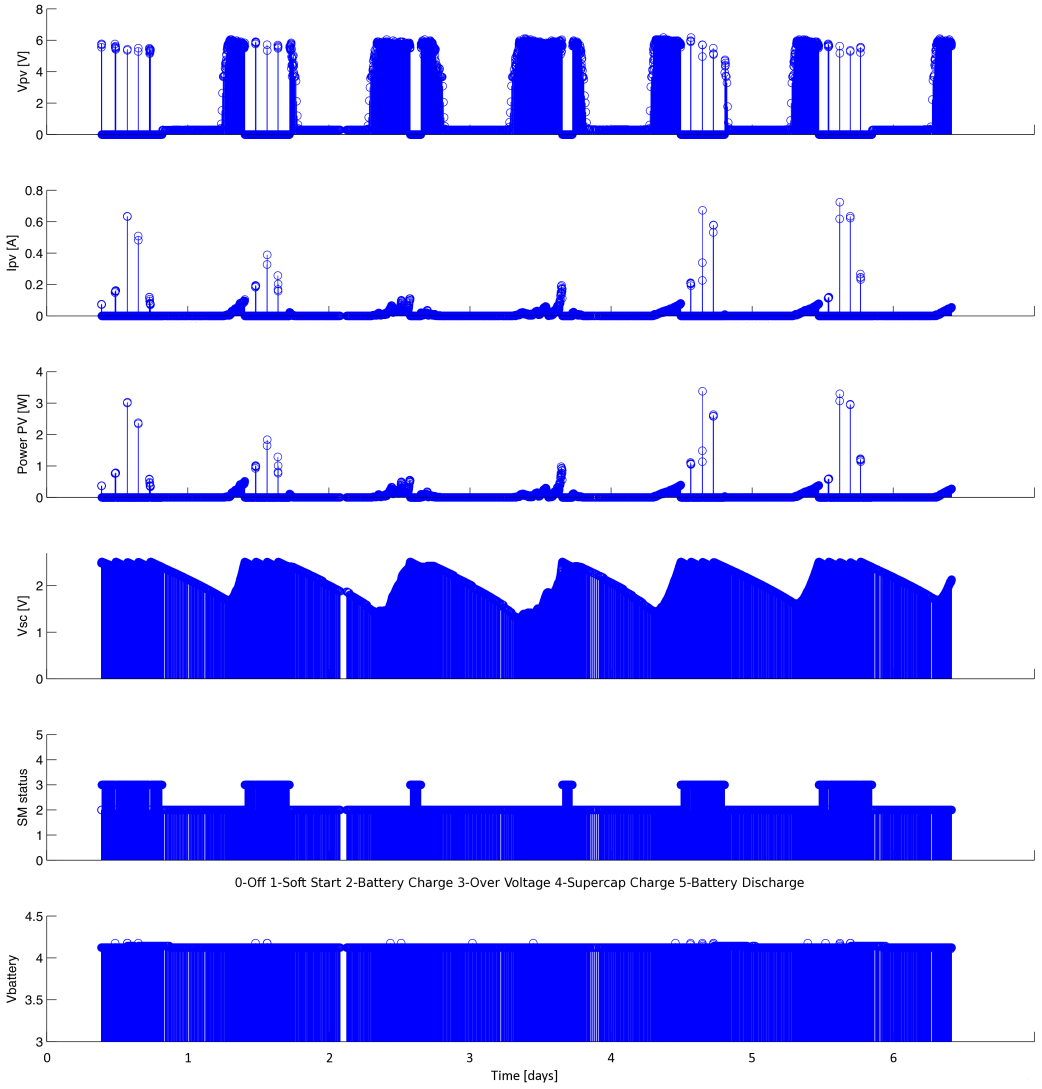


Figure 2.25: Measured voltages, currents and state variables of the circuit prototype after a period of 6 days.

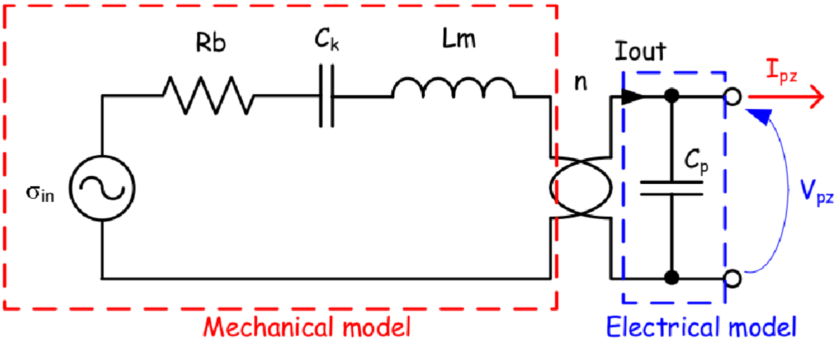


Figure 2.26: Equivalent circuit for a piezoelectric generator.

2.2 Piezoelectric-Based Wireless Sensor Networks

As reported in Table 2.1, another source that can be harvested with quite good efficiency are the vibrations; among all, piezoelectric generators (PZGs) are very promising because of their high efficiency as compared to other methods [33]. Piezoelectric materials exhibit the unique property known as the piezoelectric effect. When these materials are subjected to a compressive or tensile stress, an electric field is generated across the material, creating a voltage gradient and a subsequent current flow. The materials are composed of polar molecules aligned along a certain axis (poling axis), and therefore present a net dipolar moment. When a stress is applied to the piezoelectric film, the distance between the dipoles is modified and an electric field is created, so that a charge appears at the surface in order to compensate this field. The phenomenon of piezoelectricity can be described by following equations:

$$\begin{array}{l} \{S\} = [s^E]\{T\} + [D]^T\{E\} \\ \{D\} = [d]\{T\} + [\varepsilon]^T\{E\} \end{array} . \tag{2.11}$$

where $\{S\}$ is the six-dimensional strain vector, $\{T\}$ is the vector of stresses $[N/m^2]$, $\{D\}$ is the three-dimensional electric displacement vector $[C/m^2]$, $\{E\}$ is the electric field vector, $[s^E]$ is the six by six compliance matrix evaluated at constant electric field, $[d]$ is the three by six matrix of piezoelectric strain coefficients $[\frac{C/m^2}{N/m^2}]$, and $[\varepsilon^T]$ is the three by three dielectric constant matrix evaluated at constant stress. If a mechanical stress is induced on the piezoelectric element a difference of potential V_{pzo} is generated across the material due to the piezoelectric effect described by $[d]$.

Piezoelectric Generator Model

Considering a bender generator system, a convenient method of modelling piezoelectric elements such that system equations can be easily developed, is to treat the mechanical and electrical portions of the piezoelectric system as circuit elements [34]. The electromechanical coupling is then modelled as a transformer. An equivalent circuit for the bender system is shown in Figure 2.26; the equivalent inductor, L_m, represents the mass or inertia of the generator, the equivalent resistor, R_b, represents mechanical damping, the equivalent capacitor, C_k, represents the mechanical stiffness, σ_{in} is an equivalent stress generator that represents the stress developed as a result of the input vibrations and n represents the equivalent turns ratio of the transformer. The mechanical model can be calculated starting from the physical dimension of the bender and the acceleration induced by the vibration as described in [34]. In general the value of the impedance of the mechanical model reported to the secondary side (electric model side) is higher compared to the electrical impedance.

Piezoelectric materials are characterized by two characteristic frequencies: mechanical resonance frequency f_{ris} (i.e. resonance between C_k and L_m) and mechanical antiresonance frequency f_{a-ris}(i.e. resonance between the series of C_k and C_p - reported at the primary side - and L_m). At the mechanical resonance frequency f_{ris}, impedances C_k and L_m cancels each other. Although the mechanical resonance frequency is usually referred as the one needed for the optimum power generation , it has been shown that at both the resonance and antiresonance frequencies it is possible to harvest the maximum power from the generator. However, when the vibration frequencies are different from the mechanical resonance or antiresonance frequencies, the power extractable drops rapidly when the load is purely resistive. As an example, Figure 2.27 reports the optimal harvested power as a function of the excitation frequency when for each frequency the load resistance is adapted in order to obtain the maximum power. Thus, as can be seen from Figure 2.27, the piezoelectric generator is *band-limited*, since outside the resonance (and antiresonance) frequency the generation power is much smaller. Since it is difficult to design a mechanical system perfectly tuned with the frequency of the external stimulus, and because of the external vibrations are usually characterized by different frequencies, there is a need to increase the *bandwidth* of the piezoelectric generator. In fact, in literature there are several papers that investigate this issue from the mechanical point of view [35]: one example is the use of an array of piezoelectric material tuned for different frequencies.

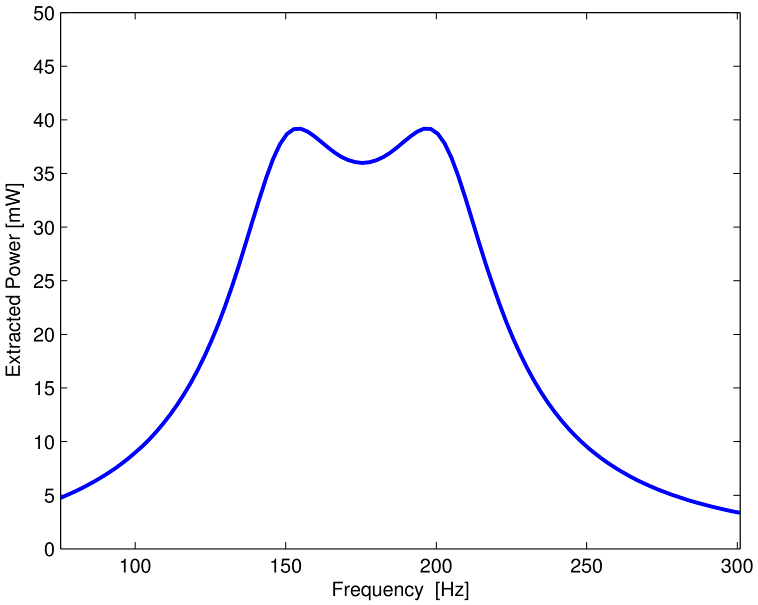


Figure 2.27: Maximum extracted power with resistive load matching.

Proposed Optimal Energy Extraction Solution

Considering the equivalent electric circuit of the piezoelectric source in Figure 2.26, to obtain the maximum energy transferring for each operation frequency is necessary to apply an $R_{eq} - L_{eq}$ in parallel to the piezoelectric generator. To achieve this goal, a bidirectional converter is used; in fact, due to the phase-shift between current and voltages, the instantaneous power can be negative for some time intervals.

As reported in Figure 2.28, the maximum output power can be extracted in a wide range of frequencies by adding the reactive load matching. Another example is in Figure 2.29, where the maximum output power at two different frequencies (100 Hz and 200 Hz) is reported as a function of the two components $(R_{eq} - L_{eq})$ of the load: at 100 Hz (Figure 2.29-a) , the maximum power can be obtained by using an inductor value of about 11 H and a resistance of 51 $k\Omega$; instead at 200 Hz (Figure 2.29-b) the maximum obtainable power is reached by using a resistance of 25 $k\Omega$ and a parallel inductance that approaches infinite value, so the maximum power extracted is obtainable only by a resistive impedance.

The circuit configuration of a piezo-harvester based on the resistive load matching is shown in Figure 2.30: a diode rectifier with capacitive filter is then followed by a DC-DC converter, whose operating point is adapted to ensure the optimum load matching. In our case, the need of bidirectional power transfer and the presence of ac voltage and current at the output of the generation requires a more-complex and less-efficient bidirectional AC-DC converters. In order to sim-

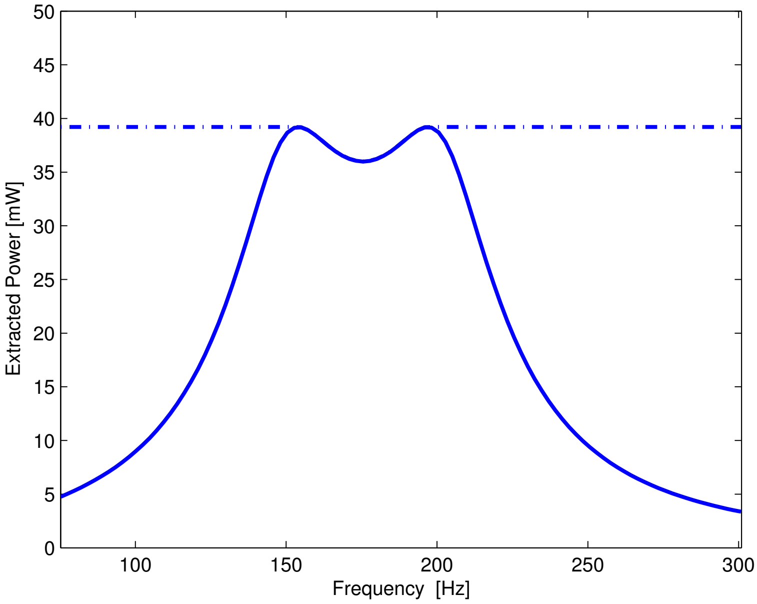


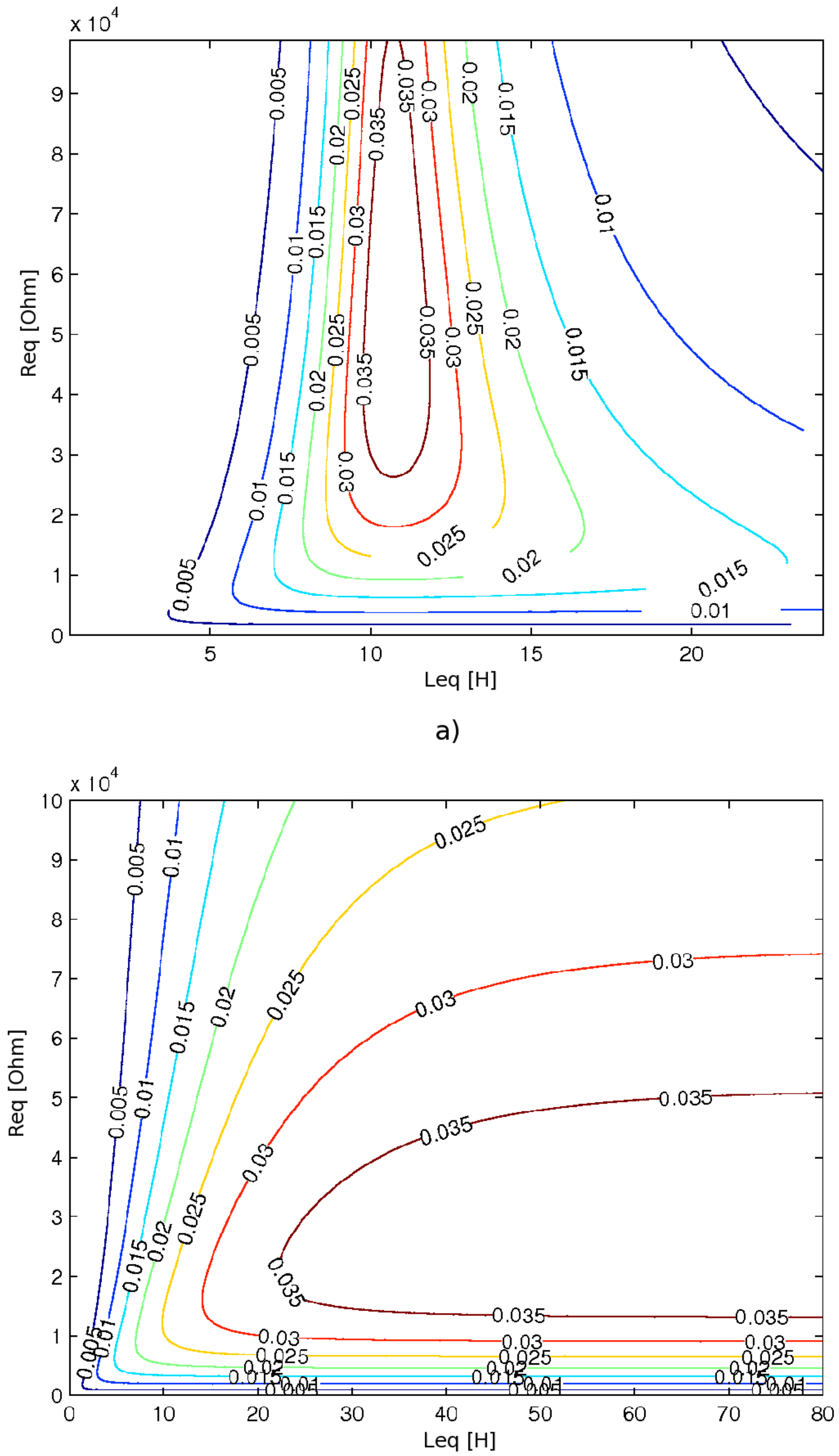
Figure 2.28: Maximum extracted power [W], with resistive matching (continued line), and both resistive-inductive load matching (dotted line).

plify the circuit, potentially enabling higher efficiency, a bias voltage is applied at the generator output so that voltage V_{pz} is always positive, the rectifier is avoided and only a bidirectional dc-dc converter, whose operating point is time-varying, is needed.

The equivalent load behaviour is reported in Figure 2.31-a and the circuit implementation in Figure 2.31-b, where the switching frequency input filter is not reported.

The main control algorithm is reported in Figure 2.31-b: the emulation of the resistive and reactive input impedance is obtained filtering the ac component of the piezoelectric generator with the transfer function of the desired load admittance (i.e. $1/R_{eq} + 1/(sL_{eq})$). The resulting signal is the current reference of the average input current control. Moreover, the DC-DC converters works in DCM mode and the bidirectional mode has been selected as follows: when the reference input current is positive, then the High Side (HS) driver is enabled and the Low Side (LS) one disabled; the opposite happens when the reference input current is negative.

The microcontroller is used for the adaptation of the resistive and reactive parameters: this is obtained using an MPPT based on the average (averaged over the input perturbation frequency) battery current. The goal is to optimize the generated energy, but since the voltage battery is constant or slowly varying, the maximization of the harvested power is equivalent to the maximization of the average battery current. The MPPT algorithm works on a bi-dimensional domain



a)

b)

Figure 2.29: Power extracted over inductance e resistance values at 100 Hz (a) and 200 Hz (b).

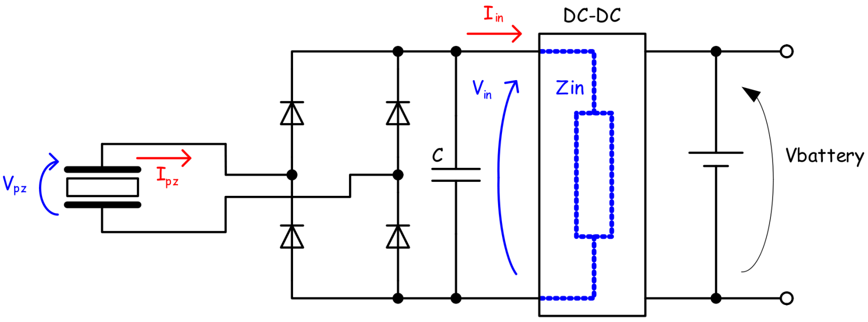


Figure 2.30: Energy harvesting systems with AC-DC rectifier (resistive load matching).

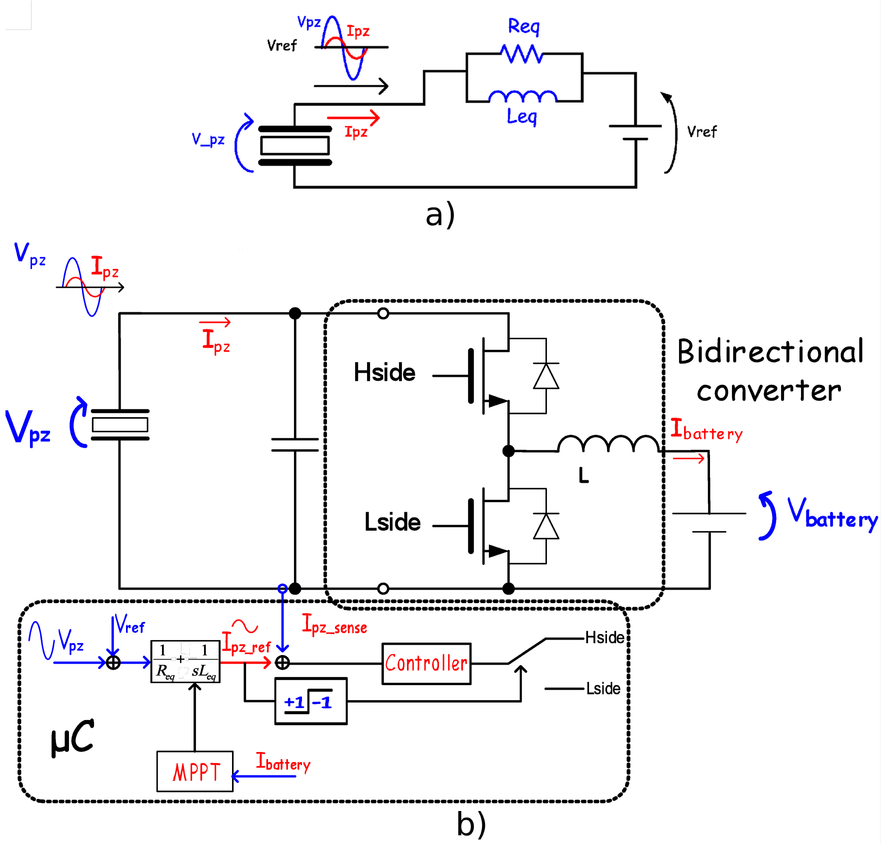


Figure 2.31: a) Electrical equivalent of the proposed scheme. b) Proposed scheme.

and the minimization algorithm is the same used in the previous section; in order to understand the algorithm, let's consider a simple example shown in Figure 2.6. The power obtained from the piezo (i.e. the cost function) is measured in three different points, being each point a vector $\vec{v_i} = [R_{eq_i} \quad L_{eq_i}]$. The first step is to identify the point with the minimum power and, for the purpose of explanation, let's assume that:

$$P(\vec{a}) < P(\vec{b}) < P(\vec{c}) \tag{2.12}$$

The lowest point $\vec{a}$ is then moved to the opposite side (point $\vec{d}$) of the original simplex, as seen in Figure 2.6-2, thus reflecting point $\vec{a}$ along the line $\vec{b} - \vec{c}$:

$$\vec{d} = \vec{b} + \vec{c} - \vec{a} \tag{2.13}$$

If the new point $\vec{d}$ has an extracted power higher than the previous highest $\vec{c}$, the new point is expanded, as in Figure 2.6-3:

$$\vec{e} = 2 \cdot \vec{d} - \frac{(\vec{b} + \vec{c})}{2} \tag{2.14}$$

If the new point $\vec{d}$ has a power lower than the point $\vec{b}$, $\vec{d}$ is contracted as in Figure 2.6-4 in:

$$\vec{e} = \vec{d} - \frac{\vec{d} - \frac{\vec{b}+\vec{c}}{2}}{2} \tag{2.15}$$

If the new point $\vec{e}$ is still the lowest among $\vec{b}, \vec{c}, \vec{e}$, points $\vec{b}$ and $\vec{e}$ are contracted around the highest point $\vec{c}$ as in Figure 2.6-5:

$$\begin{aligned} \vec{e} &= \vec{e} - \frac{\vec{e} - \vec{c}}{4} \\ \vec{b} &= \vec{b} - \frac{\vec{b} - \vec{c}}{4} \end{aligned} \tag{2.16}$$

In all the other cases, the algorithm starts again with the updated points of the simplex.

The proposed solution is verified using simulation and experimental results by a prototype built using discrete components. The controller utilized for the power stage is a commercial pwm controller (Si9145) and the proposed control system is implemented on a microcontroller platform (PIC18f2620). The power mosfets are BSP297 with a maximum V_{DS} of 200 V. The switching frequency is 100 kHz and the inductor is 1000 μH, this values allows the converter to work in DCM, and guarantees a small current ripple.

The microcontroller generates the current reference as explained in previous section and commutates the control depending on the sign of the current. As previ-

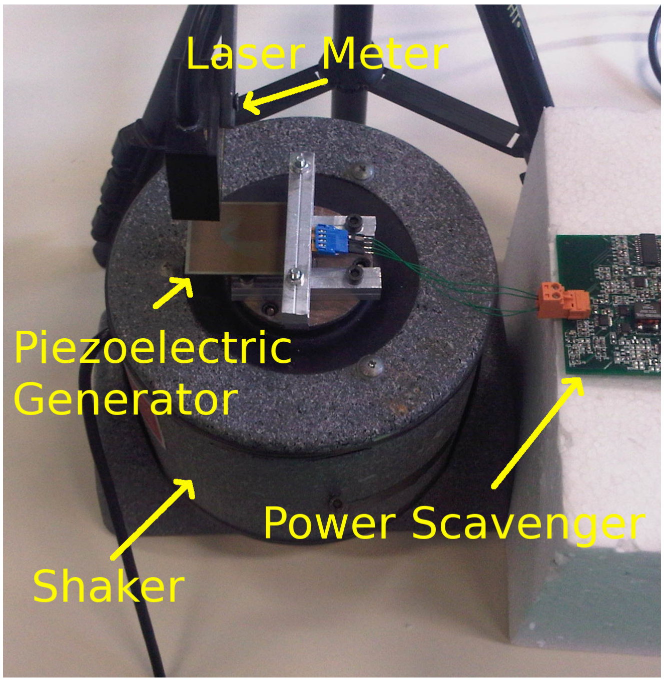


Figure 2.32: Measurement setup for the overall system.

ously mentioned, the piezo harvester used is a V20W, produced by MIDE group, with a 3 g mass applied to it, obtaining a mechanical resonance frequency of 163 Hz. The measurement setup is illustrated in Figure 2.32.

Figure 2.33 reports the main circuit waveforms under steady-state conditions: (from top to bottom) piezoelectric voltage (10 V/div), piezoeletric current - output of the sensing amplifier (5 mA/div), Low Side (LS) gate signal and (HS) High Side gate signal. As can be seen, the LS and HS signals are enabled as expected and the current and the voltage have the same excitation frequency, which is 178 Hz in this specific case, as imposed by a mechanical controlled shaker where the piezo-harvester was fixed. Moreover, current and voltage presents a significant phase shift, as expected. In fact, being the excitation frequency above the resonant one, a significant reactive component is expected as the output result of the MPPT algorithm.

In order to check the properties of the resistive and reactive load matching, the MPPT algorithm has been disabled and the load parameters have been inserted manually for different frequency values. Under these conditions, it was possible to establish the power that can be generated by our prototype under different loading conditions. For example, in Figure 2.34 it is shown the power extracted at a frequency of 141 Hz varying the load parameters R_{eq} and L_{eq}, reported in the Y and X-axis, respectively. As can be seen, the power can be optimized when a specific pair of R_{eq}, L_{eq} is used, which is indeed the point of convergence of the MPP algorithm. Similar tests were made at a frequency of 184 Hz, above the

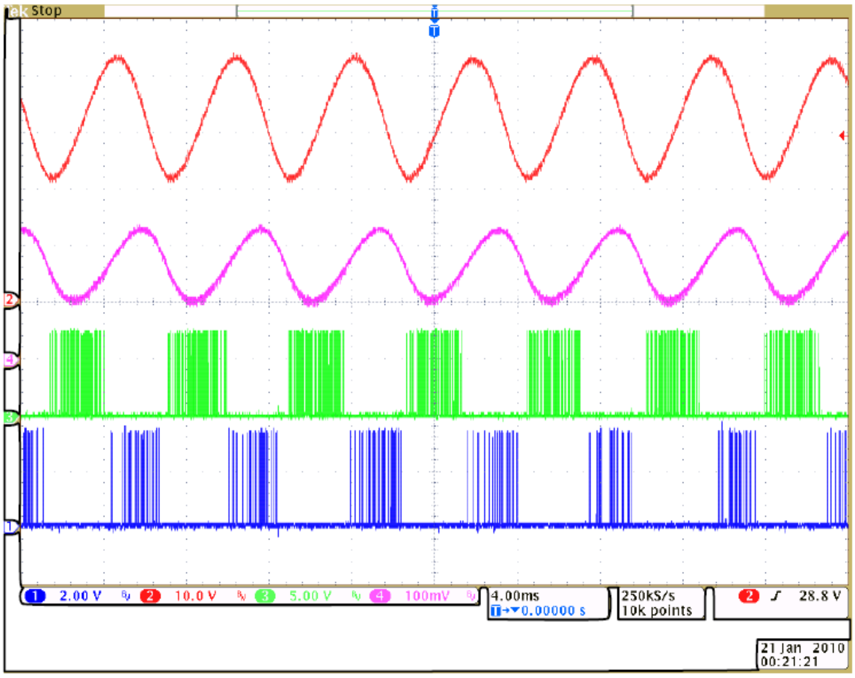


Figure 2.33: Main circuit waveforms (from top to bottom): piezoelectric voltage (10 V/div), piezoeletric current - output of the sensing amplifier (5 mA/div), Low Side gate signal and High Side gate signal

mechanical resonance, and the results are shown in Figure 2.35.

Figure 2.36 shows the comparison between extracted power on optimal resistive load and optimal inductive-resistive load at different frequencies. It is interesting to see that it is possible to increase the generated power for frequencies different from the mechanical resonance and antiresonance, thus being able to enlarge the bandwidth of the generator. In agreement with the theoretical expectation, the power generated between the mechanical resonance and antiresonance frequencies does not change respect to a resistive load matching. Instead, while being able to extract more power outside this frequency range, the obtained results is much less than the theoretical expectation (which should have been a flat curve) and the reasons of this discrepancy are under investigation.

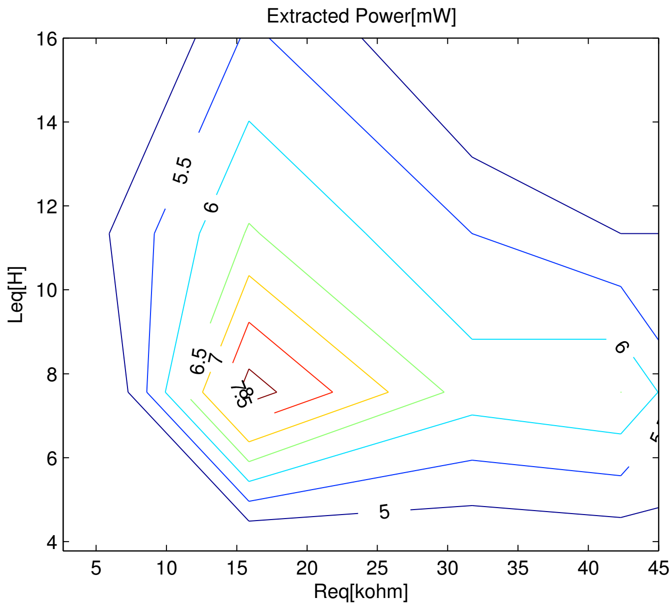


Figure 2.34: Extracted Power for variable load at the frequency of 141 Hz.

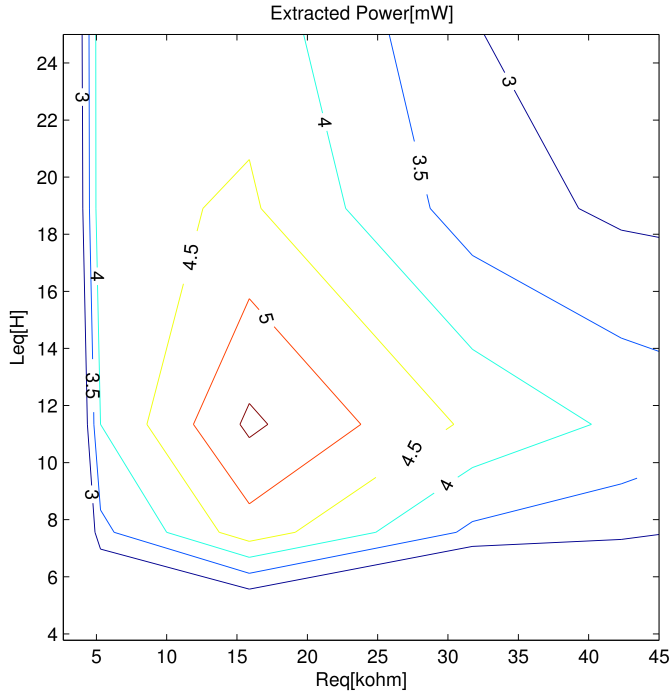


Figure 2.35: Extracted Power for variable load at the frequency of 184 Hz.

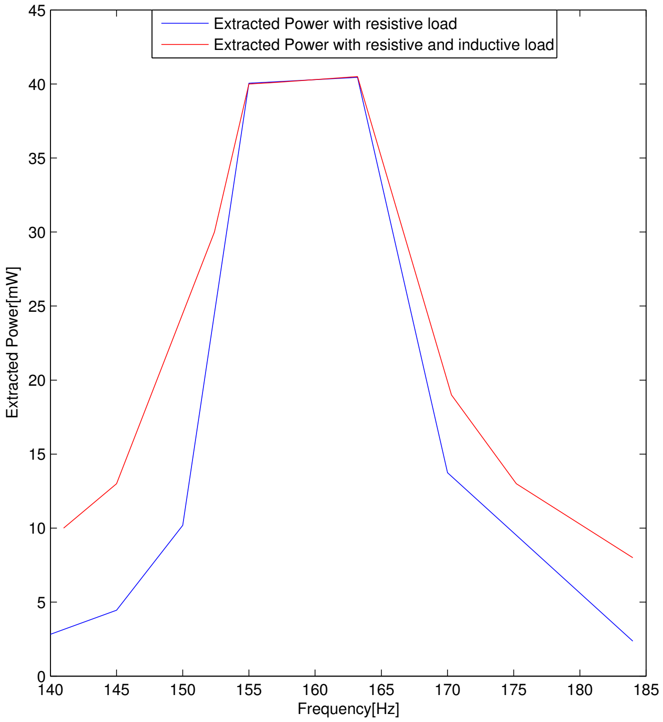


Figure 2.36: Comparison between maximum power extraction with resistive load and inductive and resistive load for variable frequency

2.3 Wiegand-Based Wireless Sensor Networks

A Wiegand device typically releases a $\sim 10\ \mu s$ voltage pulse several volts wide when subject to an external, time-varying magnetic field. Due to the sharpness of the magnetic transition, pulse generation occurs regardless of how slow the magnetic field variation is, an attractive feature which enables its use in energy harvesting scenarios even when low-frequency sources are considered.

Sensors based on the Wiegand effect [37] are employed in a number of everyday life applications, including pulse generators in absolute encoders for high-performance motion control [38], as well as keycard door locks for electronic entry systems relying on the Wiegand protocol [39]. The core of a Wiegand sensor consists of a ferromagnetic material such as Vicalloy [40] having non-uniform magnetic properties which enable a sharp magnetic hysteresis to occur.

As illustrated in Figure 2.37, a Wiegand wire presents an inner core having a soft (small coercivity) magnetic loop and an outer shell having a hard (high coercivity) magnetic loop. The magnetic field produced by the magnetized shell has a natural return path through the core when the device is at rest. However, when an external magnetic field overcomes the shell magnetic biasing and reverses the soft core magnetization, such internal return path no longer exists and the flux lines must temporarily invade the space surrounding the Wiegand wire. The resulting flux pulse is picked up by a winding and transduced into a triangular voltage pulse such as the one illustrated in Figure 2.38. The switchover transient ends when the outer shell reverses polarity as well, generating a much smaller pulse and bringing the Wiegand device to a new rest state having a magnetization opposite to the starting one. The external magnetic field represents the actuator and must be alternating for the Wiegand sensor to keep pulsing. However, the rate of variation of the external field is largely irrelevant, since the two magnetic states of the Wiegand device alternate according to a large and sharp hysteresis loop, ensuring the generation of a pulse which is basically constant even at very low input frequencies [41]. In [43] a thin-film-based sensor consisting of $NiFe/CoFe$ multilayer thin film deposited on a thermally oxidized Si substrate was also studied, and a sensor element was fabricated by patterning the film by photolithography and wet-etching processes. This thin-film based sensor exhibited a constant output voltage for excitation frequencies down to 0.1 Hz.

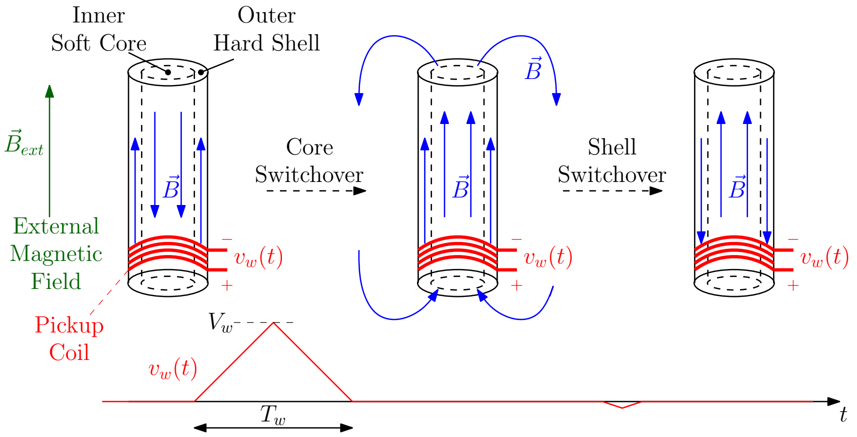


Figure 2.37: Simplified representation of the (open-circuit) voltage pulse generation in a Wiegand sensor.

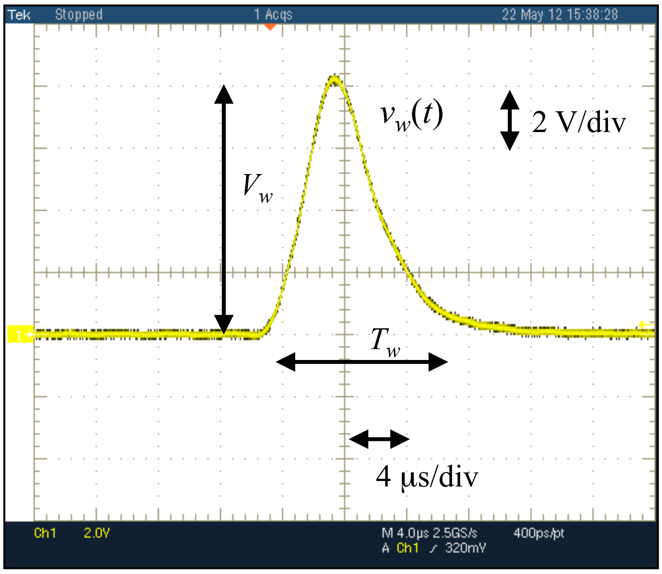
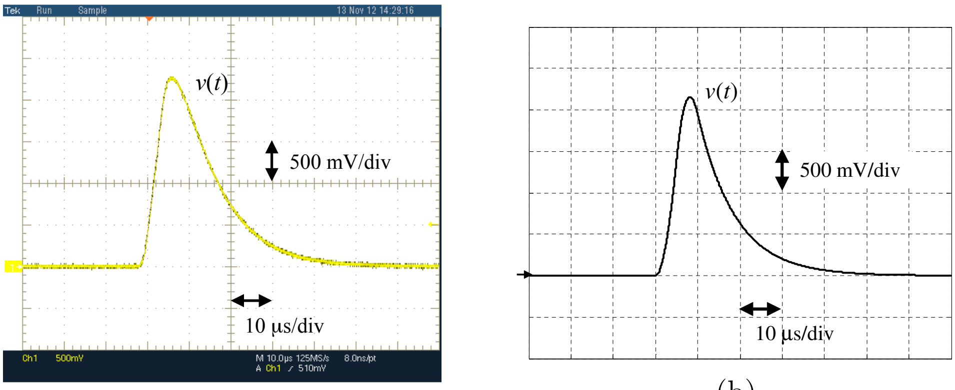


Figure 2.38: Experimental open-circuit votage pulse $v_w(t)$ of a commercial Wiegand device [42].



(a) (b)

Figure 2.39: Experimental (a) and simulated (b) output voltage pulse $v(t)$ of the Wiegand device on a 1 $k\Omega$ resistive load.

Electrical Characterization of the Wiegand Source

Figure 2.38 illustrates the open-circuit pulse $v_w(t)$ generated by a commercial Wiegand sensor [42] when excited by an external magnet. The sample produces a $T_w \approx 10\ \mu s$ triangular pulse, about $V_w \approx 8\ V$ wide. When loaded with a 1 $k\Omega$ resistor, the sensor produces the pulse illustrated in Figure 2.39(a).

Based on such measurements, an equivalent electrical model of the Wiegand source can be formulated as an RL impedance $R_w = 350\ \Omega$ and $L_w = 12\ mH$, in series with a triangular pulse generator $v_w(t)$. Figure 2.39(b) confirms that the simulated Wiegand pulse on a 1 $k\Omega$ load well matches the experimental waveform. The foregoing model is consistent with the Wiegand sensor being, in essence, a coil wrapped around a ferromagnetic core.

Given the above electrical model, it is possible now to look for the optimal load which yields maximum energy extraction from a single Wiegand pulse. The optimal load consists of a resistance $R_{opt} = R_w$ in series with a negative inductance $L_{opt} = -L_w$ as shown in Figure 2.40(a); this optimal load imposes that

$$v_{R_w}(t) = \frac{v_w(t)}{2} \tag{2.17}$$

so that $i_w(t)$ and $v_{L_w}(t)$ can be expressed as

$$i_w(t) = \frac{v_w}{2R_w} \Rightarrow v_{L_w}(t) = \frac{L_w}{2R_w}\frac{dv_w(t)}{dt} \tag{2.18}$$

It is therefore possible to express the optimal load voltage $v_{opt}(t)$ in terms of the Wiegand open-circuit pulse $v_w(t)$:

$$v_{opt}(t) = \frac{v_w(t)}{2} - \frac{L_w}{2R_w}\frac{dv_w(t)}{dt} \tag{2.19}$$

The derived optimal waveform $v_{opt}(t)$ is sketched in Figure 2.40(b) and resembles a rectangular pulse with amplitude

$$V_{opt,max} \approx V_w \frac{\tau_w}{T_w} \approx 27\ V \tag{2.20}$$

where $\tau_w = L_w/R_w$. Such square wave is synchronized with the Wiegand pulse $v_w(t)$.

The maximum energy per pulse available from the sensor in the optimal condition can be calculated as follows:

$$E_{w_{max}} = \int_0^{T_w} \frac{{v_w}^2(\tau)}{4R_w} d\tau = \frac{V_w^2}{12R_w} T_w \tag{2.21}$$

which evaluates to $E_{w_{max}} \approx 152\ nJ/$pulse for the commercial device considered here [42].

Due to the small amount of energy generated by each Wiegand pulse, efficient emulation of the optimal load behaviour is a nontrivial task. Observe, for instance, that $V_{opt,max} \approx 27\ V$ represents a rather high voltage in the considered applications, as it is incompatible with modern low-cost consumer rechargeable batteries. Lithium-Ion (Li-Ion) batteries, for instance, have a typical open-circuit voltage of about $4.2\ V$. Generating $V_{opt,max}$ from the battery voltage would involve a step-up converter with associated control circuitry. Stacking multiple batteries in series, on the other hand, would pose similar conversion issues for powering the on-board electronics.

In order to facilitate the implementation of the energy harvester, the first step in our analysis is to approximate $v_{opt}(t)$ with a simpler waveform, and evaluate the energy loss due to such simplification. Referring to Figure 2.41, the considered waveform is a rectangular pulse defined, for a *positive* Wiegand pulse, as

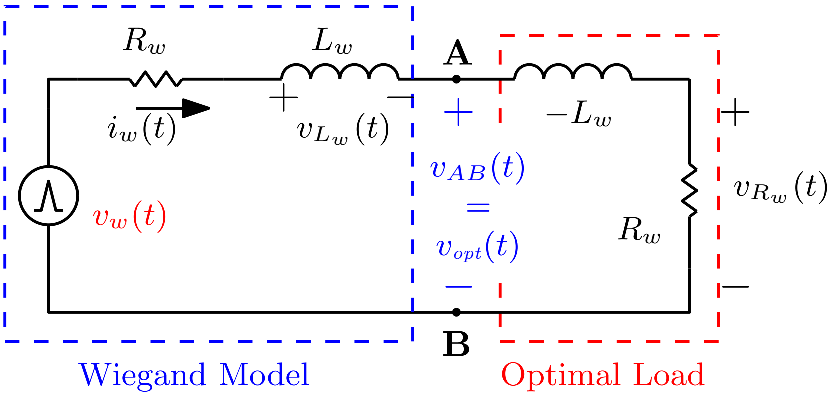
$$v_{rect}^{+}(t) = \begin{cases} -V_{Bat}, & 0 < t < \dfrac{T_w}{2} \\ +V_{Bat}, & \dfrac{T_w}{2} < t < T_0 \end{cases} \tag{2.22}$$

where T_0 is defined as the instant at which the Wiegand current reaches zero:

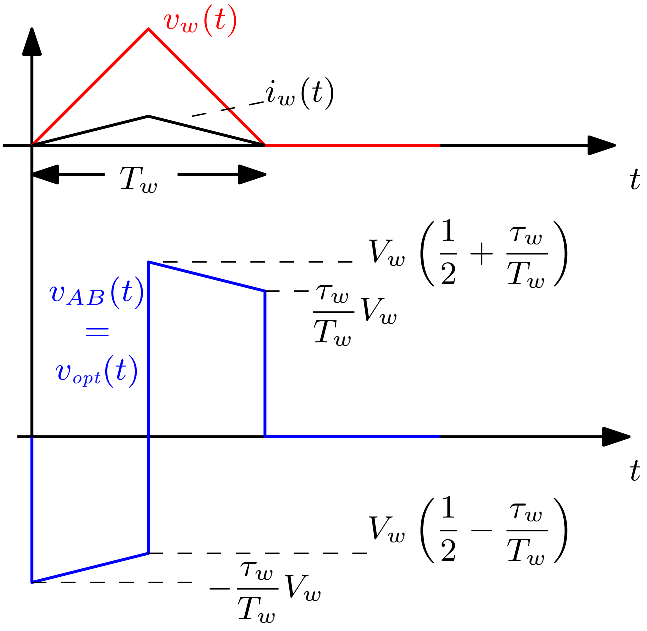
$$i_w(t = T_0) = 0 \tag{2.23}$$

For a *negative* Wiegand pulse, the corresponding rectangular pulse would simply be $v_{rect}^{-}(t) = -v_{rect}^{+}(t)$.

In other words, the proposed simplification consists of applying the full negative battery voltage to the Wiegand device up to $T_w/2$, and successively let the Wiegand current free wheel to zero, delivering the energy to the battery. Observe that the $[T_w/2, T_0]$ discharge phase in the proposed approximation is not equal



(a)



(b)

Figure 2.40: Equivalent electrical model of the Wiegand source (a) and main waveforms with the optimal load (b).

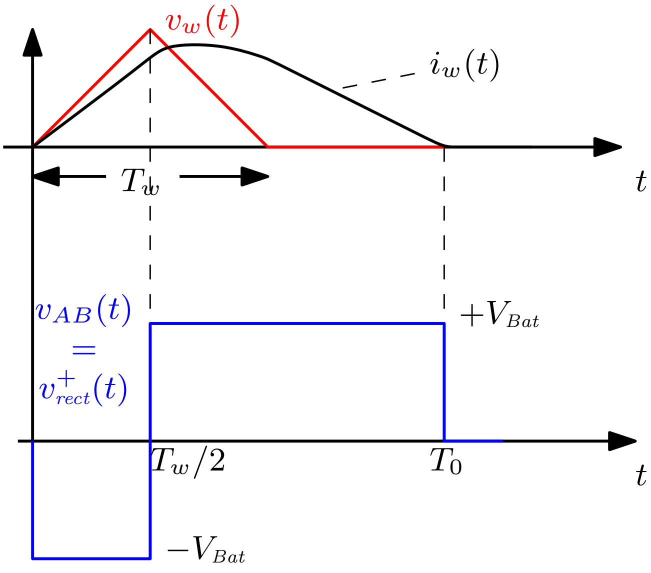


Figure 2.41: Proposed rectangular approximation for energy extraction from the Wiegand device.

to $T_w/2$ due to the fact that the applied voltage load is not the ideal one.

The maximum available energy (2.21) has been compared with the energy $E_{w,r}$ extracted with the aforementioned rectangular approximation for a commercial Wiegand device [42]. $E_{w,r}$ has been evaluated theoretically and simulated by a SPICE-based simulation model. Results are compared in Figure 2.42 as a function of V_{Bat}. To complete the picture, the energy $E_{w\,diode}$ extracted by an ideal full-wave diode rectifier is also shown.

As expected, the rectangular pulse approximation (2.22) well approaches the ideal performance when V_{Bat} is in proximity of $V_{opt,max}$. Quite interestingly, however, Figure 2.42 also suggests that small V_{Bat}'s still allow for a a marked improvement with respect to passive rectification. For $V_{Bat} = 4.2\ V$, for instance, the rectangular approximation would allow to ideally extract $E_{w,r} \approx 76\ nJ$/pulse, i.e. almost six times the energy than with a diode rectifier and about 50% of the maximum available energy.

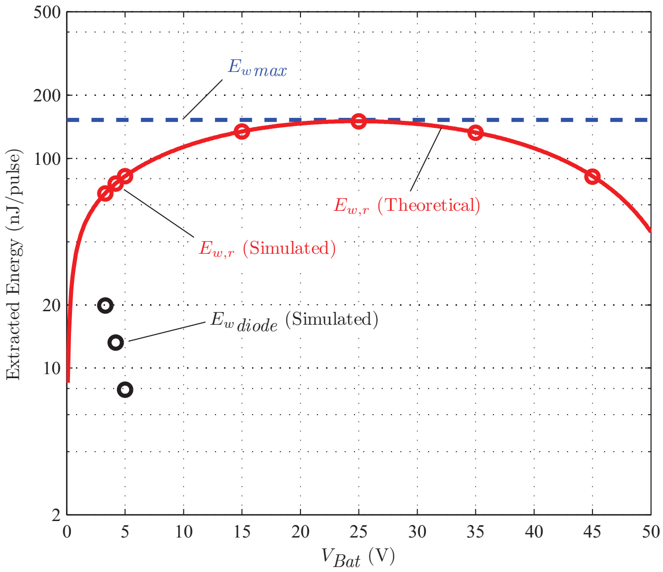


Figure 2.42: Available energy per pulse from the Wiegand device [11]: comparison between maximum available energy $E_{w_{max}}$, extracted energy $E_{w,r}$ with the rectangular approximation, and extracted energy $E_{w_{diode}}$ with full-wave diode rectification.

Proposed Optimal Energy Extraction Solution

Based on the foregoing observations, the solution proposed in this work and reported in Figure 2.43 consists of a Full- Bridge (FB) rectifier interfaced directly with a Li-Ion battery and controlled in order to generate the rectangular pulse (2.22). The gate signals are generated via a low-power circuitry triggered by the Wiegand output voltage itself. The control stage is illustrated in Figure 2.44, while main waveforms are shown in Figure 2.45.

When one of the two terminal voltages $v_A(t)$ or $v_B(t)$ of the Wiegand sensor starts increasing, a monostable is triggered, enabling the full bridge. Suppose, for instance, that $v_A(t)$ starts increasing due to a positive pulse. The control circuitry then drives the FB to $v_A(t) = 0$ and $v_B(t) = V_{Bat}$, so that the voltage seen by the Wiegand sensor is $v_{AB}(t) = -V_{Bat}$. Likewise, when $v_B(t)$ increases due to a negative pulse, the FB is driven to $v_A(t) = V_{Bat}$ and $v_B(t) = 0$, and therefore $v_{AB}(t) = +V_{Bat}$.

After $T_w/2$ seconds, equal to 5 μs for the commercial Wiegand sensor used in this work, the monostable turns off and the Wiegand inductive current brings the FB diodes into free-wheeling conduction. This way, the voltage applied to the device reverses its sign, completing the generation of the $[T_w/2, T_0]$ portion of $v^+_{rect}(t)$. Referring to Figure 2.45, control operation can be split into four phases:

- $[0, t_1]$: at instant t_0, the Wiegand voltage $v_A(t) - v_B(t)$ starts increasing.

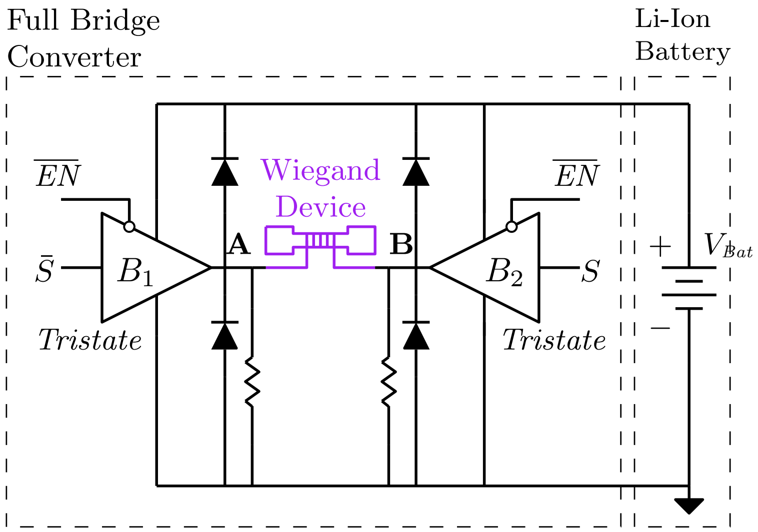


Figure 2.43: Proposed full-bridge Wiegand energy harvester.

Signal EN is low, so the FB tristate buffers B_1 and B_2 are disabled, while the controller tristate buffer B_3 in Figure 2.44 is enabled.

- $[t_1, t_2]$: when $v_A(t)$ exceeds threshold V_{th} at instant t_1, $Comp_3$ asserts S to logic 1. Signal S determines the polarity of the Wiegand pulse.

- $[t_2, T_w/2]$: at instant t_2 the non inverting input of $Comp_1$ also exceeds V_{th}. An impulse at input SET is generated, allowing flip-flop F_1 to be set. As a result, $EN = 1$ and $\overline{EN} = 0$, so B_3 goes into high impedance state freezing signal S. At the same time, tristate buffers B_1 and B_2 of the FB are enabled and connect A to ground and B to V_{Bat}, so that $v_{AB}(t) = -V_{Bat}$.

- $[T_w/2, T_0]$: at $T_w/2$ $Comp_2$ output goes high, resetting F_1 with a short pulse. This forces $\overline{EN}$ to logic 1 and consequently B_1 and B_2 go into an high impedance state. With B_1 and B_2 in a high impedance state, the Wiegand current brings the FB diodes into free-wheeling conduction, forcing $v_{AB}(t)$ to $+V_{Bat}$. The transient ends at instant t_4 when the Wiegand current reaches zero, turning off the FB diodes. Observe that the monostable pulse width T_{pulse} must be designed so that $t_2 + T_{pulse} = T_w/2$.

An additional feature of the proposed circuit is that of inherently realizing a passive rectification when the battery voltage is low and the control circuitry is not operating, therefore enabling a form of *cold start* operation.

A SPICE simulation model of the system has been set up in order to verify the controller operation. Simulated voltage and current of the Wiegand sensor during

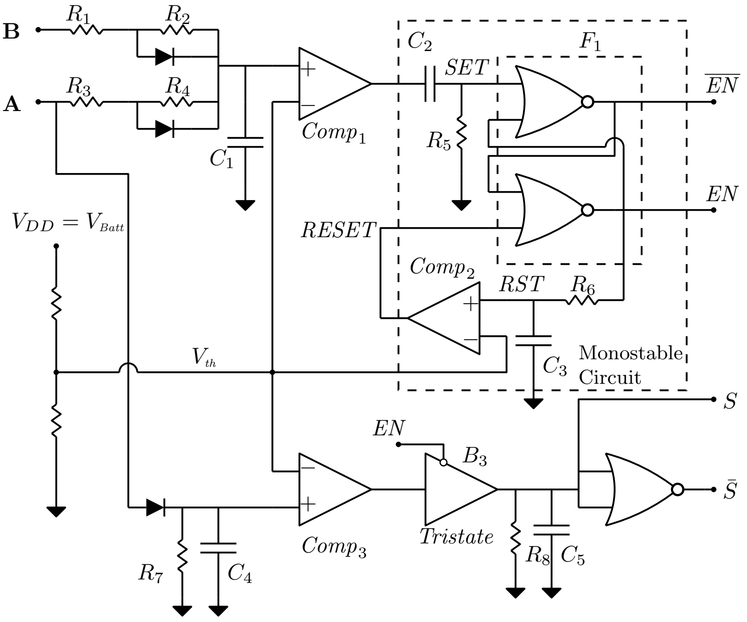


Figure 2.44: Control circuit of the full-bridge harvester.

a positive pulse are reported in Figure 2.46. The simulated energy delivered by the Wiegand device amounts to 61 nJ, slightly smaller than the ideal 76 nJ/pulse predicted by Figure 2.42. The discrepancy is to be expected, as the voltage pulse $v_{AB}(t)$ generated by the proposed circuit only approximates the desired $v_{rect}^{+}(t)$ to a certain extent. The major contribution to the smaller extracted energy is the presence of the threshold voltage V_{th}, which only triggers the control circuit with a certain delay with respect to the physical Wiegand pulse. Other nonidealities consist of the non-perfect alignment of the switching instant t_2+T_{pulse} with respect to $T_w/2$, and voltage drops across the FB devices and diodes during the pulse generation.

Comparators $Comp_1$, $Comp_2$ and $Comp_3$ have the main purpose of ensuring fast logic transitions at the input of the cascaded logic gates, limiting cross-conduction energy losses. This provision is of utmost importance especially in a discrete realizations such as the one that will be described in the next Section. On the other hand, a fully integrated realization of the proposed energy harvester could most likely be implemented without comparators thanks to much lower power dissipation during logic transitions.

Including the comparators in the control circuit, on the other hand, introduces static power dissipation associated with the comparators bias currents, which are in the order of tens of microamperes for commercial discrete devices. In order to mitigate this problem, an optional battery disconnect circuitry can be included as shown in Figure 2.47. Devices M_2 and M_1 are turned on before instant t_1 in order to pre-bias the control circuitry. At $t = t_1$, when $\overline{EN}$ goes to logic 0, M_2

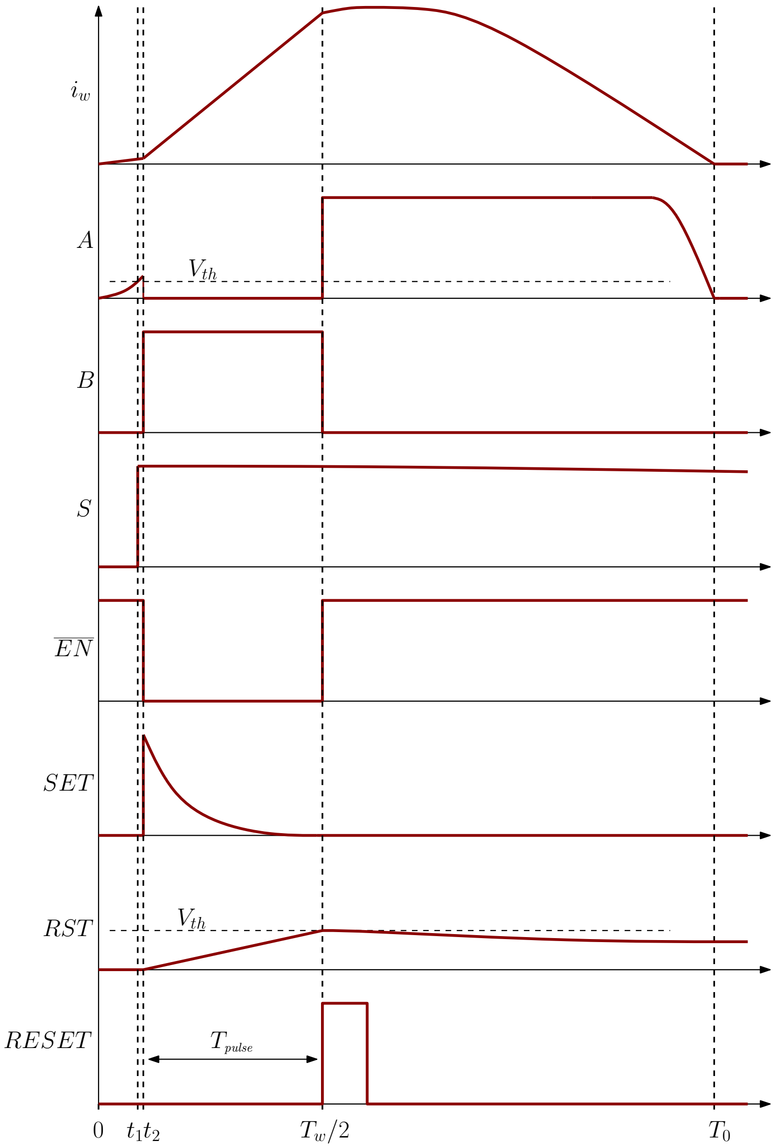


Figure 2.45: Control operation of the proposed energy harvester.

is turned off, allowing M_1 to disconnect the battery from the circuit after the Wiegand transition completes.

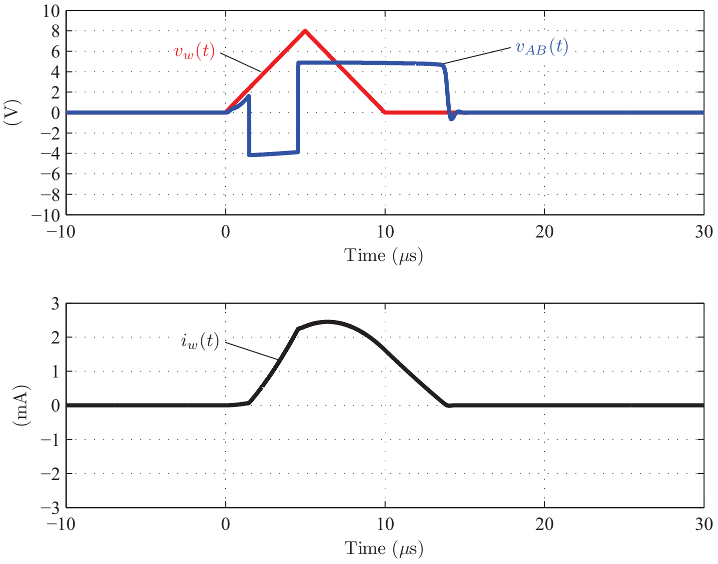


Figure 2.46: SPICE simulation of the Wiegand sensor voltage and current during a positive pulse.

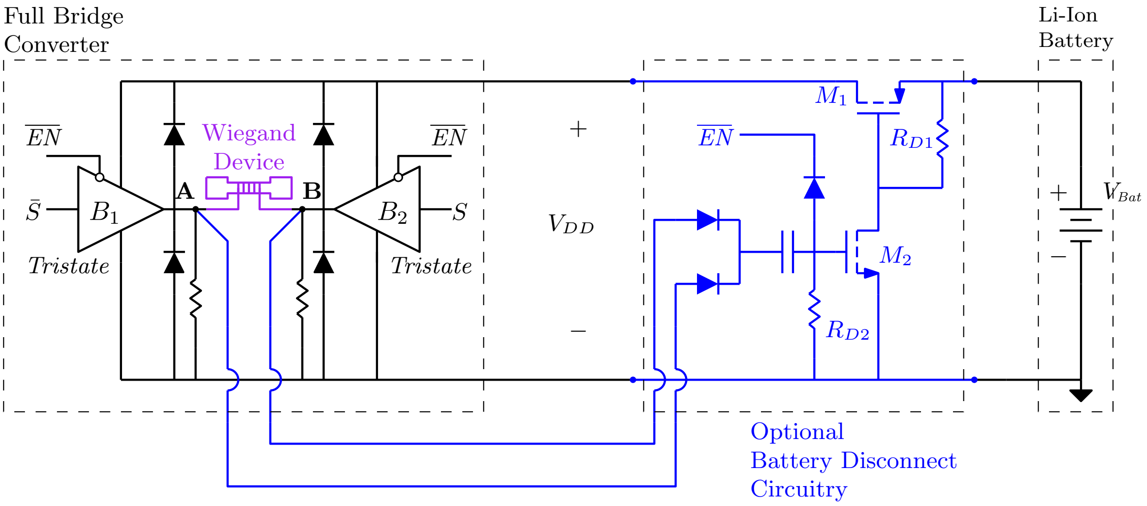


Figure 2.47: Proposed full-bridge Wiegand energy harvester with optional battery disconnect circuitry.

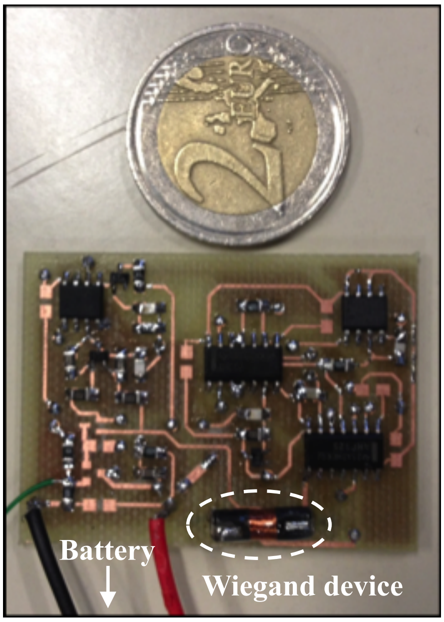


Figure 2.48: Picture of the realized prototype.

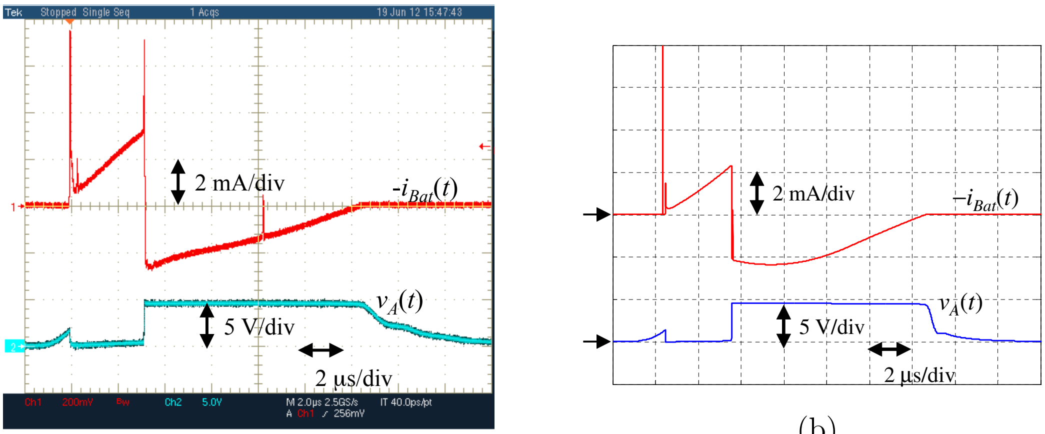
Implementation and Experimental Results

As anticipated, a prototype of the proposed Wiegand harvester has been realized using discrete components. The prototype is pictured in Figure 2.48.

Due to the small energy budget available, the FB has been realized with two tristate buffers using a SN74AHC125 device from TI, which guarantees limited gate charge losses of the transistors. The comparators used are MAX989 from Maxim, which report a current consumption of just 11 μA and a delay time of 300 ns. As detailed in Figure 2.44, the monostable circuit is realized as two NOR gates in flip-flop configuration, followed by a feedback-connected delay element consisting of a RC network and a comparator. A SN74HC02D NOR device from TI has been employed, while the time constant R_6C_3 has been designed to achieve the desired monostable pulse width of $T_w/2 = 5$ μs.

Experimental operation of the energy harvester is illustrated in Figure 2.49(a), which reports main waveforms during a positive Wiegand pulse. For comparison, Figure 2.49(b) reports the simulated waveforms obtained with the SPICE model described in the previous Section. In the test, the Wiegand device [42] was excited *manually* by sweeping a small magnet in proximity of the device, a proof that energy extraction is feasible even under slow magnetic variations.

Experimentally, it has been observed that although the speed of the applied magnetic field does not significantly affect the generated voltage pulse, the *orientation* of the latter does. As a result, the total measured energy per pulse E_{Bat} delivered to the battery ranges between 24 to 29 nJ/pulse depending on the magnet orientation with respect to the Wiegand device.



(a) (b)

Figure 2.49: Experimental (a) and simulated (b) waveforms of the proposed energy harvester during a positive Wiegand pulse.Upper trace: battery current $i_{Bat}(t)$ measured through a 100 Ω shunt resistor (200 mV/div, or 2 mA/div); lower trace: leg A output voltage $v_A(t)$ (5 V/div). Time base: 2 μs/div.

To further assess the validity the proposed solution, a simple alternative approach based on passive rectification has been experimentally tested. A full-wave diode rectifier realized with BAT54A schottky devices has been realized, directly connecting the Wiegand device to the battery. The measured extracted energy per pulse in this case is about 8 to 10 nJ, in line with the values forecast by Figure 2.42, and drastically smaller than what obtained with the proposed solution.

A breakdown analysis of the prototype energy losses has been carried out by means of a mixed simulation/experimental investigation. Power stage losses have been added to the SPICE simulation model described in the previous Section by including finite on-resistances of the FB tristate buffer devices. For the purpose, datasheet values have been employed. In these conditions, the energy extracted from the Wiegand sensor is equal to $E_w \approx 61\ nJ$/pulse, while the simulated output energy delivered to the battery was $E_{Bat} = 43.4\ nJ$. This latter number can be thought as the net energy that would be delivered to the battery by the power stage circuit if the controller was loss free.

To validate the 43.4 nJ figure, the FB rectified current was measured during a Wiegand pulse, excluding the contribution from the control logic current. Figure 2.50 reports the measured current pulse, whose the average value over a 20 μs window is 456 μA. The measured net energy delivered by the power stage to the 4.2 V battery therefore amounts to 4.2 V $\cdot$ 456 μA $\cdot$ 20 μs $=$ 38.3 nJ/pulse, in good agreement with the simulation estimate.

Control losses, more difficult to model, have been directly measured by removing the Wiegand device from the prototype, and triggering the control logic with a signal generator, measuring the consequent controller current absorption. Result indicate an energy consumption of 12.4 nJ/pulse, which can be ascribed

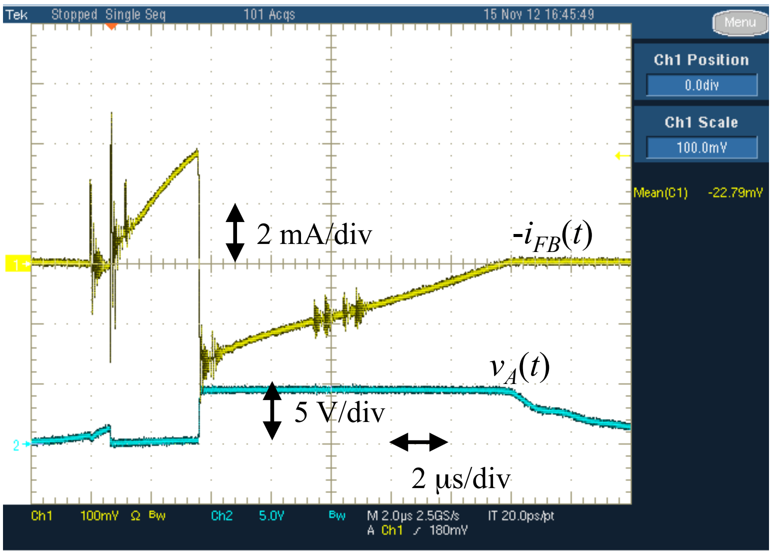


Figure 2.50: Experimental waveforms of the proposed energy harvester during a positive pulse Wiegand pulse, neglecting controller current absorption. Upper trace: full bridge rectified current $i_{FB}(t)$ measured through a 50 Ω shunt resistor (100 mV/div, or 2 mA/div); lower trace: leg A output voltage $v_A(t)$ (5 V/div). Time base: 2 μs/div.

to both static and dynamic power dissipation of the logic gates during the event.

Overall, the total energy loss associated with the proposed harvesting circuit are

$$E_{loss} \approx \underbrace{(61 - 43.4)\text{ nJ}}_{\text{Power stage (simulated)}} + \underbrace{(12.4)\text{ nJ}}_{\text{Control logic (measured)}} = 30\text{ nJ} \tag{2.24}$$

Given a measured net extracted energy of roughly 29 nJ/pulse in the best case, one can infer that the Wiegand generated energy is $29 + 30 \approx 59$ nJ/pulse, in excellent agreement with the 61 nJ/pulse simulated in previous section.

For improved efficiency results, an integrated implementation of the proposed solution is mandatory. One major advantage of a fully integrated implementation is the dramatic reduction of the overall bias current. In the proof-of-concept discrete prototype evaluated in this work, quiescent current required for biasing the control circuitry amounts to roughly 50 μA. Taking into account an extracted energy of about 30 nJ/pulse, the system is energy autonomous as long as the frequency of the pulses is

$$f_{pulses} > \frac{50\mu\text{A} \cdot V_{Batt}}{30\text{ nJ}} \approx 7\text{ kHz}. \tag{2.25}$$

Frequency (2.25) results to be rather high for most energy harvesting applications. As anticipated, a Battery Disconnect Circuitry (BDC) can be included to disconnect the battery from the system right after the generation of each pulse

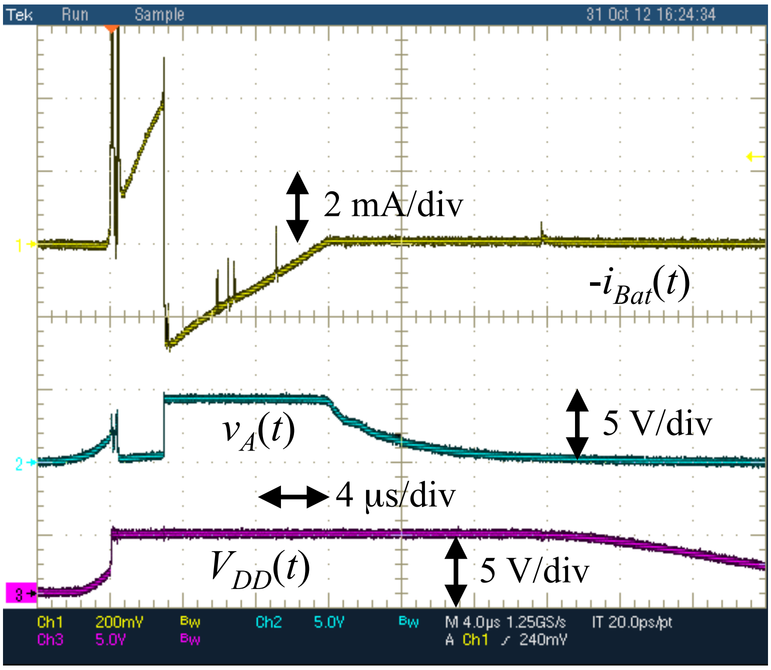


Figure 2.51: Experimental waveforms of the proposed energy harvester during a positive pulse Wiegand pulse and with the Optional Battery Disconnect Circuitry enabled. Upper trace: battery current $i_{Bat}(t)$ measured through a 100 Ω shunt resistor (200 mV/div, or 2 mA/div); middle trace: leg A output voltage $v_A(t)$ (5 V/div); lower trace: control logic supply voltage $V_{DD}(t)$ (5 V/div). Time base: 4 μs/div.

and improve low frequency efficiency. Experimental waveforms of the proposed harvester during a positive pulse with the BDC enabled are shown in Figure 2.51. In the figure, Channel 3 reports the supply voltage $V_{DD}(t)$ of the controller during circuit operation. After about 25 μs from the start of the Wiegand pulse the battery is disconnected from the circuit.

Including the BDC brings an additional source of energy dissipation into the power budget, due to both gate charge losses of devices M_1 and M_2 and conduction losses in M_1, M_2 and the pull-up resistor R_{D1}. An experimental investigation has been carried out to assess the validity of the BDC provision. The BDC network was added to the existing prototype using low-Q_g commercial MOSFET devices Si1016X. These exhibit a total of $Q_g = 2.25\ nC$, implying an energy loss of roughly 10 nJ/pulse. Measured maximum extracted energy with the incorporated BDC provision was about 10 to 12 nJ/pulse, independently of the excitation frequency. Smaller dissipation figures are achievable with a a fully integrated solution.

Conclusions

Power management systems have not to be considered as simple conversion stages, but as complex and intelligent systems, which aim to optimize the overall efficiency of the devices, manage in some cases different energy sources and optimize the charge/discharge of the energy storages also in hard environment conditions, because despite the great improvements made in batteries in therms of energy density and power density, the bottleneck in remote applications remains the energy needed for supply the electronic systems. In this thesis examples of complex power distribution systems are presented. Regarding power management systems in harsh environment, the effects of temperature, radiation, magnetic field and long cables for the LHC upgrade have been taken in care; ASIC DC/DC converters have been tested under radiation conditions, showing a good match with the simulation models, sign that the studies done are correct. Power distribution systems in remote applications examples covered only a small part of all the possible scenarios, in fact a lot of other sources can be considered, such as, for instance, thermoelectric generators; from the power electronics point of view, the future for this kind of applications is moving towards multi source systems, in order to collect all the available energy in the environment. Moreover a lot of harvesting sources and battery chemistries are under investigation and research, for this reason a continuous work in finding optimal architectures and strategies is almost necessary.

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