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Modelling, Simulation and Characterization of Tunnel-FET Devices for Ultra-low Power Electronics

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Contents

Abstract

In the last years a significant effort has been spent by the microelectronic industry to reduce the chip power consumption of the electronic systems since the latter is becoming a major limitation to CMOS technology scaling.

Many strategies can be adopted to reduce the power consumption. They range from the system to the electron device level. In the last years Tunnel Field Effect Transistors (TFET) have imposed as possible candidate devices for replacing the convential MOSFET in ultra low power application at supply voltages $V_{\mathrm{DD}} < 0.5$V. TFET operation is based on a Band-to-Band Tunneling (BtBT) mechanism of carrier injection in the channel and they represent a disruptive revolutionary device concept.

This thesis investigates TFET modeling and simulation, a very challenging topic because of the difficulties in modeling BtBT accurately. We present a modified Multi Subband Monte Carlo (MSMC) that has been adapted for the simulation of Planar Ultra Thin Body (UTB) Fully Depleted Semiconductor on Insulator (FD-ScOI) homo- and hetero-junction TFET implemented with arbitrary semiconductor materials. The model accounts for carrier quantization with a heuristic but accurate quantum correction validated by means of comparison with full quantum model and experimental results.

The MSMC model has been used to simulate and assess the performance of idealized homo- and hetero-junction TFETs implemented in Si, SiGe alloys or InGaAs compounds.

In the second part of the thesis we discuss the characterization of TFETs at low temperature. Si and SiGe homo- and hetero-junction TFETs fabricated by CEA-LETI (Grenoble, France) are considered with the objective to identify the possible presence of alternative injection mechanisms such as Trap Assisted Tunneling.

Résumé

Dans les dernières années, beaucoup de travail a été consacré par l'industrie électronique pour réduire la consommation d'énergie des composants micro-électroniques qui représente un fardeau important dans la spécification des nouveaux systèmes.

Afin de réduire la consommation d'énergie, nombreuses stratégies peuvent être adoptées au niveau des systèmes micro-électroniques et des simples dispositifs nano-électroniques. Récemment le Transistor Tunnel à effet de champ (Tunnel-FET) s'est imposé comme un candidat possible pour remplacer les dispositifs MOSFET conventionnels pour applications de très basse puissance à des tensions d'alimentation $V_{\mathrm{DD}} < 0.5\mathrm{V}$.

Nous présentons un modèle Multi-Subband Monte Carlo modifié (MSMC) qui a été adapté pour la simulation de TFET Ultra Thin Body Fully Depleted Seminconductor on Insulator (FD-SOI UTB) avec homo- et hétéro-jonctions et des matériaux semi-conducteurs arbitraires. Nous prenons en considération la quantification de la charge avec une correction quantique heuristique mais précise, validée via des modèles quantiques complets et des résultats expérimentaux.

Le modèle MSMC a été utilisé pour simuler et évaluer la performance de FD-SOI TFETs idéalisées avec homo- et hétéro-jonction en Si, alliages SiGe ou composés InGaAs.

Dans la deuxième partie de l'activité de doctorat un travail de caractérisation à basse température a été réalisé sur les TFETs en Si et SiGe homo- et hétéro-jonction fabriqués par le centre de recherche français du CEA -LETI. L'objectif est d'estimer la présence de l'effet Tunnel comme principal mécanisme d'injection et la contribution d'autres mécanismes d'injection comme le Trap Assisted Tunneling.

Chapter 1

Introduction

1.1 Scaling and power consumption trends in nanoelectronics industry

Over the last 40 years the electronics industry has constantly grown driven by *scaling*: that is, the continued reduction of the dimension of the switching device. In 1965 Moore extrapolated his famous law [1] stating that the device density in a chip approximately doubles every year. More recently the predicted trend has been corrected to about 1.5 years for doubling the density. To meet these expectations the microelectronic industry has made huge investments in research and development. The main reason for the success of Moore's Law and of the industrial effort to follow it resides in the extraordinary scalability of the Metal Oxide Semiconductor Field Effect Transistor (MOSFET), the fundamental building block of digital integrated circuits [2]. Until the beginning of the 1990's scaling has continued by reducing the device dimensions and the power supply voltage V_{DD} without appreciably changing the structure of the MOS transistor. A large number of innovations has nevertheless been introduced, like new materials with lower dielectric constant for isolating the interconnections, or new process steps like source/drain silicidation to reduce series resistances, lightly doped extension to contain channel hot electron degradation or shallow trench isolation to increase device density. Additional innovations allowed the device to scale further by reducing detrimental effects such as short-channel effects and by improving the electrostatic control of the gate over the channel.

In recent years, pure geometrical scaling has become more and more challenging. Beyond a certain limit the reduction of the SiO_2 oxide thickness and of the gate length becomes extremely difficult. In addition to reduce short channel effects it is indeed necessary to achieve a low off-state gate leakage and a stable and reliable oxide. The introduction of high-κ materials in the gate stack permitted Equivalent Oxide Thickness (EOT) reduction while maintaining a larger physical oxide thickness. The gate leakage has been reduced, but at the cost of reduced channel mobility [3, 4, 5, 6, 7]. To further improve the performance of the device, strain and band engineering has been introduced in the device design, thus allowing for higher drain currents without an actual reduction of the gate length [8]. The introduction of new device structures such as Fully Depleted Silicon On Insulator (FD-SOI), Double Gate (DG), Bulk FinFETs and SOI-FinFETs with enhanced electrostatic control of the gate over the channel reduces short-channel effects and leads to higher ON currents and better dynamic performance.

Another important aspect to take into account for CMOS technology development is the power consumption. In a digital integrated system the energy consumption for clock cycle can be estimated by the following equation [9]:

$$E_{\mathrm{tot}} = E_{\mathrm{stat}} + E_{\mathrm{dyn}} = \frac{1}{f} N V_{\mathrm{DD}} I_{\mathrm{off}} + aNCV_{\mathrm{DD}}^2 \tag{1.1}$$

where a is the activity factor (that is the probability for switching to take place), N is the number of logical gates, C is the average capacitance for the gates, f is the clock frequency that is supposed to be equal to the maximum $f_{max} = \frac{I_{\mathrm{on}}}{L_D C V_{\mathrm{DD}}}$, where L_D is the maximum number of logical gates that can be found in series in the combinatory logic circuit. The reduction of the supply voltage V_{DD} allows to scale down the power consumption of the system. Assuming to scale V_{DD} by the same factor β as the geometrical scaling, following the Dennard's scaling approach [10], the areal power density is constant while the power delay product scales down by a factor β^3. Scaling both the geometrical dimensions as the supply voltage is therefore a good strategy to scale down the devices and increase the performances maintaining stable the areal density power consumption. However as V_{DD} decreases, also the threshold voltage V_{TH} must be reduced to ensure functionality at circuit level and to maintain a sufficiently high ON state current.

In properly designed MOSFET with a channel longer than 10nm the mechanism of charge injection into the channel is thermionic emission over the source/channel barrier, and in the sub-threshold region the current increases exponentially with a semi-logarithmic swing expressed

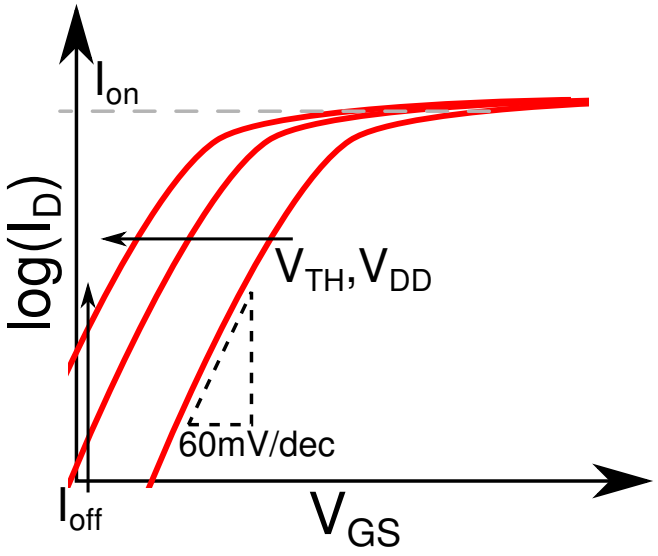

Figure 1.1: Schematic representation of MOSFET trans-characteristics. Reducing V_{DD} and V_{TH} the on current I_{on} is constant but the off current I_{off} increases exponentially if a constant subthreshold slope is maintained.

as [11]:

$$SS = \frac{\partial V_{\mathrm{G}}}{\partial \log_{10}(I_{\mathrm{D}})} = \frac{\partial V_{\mathrm{G}}}{\partial \Psi_S}\frac{\partial \Psi_S}{\partial \log_{10}(I_{\mathrm{D}})} \tag{1.2}$$

$$= \left(1 + \frac{C_{\mathrm{D}}}{C_{\mathrm{ox}}}\right)\frac{k_{\mathrm{B}}T}{q}\ln(10) \approx \ln(10)\frac{k_{\mathrm{B}}T}{q} \approx 60\mathrm{mV/dec}\ @\ T = 300K \tag{1.3}$$

where Ψ_S is the potential at the semiconductor/oxide interface, C_{ox} is the oxide capacitance and C_{D} the depletion capacitance [12]. The SS is incompressible below 60mV/dec and reducing V_{DD} and V_{TH} means that the off state current at V_{GS}=0V (I_{off}) will increase exponentially as reported in fig. 1.1. In practice short channel effects degrade appreciably the MOSFET characteristics and contribute to increase remarkably the I_{off} at short channel lengths. By reducing the gate dielectric thickness and accurately tailoring the dopant profiles, it has been possible to control SCE at the expense of reduced mobility [7]. Strain engineering also helped recover the degradation of channel transport properties [13]. The life of the bulk MOSFET architecture could then be extended until the 32 nanometer node. Alternative device geometries have been recently proposed and developed such as the FinFETs and the Trigate [14] or the Ultra Thin Body Silicon on Insulator (UTB-SOI) [15], that provide better electrostatic control of the gate on the channel and allow to approach the minimum thermionic emission limited SS value. However for a MOSFET it is not possible to go below the 60mV/dec limit at T=300K.

The reduction of power consumption in modern integrated circuits has become a compelling necessity addressed at various levels of the system design. CMOS technology is thus requested to provide enabling solutions for the power issue. An example is found in a complex integrated microelectronics system where different parts of the circuit with different functionalities (Input/Output, Memories, Core Logic, etc.) may need to fulfill different performance specifications and also to work at different supply voltages. These parts can be implemented with CMOS devices featuring different V_{TH}, and correspond to different values of I_{off} and I_{on}, following the so called Multi-threshold CMOS technology [16, 17], as reported schematically in fig. 1.2. The use of different thresholds voltages permits to distribute the power consumption where it is requested for fulfilling the performance requirements of the integrated system. Devices with

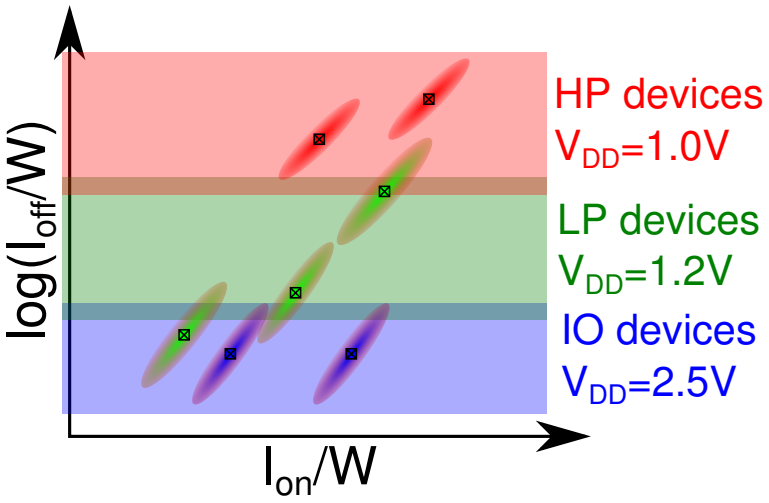

Figure 1.2: Schematic representation of the (I_{on},I_{off}) distribution for the devices included in the design kit of a Multi-threshold CMOS technology. The ellipse represent a Gaussian distribution that has its average value in the center represented with the x symbol. The color of the ellipse indicates the V_{DD} potential at which the device is designed to work, red for the high performance device with the lowest V_{DD}, green for the low power devices with an intermediate V_{DD} and blue for the Input-Output devices that work at the highest V_{DD}.

a higher I_{on} will be placed where high performances are requested allowing higher operation frequencies at the cost of a higher I_{off}. On the other hand in the part of the circuit where performance is not the priority, the use of slower devices (higher V_{TH}, lower I_{on} and lower I_{off}) reduces the power consumption by reducing the operation frequency and the static consumption. Interestingly, some of the new device architectures offer the remarkable advantage that the threshold voltage can be changed to some extent by adjusting an additional control voltage. This is for instance the case of the back-gate voltage in UTB-SOI MOSFETs [18]. Furthermore, at the circuit level as well as at the system level, a great variety of technological solutions and system design strategies can be applied to reduce the power consumption of the global microelectronic system, but a through analysis of all of them goes beyond the objectives of this introductory chapter and thesis.

1.2 Devices concepts for reduction of power consumption

To further improve the power performance of the electronic systems and scale the V_{DD} below the already quite aggressive target of 0.5V significant innovations will likely be necessary. In particular the incompressible barrier of 60mV/dec for the SS needs to be overcome. Ionescu et al. have pointed out in [19] that if a device structure can achieve a fixed I_{on}/I_{off} ratio at a fixed I_{on} with a lower V_{DD} this will result is a reduced energy consumption. This can be obtained only through a reduction of the SS, that is, by compressing the switching transition between the I_{off} and the I_{on} at a lower V_{DD}.

Many device concepts have been proposed to obtain lower SS values below the thermionic emission limit. They can be divided in two groups: the first tries to address the SS reduction by enhancing the gate-to-channel coupling i.e. by making the derivative of the channel surface potential with respect to the gate voltage higher than 1. Following this perspective a solution based on micro and nano-mechanical electrodes has been proposed. It exploits the instability point between the mechanical and the electrical force and allows a very abrupt transition

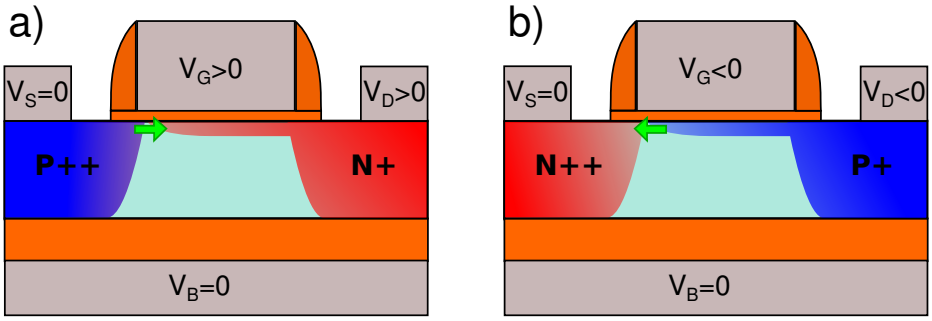

Figure 1.3: Schematic representation of the Tunnel FET device with an n-type configuration (a) and a p-type configuration (b). V_S and V_D respectively denote the source and drain voltage and identify the corresponding terminal.

between the on-state and the off-state with interesting I_{on} [20, 21]. The main drawback of this solution is related to the reliability of the micro-mechanical parts of the device.

An alternative concept that falls in the same category is the recently proposed Negative Capacitance-FET (NC-FET) [22, 23]. If a ferroelectric material is inserted in the gate stack, a negative capacitance arises. The result is a sort of "gate voltage amplification effect" that allows the gain between the applied gate potential and the surface potential to be larger than one. A major drawback for this concept is the presence of hysteresis caused by the ferroelectric polarization and the great difficulty in growing a high quality single crystalline ferroelectric material over the channel semiconductor or the gate oxide.

The second approach employs alternative injection mechanisms for the carriers: examples are the Impact Ionization MOSFET (IMOS) [24, 25, 26, 27] and the Punch Through Impact Ionization MOSFET (PIMOS) [28], where the charge in the channel is generated by impact ionization. All the device concept reported above show very interesting I_{on}/I_{off} ratio and SS but they all face difficulties in trying to overcome issues related to voltage and gate length scalability as well as consumption of chip area.

A promising device concept that relies on an alternative injection mechanism with respect to thermionic emission is the Tunnel Field Effect Transistor (TFET) [11, 19]. Its structure is schematically reported in fig. 1.3 for both p-type (pTFET) and n-type (nTFET) configurations. It consists of a gated p-i-n diode, where the carriers are injected from the source to the channel through a potential barrier via Band to Band Tunneling (BtBT) transitions from the valence band to the conduction band. The TFET device can be easily fabricated in complementary fashion, thus it is amenable to CMOS technology implementation. For the n-type device, the n+ region is the drain region and the p++ region is the source, the drain and the gate are biased with positive potential. On the other hand, in the p-type device the p+ region is the drain, the n++ region is the source, and the drain and gate are biased with a negative potential.

This is the structure of the thesis:

- After this first introductory chapter it follows the second chapter that describes the operation of the TFETs and reports the most interesting experimental results proposed in literature.

- In the third chapter the main semi-classical models for the estimation of the BtBT generation rate are classified and presented, both for the direct as for the phonon assisted tunneling transitions. The local and non-local direct BtBT model are derived, while for the phonon assisted tunneling a review of the main models found in literature is presented together with the evaluation of an approach for the BtBT parameters choice through the

band structure obtained with a 30 band k·p bands structure [29, 30].

- In the fourth chapter the implementation of the direct and phonon assisted dynamic non-local model implementation in a state-of-the-art Multi Subband Monte Carlo simulator is presented. The implemented blocks needed for the simulation of TFET are then described and validated by means of comparison with the results of TCAD software [31]. A heuristic correction methodology for taking into account the subband splitting effect on BtBT is presented and its results compared with the those of more fundamental models as the one proposed in [32].

- In the fifth chapter five study cases regarding the simulation and the optimization of certain geometry parameters of FD-SOI TFET structures implemented in Si, SiGe or III-V compound semiconductors. A specific attention has been payed in the choice of the BtBT model parameters for the simulation of the devices, taking into account other important physical effects affecting the Band Gap of the semiconductor (e.g. Band Gap Narrowing).

- In the sixth chapter the temperature characterization of Si/SiGe hetero-junction devices fabricated by CEA-LETI (France) is reported. An investigation of the injection mechanisms taking place inside the device is carried out, through the investigation of the trans-characteristic curves of devices of different lots.

- The seventh chapter regards the characterization of the device of TFETs fabricated by CEA-LETI, biased with opposite biasing at the front gate and at the back of the device. This to experimentally evaluate the working mechanism of an interesting new TFET device concept, that is, the Electron Hole Bilayer TFET [33].

- The first appendix regards the adaptation of the full quantum model in [32] in the case of a FD-SOI TFET device structure.

- The conclusion of this thesis reports the conclusions and the final remarks.

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Chapter 2

The Tunnel FET (TFET) device

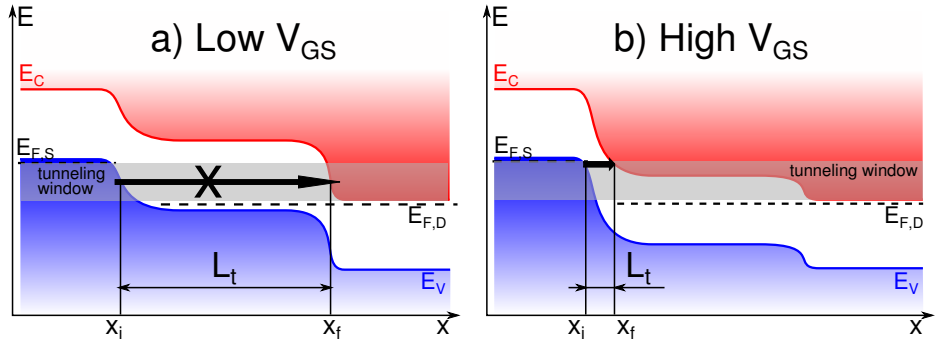

Figure 2.1: Schematic representation of the valence and conduction bands at low V_{GS} (plot a) and at high V_{GS} (plot b).

2.1 The TFET device principle

To illustrate the TFET working principle we sketch in fig. 2.1 the switching mechanism of an n-type device by representing the band profiles along the channel. Two concepts are key to understand TFET operation: the tunneling distance L_t and the tunneling window in energy. Supposing that an electron is in the valence band at point x_i with a negligible kinetic energy, its total energy is $E \approx E_V(x_i)$. The electron, subject to the electric field given by dE_V/dx could have an elastic transition from the valence band across the potential barrier represented by the band gap to reach the conduction band at the point x_f. Since the energy is conserved $E_C(x_f) = E_V(x_i)$. This kind of transition is called as Tunneling process and the distance between its initial and final points is called Tunneling Length L_t. The tunneling window in energy is related to the fact that the transition can happen only if the minimum of the conduction band $E_{C,min}$ is lower than the maximum of the valence band $E_{V,max}$. Therefore the points in the channel where an electron can start the tunneling transition to the conduction band are characterized by the following relation $E_{C,min} \leq E_V(x_i) \leq E_{V,max}$.

In presence of a strongly degenerate semiconductor material this definition of the tunneling window does not hold anymore. If at the starting point of the transition the semiconductor material is degenerate and acceptor doped the Fermi Level will be inside the valence band. Consequently the probability of finding an electron for energies higher than the Fermi level will decrease exponentially. Clearly no transition can happen if there are no electrons to be moved to the conduction band. On the other hand if the transition ends in a section of the channel where the semiconductor is degenerate and donor doped the probability to find an electron at energies lower then the Fermi Level is near to one. This means that the states lower in energy than the Fermi Level will be full, and for the Pauli's exclusion principle, they cannot be a target for the electron tunneling. Therefore the tunneling window can be defined as the energy interval between $\min(E_{V,max}, E_{F,S})$ and $\max(E_{C,min}, E_{F,D})$, as illustrated in fig. 2.1, where the source is degenerate and the window is limited by the Fermi level at the source side and the minimum of the conduction band at the drain side. V_{GS} controls the switching of the device by moving down the conduction and the valence band in energy. As the V_{GS} potential increases an inversion layer is created under the oxide/semiconductor interface and the conduction band must decrease consistently with the occupation statistics. Since the conduction band is pinned at the source, as the V_{GS} increases, the tunneling distance is reduced as illustrated in fig. 2.1-a and -b. The consequent reduction of the tunneling length implies an exponential increase of the BtBT transition probability and therefore of the BtBT current.

A distinctive feature of the non-thermionic BtBT injection mechanisms is the variable logarithmic slope in the sub-threshold region of the $I_{DS} - V_{GS}$ characteristics. Seabaugh et al. have shown [1] that for a TFET if the BtBT current at the source/channel junction is computed

using the Kane model [2] (that will be presented in the chapter 3) the Subthreshold Swing can be expressed as:

$$SS = \left(\frac{d \log_{10}(I_{\mathrm{D}})}{dV_{\mathrm{GS}}} \right)^{-1} = \log(10) \left[\frac{1}{V_{\mathrm{R}}} \frac{\partial V_{\mathrm{GS}}}{\partial V_{\mathrm{R}}} + \frac{B + \xi}{\xi^2} \frac{\partial \xi}{\partial V_{\mathrm{GS}}} \right]^{-1} \tag{2.1}$$

where $V_{\mathrm{R}} = E_{\mathrm{V,max}} - E_{\mathrm{C,min}}$ is the band overlap in eV, ξ is the applied electric field at the source/channel junction, and B is the exponential constant in the Kane model [2] given by:

$$B = \frac{4\sqrt{2m_r^*} E_{\mathrm{G}}^{3/2}}{3q\hbar} \tag{2.2}$$

where $m_r^* = (m_c^{-1} + m_v^{-1})^{-1}$ is the reduced mass, being m_c and m_v the effective mass for the conduction and valence band, respectively. Assuming that the electrostatic control is optimal, we have $\frac{\partial V_{\mathrm{GS}}}{\partial V_{\mathrm{R}}} \approx 1$. If we consider only the first term in eq. 2.1 and we assume that the electrostatic control of the gate on the channel is optimal, we can approximate $V_{\mathrm{R}} \approx V_{\mathrm{GS}} - V_{\mathrm{GS0}}$ where V_{GS0} is the gate potentials at which $V_{\mathrm{R}} = 0$. Under these assumption SS $\approx \log(10) V_{\mathrm{R}}$. On the other hand, considering only the second term of the sum in eq. 2.1, SS will be small as far the gate voltage is able to control the value of the electric field applied to the source/channel junction [3]. In other words, as far as $\frac{\partial \xi}{\partial V_{\mathrm{GS}}}$ is large. This condition can be obtained if the gate edge is well aligned with the source-channel junction, if the source doping has a shallow profile at the junction and if the source doping is high [3, 4].

The SS dependence on V_{GS} is an extremely interesting feature that should result in SS lower than the thermionic emission limit at low V_{GS}. Experiments systematically show that the slope is indeed variable with V_{GS} but unfortunately it is difficult to observe an SS<60mV/dec at room temperature. The reasons for this are multiple but the most significant ones are a non-effective electrostatic control, other injection mechanisms (e.g. the Trap-Assisted Tunneling), and the ambipolar leakage at the channel/drain junction.

2.2 TFET I-V characteristics

Fig. 2.3 reports the trans-characteristics and the output characteristics of a n-type FD-SOI Silicon TFET (sketched in fig. 2.2) as obtained with the Sentaurus Device (SDevice) simulator [5]. The BtBT model used in this simulation is the dynamic non-local phonon assisted model, that will be presented in chapter 3. The gate metal work-function E_{wf}=4.08eV is chosen to obtain $I_{\mathrm{D}} \approx$1pA/μm at V_{GS}=0V, the corresponding SS is approximately 55mV/dec. The considered device is aggressively scaled in the vertical direction, but nevertheless simulations show an ON-state current ($V_{\mathrm{GS}} = 3$V and $V_{\mathrm{DS}} = 1$V) that is only $\approx 1\mu$A/μm. This value is too low for applications as those guiding the specification of the International Road Map for Semiconductor Industry (ITRS) for ultra low standby power (LSTP) applications, which are the less demanding in terms of I_{on} current [6]. Indeed the LSTP ITRS for $V_{\mathrm{DD}} = 0.5$V requires I_{off}=1pA/μm and I_{on}=10μA/μm. The main difference between plot a) and c) is at $V_{\mathrm{GS}} < 0$V where plot c), which refers to the higher drain doping density, shows a non negligible current for both positive and negative V_{GS} due to BtBT at the drain side of the channel. Plots b) and d) report the output characteristics. As can be seen, differently from a conventional MOSFET, at low V_{DS} the current does not have a linear behavior; rather it is characterized by an exponential onset. At higher V_{DS} the output characteristics are linear until I_{D} reaches the saturation and, then, the current becomes flat and no longer shows a dependence on V_{DS}.

The main reason behind the low I_{on} current is the large band gap of silicon ($E_{\mathrm{G}} = 1.12$eV), that requires high V_{DS} and V_{GS} potentials to reduce appreciably the tunneling distance. Therefore, a straightforward strategy to enhance the device performance, is the choice of channel materials with lower band gap like SiGe alloys, Ge or narrow band gap III-V compounds, and

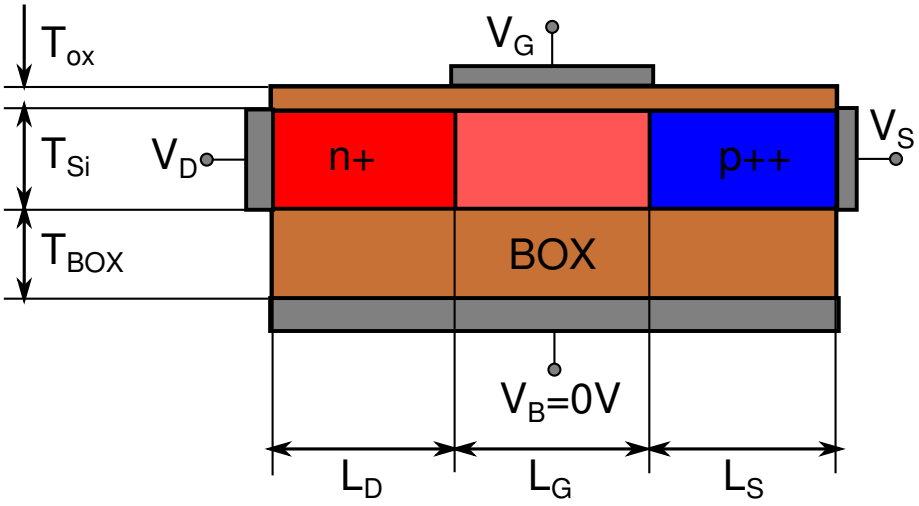

Figure 2.2: Sketch of the simulated UTB FD-SOI TFET. The channel material is pure unstrained Silicon with a thickness T_{Si}=5nm, the gate dielectric has an equivalent oxide thickness EOT=0.7nm, source acceptor doping is $N_{\mathrm{A,s}} = 10^{20}\mathrm{cm}^{-3}$, the channel is intrinsic. The drain donor doping density is considered to have two different values $N_{\mathrm{D,d}} = 10^{18}\mathrm{cm}^{-3}$ and $N_{\mathrm{D,d}} = 10^{20}\mathrm{cm}^{-3}$ to evaluate its effect on ambi-polar leakage effect. Gate length L_{G}=30nm, source region length L_{D}=50nm , drain region length L_{S}=100nm. The gate edges are aligned with the source and the drain junctions. The doping profile is abrupt.

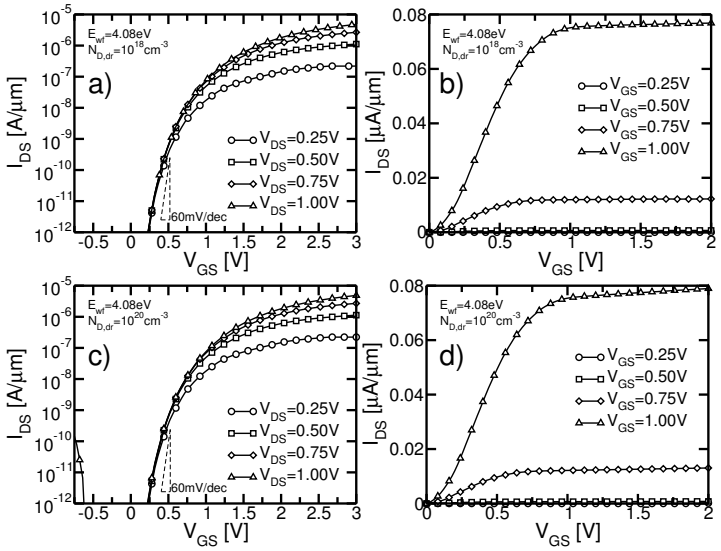

Figure 2.3: Trans-characteristics and output characteristic of a n-type FD-SOI Tunnel FET represented in fig. 2.2 simulated with Sentaurus Device. In plots a) and b) the drain doping has a value of $N_{\mathrm{D,d}} = 10^{18}\mathrm{cm}^{-3}$ while in plots c) and d) the drain doping density has a higher value corresponding to $N_{\mathrm{D,d}} = 10^{20}\mathrm{cm}^{-3}$.

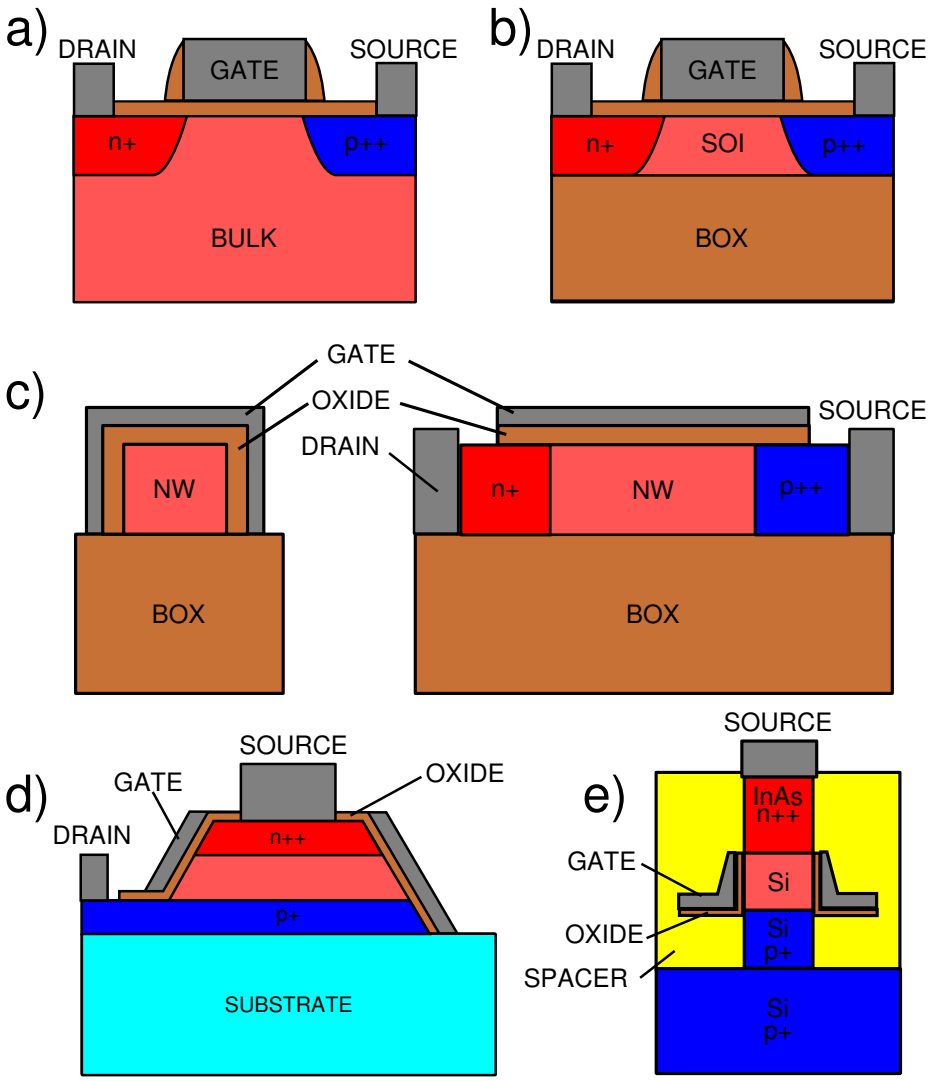

Figure 2.4: Schematic representation of TFET structures that have been experimentally implemented. a) bulk planar structure, b) UTB FD-SOI planar structure [7, 8, 9, 10, 11, 12, 13, 14], c) Ω-gated nanowire [15, 16, 17, 18] (left: section view at the mid distance between source and drain, right: section along the transport direction, d) 3D mesa structure typical of the TFET implemented with III-V compounds [19, 20, 21], e) vertical nanowire hetero-junction structure using Si (111) in the substrate and in the drain and channel part of the nanowire while InAs and epitaxially grown over the Si for the source (to separate the gate oxide from the drain region a dielectric spacer is used) [22, 23, 24].

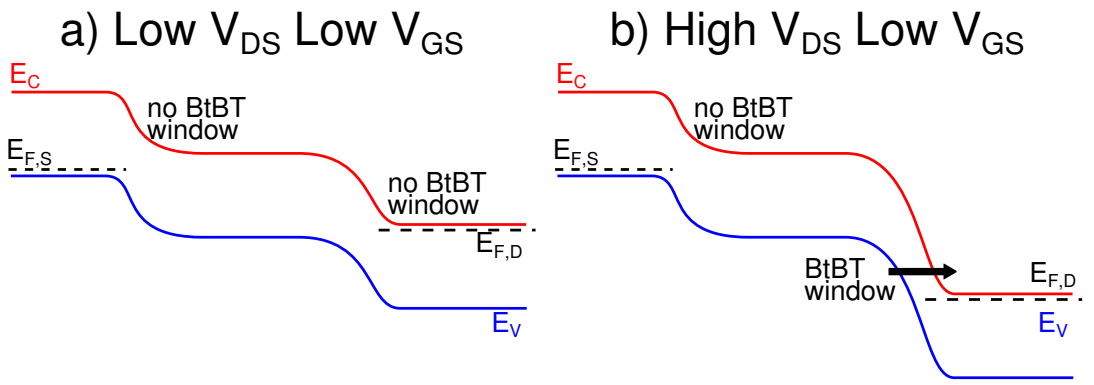

Figure 2.5: Schematic representation of the band profile at V_{GS} and low V_{DS} (plot a) and at low V_{GS} and high V_{DS} (plot B).

to improve as much as possible the electrostatic control of the gate electrode on the channel, by using alternative structures as schematically presented in fig. 2.4. Fig. 2.4-a represents the bulk planar structure that features an inefficient electrostatic control. Alternative structures that improved the electrostatic control are the UTB FD-SOI planar structure [25, 14] (fig. 2.4-b) and the Ω-gated nanowire [17, 18] (fig. 2.4-c). For the latter the left sketch shows the section view at the mid distance between source and drain while the right one shows the section along the transport direction. The electrostatic control improves if the EOT and the semiconductor thickness (for the SOI planar structure) or the nanowire section area (for the nanowire structure) are reduced. These structures have been used in conjunction with channel materials like strained or unstrained Si, SiGe alloys or Ge [14, 18]. Fig. 2.4-d instead shows the 3D MESA structure that has been used for prototypic TFETs implemented with III-V compounds [21]. Finally fig. 2.4-e reports a vertical hetero-junction InAs-Si nanowire structure [24, 22]. The combined effect of the nanowire structure and the hetero-junction with a narrow band gap material (InAs) and a wide band gap material (Silicon) theoretically should allow for a good electrostatic control, high ON-state current and reduced ambipolar leakage.

2.2.1 Leakage current at low V_{GS}

Fig. 2.5 reports the conduction and valence band profiles in a generic TFET device at low V_{GS} and with either a low V_{DS} (plot a) or a high V_{DS} (plot b). The quasi Fermi level at the source is taken as a reference and the quasi Fermi level at the drain is obtained as $E_{F,D} = E_{F,S} - qV_{DS}$ where q is the elementary charge. In plot a) BtBT cannot take place neither at the source channel junction nor at the channel drain junction because the valence band edge at the source and at the channel are higher than the conduction band edge at the channel and at the drain respectively. Consequently the only tunneling window is the one directly between source and drain that is characterized by an excessively long tunneling path.

At low V_{GS} increasing the drain potential moves down the electron quasi Fermi level along the drain and the whole channel. In the drain the bands go down in energy while in the channel the band profile is controlled mainly by the gate potential. Consequently at the source the BtBT transition will be prevented by the absence of a tunneling window, but, at the same time, the channel/drain junction will be subjected to an increasing field leading to the opening of a tunneling window and consequently to the generation of a BtBT leakage current. Clearly this ambipolar leakage current will be higher if the band gap of the material is narrower.

A first option for the reduction of the ambipolar leakage current is to reduce the dopant density of the drain. Fig. 2.6 reports the band profiles at the upper semiconductor/oxide interface as simulated with SDevice for the TFET device in fig. 2.2 considering either a drain

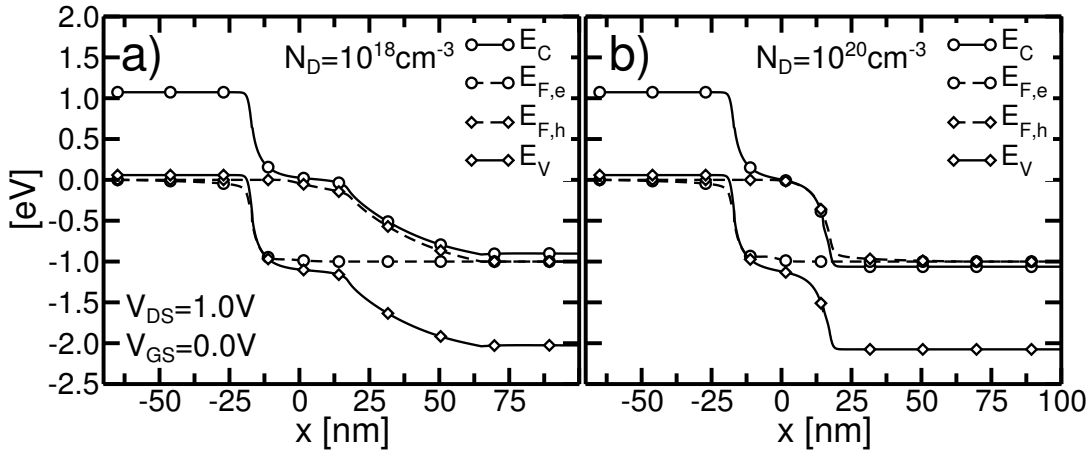

Figure 2.6: Band profiles at the upper semiconductor/gate interface as simulated with Sentaurus SDevice for the TFET device in fig. 2.2 considering either a drain doping density $N_{\mathrm{D}} = 10^{18}\mathrm{cm}^{-3}$ (plot a) or $N_{\mathrm{D}} = 10^{18}\mathrm{cm}^{-3}$ (plot b).

doping density $N_{\mathrm{D}} = 10^{18}\mathrm{cm}^{-3}$ (plot a) or $N_{\mathrm{D}} = 10^{20}\mathrm{cm}^{-3}$ (plot b). The reduction of the drain doping density results and in a larger junction depletion width that corresponds to a longer tunneling distance. The main drawback of this approach is that low drain doping levels imply a higher resistance at the drain, degrading the performance at high V_{GS} when a larger amount of current is supposed to pass through the device.

A second approach is the one followed in [25, 26] where an underlap between the gate and the drain is introduced in the device design to reduce the electro-static coupling between the gate and the channel/drain junction. This solution allows for higher drain doping concentration and, therefore, for a higher conductance of the drain region.

A third approach is to introduce a hetero-junction between the source and the channel, with the source implemented with a low band gap material (SiGe, Ge, InAs, InGaAs) and the channel and the drain with a wider band gap material. At low V_{GS} the leakage BtBT at the drain is exponentially reduced by the wide band gap of the second material. At high V_{GS} the BtBT transition at the source is enhanced by the narrower band gap of the source material. Fig. 2.7 reports a qualitative representation of the band profiles at the two sides of a hetero-junction made by a narrow band gap material in the source and a wide band gap material in the channel and in the drain. Materials have different electron affinities. In plot a) we sketch the case when the affinity is almost the same for the source and the channel (e.g. $\mathrm{Si}_{0.85}\mathrm{Ge}_{0.15}$/Si). In this case the current is mostly dominated by the BtBT transition at the source-channel junction. The electron, after the transition in the conduction band, can flow to the drain. In plot b) we sketch the case when $\chi_{ch} < \chi_s$ that implies the presence of a barrier in the conduction band at the hetero-junction. The BtBT transition probability is reduced and if the tunneling path ends at the left side of the hetero-junction the barrier may prevent the particle to move toward the drain. The barrier can be overcome by the particle only through thermionic injection (which implies a SS degradation) or through Fowler-Nordheim tunneling (which can cause a reduction of the current). This particular configuration should thus be avoided. In plot c) we represent the case of the staggered hetero-junction ($\chi_{ch} > \chi_s$). In this case the tunneling probability at the source-channel junction is enhanced by the descending step in the conduction band at the hetero-junction, that reduces the tunneling distance. The drawback with this particular configuration is that it becomes more difficult to switch off the device: a negative V_{GS} or a particularly high work function energy E_{wf} may be required. Finally in plot d) we represent the case when $\chi_{ch} - \chi_s > E_{\mathrm{G,s}}$ resulting in the so called "broken band gap" hetero-junction

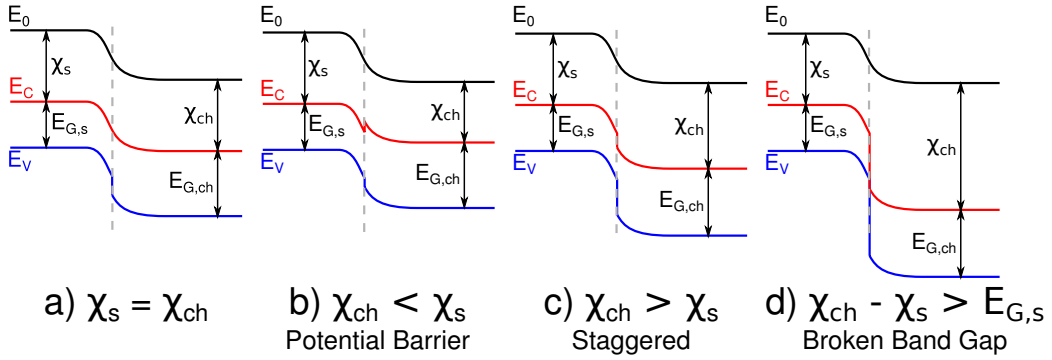

Figure 2.7: Schematic representation of the band profiles at the two sides of a hetero-junction between low E_G source and high E_G channel of a typical TFET. The energetic level of the vacuum E_0 is taken as reference. Plot a) represent the case when the electron affinities χ_s and χ_{ch} have the same value. Plot b) represent the case when $\chi_{ch} < \chi_s$ with the creation of a potential barrier. Plot c) represent the case when $\chi_{ch} > \chi_s$ resulting in a staggered hetero-junction. Plot d) represent the case when $\chi_{ch} - \chi_s > E_{G,s}$ resulting in a broken band gap hetero-junction.

that permits tunneling path with a length theoretically equal to zero. As qualitatively sketched in fig. 2.8 for any gate potential V_{GS} BtBT always takes place and the only way to shut down the whole device is to have $V_G \ll 0$V creating a potential barrier in the channel and in the source (fig. 2.8-b) that prevents the generated electrons and holes to flow toward the drain and the source, respectively. Therefore, with this configuration, it is possible to have very high I_{on}, as well as, with a high I_{off}.

Another important element to take into account when introducing a hetero-junction in a device design is the possible lattice mismatch between the two materials, that induces strain and that entails the possible presence of defects and traps at the interface. Strain can enhance or degrade the BtBT transition probability depending on the particular strain configuration introduced by the hetero-junction and it is not trivial to evaluate without an accurate analysis of the band gap between the valleys of valence and conduction band and the respective effective masses. Traps are energy states in the band gap that can be occupied by an electron. Fig. 2.9 reports the main transitions involving an electron and a trap. Steps 1) and 2) are typical of Trap-Assisted-Tunneling (TAT) and are enhanced by the electric field that lowers the barrier seen by the electron allowing it to tunnel from the valence band into the trap and then from the trap into the conduction band. Steps 3) and 4) are typical of the Shockley Read Hall (SRH) generation mechanism, where the thermal interaction of the electron with the lattice vibrations gives it the energy to reach the trap energy level and then from the trap to reach the conduction band. It is not mandatory for the particle to accomplish steps 1) and 2) alone or steps 3) and 4) alone. The particle can reach the trap by tunneling (1) or through the interaction with the lattice vibration (3). Once in the trap it can reach the conduction band again by tunneling (2) or by interaction with phonons (4). Traps in the device are found mainly at the interface between oxide and semiconductor and at the hetero-junction interfaces where as said above the lattice mismatch can cause dislocations and defects. The trap concentration may be significantly high e.g. in SiGe the dislocation density is about $10^5 - 10^6 \text{cm}^{-2}$ [27, 28]. Given the proximity both in energy and in physical distance of the traps the transition probability is much higher than considering the pure BtBT from the valence to the conduction band. At low V_{GS}, where the electric field is weak and the tunneling distance is longer, jumping from the valence to a trap and then jumping from trap to trap, represents for the particle a path to reach the conduction band with a total probability that is the product of the probability of all

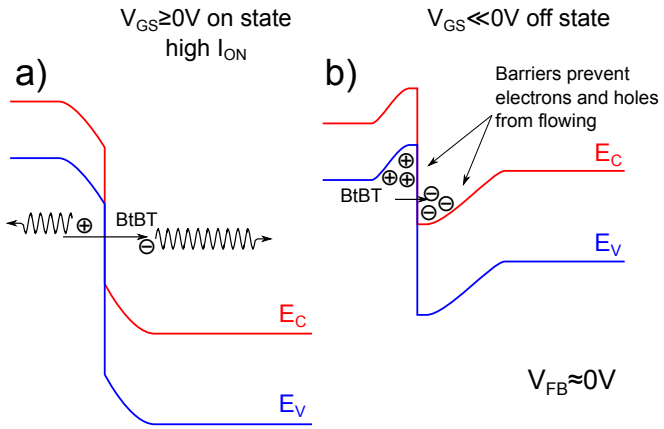

Figure 2.8: Qualitative sketch of a TFET source/channel broken gap hetero-junction. BtBT takes place for any V_{GS}, but considering, for the sake of simplicity, the flat band voltage to be $V_{FB} \approx 0$V, for $V_{GS} \ll 0$V, two barriers that prevent the carriers to move are generated in the source and the drain.

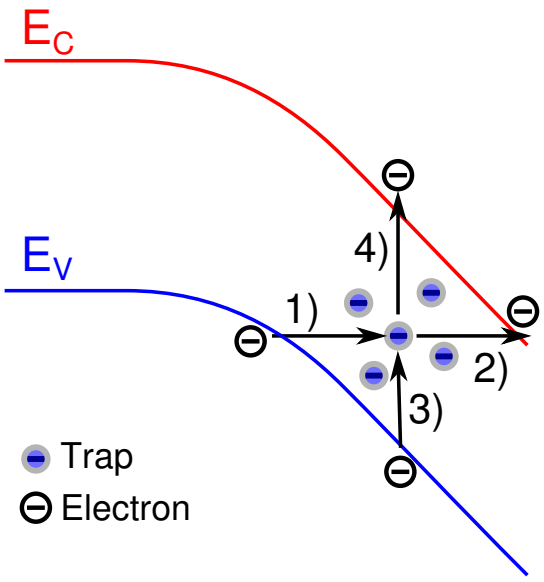

Figure 2.9: Schematic representation of the available transitions for an electron in the valence band to cross the potential barrier and reach the conduction band in the presence of a trap. Steps 1) and 2) are typical of the Trap Assisted Tunneling transitions and are enhanced by the field. Steps 3) and 4) are typical of Shockley Read Hall transitions and are driven by the interaction of the electrons with phonons.

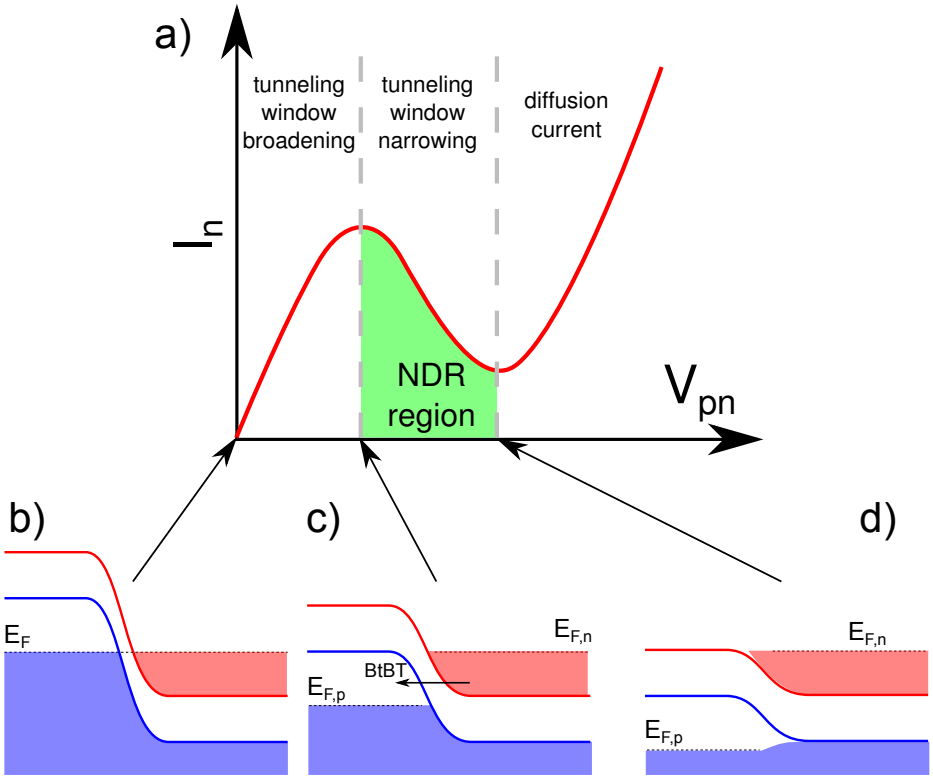

Figure 2.10: Qualitative representation of the characteristic of an Esaki diode (plot a) and of the bands profile in point of equilibrium (plot b), of maximum tunneling window (plot c), and in the point where diffusion current become dominant (plot d) as in a conventional p-n junction.

the step and that is much higher than the probability of the single BtBT transition. Indeed the pure BtBT transition probability decreases exponentially with the tunneling distance.

Another physical effect that can degrade the trans-characteristics of a TFET at low V_{GS} is the Drain Induced Barrier Thinning (DIBT). Similarly to the MOSFET counterpart, the Drain Induced Barrier Lowering (DIBL), in the TFET with a short channel the drain bias has an effect on the electrostatic of the whole channel with a reduction of the tunneling distance at the source that is modulated by the drain potential. Liu et al. have compared the effect of the channel scaling on the MOSFET DIBL and on the TFET DIBT [29]. They found that the worsening with the channel scaling of the DIBT for the TFET structure is much lower than the DIBL for a corresponding MOSFET when the channel length is not aggressively scaled ($L_G > 30$nm). On the other hand for short L_G (or considering a worse electrostatic control of the gate on the channel) the DIBT effect increases exponentially with a severe degradation of the ambipolar leakage of the device.

2.3 Overview of the Experimental TFETs in literature

In 1954 Esaki [30] has demonstrated that in a Germanium p-n junction with degenerate doping concentrations the inter band tunneling (Band to Band Tunneling BtBT) was the reason for the Negative Differential Resistance (NDR) that was found in I-V characteristic as sketched in fig. 2.10-a. At $V_{pn} = 0$V (equilibrium condition) no exchange of charge is possible (fig. 2.10-b). As V_{pn} increases the tunneling window begins to broaden and consequently BtBT

current begins to flow until it reaches its maximum when $E_{F,n} \approx E_{C,p}$ (fig. 2.10-c), where $E_{C,p}$ is the conduction band edge in the p++ region. For higher V_{pn} the tunneling window begins to narrow again with a consequent reduction of the tunneling current and NDR behavior. Eventually the current starts to increase again when V_{pn} is high enough to counterbalance the built-in potential barrier (fig. 2.10-d) allowing the electrons and holes to diffuse in the p++ and n++ region, respectively.

After the work of Esaki his tunnel diode has been used in high frequency circuits exploiting the NDR part of the device characteristic. Quin et al. in 1978 [31] have proposed the first gated p-i-n structure with the aim of investigating the subband splitting and the effective mass in the quantized 2D electron gas. The research on tunneling structures has then been focused on the control of the NDR in three-electrode structures. In 1978 Leburton [32] proposed the first vertical p-i-n structure called Bipolar Tunneling FET with the aim of implementing a high speed transistor using the steep NDR region expected in the output characteristic of that device and controlling it with a gate electrode. Various results have been presented trying to improve the control of the NDR behavior with a gate electrode [33, 34, 35, 36, 37].

In 2000 Hansch et al. proposed and fabricated a vertical structure with a lateral gate implemented in Silicon and found that the device allowed for high gain with a low off-state current and therefore was an interesting option as low power consumption device. In 2004 Bhuwalka and Wang [38, 39] for the first time introduced the theoretical analysis of the subthreshold swing of tunneling device and Zhang in 2005 [40] derived an analytic expression demonstrating that the gate controls both the electrostatics of the tunnel junction and the band overlap allowing for less than 60-mV/decade subthreshold swing at room temperature.

2.3.1 Experimental Si, SiGe, Ge TFET devices

Many device structures have been proposed in the literature trying to overcome the limitations of the basic TFET structure. In 2007 Choi et al. [7] presented the first experimental result of a sub 60mV/dec subthreshold swing. It was a SOI structure with a raised epitaxial grown drain. The SiO_2 oxide thickness was T_{ox}=2nm, the gate length L_G=70nm the Silicon thickness T_{Si}=70nm. The trans-characteristic at V_{DS} = 1.0V shows that the minimum I_D current is limited by the ambi-polarity leakage at I_{off}=1nA/μm with an on state current I_{on}=12.1μA/μm at V_{GS}=1.0V. The minimum SS found was 52.1mV/dec.

As stated above, to improve the ON current a first option is to use a material with a narrower band gap like SiGe or Germanium and in 2008 Mayer et al. [25] compared the result of TFET devices implemented as Fully Depleted SOI, $Si_{1-x}Ge_x$ on insulator and Ge on Insulator with HfO_2 gate oxide (T_{ox}=3nm). To reduce the I_{off} an intrinsic region (not covered by the gate) has been introduced between the drain and the channel. The ON-state current for the SOI is $I_{on} \approx 1\mu A/\mu m$ (both n-type and p-type configurations). The comparative results reported in this work demonstrate that the on-state current improvement given by the introduction of $Si_{1-x}Ge_x$ with x=0.15 and x=0.30 is in the order of 10x and 15x with respect to the SOI device. On the other hand the I_{on} of the Germanium on Insulator device is much higher with $I_{on} \approx 3\mu A/\mu m$ and $I_{on} \approx 1\mu A/\mu m$ for the p-type and the n-type configuration, respectively. The OFF-state current I_{off} ≈1pA/μm for the SOI, while for the GeOI devices the ambipolar leakage current is much higher with a reduced I_{on}/I_{off} ratio. The minimum subthreshold swing found in the p-type configuration is 42mV/dec for the SOI devices.

Trying to enhance the I_{on} further by the band gap reduction, in 2008 Krishnamohan et al. [9] have proposed a hetero-junction SOI TFET with a channel composed by a stack of a layer of Silicon followed by a compressively strained Ge layer and a Silicon cap layer. The strained Germanium layer presents a lower band gap. The measurements are carried out in a double gate mode, with a back-gate potential $V_{BG} = V_{FG} \cdot C_{ox,1}/C_{ox,2}$ where $C_{ox,1}$ and $C_{ox,2}$ are the oxide capacitance of the front gate stack and of the BOX respectively and V_{FG} is the bias potential of the front gate. At the lower value of V_{DS} = 0.1V, SS=50mV/dec is reported but the ambipolar

leakage current increases with $V_{\rm DS}$, thus increasing $I_{\rm off}$. At $V_{\rm DS}$=1V the ON-state current is $I_{\rm on}$ ≈1μA/μm.

An alternative structure implemented with Germanium on Insulator has been proposed by Kazazis et al. [8] featuring a epitaxially grown raised Ge source: the gate oxide is HfO_2 with $T_{\rm ox}$=6nm. The authors obtained $I_{\rm on}$ ≈1.6μA/μm and $I_{\rm off}$ ≈0.16μA/μm. The on-state current is interesting but the ambipolar behavior due to the narrower Germanium band gap and to a not so effective electrostatic control degrades significantly the $I_{\rm on}/I_{\rm off}$ ratio.

To overcome this limitation, in 2009 Kim et al. [10] have proposed a planar hetero-junction SOI TFET device with a Germanium source. The gate oxide is SiO_2 with $T_{\rm ox}$ = 3nm and the silicon thickness is $T_{\rm Si}$ = 70nm. At $V_{\rm DS}$=$V_{\rm GS}$=0.5V the obtained ON-State current is $I_{\rm on}$ = 0.42μA/μm while $I_{\rm off}$ ≈ 0.1pA/μm. The reported minimum SS is approximately 40mV/dec.

Following a strategy similar to the one proposed by Mayer et al. [25] for the reduction of the ambipolar leakage current, in 2010 Wan et al. [11, 26] proposed an SOI device with a semiconductor thickness of $T_{\rm Si}$=20nm. Results are reported for a 6nm SiO_2 gate oxide and a 3nm HfO_2 gate oxide. Clearly the better electrostatics obtained with the thinner HfO_2 gate oxide allows for higher $I_{\rm on}$ and steeper SS. The $I_{\rm on}$ is nevertheless low and approximately equal to 10 nA/μm at high $V_{\rm DS}$ and $V_{\rm GS}$. The noise spectrum of the current has been measured and found to be characterized by a Lorentzian distribution $1/f^2$, consistently with a random telegraph noise source that is considered to be a distinctive characteristic of the BtBT injection mechanism with respect to the thermionic injection typical of MOSFET device that has a $1/f$ low frequency noise distribution.

An additional strategy for improving the on-state current has been proposed in 2010 by Jeon et al. [12], exploiting dopant segregation, a mechanism that occurs during the silicidation: the dopant atoms are moved from the silicidated region to the pure semiconductor region, resulting in very high dopant concentrations and shallow doping profiles. Jeon et al. proposed a planar hetero-junction SOI TFET with silicidated source and drain that, exploiting dopant segregation, presented high doping density and shallow profiles that enhanced the field at the junction. The reported minimum SS is 46mV/dec and, at $V_{\rm DS}$ = −1.0V, the p-type shows $I_{\rm on}$ ≈ 0.3μA/μm and $I_{\rm on}/I_{\rm off}$ ≈ 10^7.

As stated above, the SS can be improved by choosing a device geometry that allows for better electrostatic control. In 2010 Leonelli et al. [15] have proposed a FinFET like structure with multiple channels on a SOI substrate. A high-κ material is used for the gate stack. $I_{\rm off}$ ≈1pA/μm, $I_{\rm on}$ ≈2μA/μm, and a minimum SS=42mV/dec are reported.

In 2011 Zhao et al. [13], trying to exploit strain in a hetero-junction structure, proposed a structure with compressively strained $Si_{0.5}Ge_{0.5}$ ($\epsilon_{SiGe} = -1.4\%$) epitaxially grown source and a tensile strained ($\epsilon_{Si} = 0.8\%$) SOI channel. The on-state current at $V_{\rm D}$ = −1V is $I_{\rm on}$ ≈1μA/μm while $I_{\rm off}$ ≈1nA/μm with a SS≈80mV/dec.

The nanowire is an alternative geometry that also allows for good electrostatic control and in 2012 Knoll et al. [41] have presented a nanowire TFET device with dopant segregation in presence of silicidation and tilted doping implantation, that permits to have p++ and n++ pocket aligned with the gate edges. A high-κ HfO_2 gate oxide is used with $T_{\rm sc}$=3nm. At $V_{\rm DS}$=-0.5V the p-type trans-characteristics features an $I_{\rm off}$=1pA/μm and an $I_{\rm on}$=100nA/μm at $V_{\rm GS}$=-0.5V with a minimum SS≈60mV/dec.

In 2012 Richter et al. [17] have presented an Ω-gated nanowire device and compared a device implemented in unstrained Silicon and one implemented in tensile strained Silicon (ϵ=0.5%). The nanowire devices have been fabricated using two distinct gate oxide stacks: SiO_2 with $T_{\rm ox}$=5nm or a 3nm layer of HfO_2 over a 2nm layer of SiO_2. The introduction of tensile strain reduces the band gap with a consequent six times increase of the current compared to the unstrained Si device. Considering the p-type configuration, the strained device implemented with HfO_2 in the gate oxide shows better electrostatic control and a steeper minimum SS=76mV/dec. At $V_{\rm DS}$ = −0.9V, the OFF-state current is $I_{\rm off}$ ≈ 1pA/μm at $V_{\rm GS}$ = −0.5V and the ON-state current is $I_{\rm on}$ ≈ 0.4μA/μm at $V_{\rm GS}$ = −2.5V. At high $V_{\rm GS}$ = −4.5V the output characteris-

tic of this device presents negative differential conductance that is attribute to hot electrons generated in the high field region between source and drain, that can be injected in the oxide. These charges trapped in the oxide screen the gate, thus reducing the electrostatic control at the source/channel junction, explaining the reported I_D reduction.

A further experimental analysis of TFET structures containing strained SiGe layers has been carried out in 2012 by Villalon et al. [14] in a work where different strained Si/SiGe on Insulator Hetero-junction TFET structures are presented and compared with MOSFETs fabricated on the same wafer and using the same technological process. For all the presented structures the source and the drain are epitaxially grown $Si_{0.7}Ge_{0.3}$ and the gate stack contains HfO_2 with an EOT 1.2nm. The composition of the channel, instead, is different. The best SS results are obtained by a structure with the channel composed by a 3.6nm layer of Silicon and by a 3.6nm of $Si_{0.95}Ge_{0.05}$ with SS=33mV/dec at $V_{DS} = -0.1$V. The structure with a channel composed by a 3.6nm Si layer, a central 2.3nm compressively strained $Si_{0.85}Ge_{0.15}$ layer and a 1.5nm Si cap layer, presents the best I_{on} current found for a p-type Si/SiGe heterostructure TFET, that is $I_{on} \approx 100\mu A/\mu m$ at $V_{DS} = -1.0$ and $V_{GS} = -2.5$V. These results suggest that with a careful optimization of strain on the TFET structure it is possible to obtain high drain currents even working with materials like Si and $Si_{0.85}Ge_{0.15}$ that have wider band gap with respect to III-V materials.

Another interesting result has been recently presented by Knoll et al. [18] in 2013. They report a tensile strained Si Nanowire Homo-junction TFET, where the dopant segregation technique already used in [12] and [17] is exploited to obtain very high dopant density with shallow profiles. The gate stack is composed by a 3nm HfO_2 layer. The electrostatic control of the fabricated devices allows for a SS lower than 60mV/dec and at $|V_{DS}| = 0.5$V and $|V_{GS}| = 1.5$V both the n-type configuration and the p-type configuration presents a I_{on} current higher than $1\mu A/\mu m$. An inverter circuit is also implemented with the presented device and the characteristic presents a voltage gain $A_V \approx 13$ at $V_{DD} = 0.4$V.

Tab. 2.1 and fig. 2.11 summarize I_{on}, I_{off} and SS performances and the trans-characteristics, respectively, to permit an easy comparison of the main results of the Si, SiGe and Ge TFETs reported in literature and that have been shortly reviewed in this section.

2.3.2 Experimental results for III-V compound semiconductor TFETs

III-V compounds as InAs or InGaAs are characterized by a reduced band gap that for InAs or InSb can reach the value of 0.357eV and 0.17eV, respectively. As stated previously the narrower band gap permits higher ON-state current, but using a hetero-junction approach is then mandatory to reduce the ambipolar leakage current. In 2010 Zhao et al. [19] has presented an 3D MESA $In_{0.53}Ga_{0.47}As/In_{0.7}Ga_{0.3}As/In_{0.53}Ga_{0.47}As$ heterostructure. The gate oxide stack is composed by a 5nm layer of HfO_2. The minimum SS reported is equal to 86mV/dec, and at $V_{DS} = 0.45$V and $V_{GS} = 1.0$V the on-state current is $I_{on} \approx 50\mu A/\mu m$. An improved version of this device is presented in [42] comparing different gate stack materials (a HfO_2 and a Al_3O_2/HfO_2) and different EOTs. A better alignment between the $In_{0.53}Ga_{0.47}As/In_{0.7}Ga_{0.3}As/In_{0.53}Ga_{0.47}As$ layers and the doping junction allowed for an 80% improvement of I_{on} current for the device with the HfO_2 gate stack, but on the other hand the lowest SS is found with the Al_3O_2/HfO_2 structure due to the better InGaAs-oxide interface, at the cost of a lower I_{on} current.

To make an analysis of the impact of the hetero-junction on the performance of the III-V compound TFET in 2011 Mohata et al. [43, 20] have compared various 3D MESA TFET structures. The homo-junctions are implemented in $In_{0.53}Ga_{0.47}As$ or $In_{0.7}Ga_{0.3}As$. The hetero-junctions are implemented in two fashions: the first with a $GaAs_{0.5}Sb_{0.5}$ source and with $In_{0.53}Ga_{0.47}As$ in the channel, the second with a $GaAs_{0.35}Sb_{0.65}$ source and $In_{0.7}Ga_{0.3}As$ in the rest of the channel. The gate oxide stack for all the structures is composed by Al_3O_2/HfO_2 with an EOT of 1.5nm. The hetero-junctions present highly staggered band misalignment. The best

Table 2.1: Summary of the most significant experimental results presented in the literature regarding TFET devices implemented in Si, $Si_{1-x}Ge_x$ and Germanium as both homo-junction and hetero-junction device. $V_{GS,off}$ is the V_{GS} at which $I_D = I_{off}$.

Authors and Reference	V_{DS}	$V_{GS} - V_{GS,off}$	I_{on} [μA/μm]	I_{off} [pA/μm]	min SS [mV/dec]
Planar Semiconductor on Insulator Structures					
	n-type TFETs				
Choi et al. [7]	1.0V	1.0V	12.1	1000	52.1 @V_{DS}=0.1V
Kazazis et al. [8]	0.5	1.0	1.73	16000	495 @V_{DS}=10mV
Krishnamohan et al. [9]	1.0V	1.0V	1	0.5	50 @V_{DS}=0.5V
Kim et al. [10]	0.5V	0.5V	0.42	0.1	40 @V_{DS}=0.5V
Wan et al. [11, 26]	1.0V	1.0V	$7.3 \cdot 10^{-4}$	1	350 @V_{DS}=-1.0V
	p-type TFETs				
Mayer et al. [25]	-1.0V	-1.0V	0.16	1	42 @V_{DS}=-0.1V
Jeon et al. [12]	-1.0V	-1.0V	0.3	0.1	46 @V_{DS}=-1.0V
Zhao et al. [13]	0.8V	0.8V	0.38	82	80 @V_{DS}=-0.4
Wan et al. [11, 26]	-1.0V	-1.0V	0.00184	1	350 @V_{DS}=-1.0V
FINFET and Nanowire Structures					
	p-type TFETs				
Leonelli et al. [15]	-1.2V	-1.2V	0.5	5	46 @V_{DS}=-0.1V
Richter et al. [17]	-0.9V	-2V	0.4	1	76 @V_{DS}=-0.3
Villalon et al. [14]	-1.0V	-2.5V	100	1000	33 @V_{DS}=-0.1
Knoll et al. [18]	-0.5V	-1.5V	10	1	90 @V_{DS}=-0.1

on-state current is found for the $GaAs_{0.35}Sb_{0.65}$ hetero-junction structure with $I_{on} \approx 190\mu A/\mu m$ at $V_{DS} = 0.5V$ and $V_{GS} = 2.5V$ that is more than three times higher than the current found for the $In_{0.7}Ga_{0.3}As$ homo-junction but at the cost of a low $I_{on}/I_{off} < 100$, on the contrary the $In_{0.7}Ga_{0.3}As$ at $V_{DS} = 0.5V$ has a $I_{on}/I_{off} \approx 5 \cdot 10^4$.

In 2011 Dewey et al. [21] have also presented a 3D MESA TFET implemented as homo-junction and hetero-junction. The homo-junction is implemented in $In_{0.53}Ga_{0.47}As$ while the hetero-junction has the source and the channel in $In_{0.53}Ga_{0.47}As$, interleaved by a low band gap $In_{0.7}Ga_{0.3}As$ region. The gate oxide is composed by $TaSiO_x$ with an EOT that ranges from 2.4nm to 1.1nm. Also the source dopant density has been changed to compare different source doping levels. The best results in terms of current and SS have been found with the hetero-junction structure featuring EOT = 1.1nm: $I_{on} \approx 5\mu A/\mu m$ (at $V_{DS} = 0.3V$ and $V_{GS} = 0.8V$) and $I_{off} \approx 100pA/\mu m$ at $V_{GS} = 0V$. The trans-characteristic at $V_{DS} = 0.05V$ presents a SS $\approx$ 57mV/dec.

In 2010 Bjork et al. [44] proposed a nanowire hetero-junction Si-InAs Esaki Tunnel Diode. The donor doped InAs nanowire is selectively grown over an acceptor doped Si substrate with (111) orientation. With a reverse bias of $V_D = 0.5V$ the obtained tunneling current is $50kA/cm^2$. The lattice mismatch between Si and InAs induces a large number of dislocations and defects in the crystal. Bessire et al. [45] have analyzed the effect of defects on the characteristics of the tunnel-diode and demonstrated the presence of trap-assisted tunneling that induces a strong excess current in forward biasing.

In 2011 Schmid et al. and Moselund et al. [46, 24] have presented the results for a vertical hetero-junction Si-InAs nanowire TFET. Over the p+ doped silicon substrate with (111) orientation a first Silicon nanowire is epitaxially grown. The first section is p+ doped (drain) the second undoped (channel), on which a second n doped InAs nanowire is selectively grown (source). The Al_3O_2/TiN gate stack is deposited around the source and the drain. The source is contacted through silicidation of the upper part of the nanowire. Measurements show that there is a strong dependence of the trans-characteristics on temperature, indicating a strong component of trap assisted tunneling. The I_{on}/I_{off} is approximately 10^6 and $I_{on} \approx 2.4\mu A/\mu m$ at

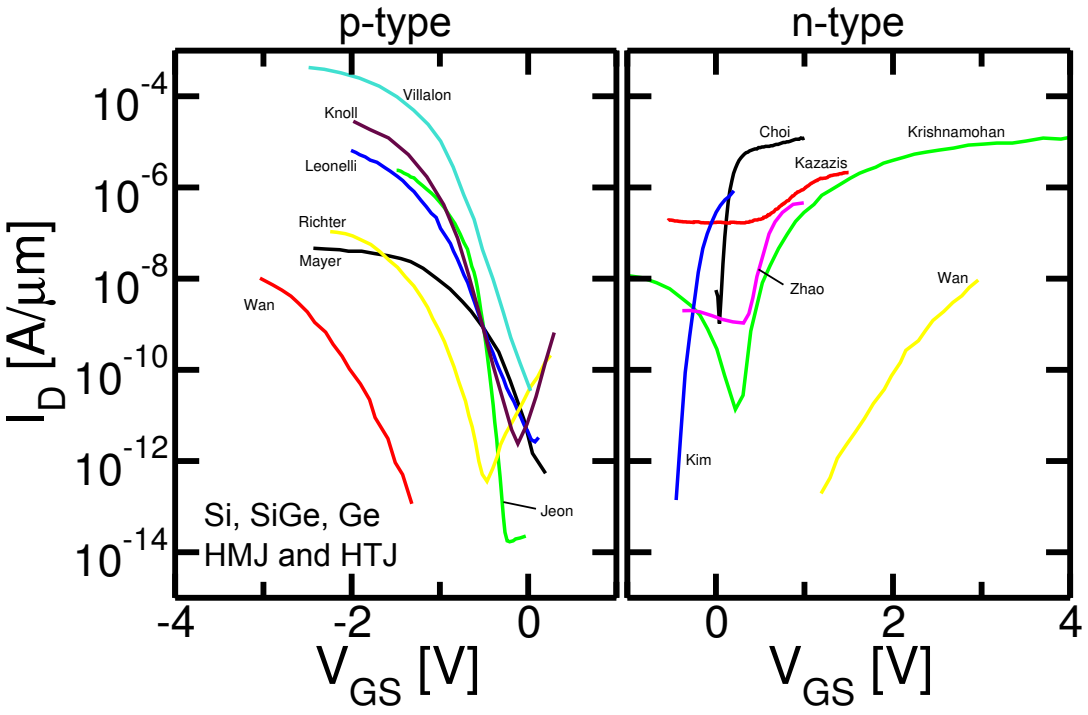

Figure 2.11: Trans-characteristic of the most significant experimental homo- and hetero-junction TFETs implemented in Si, SiGe or Ge. The references as well as the biasing potentials corresponding to the names in plot are reported in tab. 2.1.

V_{GS}=V_{DS}=-1V. The SS averaged over three order of magnitude is 150mV/dec. A similar device concept was presented also by Tomioka et al. [22] in 2011 with a nanowire diameter of 90nm. The gate dielectric is $Hf_{0.8}Al_{0.2}O_x$ with T_{ox}=20nm (EOT≈3.7nm). At $V_{DS} = V_{GS} = 0.5$V the achieved $I_{on} = 0.1\mu A/\mu m$ while at $V_{GS} = 0$V the I_{off} current is in the order of $10pA/\mu m$, with $I_{on}/I_{off} \approx 10^4$. At a lower V_{DS}=0.1V the minimal SS reported is equal to 116mV/dec. This device structure has been optimized and new results have been presented by Tomioka in 2012 [23]. With the reduction of the nanowire diameter reduction to 30nm and an optimization of the doping they have achieved an $I_{on} = 1\mu A/\mu m$ at $V_{GS} = 0.5$V and $V_{DS} = 1$V, an $I_{off} = 1pA/\mu m$ at $V_{GS} = -0.5$V and a minimum SS = 21mV/dec at $V_{DS} = 1.0$V.

2.4 Summary

In this chapter an introduction to the architecture and to the operation of the Tunnel FET has been proposed. The main physical mechanisms affecting the performance of the device have been presented, together with an ample overview of the experimental results regarding TFETs in the scientific literature. The results reported in the literature point out how difficult it is to realize TFETs able to achieve a on-state current with a high I_{on}/I_{off} ratio at low power supply voltages V_{DD}. To achieve such a result a significant optimization effort is required, that demands careful modeling work and state-of-the-art simulation tools. By simulation one can explore the design parameter space in the attempt to find the optimum configuration. This work is demands availability of an accurate modeling of the main injection mechanism taking place in the TFET, namely Band to Band Tunneling. In the next chapter a review of the models for both phonon assisted and direct Band to Band Tunneling is presented.

Table 2.2: Summary of the most significant experimental results presented in the literature regarding TFET devices implemented in III-V compounds both as homo-junction or hetero-junction device. $V_{GS,off}$ is the V_{GS} at which $I_D = I_{off}$.

Authors and Reference	V_{DS}	$V_{GS} - V_{GS,off}$	I_{on} [μA/μm]	I_{off} [pA/μm]	min SS [mV/dec]
3D MESA Structure					
	n-type TFETs				
Zhao et al. [19, 42]	1.05V	1.05V	30	0.1	80 @V_{DS}=50mV
Mohata et al. [43, 20]	0.5V	1.5V	135	5000	160 @V_{DS}=0.3V
Dewey et al. [21]	0.3V	0.8V	5	100	57 @V_{DS}=50mV
InAs/Si Hetero-structure Nanowire					
	n-type TFETs				
Tomioka et al. [22, 23]	1.0V	1.0V	1	1	21 @ V_{DS}=1.0V
	p-type TFETs				
Moselund et al. [24]	-0.5V	-1.5V	0.4	3	275 @ V_{DS}=-0.5V

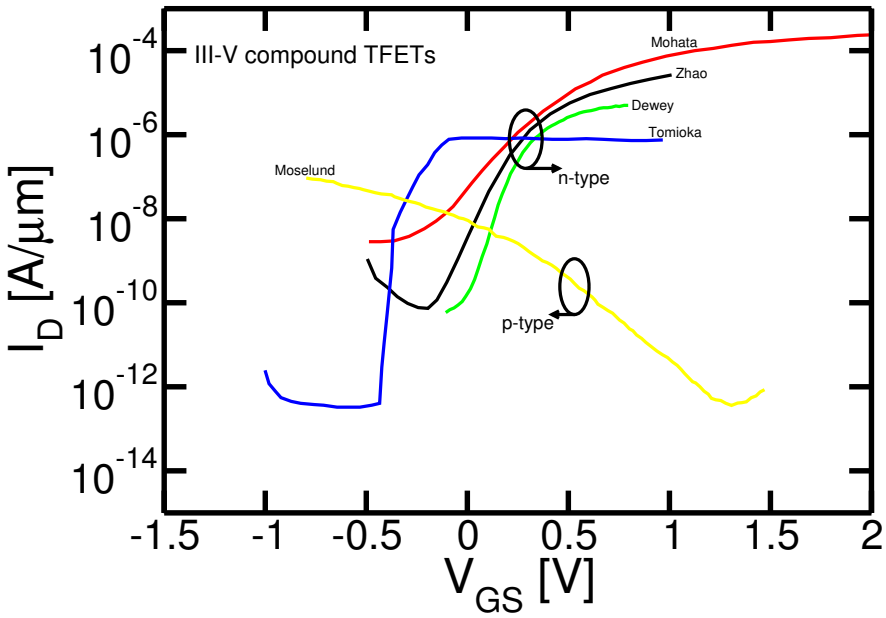

Figure 2.12: Trans-characteristic of the most significant experimental homo- and hetero-junction TFETs implemented in III-V compound materials. The references as well as the biasing potentials corresponding to the names in the figure are reported in tab. 2.2.

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Chapter 3

Band to band tunneling models

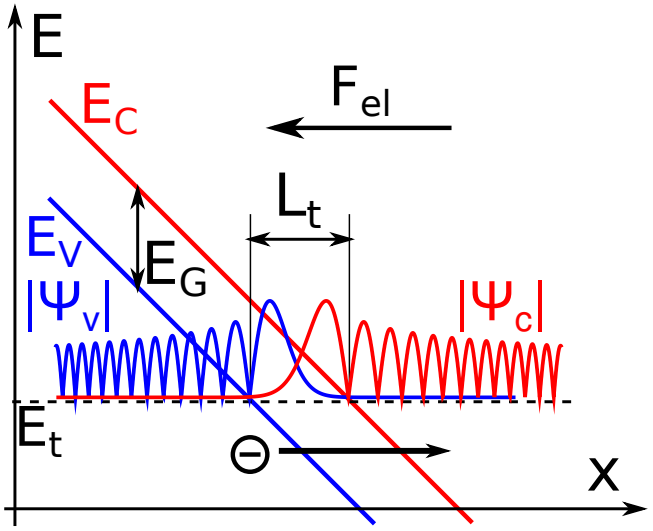

Figure 3.1: Schematic representation of the conduction and the valence band (E_C and E_V respectively) and of the wave-function of an electron in the conduction band Ψ_C and in the valence band Ψ_V in presence of a constant field $\mathbf{F}_\mathrm{el}$.

3.1 Band to Band Tunneling Transitions

Band to Band Tunneling is a physical mechanism that allows an electron in the valence band to reach the conduction band through the imaginary branch of the dispersion relation. Fig. 3.1 sketches the conduction and valence band profiles ($E_\mathrm{C}(x)$ and $E_\mathrm{V}(x)$ respectively) in the presence of a constant field $\mathbf{F}_\mathrm{el}$. The electron in the valence band is characterized by the wave-function Ψ_V and has an energy E_t that is constant along the tunneling path and it is referred as the "tunneling energy". The probability density for the electron to be found in an incremental segment dx at a coordinate x is given by $|\Psi_\mathrm{V}(x)|^2$. For the x values where $E_\mathrm{t} < E_\mathrm{V}(x)$ the electron lies in a real branch of the dispersion relation and we can write Ψ_V as an infinite series of plane waves with real wave-number. On the other hand where $E_\mathrm{t} > E_\mathrm{V}(x)$ the wave-number becomes imaginary, implying that the wave-function Ψ_V can be expressed as a sum of evanescent waves that exponentially decay along x. For the wave-function $\Psi_\mathrm{C}(x)$ of an electron in the conduction band the opposite holds: for the x where $E_\mathrm{t} > E_\mathrm{C}(x)$ the electron can be considered in the real branch of the dispersion relation and for $E_\mathrm{t} < E_\mathrm{C}(x)$ in the imaginary one. Inside the band gap the wave-function Ψ_V decreases exponentially along the positive x direction and Ψ_C along the negative x direction. Two different wave-functions represent two different states of the electrons the system [1, 2] and, if a non null overlap exists, between the conduction and valence band wave-functions then the transition between the state in the valence band and the state in the conduction band becomes possible. The difficult task then becomes the accurate computation of the transition probability.

3.2 Band Structure of indirect and direct band gap material

In the following the fundamental concepts of semiconductor physics like the Brillouin Zone of the Band Structure are assumed to be known. An extensive presentation of these concept can be found in many textbooks such as, for instance, [3, 4]. For the sake of a self contained treatment only the most relevant concepts will be refreshed in the following.

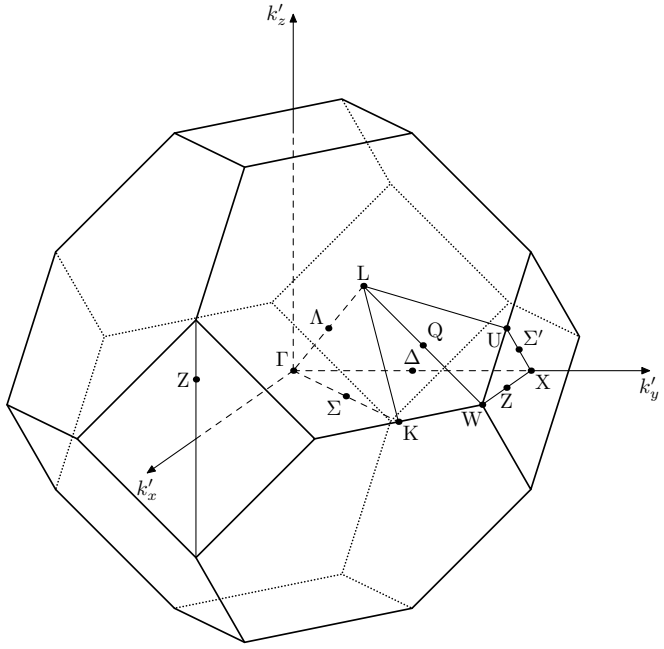

Figure 3.2: Representation of the Brillouin Zone for a Face Centered Cubic lattice (Diamond, Zincblende) with indication of the most significant points (Γ, X, L, etc.) and of the irreducible wedge.

Fig. 3.2 reports the Brillouin zone for a Face Centered Cubic lattice as that of Si, Ge, and GaAs. The most important points in the Brillouin zone are the Γ, the L and the X points and tab. 3.1 reports their coordinates in the reciprocal space. The symmetry of the crystal is reflected in the symmetry of the Band Structure $E(\mathbf{k})$ in the Brillouin Zone with the consequence that for Silicon and Germanium it is sufficient to know the $E(\mathbf{k})$ in a reduced part of the BZ that is denoted as the "irreducible wedge" and, in the rest of the BZ, the band structure can be derived by means of symmetry considerations.

Semiconductor materials can be divided in two groups: those with a direct band gap and the ones with an indirect band gap. In the former materials the minima of the conduction band come at the same $\mathbf{k}$ value as the maxima of the valence band. This condition is not satisfied in indirect band gap semiconductors. Fig. 3.3 reports a qualitative one dimensional representation of the band structure of an indirect band gap semiconductor (plot a) and of a direct band gap one (plot b). The materials of the IV group of the periodic table (like Silicon and Germanium) are characterized by a band structure with the minimum of the valence band that is two fold degenerate (light hole valley and heavy hole valley) and that is found at the Γ point.

The conduction band minimum for Silicon is six-fold degenerate and it is found in the six Δ points of the Brillouin zone that correspond to $\mathbf{k}_{\min} = 2\pi/a(\pm 0.85, 0, 0)$, $\mathbf{k}_{\min} = 2\pi/a(0, \pm 0.85, 0)$, $\mathbf{k}_{\min} = 2\pi/a(0, 0, \pm 0.85)$. Germanium has a minimum that is eight fold degenerate and that can be found at the eight L point of the Brillouin Zone. A particle transition from the Γ point in the Brillouin Zone to the Δ point requires the acquisition of a crystal momentum equal to $\hbar|\mathbf{k}_{\min}|$. Given the momentum conservation law it is impossible for a single particle to make the transition, in an indirect band gap material, unless an interaction with another particle occurs with an exchange of momentum. The typical tunneling mechanism that takes place in an indirect band gap semiconductor is the so called "phonon-assisted" BtBT where the electron interacts with a phonon with an exchange of momentum and a slight change in energy, that allows the particle to move from the valence to the conduction band.

Table 3.1: Coordinates in the reciprocal space of the most significant point of the Brillouin Zone. a is lattice constant. The axis are represented as directions in the Miller notation [3]

Point	Coordinates	Degeneracy	Axis
Γ	(0,0,0)	1	
L	$2\pi/a(\pm 0.5, \pm 0.5, \pm 0.5)$	8	$\Lambda < 1,1,1 >$
X	$2\pi/a(\pm 1, 0, 0)$ $2\pi/a(0, \pm 1, 0)$ $2\pi/a(0, 0, \pm 1)$	6	$\Delta < 1,0,0 >$
K	$2\pi/a(\pm 0.75, \pm 0.75, 0)$ $2\pi/a(\pm 0.75, 0, \pm 0.75)$ $2\pi/a(0, \pm 0.75, \pm 0.75)$	12	Σ $(\pm 1, \pm 1, 0)$

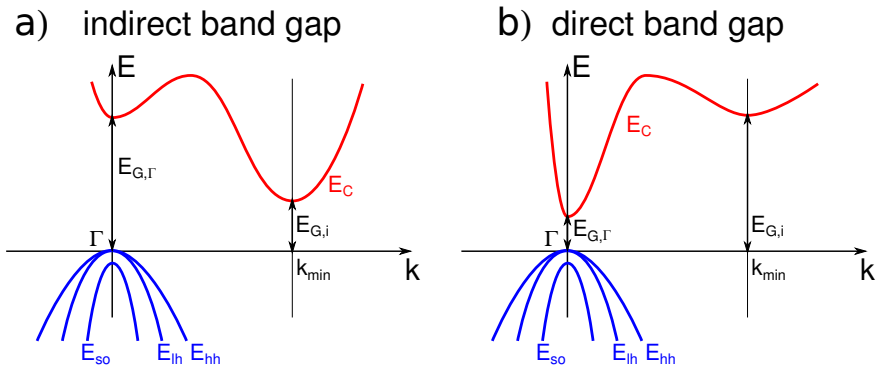

Figure 3.3: Schematic one dimension representation of the band structure of a indirect band gap material (plot a) and of a direct band gap material (plot b).

On the other hand, the III-V compounds (as InAs, InGaAs, GaAs, etc.) are characterized by a zincblende crystal that also has a Face Centered Cubic lattice, and for these materials the maximum of the valence band and the minimum of the conduction band are both found at the Γ point. This implies that a transition from the valence to the conduction band does not require the exchange of crystal momentum.

Different BtBT mechanisms require different models to compute the transition probability; the models have parameters to calibrate that depend on the characteristics of the semiconductor. In the next sections an overview of the semi-classical BtBT models for direct and phonon-assisted BtBT will be provided. The model calibration will be discussed in sect. 3.7.

The first attempt to evaluate the tunneling current was carried out by Zener in 1934 [5] to explain the breakdown of dielectric materials. He derived a first expression for the BtBT generation rate G_{bbt} in presence of a constant field $\mathbf{F}_{\mathrm{el}}$:

$$G_{\mathrm{bbt}} = \frac{q|\mathbf{F}_{\mathrm{el}}|a}{2\pi\hbar} \exp\left(-\frac{maE_{\mathrm{G}}}{|q\mathbf{F}_{\mathrm{el}}|}\right) \tag{3.1}$$

where a is the lattice constant of the considered material, E_{G} is the band gap, m is the rest mass of the electron and q is the elementary charge. Zener's work was refined by McAfee et al. in 1951 [6], who described the breakdown current in Germanium p-n diodes using an improved version of the Zener theory adapted to materials with a larger band gap. One year later a few other works demonstrated that in diodes with wide junctions, impact ionization is the cause of the breakdown behavior [7, 8].

The first analytical model for calculating the transition probability for the phonon assisted Band to Band Tunneling has been proposed by Keldysh in 1958 [9] using a second order perturbation theory and independently by Price et al. who derived a phonon assisted tunneling model via the WKB approach [10].

3.3 Local-direct BtBT Model

In 1961 Kane has derived an analytical model for the computation of the direct and phonon assisted generation rate G_{bbt} [11] considering a constant field $\mathbf{F}_{\mathrm{el}}$. Kane's BtBT model is based on the so called Kane dispersion relations for valence and conduction band:

$$E_{\mathrm{V}}(\mathbf{k_t}) = \frac{E_{\mathrm{G}}}{2} + \frac{\hbar^2|\mathbf{k_t}|^2}{2m_0} - \sqrt{E_{\mathrm{G}}^2 + \frac{E_{\mathrm{G}}\hbar^2|\mathbf{k_t}|^2}{m_r}} \tag{3.2}$$

$$E_{\mathrm{C}}(\mathbf{k_t}) = \frac{E_{\mathrm{G}}}{2} + \frac{\hbar^2|\mathbf{k_t}|^2}{2m_0} + \sqrt{E_{\mathrm{G}}^2 + \frac{E_{\mathrm{G}}\hbar^2|\mathbf{k_t}|^2}{m_r}} \tag{3.3}$$

where $\mathbf{k_t} = (k_x, k_y, k_z)$ is the total wave-vector with components that can either be real or imaginary and m_r is the reduced mass. Considering $|\mathbf{k_t}|$ to be real and small, the Kane dispersion relation for the valence and the conduction band can be approximated as:

$$E_{\mathrm{V}} = -\frac{\hbar^2|\mathbf{k_t}|^2}{2}\left(\frac{1}{2m_r} - \frac{1}{m_0}\right) \tag{3.4}$$

$$E_{\mathrm{C}} = E_{\mathrm{G}} + \frac{\hbar^2|\mathbf{k_t}|^2}{2}\left(\frac{1}{2m_r} + \frac{1}{m_0}\right) \tag{3.5}$$

Under the Effective Mass Approximation (EMA) the effective mass of electrons and holes can be linked to the reduced mass:

$$\frac{1}{m_c} = \frac{1}{2m_r} + \frac{1}{m_0} \tag{3.6}$$

$$\frac{1}{m_v} = \frac{1}{2m_r} - \frac{1}{m_0} \tag{3.7}$$

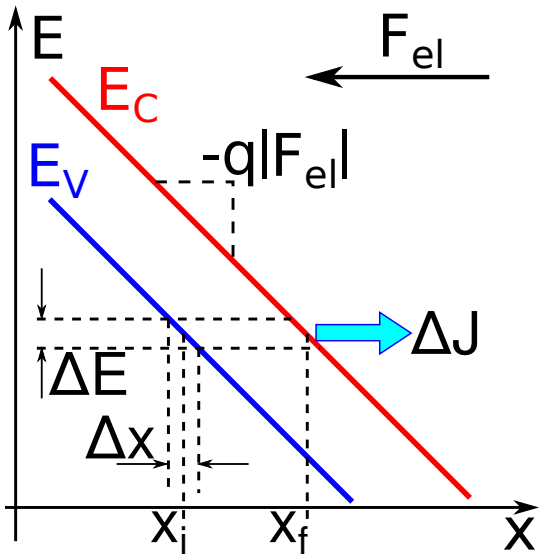

Figure 3.4: Schematic representation of BtBT in the presence of constant electric field $\mathbf{F}_{\text{el}}$. A single energy bin ΔE is plotted, which contributes a tunneling current ΔJ. Δx is the length necessary for the band to change by $-\Delta E$. x_i and x_f are the beginning and ending point of the tunneling path.

and therefore:

$$\frac{1}{m_r} = \frac{1}{m_c} + \frac{1}{m_v} \tag{3.8}$$

Kane calculates that the BtBT transition probability T can be expressed as [11]:

$$T = \frac{\pi^2}{9} \exp\left(-2 \int_{x_i}^{x_f} \Im(k_x(x)) dx\right) \tag{3.9}$$

where x_i and x_f are the classical turning points at the beginning and at the end of the tunneling path as reported in fig. 3.4. The term k_x can be computed from the Kane dispersion relation considering $|\mathbf{k_t}|^2 = \Re(k_x)^2 + \Im(k_x)^2 + |\mathbf{k}_\perp|^2$, where $\Re(k_x)$ and $\Im(k_x)$ are the real and imaginary part of the wave-vector along the tunneling direction, respectively. $\mathbf{k}_\perp$ is the wave vector transversal to the tunneling direction. The term $\hbar^2|\mathbf{k_t}|^2/2m_0$ is assumed to be negligible with respect to the term under the square root, since in III-V compound semiconductors (InAs, InGaAs, etc.) $m_r \approx m_c \ll m_0$. The conduction and the valence band profiles along the x direction are $E_{\text{C}}(x) = E_{\text{G}} - q|\mathbf{F}_{\text{el}}|x$ and $E_{\text{V}} = -q|\mathbf{F}_{\text{el}}|x$ and under this assumption we can express $\Im(k_x)$ as:

$$\Im(k_x) = \sqrt{\frac{m_r}{E_{\text{G}}\hbar^2}} \sqrt{\tilde{E}_{\text{G}}(\mathbf{k}_\perp)^2 - 4\left(q|\mathbf{F}_{\text{el}}|x - \frac{E_{\text{G}}}{2}\right)^2} \tag{3.10}$$

with $\tilde{E}_{\text{G}}(\mathbf{k}_\perp) = \sqrt{E_{\text{G}} + \frac{E_{\text{G}}\hbar^2|\mathbf{k}_\perp|^2}{m_r}}$, that can be considered as the effective band gap for the particle that has a kinetic energy in the directions perpendicular to the tunneling. The start and end points of the tunneling path can be computed by imposing $\Im(k_x(x)) = 0$. Under this

assumption we derive:

$$\tilde{E}_{\mathrm{G}}(\mathbf{k}_\perp)^2 = 4\left(q|\mathbf{F}_{\mathrm{el}}|x - \frac{E_{\mathrm{G}}}{2}\right)^2 \tag{3.11}$$

$$\tilde{E}_{\mathrm{G}}(\mathbf{k}_\perp) = \pm 2\left(q|\mathbf{F}_{\mathrm{el}}|x - \frac{E_{\mathrm{G}}}{2}\right) \tag{3.12}$$

$$x_\pm = \frac{1}{q|\mathbf{F}_{\mathrm{el}}|}\left(\frac{E_{\mathrm{G}}}{2} \pm \frac{\tilde{E}_{\mathrm{G}}(\mathbf{k}_\perp)}{2}\right) \tag{3.13}$$

where $x_+ = x_f$ and $x_- = x_i$ (fig. 3.4). To perform the integral in eq. 3.9 we express $\Im(k_x)$ as:

$$\Im(k_x) = \sqrt{\frac{m_r \tilde{E}_{\mathrm{G}}(\mathbf{k}_\perp)^2}{\hbar^2 E_{\mathrm{G}}}}\sqrt{1 - \frac{4}{\tilde{E}_{\mathrm{G}}(\mathbf{k}_\perp)^2}\left(q|\mathbf{F}_{\mathrm{el}}|x - \frac{E_{\mathrm{G}}}{2}\right)^2} \tag{3.14}$$

$$\Im(k_x) = \sqrt{\frac{m_r \tilde{E}_{\mathrm{G}}(\mathbf{k}_\perp)^2}{\hbar^2 E_{\mathrm{G}}}}\sqrt{1 - a^2} \tag{3.15}$$

$$a = \frac{2}{\tilde{E}_{\mathrm{G}}(\mathbf{k}_\perp)}\left(q|\mathbf{F}_{\mathrm{el}}|x - \frac{E_{\mathrm{G}}}{2}\right) \tag{3.16}$$

then we change the integration variable from x to a. We recompute the extremes of integration for a as:

$$a_i = -1 \quad a_f = +1 \tag{3.17}$$

The integral then becomes:

$$\int_{x_i}^{x_f} \Im(k_x(x))dx = \sqrt{\frac{m_r}{E_{\mathrm{G}}\hbar^2}}\frac{\tilde{E}_{\mathrm{G}}(\mathbf{k}_\perp)^2}{2q|\mathbf{F}_{\mathrm{el}}|}\int_{-1}^{+1}\sqrt{1-a^2}da \tag{3.18}$$

$$\int_{x_i}^{x_f} \Im(k_x(x))dx = \sqrt{\frac{m_r}{E_{\mathrm{G}}\hbar^2}}\frac{\tilde{E}_{\mathrm{G}}(\mathbf{k}_\perp)^2}{4q|\mathbf{F}_{\mathrm{el}}|}\left[a\sqrt{1-a^2} + \sin^{-1}(a)\right]\Big|_{-1}^{1} \tag{3.19}$$

$$\int_{x_i}^{x_f} \Im(k_x(x))dx = \frac{\pi\tilde{E}_{\mathrm{G}}(\mathbf{k}_\perp)^2}{4q|\mathbf{F}_{\mathrm{el}}|\hbar}\sqrt{\frac{m_r}{E_{\mathrm{G}}}} \tag{3.20}$$

Replacing $\tilde{E}_{\mathrm{G}}(\mathbf{k}_\perp)$ with its definition it follows that:

$$\int_{x_i}^{x_f} \Im(k_x(x))dx = \frac{\pi}{4q|\mathbf{F}_{\mathrm{el}}|\hbar}\left(E_{\mathrm{G}}^{3/2}\sqrt{m_r} + \sqrt{\frac{E_{\mathrm{G}}}{m_r}}\hbar^2|\mathbf{k}_\perp|^2\right) \tag{3.21}$$

The direct BtBT transition probability of a particle $T(\mathbf{k}_\perp)$ for the particle with transverse wave vector $\mathbf{k}_\perp$ can be written as:

$$T(\mathbf{k}_\perp) = \frac{\pi^2}{9}\exp\left(-\frac{\pi E_{\mathrm{G}}^{3/2}\sqrt{m_r}}{2q|\mathbf{F}_{\mathrm{el}}|\hbar}\right)\exp\left(-\frac{\pi\hbar|\mathbf{k}_\perp|^2\sqrt{E_{\mathrm{G}}}}{2q|\mathbf{F}_{\mathrm{el}}|\sqrt{m_r}}\right) \tag{3.22}$$

At this point the total BtBT generation rate G_{bbt} can be computed using the Landauer formula [12], where dJ/dE is the contribution of the energy interval between E and $E+dE$ on the total current.

$$\frac{dJ}{dE} = \frac{n_{\mathrm{sp}}q}{\pi\hbar A}\sum_{\mathbf{k}_\perp} T(\mathbf{k}_\perp)[f_v(E) - f_c(E)] \tag{3.23}$$

$$\frac{dJ}{dE} = \frac{q\pi}{9\hbar A}\exp\left(-\frac{\pi E_{\mathrm{G}}^{3/2}\sqrt{m_r}}{2q|\mathbf{F}_{\mathrm{el}}|\hbar}\right)\sum_{\mathbf{k}_\perp}\exp\left(-\frac{\pi\hbar|\mathbf{k}_\perp|^2}{2q|\mathbf{F}_{\mathrm{el}}|}\sqrt{\frac{E_{\mathrm{G}}}{m_r}}\right)[f_v(E) - f_c(E)] \tag{3.24}$$

having $n_{\mathrm{sp}} = 2$. Using the charge continuity equation it is possible to compute the G_{bbt} from the dJ/dE term:

$$\nabla \cdot \mathbf{J_n} = q\frac{dn}{dt} = qG_{\mathrm{bbt,e}} \tag{3.25}$$

$$\nabla \cdot \mathbf{J_p} = -q\frac{dp}{dt} = -qG_{\mathrm{bbt,h}} \tag{3.26}$$

expressions that in the unidimensional case become:

$$\frac{dJ_n}{dx} = -qG_{\mathrm{bbt,e}} \tag{3.27}$$

$$\frac{dJ_p}{dx} = qG_{\mathrm{bbt,h}} \tag{3.28}$$

$$\tag{3.29}$$

and that can be arranged as:

$$\frac{dJ_n}{dE}\frac{dE}{dx} = -qG_{\mathrm{bbt,e}} \tag{3.30}$$

$$\frac{dE}{dx} = -q|\mathbf{F}_{\mathrm{el}}| \tag{3.31}$$

where E is the potential energy. In the presence of uniform field has a constant slope equal to $-q|\mathbf{F}_{\mathrm{el}}|$ as reported in fig. 3.4. It follows:

$$G_{\mathrm{bbt,e}} = |\mathbf{F}_{\mathrm{el}}|\frac{dJ_n}{dE} \tag{3.32}$$

$$= \frac{q\pi|\mathbf{F}_{\mathrm{el}}|}{9\hbar A}\exp\left(-\frac{\pi E_{\mathrm{G}}^{3/2}\sqrt{m_r}}{2q|\mathbf{F}_{\mathrm{el}}|\hbar}\right)\sum_{\mathbf{k}_\perp}\exp\left(-\frac{\pi\hbar|\mathbf{k}_\perp|^2}{2q|\mathbf{F}_{\mathrm{el}}|}\sqrt{\frac{E_{\mathrm{G}}}{m_r}}\right)[f_v(E) - f_c(E)] \tag{3.33}$$

In the limit of continuous $\mathbf{k}_\perp$ values the sum over $\mathbf{k}_\perp$ can be computed by a double integral in the Brillouin Zone (BZ) over the surface perpendicular to the tunneling direction, using the following substitution [13]:

$$\frac{1}{A}\sum_{\mathbf{k}_\perp} \longrightarrow \frac{1}{4\pi^2}\int d\mathbf{k}_\perp \tag{3.34}$$

Considering negligible the dependence on the occupation of the valence and conduction bands (i.e. assuming $f_v = 1$ and $f_c = 0$), the electron generation rate $G_{\mathrm{bbt,e}}$ can be written as:

$$G_{\mathrm{bbt,e}} = \frac{q|\mathbf{F}_{\mathrm{el}}|}{36\hbar\pi}\int_0^{+\infty} dE\exp\left(\frac{-\pi E_{\mathrm{G}}^{3/2}\sqrt{m_r}}{2q|\mathbf{F}_{\mathrm{el}}|\hbar}\right)\int d\mathbf{k}_\perp\exp\left(-\frac{\pi\hbar|\mathbf{k}_\perp|^2}{2q|\mathbf{F}_{\mathrm{el}}|}\sqrt{\frac{E_{\mathrm{G}}}{m_r}}\right) \tag{3.35}$$

The integral in $\mathbf{k}_\perp$ can be solved by changing the $\mathbf{k}_\perp$ coordinates from Cartesian to polar $(k_\perp, \theta)$ obtaining:

$$\int_{\mathbb{R}^2} d\mathbf{k}_\perp\exp\left(-\frac{\pi\hbar k_\perp^2}{2q|\mathbf{F}_{\mathrm{el}}|}\sqrt{\frac{E_{\mathrm{G}}}{m_r}}\right) = \int_0^{2\pi} d\theta\int_0^{+\infty} k_\perp\exp\left(-\frac{\pi\hbar k_\perp^2}{2q|\mathbf{F}_{\mathrm{el}}|}\sqrt{\frac{E_{\mathrm{G}}}{m_r}}\right) \tag{3.36}$$

$$= \frac{4q|\mathbf{F}_{\mathrm{el}}|}{\hbar}\sqrt{\frac{m_r}{E_{\mathrm{G}}}} \tag{3.37}$$

Now it is possible to write the generation rate as:

$$G_{\mathrm{bbt,e}} = \frac{q^2\sqrt{m_r}|\mathbf{F}_{\mathrm{el}}|^2}{9\hbar\sqrt{E_{\mathrm{G}}}}\exp\left(\frac{-\pi E_{\mathrm{G}}^{3/2}\sqrt{m_r}}{2q|\mathbf{F}_{\mathrm{el}}|\hbar}\right) \tag{3.38}$$

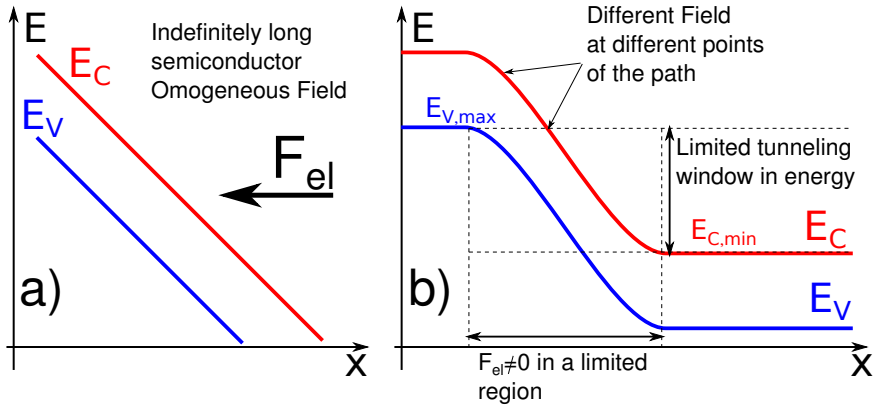

Figure 3.5: Schematic of the band profiles considering the case analyzed by Kane (plot a) and an actual pn junction (plot b).

that can be rewritten as:

$$G_{\mathrm{bbt,e}} = A\left(\frac{|\mathbf{F}_{\mathrm{el}}|}{F_0}\right)^2 \exp\left(-\frac{B}{|\mathbf{F}_{\mathrm{el}}|}\right) \tag{3.39}$$

with A, B are equal to:

$$A = \frac{\pi\sqrt{m_r}(qF_0)^2}{9h^2\sqrt{E_G}} \tag{3.40}$$

$$B = \frac{\pi^2\sqrt{m_r}E_G^{\frac{3}{2}}}{qh} \tag{3.41}$$

where F_0 is a normalization field.

This expression can be used in a transport model, as e.g. the drift-diffusion, coupled with a Poisson solver to simulate the BtBT generation effect on the electrostatics and transport of a device. The Kane tunneling model works only in the case of an indefinitely extended semiconductor with a constant field $\mathbf{F}_{\mathrm{el}}$. This situation is extremely different from what can be found in a real device such as an Esaki diode or a Tunnel FET. Indeed eq. 3.39 embodies a so called Local Model where G_{bbt} at the location (x, y, z) only depends on the field at the same location. Clearly this picture is adequate to describe a real device such a tunnel diode or a TFET only if the device dimensions where the field exists are much longer than the generation region. In reality however, the electric field changes appreciably over the tunneling path. Moreover electrons and holes are generated at different locations, that is at the beginning and end of the tunneling path and not at the same place as suggested by eq. 3.39.

To understand the limitations of using a local model, fig. 3.5 reports the idealized energy band profile used in Kane's model and those found in an actual diode. In the real pn junction the field, $\mathbf{F}_{\mathrm{el}}$, is non zero only in a limited region of the device where it is usually approximated as a constant. The most significant difference is given by the fact that the value of the potential energy is not linear along the tunneling path and k_x and the related integrals must be computed accordingly to the actual value of the potential energy profile along the tunneling path. As shown in [14] this approximation implies a significant overestimation of the BtBT current.

Another limitation of the Kane Model is given by the fact that it does not account for the occupation of the valence and of the conduction band. In an indefinitely extended semiconductor with homogeneous electric field the valence band will always be full and the conduction band always completely empty, with the result that even at equilibrium eq. 3.39 predicts a non null generation rate. Moreover in a real junction the allowed values for $|\mathbf{k}_\perp|$ are limited as will be shown in the derivation of the Non Local Model.

In 1992 Hurkx et al. [15] have proposed a local model similar to the Kane's one that approximates the occupation term $f_v - f_c$ with an expression similar to the one derived for the generation-recombination rate of Schockley Reed Hall trap assisted generation-recombination [3]:

$$G_{\mathrm{bbt}} = A|\mathbf{F}_{\mathrm{el}}|^2 \exp(-B/|\mathbf{F}_{\mathrm{el}}|) \underbrace{\frac{np - n_i^2}{(n+n_i)(p+n_i)}}_{\approx f_v - f_c} \tag{3.42}$$

where n_i is the carrier concentration of the undoped semiconductor. For a non degenerate semiconductor the carrier distribution in energy is approximated by the Maxwell-Boltzmann statistics and at the equilibrium $np = n_i^2$, therefore at the equilibrium the generation rate is equal to zero.

3.4 Non Local Direct BtBT Model

To overcome the limitations of local BtBT models it is necessary to derive an expression for the generation rate that takes into account the dependence of k_x on the whole E_{C} and E_{V} profiles along the tunneling path. This model typology is called "Non Local Direct BtBT model". We derive in the following such a model using the Kane dispersion relation 3.2 as a starting point:

$$E_{\mathrm{V}}(\mathbf{k_t}) = \frac{E_{\mathrm{G}}}{2} + \frac{\hbar^2|\mathbf{k_t}|^2}{2m_0} - \sqrt{E_{\mathrm{G}}^2 + \frac{E_{\mathrm{G}}\hbar^2|\mathbf{k_t}|^2}{m_r}} \tag{3.43}$$

Tedious but straightforward algebra leads to rewrite eq. 3.43 as:

$$k_t(E_{\mathrm{t}}, x) = \frac{1}{\hbar}\sqrt{m_r E_{\mathrm{G}}(1 - \alpha(E_{\mathrm{t}} - E_{\mathrm{V}}(x))^2)} \tag{3.44}$$

$$\alpha(E_{\mathrm{t}} - E_{\mathrm{V}}(x)) = -\frac{m_0}{2m_r} + 2\sqrt{\frac{m_0}{2m_r}\left(\frac{E_{\mathrm{t}} - E_{\mathrm{V}}(x)}{E_{\mathrm{G}}} - \frac{1}{2}\right) + \frac{m_0^2}{16m_r^2} + \frac{1}{4}} \tag{3.45}$$

where E_{t} is the tunneling energy, and x is the coordinate along the tunneling path. As stated above the total wave vector k_t contains both the component along the tunneling direction k_x and the components on the plane perpendicular to the tunneling direction $\mathbf{k}_\perp$. $k_t(x) = |\mathbf{k_t}(x)|$ is the absolute value of the total wave vector along the tunneling path and as seen is eq. 3.44 it depends at each point of the tunneling path on $E_{\mathrm{t}} - E_{\mathrm{V}}(x)$ and on $E_{\mathrm{G}}(x)$ at that location x. This expression is general and permits to consider also different semiconductors along the tunneling path that is a typical situation for hetero-junction tunneling devices. The imaginary part of the wave vector along the tunneling direction is $\Im(k_x(x)) = k_t\sqrt{1 + {\mathbf{k}_\perp}^2(x)/k_t^2(x)}$. The tunneling path should begin at the classical turning points where $\Im(k_x(x)) = 0$ as discussed in previous section (eq. 3.13) and they depend on the value of $\mathbf{k}_\perp$. A larger transverse wave vector $|\mathbf{k}_\perp|$ of the particle makes the tunneling path longer and thus reduces exponentially the tunneling probability. Therefore we can consider only small $\mathbf{k}_\perp$ values to give a significant contribution to tunneling probability and if $k_\perp^2$ is small with respect to the term k_t, we can approximate the square root to the corresponding Taylor series truncated to the first term:

$$\Im(k_x) \approx k_t + \frac{k_\perp^2}{2k_t} \tag{3.46}$$

and this can be used in eq.3.9 for computing the tunneling probability.

$$T(E_{\mathrm{t}}, \mathbf{k}_\perp) = \frac{\pi^2}{9} \exp\left(-2\int_{x_i}^{x_f} k_t(E_{\mathrm{t}}, x)dx\right) \exp\left(-k_\perp^2 \int_{x_i}^{x_f} \frac{dx}{k_t(E_{\mathrm{t}}, x)}\right) \tag{3.47}$$

By using the Landauer formula (eq. 3.23) with the substitution presented in the previous section eq. 3.34 we obtain:

$$\frac{dJ}{dE_\mathrm{t}} = \frac{q}{36\pi\hbar}\exp\left(-2\int_{x_i}^{x_f} k_t(E_\mathrm{t},x)dx\right)\iint d\mathbf{k}_\perp \exp\left(-|\mathbf{k}_\perp|^2\int_{x_i}^{x_f}\frac{dx}{k_t(E_\mathrm{t},x)}\right)d\mathbf{k}_\perp \tag{3.48}$$

Consistently with the assumption that significant contributions to the integral are obtained for small $|\mathbf{k}_\perp|$, we consider the x_i and the x_f coordinates to be negligibly affected by the value of $|\mathbf{k}_\perp|$ and we set $E_\mathrm{V}(x_i) = E_\mathrm{C}(x_f) = E_\mathrm{t}$. The integral in $\mathbf{k}_\perp$ is expressed in polar coordinates $(k_\perp, \theta)$ as:

$$\int_{\mathbb{R}^2}\exp\left(-|\mathbf{k}_\perp|^2\int_{x_i}^{x_f}\frac{dx}{k_t(E_\mathrm{t},x)}\right)d\mathbf{k}_\perp = \int_0^{2\pi}d\theta\int_0^{k_\mathrm{max}} dk_\perp k_\perp \exp\left(-k_\perp^2\int_{x_i}^{x_f}\frac{dx}{k_t(E_\mathrm{t},x)}\right) \tag{3.49}$$

where k_max is the maximum absolute value of the transverse wave vector that allows the transition to take place. The BtBT transition is elastic. Therefore the sum of the kinetic and the potential energies is constant along the tunneling path as well as the energy traversal to the tunneling direction. Therefore for the turning points, x_i and x_f, where $\Im[k_x] = 0$, we can write:

$$-\frac{\hbar^2 k_\perp^2}{2m_v} + E_\mathrm{V}(x_i) = E_\mathrm{t} \tag{3.50}$$

$$\frac{\hbar^2 k_\perp^2}{2m_c} + E_\mathrm{C}(x_f) = E_\mathrm{t} \tag{3.51}$$

from which we derive

$$E_\mathrm{V}(x_i) = E_\mathrm{t} + \frac{\hbar^2 k_\perp^2}{2m_v} \tag{3.52}$$

$$E_\mathrm{C}(x_f) = E_\mathrm{t} - \frac{\hbar^2 k_\perp^2}{2m_c} \tag{3.53}$$

Given the valence and conduction band profiles in fig. 3.5-b, the energy window for tunneling is comprised between the minimum conduction band value $E_\mathrm{C,min}$ and the maximum valence band value $E_\mathrm{V,max}$. Therefore we must have $E_\mathrm{V}(x_i) \leq E_\mathrm{V,max}$ and $E_\mathrm{C}(x_f) \geq E_\mathrm{C,min}$. Both conditions can be fulfilled only if $\mathbf{k}_\perp \leq k_\mathrm{max}$ with k_max derived as:

$$k_\mathrm{max} = \min\left(\sqrt{\frac{2m_v}{\hbar^2}(E_\mathrm{V}-E_\mathrm{t})}, \sqrt{\frac{2m_c}{\hbar^2}(E_\mathrm{t}-E_\mathrm{C})}\right) \tag{3.54}$$

It is therefore possible perform analytically the integral in $d\mathbf{k}_\perp$ as:

$$\int\exp\left(-|\mathbf{k}_\perp|^2\int_{x_i}^{x_f}\frac{dx}{k_t(E_\mathrm{t},x)}\right)d\mathbf{k}_\perp = \frac{\pi}{\int_{x_i}^{x_f}k_t^{-1}(x)dx}\left[1-\exp\left(-{k_\mathrm{max}}^2\int_{x_i}^{x_f}\frac{dx}{k_t(E_\mathrm{t},x)}\right)\right] \tag{3.55}$$

and the quantum conductance dJ/dE_t can be written as:

$$\frac{dJ}{dE_\mathrm{t}} = \frac{q}{36\hbar}\frac{1}{\int_{x_i}^{x_f}k_t^{-1}(x)dx}\exp\left(-2\int_{x_i}^{x_f}k_t(E_\mathrm{t},x)dx\right)\left[1-\exp\left(-{k_\mathrm{max}}^2\int_{x_i}^{x_f}\frac{dx}{k_t(E_\mathrm{t},x)}\right)\right] \tag{3.56}$$

The continuity equation for the holes in a solution domain where the electric field is variable, can be stated, for each point x, as

$$\frac{dJ}{dE_\mathrm{t}}\frac{dE_\mathrm{t}}{dx} = \frac{dJ}{dE_\mathrm{V}}\frac{dE_\mathrm{V}}{dx} = qG_\mathrm{bbt,h}(x) \tag{3.57}$$

But as said above $E_\mathrm{t} = E_\mathrm{V}(x)$ where x is the starting point of the tunneling path. The term $dE_\mathrm{t}/dx = q|\mathbf{F}_\mathrm{el}(x)|$ where $|\mathbf{F}_\mathrm{el}(x_i)|$ is the electric field at the starting point of the tunneling path. Finally, the generation rate of holes at the point starting point of the tunneling path x_i can be computed as:

$$G_\mathrm{bbt,h}(x_i) = \frac{q|\mathbf{F}_\mathrm{el}(x_i)|}{36\hbar} \frac{1}{\int_{x_i}^{x_f} k_t^{-1}(x)dx} \times \\ \times \exp\left(-2\int_{x_i}^{x_f} k_t(E_\mathrm{t}, x)dx\right)\left[1 - \exp\left(-{k_\mathrm{max}}^2 \int_{x_i}^{x_f} \frac{dx}{k_t(E_\mathrm{t}, x)}\right)\right] \times \\ \times [f_v(E_\mathrm{V}(x_i)) - f_c(E_\mathrm{C}(x_f))] \quad (3.58)$$

For each hole generated by BtBT at the starting point x_i of the tunneling path corresponds an electron at the ending point x_f, and therefore the $G_\mathrm{bbt,e}(x_f) = G_\mathrm{bbt,h}(x_i)$. This is the expression implemented in SDevice (eq. 375, 376 in [16]).

3.5 Tunneling Path in 2D and 3D domains

The derivation proposed above for the Non Local Direct BtBT model is valid considering a 1D domain where there are only one starting and one ending point and the tunneling path is unique. The model can be generalized to a two-dimensional or three-dimensional domain as follows. Considering a tunneling energy E_t in a two-dimensional or three-dimensional domain there is a whole locus of points where $E_\mathrm{V} = E_\mathrm{t}$ and another one where $E_\mathrm{C} = E_\mathrm{t}$ (curves in a two-dimensional domain, surfaces in a three-dimensional one), and this means that for each point where $E_\mathrm{V}(x_i) = E_\mathrm{t}$, an infinite number of tunneling paths exist with ending point x_f such that $E_\mathrm{C}(x_f) = E_\mathrm{t}$. A rule should thus be defined to select the most relevant tunneling path. In 2012 De Michielis et al. [14] have analyzed the different impact of three approaches for the determination of the tunneling direction:

- *Horizontal Tunneling*: The tunneling direction is parallel to the transport direction
- *Along* $-\nabla E_\mathrm{V}$: The tunneling direction is given by the opposite of the gradient of the valence band profile at the starting point of the path. The tunneling path is a piecewise linear curve that is specularly reflected if it crosses a semiconductor/oxide interface.
- *Minimum Tunneling Path*: The tunneling direction is the one with the minimum tunneling distance.

The simulations in [14] showed that for a planar Silicon Double Gate TFET with film thickness T_Si the horizontal tunneling path predicts a much lower generation rate than the other two criteria discussed above. The minimum length tunneling path rule clearly gives a slightly higher generation rate than the one obtained by the direction of the electric field. Only a full quantum simulation can assess which of the following is the most accurate in a given field profile.

All the results presented in the following of this thesis work, if not otherwise specified, will be obtained using the second rule, that is also the one used in the Synopsys TCAD software SDevice [16] and that is sketched in fig. 3.6.

The generation rate for the electrons in a 2D or 3D simulation domain cannot be determined as $G_\mathrm{bbt,e}(\mathbf{x_f}) = G_\mathrm{bbt,h}(\mathbf{x_i})$ as in a 1D simulation domain. In fact tunneling paths that start from different points $\mathbf{x_i}$ can converge to the same $\mathbf{x_f}$. If Ω is the simulation domain we define $\mathbf{f}_\mathrm{path} : \Omega \to \Omega$, as the surjective function that links the ending point of the unique tunneling paths that start at the point $\mathbf{x_i}$ to its ending point $\mathbf{x_f}$. The generation rate for the electrons in a particular point $\mathbf{x}$ can be expressed as the integral of all the tunneling contributions related to the tunneling paths that converge to the point $\mathbf{x}$:

$$G_\mathrm{bbt,e}(\mathbf{x}) = \int_\Omega d\mathbf{x_i} G_\mathrm{bbt,h}(\mathbf{x_i}) \delta(\mathbf{f}_\mathrm{path}(\mathbf{x_i}) - \mathbf{x}) \quad (3.59)$$

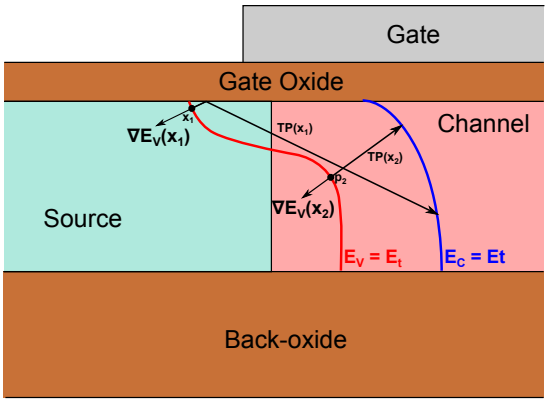

Figure 3.6: Sketch of the tunneling path as a straight line in the direction opposite to the gradient of the valence band which ends when reaching a conduction band energy equal to the valence band energy (E_t) at the starting point and specularly reflected when hitting a semiconductor/dielectric interface.

where $\delta(\mathbf{x})$ is the Dirac's delta function.

Another important aspect to consider when simulating planar or nanowire TFET devices is that the non-local model has been derived using the WKB method and the Kane Dispersion Relation whose validity holds only considering a free 3D gas of particles. On the other hand in Ultra Thin Body UTB devices a strong bias- and size-induced quantization is expected to occur. Quantum confinement splits the conduction and valence band energies and effectively broadens the band gap in the sense that the actual distance in energy between the valence subbands and the conduction subbands is wider than the nominal band gap. In the next chapter, a heuristic correction approach that take into account, at least at the first order, the size- and bias-quantization effect will be presented.

3.6 Phonon Assisted BtBT models

A local model for the phonon-assisted BtBT tunneling improving upon the calculations initially presented by Keldysh in 1958 [9], was proposed by Kane in [11]. The model reads:

$$G_{\mathrm{bbt}} = A \left| \frac{\mathbf{F}_{\mathrm{el}}}{F_0} \right|^{2.5} \exp\left(-\frac{B}{|\mathbf{F}_{\mathrm{el}}|} \right) \tag{3.60}$$

with

$$A = \frac{g(m_v m_c)^{1.5}(1+2N_{\mathrm{op}})D_{\mathrm{op}}^2(qF_0)^{2.5}}{2^{5.25}(2\pi\hbar)^{2.5} m_r^{1.25} \rho \varepsilon_{\mathrm{op}} E_{\mathrm{G}}^{1.75}} \tag{3.61}$$

$$B = \frac{2^{3.5}\pi\sqrt{m_r}E_{\mathrm{G}}^{1.5}}{6q\pi\hbar} \tag{3.62}$$

where $\varepsilon_{\mathrm{op}}$ and D_{op} are the phonon energy and the deformation potential. $N_{\mathrm{op}} = [\exp(\frac{\varepsilon_{\mathrm{op}}}{k_{\mathrm{B}}T}) - 1]^{-1}$ is the phonon occupation statistic. ρ is the semiconductor mass density. As already said local models are not accurate enough in modern devices and a non-local formulation of the BtBT rate has to be sought.

In 1994 Tanaka [17] proposed a Non Local Model for the phonon assisted BtBT based on the solution of the Wannier equation [18] which is solved to obtain the unperturbed wave functions for the states in the valence and the conduction band. Inside the band gap the wave

functions are computed using the WKB approximation. The interaction between the bands is then computed according to the non-diagonal elements of the inter-band matrix that are calculated according to [19] for the direct BtBT and to the deformation ion model [20] for the phonon assisted model.

The model was generalized in [21] considering an arbitrary electric field direction. The unperturbed wave-functions are found by solving the Wannier equation in a coordinate system defined to have one of the coordinate axes parallel to the tunneling direction. The tunneling current is therefore expressed considering the effective masses of the conduction and of the valence band as defined in the new coordinate system. The momentum conservation of the phonon wave vector is used to compute the transition probability. It depends on the dispersion relation but not on the electric field orientation. The proposed semi-classical model for phonon assisted BtBT is accurate considering a free 3D carrier gas in a strongly variable potential profile but since it is based on WKB and on the definition of a tunneling path, its applicability to devices subjected to strong bias- and size-induced quantization remains questionable.

In 2011 Vandenberghe et al. [22, 23] have overcome this limitation proposing a full quantum model for the phonon assisted tunneling that is calculated as a phonon scattering between two evanescent states in the gap originating, respectively, from the valence to the conduction bands. The evanescent states can be described by solving the Schrödinger equation in a one-dimensional, two-dimensional or three-dimensional domain with potential energy profiles that impose size- and bias- induced quantization. The transition probability is found to be:

$$T(E_\mathrm{t}) = \Omega |M_{\mathbf{k_0}}|^2 \int_\Omega d\mathbf{r} A_\mathrm{v}(\mathbf{r},\mathbf{r};E_\mathrm{t}) A_\mathrm{c}(\mathbf{r},\mathbf{r};E_\mathrm{t}-\varepsilon_\mathrm{op}) \tag{3.63}$$

where ε_op is the interacting phonon energy, Ω is the total volume (surface) of the three-dimensional (two-dimensional) domain, $M_{\mathbf{k_0}}$ is the phonon interaction matrix that is computed following the deformation potential interaction approach [4]:

$$M_{\mathbf{k_0}} = D_\mathrm{op} |\mathbf{k_0}| \sqrt{\frac{\hbar^2}{2\rho\varepsilon_\mathrm{op}\Omega}} \tag{3.64}$$

and $\mathbf{k_0}$ is the distance in the reciprocal space between the valence and conduction band minima. $A_\mathrm{c}(\mathbf{r},\mathbf{r}';E)$ and $A_\mathrm{c}(\mathbf{r},\mathbf{r}';E)$ are the spectral density functions that are computed as:

$$A_\mathrm{c,v}(\mathbf{r},\mathbf{r}';E) = \sum_\mathbf{k} \delta(E - \mathcal{H}_\mathrm{c,v}(\mathbf{k})). \tag{3.65}$$

They specify the number of particle, in the point $\mathbf{r}$. $\mathcal{H}_\mathrm{c,v}(\mathbf{k})$ is the Hamiltonian for the conduction or the valence band for a particle characterized by a certain kinetic energy specified by the wave vector $\mathbf{k}$. The spectral functions can be rewritten as [1]:

$$A_\mathrm{c,v}(\mathbf{r},\mathbf{r}';E) = \sum_\mathbf{k} \psi^*_\mathrm{c,v}(\mathbf{r}) \mathcal{H}_\mathrm{c,v}(\mathbf{k}) \psi_\mathrm{c,v}(\mathbf{r}') \tag{3.66}$$

As an example in the appendix A we derive the equations for the application of the model in [22] for the simulation of a UTB FD-SOI TFET.

In their work Vandenberghe et al. also derive the Kane/Keldysh model for phonon-assisted tunneling in presence of a constant field and the non-local model for a gas of free electron through the derivation of the spectral function using the WKB approximation of the wave functions in the band gap. The result is a non-local model similar to the one proposed by Tanaka [17, 21] and to one implemented in the commercial TCAD software as Sentaurus SDevice [16]. The Non Local Dynamic Model for the phonon-assisted BtBT implemented in Sentaurus SDevice

Table 3.2: Multiplicity g of the BtBT transitions between valence and conduction band valleys considering [100] as the tunneling direction.

	Δ_{001}	Δ_{010}, Δ_{001}	$L_{\pm1,\pm1,\pm1}$
Γ_{lh}	4	8	8
Γ_{hh}	4	8	8

computes the generation rate using the following expressions:

$$G_{\mathrm{bbt}}(x_i) = |\nabla E_{\mathrm{V}}(x_i)| C_{\mathrm{p}} \exp\left(-2\int_{x_i}^{x_0} k_v dl - 2\int_{x_0}^{x_f} k_c dl\right) \cdot \cdot \left[f_v\left(\frac{E_{\mathrm{V}}(x_i) - E_{\mathrm{F,h}}}{k_{\mathrm{B}}T}\right) - f_c\left(\frac{E_{\mathrm{V}}(x_i) - E_{\mathrm{F,e}}}{k_{\mathrm{B}}T}\right)\right] \quad (3.67)$$

The term C_{p} is the term that takes into account the interaction with the phonon together with the occupation of the valence and of the conduction and of the phonons:

$$C_{\mathrm{p}} = \int_{x_i}^{x_f} \frac{g(1+2N_{\mathrm{op}})D_{\mathrm{op}}^2}{2^6\pi^2\rho\varepsilon_{\mathrm{op}}E_{\mathrm{G}}} \sqrt{\frac{m_c m_v}{2\pi\hbar L\sqrt{2m_r E_{\mathrm{G}}}}} dl \left(\int_{x_i}^{x_0} \frac{dl}{k_v}\right)^{-1} \left(\int_{x_0}^{x_f} \frac{dl}{k_c}\right)^{-1} \cdot \cdot \left[1 - \exp\left(-{k_{\max}}^2 \int_{x_i}^{x_0} \frac{dl}{k_v}\right)\right] \left[1 - \exp\left(-{k_{\max}}^2 \int_{x_0}^{x_f} \frac{dl}{k_c}\right)\right] \quad (3.68)$$

The integrals are performed along the tunneling path defined following the gradient of the potential rule with the specular reflections at the semiconductor/oxide interfaces. L is the length of the tunneling path l_p. For the calculation of the integrals in eqs. 3.67 and 3.68 the Keldysh dispersion relation in the band gap is used:

$$k_c(\mathbf{r}) = \sqrt{\frac{2m_c}{\hbar^2}(E_{\mathrm{t}} - E_{\mathrm{C}}(\mathbf{r}))} \quad \text{with } \mathbf{r} \in l_p \quad (3.69)$$

$$k_v(\mathbf{r}) = \sqrt{\frac{2m_v}{\hbar^2}(E_{\mathrm{V}}(\mathbf{r}) - E_{\mathrm{t}})} \quad \text{with } \mathbf{r} \in l_p \quad (3.70)$$

These relations are simpler than the Kane's dispersion relation 3.2 but in the case of phonon-assisted BtBT it is not necessary to use a dispersion relation that links both the valence and the conduction band in the band gap as in the case of direct BtBT tunneling. Indeed it is the interaction with the phonon that drives the transition and the error introduced by the Keldysh dispersion relation (eqs. 3.69 can be considered as negligible. x_0 is the crossing point where the tunneling path yields $k_v(x_0) = k_c(x_0)$ (see Fig. 3.7).

g is the multiplicity of the BtBT transition. Given a unique potential profile the transitions between different valence band valleys and conduction band valleys can have the same BtBT generation rate only if the band gap, the effective masses along the tunneling direction and the DoS effective mass are the same for the valence band and the conduction band valleys are the same. E.g. the BtBT transition in the [100] direction from the Γ_{lh} light hole valley to the Δ_{010} conduction band valley will have the same transition probability of the one targeting the valley Δ_{001} because both the conduction band valleys have the same effective masses and energy minimum. g is therefore given by multiplying the multiplicity of the valence and conduction valleys and the spin degeneracy factor. Tab. 3.2 reports as an example, the multiplicity of all the possible BtBT transitions if [100] is the tunneling direction. It is important to notice that in spite of the fact that the L valleys are eight fold degenerated their multiplicity is only four because they lie only for a half in the first Brillouin Zone and therefore their contribution to tunneling can only be computed as a half [3].

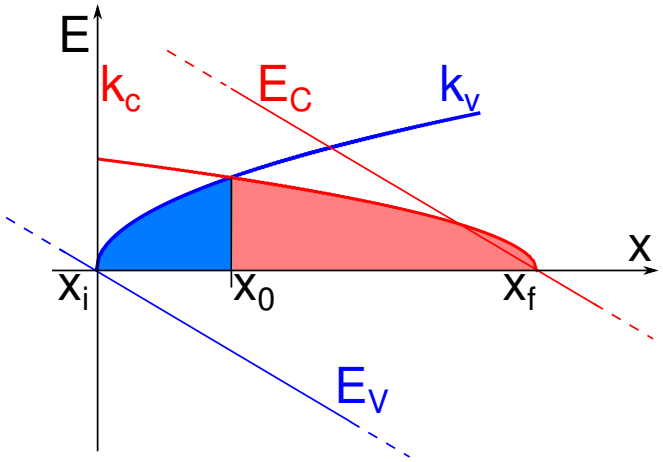

Figure 3.7: Qualitative sketch of the Keldysh dispersion relation inside the band gap for the valence and the conduction band considering a linear potential profile. At x_0 the valence and conduction dispersion relation have the same value. The tunneling path begins at x_i and ends at x_f. The valence dispersion relation k_v (or k_v^{-1}) is integrated from x_i to x_0 (blue area) whereas the conduction dispersion relation k_c (or k_c^{-1}) is integrated from x_0 to x_f (red area).

Table 3.3: Direct band gap E_G^Γ at temperature T=300K and effective masses of the Γ conduction band valley (m_c) and for light and heavy hole valence band valleys ($m_{v,lh}$ and $m_{c,hh}$ respectively) for $In_{0.53}Ga_{0.47}As$, $In_{0.7}Ga_{0.3}As$ and InAs [24, 25, 26].

Compound	E_G^Γ [eV]	m_c [m_0]	$m_{v,lh}$ [m_0]	$m_{v,hh}$ [m_0]
$In_{0.53}Ga_{0.47}As$	0.73	0.043	0.052	0.46
$In_{0.7}Ga_{0.3}As$	0.57	0.043	0.052	0.46
InAs	0.35	0.026	0.026	0.41

3.7 Calibration of the Direct and Phonon Assisted Non Local BtBT Models

The non-local models illustrated in the previous sections contains as parameters the physical properties of the semiconductor materials where the BtBT transition occurs: band gaps, effective masses and phonon properties. For III-V direct compound semiconductor materials the review paper of Vurgaftman [24] contains all the information relative to the conduction band of the most interesting III-V compounds. The information about the valence band effective masses can be found in textbook such as [25] or on the semiconductor parameter web recollections as [26].

Tab. 3.3 reports the parameters of interest for the direct BtBT of $In_{0.53}Ga_{0.47}As$, $In_{0.7}Ga_{0.3}As$ and InAs, that are compounds frequently used in experimental III-V compound TFETs [27, 28].

On the other hand in indirect band gap materials like Silicon and Germanium, both phonon parameters and band structure are required to complete the model and make it usable.

In 2012 Kao et al. [29] presented an in-depth analysis of the simulation of TFET implemented in Silicon, SiGe alloys and Germanium, pointing out that in Germanium both direct as well as the phonon assisted BtBT transitions are present simultaneously and must be considered, whereas in commercial TCAD software (e.g. Synopsys SDevice) only the phonon assisted mechanism is considered for Silicon and Germanium. In their work Kao et al. [29] report all the physical parameters of interest for the direct and phonon assisted models for $Si_{1-x}Ge_x$ alloys with x=0, 0.3, 0.5, 0.8, 1.0 considering the transverse acoustic phonon deformation potentials

and the band structure parameters for the valence and the conduction band valleys.

Regarding the effective masses of the L and the Δ valleys, [29] points out that the effective mass for electrons along the transport direction $m_{c,x}$ must be inserted in eq. 3.69. On the other hand, since the formula for the computation of C_{p} involves, the occupation of the states, in 3.68 the Density of States (DoS) effective mass $m_{c,d} = (m_{c,l}m_{c,t}^2)^{1/3}$ of a ellipsoidal valley with longitudinal and transversal effective mass ($m_{c,l}$ and $m_{c,t}$ respectively) must be used [29].

For a Germanium molar fraction x that goes from 0 to 0.85 the band structure is Si-like and, assuming [100] as the tunneling direction, the dominant BtBT transitions take place between the light hole valley Γ_{lh} and the Δ_{010} and Δ_{001} conduction band valleys that are characterized by the minimum mass along [100].

For x>0.85 the L valleys have the minimum energy lower than the Δ valleys, and all L valleys have the same mass along the transport direction $m_{c,x} = 3m_{c,l}m_{t,l}/(2m_{c,l} + m_{t,l})$ [13, 30] and the same density of state mass $m_{c,d}$.

Considering now the valence band, the light and heavy hole valleys are warped and it is not straightforward to define an effective mass value along the transport direction as for the conduction band valleys. Kao et al. for instance use the 3D Density of States (DoS) mass. The value of the 3D DoS mass can be found in literature [3, 25, 26] or can be extracted by extrapolation of the band structure data using non linear regression on the analytical expression for the DoS that, when non parabolicity of valley is considered, reads:

$$g(E) = \frac{n_{sp}}{2\pi^2}\left(\frac{2m}{\hbar^2}\right)^{3/2}\sqrt{(E_{\mathrm{V},0}-E)(1+\alpha(E_{\mathrm{V},0}-E))}(1+2\alpha(E_{\mathrm{V},0}-E)) \tag{3.71}$$

3.7.1 Non-local phonon-assisted BtBT model parameters for $Si_{1-x}Ge_x$ alloys

Kao et al. provide all the model parameters for the simulation of tunneling devices implemented in unstrained $Si_{1-x}Ge_x$, but the results in [31] show, the implementation of TFETs in unstrained SiGe does not allow for significant current improvements.

Therefore it is of great importance to estimate the current improvements made possible by strain which in turn demands to determine the model parameters for strain materials. In the following the phonon parameters are not supposed to change with the application of strain and the parameters proposed by Kao et al. [29] are used. Strain is known to deform the SiGe alloys band structure, splitting the degeneracy of the Δ and L valleys in conduction band and of the light and heavy hole valleys in the valence band, with the light hole valley that is moved to higher energies. To compute the effect of strain an advanced 30 bands k·p band structure model [32, 33] has been used to extract the parameters of the BtBT process (effective masses, band gap) for the light and heavy holes and for the Γ, Δ and L valleys in the conduction band.

Computation of the electron effective masses

The longitudinal and transverse effective masses of the Γ, Δ and L conduction band valleys were obtained by fitting the analytical non parabolic expression of the dispersion relation

$$E_{\mathrm{C}}(\mathbf{k}) - E_{\mathrm{C},0} = \frac{1}{2\alpha}\left(-1+\sqrt{1+\frac{2\alpha\hbar^2|\mathbf{k}-\mathbf{k}_{\min}|^2}{m}}\right) \tag{3.72}$$

around the minimum $E_{\mathrm{C},0} = E_{\mathrm{C}}(\mathbf{k}_{\min})$ along the longitudinal and transversal directions. Using non linear regression the values of m and α are derived by minimizing the error $|\tilde{E}_{\mathrm{C}}(\mathbf{k}) - E_{\mathrm{C}}(\mathbf{k})|^2$ where $\tilde{E}_{\mathrm{C}}(\mathbf{k})$ is the k·p band structure. This regression procedure, can be easily applied to the calculation of the effective mass along any crystallographic direction, and requires only that the wave-vectors $\mathbf{k} - \mathbf{k}_{\min}$ to parallel to it.

Table 3.4: Comparison between the Phonon Assisted BtBT parameter extrapolated from the 30 bands k·p model [32, 33] results and the parameters reported in [29] for $Si_{1-x}Ge_x$ alloys.

	k· p [32, 33]					ref. [29]				
x	E_G [eV]	$m_{c,x}$ [m_0]	$m_{c,d}$ [m_0]	$m_{v,lh}$ [m_0]	m_r [m_0]	E_G [eV]	$m_{c,x}$ [m_0]	$m_{c,d}$ [m_0]	$m_{v,lh}$ [m_0]	m_r [m_0]
0	1.12	0.19	0.33	0.15	0.084	1.12	0.19	0.33	0.16	0.087
0.3	1.00	0.19	0.33	0.13	0.077	0.98	0.19	0.33	0.13	0.075
0.5	0.94	0.19	0.33	0.11	0.069	0.92	0.19	0.33	0.10	0.066
0.8	0.90	0.20	0.33	0.084	0.057	0.86	0.19	0.33	0.067	0.050
1.0	0.66	0.14	0.25	0.066	0.045	0.66	0.12	0.22	0.044	0.032

Computation of DoS effective mass for the light and heavy hole valence band valleys

For the computation of the DoS effective mass for the light and heavy hole valley using the k·p band structure we discretized the Brillouin Zone using spherical coordinates: the longitudinal angle θ (that goes from 0 to π), the azimuthal angle ϕ (that goes from 0 to 2π) and the radius k, are discretized in N_θ , N_ϕ and N_k points respectively. The energy ranges from 0 to a generic $-E_{\max}$ with a discretization step ΔE. For each point (θ_m, ϕ_n, k_l) in reciprocal space, the value of the light and heavy hole dispersion relation is computed and the Density of States $\tilde{g}(E)$ is obtained as:

$$\tilde{g}(E) = \frac{n_{sp}}{8\pi^3 \Delta E} \sum_{m,n,l} \int_{\phi_n}^{\phi_{n+1}} d\phi \int_{\theta_m}^{\theta_{m+1}} \sin(\theta) d\theta \int_{k_l}^{k_{l+1}} k^2 dk \delta(E_C(\theta_m, \phi_n, k_l), E) \tag{3.73}$$

where

$$\delta(E_C(\theta_m, \phi_n, k_l), E) = \begin{cases} 1 & \text{if} \quad E \leq E_C(\theta_m, \phi_n, k_l) < E + \Delta E \\ 0 & \text{otherwise} \end{cases} \tag{3.74}$$

The integrals in eq. 3.73 give

$$\tilde{g}(E) = \frac{n_{sp}}{4\pi^2 \Delta E} \sum_{m,n,l} (\phi_{n+1} - \phi_n) \times \\ \times (\cos(\theta_m - \cos m + 1) \frac{k_{l+1}^3 - k_l}{3} \delta(E_C(\theta_m, \phi_n, k_l), E) \tag{3.75}$$

Again a non linear regression procedure has been used to extract the value of m and α by minimizing the error $|\tilde{g}(E) - g(E)|^2$ where $g(E)$ is given by eq. 3.71.

Fig. 3.8 shows the DoS computed from the k·p model using eq. 3.73 and the one computed with the analytical formula (eq. 3.71) using the parameters found by the non linear regression are reported in a small energy range that goes from 0 to 5meV. The Germanium molar fractions are x=0,0.3,0.5 and 1.0. For all compositions a very good fit both for heavy and light holes is found. The computed masses and band gaps of the relaxed $Si_{1-x}Ge_x$ alloys are reported in tabs. 3.4 and 3.5 and compared against those presented by Kao et al. [29].

The effective masses are in good agreement with calculations by Kao et al. in spite of the different band calculation methods used. The Band Gap in Γ calculated by the 30 bands k·p instead present discrepancies with respect to the values provided in [29]. However a $Si_{1-x}Ge_x$ alloy with Germanium molar fraction lower than 0.8 has a direct band gap wide enough ($E_G^\Gamma >$ 2.45eV) to consider direct BtBT negligible.

Finally the direct and phonon assisted generation rates are computed using the parameter sets (our and Kao's) considering a constant electric field from 0 to 10 MV/cm. The results are reported in fig. 3.9. Plot a) shows the phonon-assisted generation rate and, for all the considered molar fractions, a very good agreement is found between the results of the two sets.

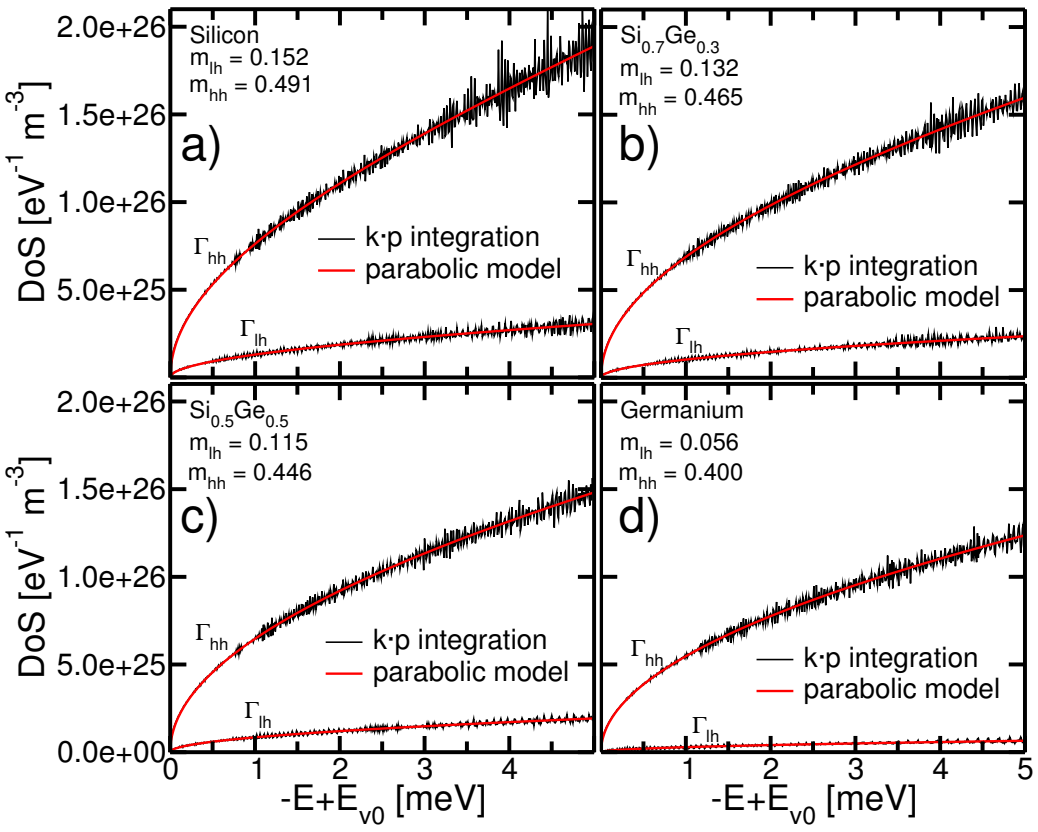

Figure 3.8: The results of the non-linear regression for the are reported in the range of 5meV in energy from the maximum of the valence band with the Germanium molar fraction x=0,0.3,0.5 and 1.0, with a very good fit both for the heavy as for the light holes.

Table 3.5: Comparison between the Direct BtBT parameter extrapolated from the 30 bands k·p model [32, 33] and the parameters reported in [29] for $Si_{1-x}Ge_x$ alloys.

	k· p [32, 33]		ref. [29]	
x	E_G^Γ [eV]	m_r $[m_0]$	E_G^Γ eV	m_r $[m_0]$
0	3.21	0.076	3.4	0.08
0.3	3.08	0.066	2.79	0.063
0.5	2.43	0.058	2.19	0.051
0.8	1.45	0.042	1.37	0.034
1.0	0.80	0.028	0.8	0.022

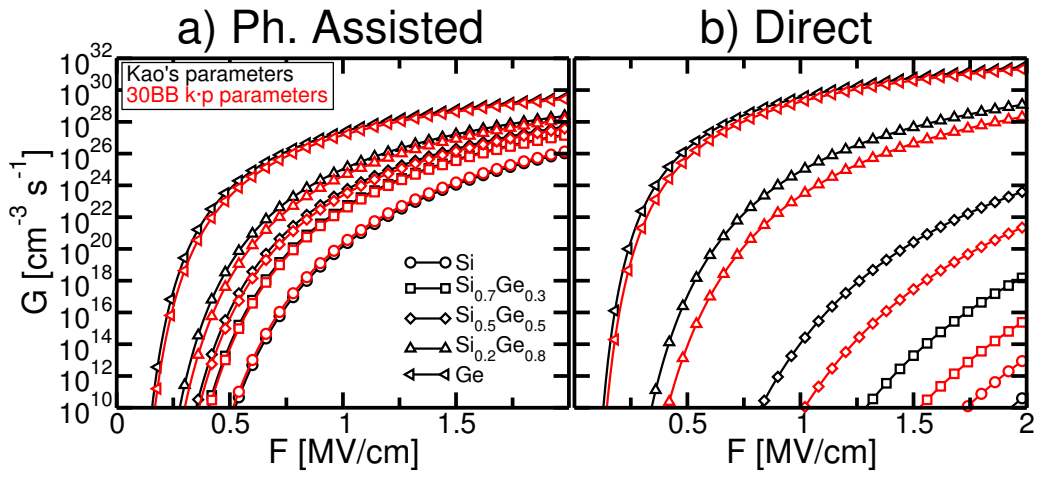

Figure 3.9: Phonon Assisted BtBT Generation Rate (plot a) and Direct BtBT Generation Rate (plot b) in the presence of a constant electric field F, computed with the Kane's models using the parameters reported in [29] or using the parameters extracted by the Band Structure computed with the 30 bands k·p model [32, 33].

On the other hand, plot b) shows that the Direct BtBT generation rate computed with the 30 bands k·p parameters is lower than the Kao's calculation for x $<$ 0.8 because of the higher direct band gap. However, since the direct BtBT rate is quite smaller than the indirect BtBT for x $<$ 0.8, we conclude that the discrepancy between models in fig. 3.9-b is not a serious concern and the k·p calculation can be used to extract the band gaps and effective masses for strained SiGe layers.

Valence DoS effective mass estimation in presence of strain

The parameters choice proposed in [29] uses the whole valence band DoS effective mass obtained with the expression $m_{v,d} = (m_{v,lh}^{3/2} + m_{v,hh}^{3/2})^{2/3}$, that holds only if the light and heavy hole bands are degenerate in the Γ point. On the other hand in presence of strain the valence bands are split and a new expression for the valence DoS effective mass must be found. The hole density of a 3D gas of free holes p, if the valleys are split, can be expressed as [3]:

$$p = \frac{4}{\sqrt{\pi}} \left(\frac{2\pi m_{v,lh} k_B T}{h^2} \right)^{3/2} \mathcal{F}_{1/2} \left(\frac{E_{V,lh} - E_F}{k_B T} \right) + \\ + \frac{4}{\sqrt{\pi}} \left(\frac{2\pi m_{v,hh} k_B T}{h^2} \right)^{3/2} \mathcal{F}_{1/2} \left(\frac{E_{V,hh} - E_F}{k_B T} \right) \quad (3.76)$$

where $\mathcal{F}_{1/2}(x)$ is the Fermi Dirac function of order one half, $m_{v,lh}$ and $m_{v,hh}$ are the DoS effective mass of light and heavy hole bands, respectively. $E_{V,hh}$ and $E_{V,lh}$ is the energy level of heavy and light hole bands. Imposing $E_{V,lh} = E_{V,hh} + \Delta E_V$ the expression above can be rewritten as:

$$p = \frac{4}{\sqrt{\pi}} \left(\frac{2\pi k_B T}{h^2} \right)^{3/2} \underbrace{\left(m_{v,lh}^{3/2} \frac{\mathcal{F}_{1/2} \left(\frac{E_{V,hh} + \Delta E_V - E_F}{k_B T} \right)}{\mathcal{F}_{1/2} \left(\frac{E_{V,hh} - E_F}{k_B T} \right)} + m_{v,hh}^{3/2} \right)}_{= m_{v,d}^{3/2}} \mathcal{F}_{1/2} \left(\frac{E_{V,hh} - E_F}{k_B T} \right) \quad (3.77)$$

Table 3.6: Parameters for the Jain Roulston Band Gap Narrowing model [36] for pure Silicon with acceptor or donor doping.

Donor		Acceptor	
$C_{1,D}$	10.23 meV	$C_{1,A}$	11.07 meV
$C_{2,D}$	13.12 meV	$C_{1,A}$	15.17 meV
$C_{2,D}$	2.93 meV	$C_{1,A}$	5.07 meV

$\Delta E_{\mathrm{V}} = E_{\mathrm{V},lh} - E_{\mathrm{V},hh}$ is given by the band structure model calculation for the strained material. $E_{\mathrm{F}} = 0.0\mathrm{eV}$ is taken as a reference and the value of $E_{\mathrm{V},hh}$ must be computed to calculate $m_{v,d}$ through the numerical solution of eq. 3.77 imposing $p = N_{\mathrm{A}}$. If the doping level is high and the semiconductor is degenerate the value of $m_{v,d}$ depends on N_{A} through the value of $E_{\mathrm{V},hh}$ in the $\mathcal{F}_{1/2}(x)$. On the other hand for non-degenerate semiconductors the Maxwell-Boltzmann approximation holds and $m_{v,d}$ can be computed, in a simpler way, as:

$$m_{v,d} = \left(m_{v,lh}^{3/2} \exp\left(\frac{\Delta E_{\mathrm{V}}}{k_{\mathrm{B}} T} \right) + m_{v,hh}^{3/2} \right)^{2/3} \tag{3.78}$$

3.7.2 Band Gap Narrowing (BGN) effect on BtBT tunneling

The Band Gap Narrowing (BGN) is an effect that reduces the bang gap of the semiconductor doped with high doping concentrations [34, 35]. TFETs require a high acceptor source doping density to have steep potential profiles at the source/channel junction to improve current and subthreshold slope of the device. Therefore, BGN becomes relevant for TFETs and must be taken into account. The Jain-Roulston model [36] is an accurate BGN model that differentiate the band gap reduction due to donor doping $\Delta E_{\mathrm{G}}(N_D)$ and the one due to acceptor doping $\Delta E_{\mathrm{G}}(N_A)$ and it reads:

$$\Delta E_{\mathrm{G}}(N_D) = C_{1,D} \left(\frac{N_D}{10^{18}} \right)^{1/3} + C_{2,D} \left(\frac{N_D}{10^{18}} \right)^{1/4} + C_{3,D} \left(\frac{N_D}{10^{18}} \right)^{1/2} \tag{3.79}$$

$$\Delta E_{\mathrm{G}}(N_A) = C_{1,A} \left(\frac{N_A}{10^{18}} \right)^{1/3} + C_{2,A} \left(\frac{N_A}{10^{18}} \right)^{1/4} + C_{3,A} \left(\frac{N_A}{10^{18}} \right)^{1/2} \tag{3.80}$$

As an example BGN parameters for pure unstrained silicon are reported in tab. 3.6

In [36] the analysis of the components that contribute to the reduction of the band gap involve both the bands: the majority one (conduction and valence band for the n-type and p-type semiconductor, respectively) and the minority one. Jain et al. identifies four contributions to the BGN

- shift $\Delta E_{\mathrm{x(maj)}}$ of the majority band edge due to exchange interaction
- shift $\Delta E_{\mathrm{cor(mino)}}$ of the minority band edge due to carrier carrier or to electron hole interaction.
- shift $\Delta E_{\mathrm{i(maj)}}$ of the majority band edge due to carrier and dopant atom interaction
- shift $\Delta E_{\mathrm{i(maj)}}$ of the minority band edge due to carrier and dopant atom interaction

A more accurate physical analysis of the effect of these interactions is far beyond the goals of this thesis work and can be found in [37, 38, 36]. The interesting point in considering separately the shifts due to these interaction is the possibility to separate the contribution to the BGN given by the conduction and by the valence band. Indeed, as pointed out in fig. 2.7 for the hetero-junctions, BGN can have different results for the BtBT if the reduction of the band gap concerns only the valence or the conduction band.

Table 3.7: Jain-Roulston BGN model parameters for n-type and p-type Silicon considering separately the contribution from the valence and conduction band (eq. 3.90).

	C_1^* [meV]	C_2^* [meV]	C_3^* [meV]	C_4^* [meV]
n-type Si	10.23	1.45	13.12	1.48
p-type Si	11.07	3.25	15.17	1.82

In [36] the expressions for the computation of the various shifts are reported and it is possible to write:

$$\Delta E_{\mathrm{x(maj)}} = C^*_{1,AD}(N_{AD}/10^{18})^{1/3} \tag{3.81}$$

$$\Delta E_{\mathrm{i(maj)}} = C^*_{2,AD}(N_{AD}/10^{18})^{1/2} \tag{3.82}$$

$$\Delta E_{\mathrm{corr(min)}} = C^*_{3,AD}(N^{1/4}_{AD}/10^{18})^{1/4} \tag{3.83}$$

$$\Delta E_{\mathrm{i(min)}} = C^*_{4,AD}(N_{AD}/10^{18})^{1/2} \tag{3.84}$$

and by comparison with eq. 3.79 we can write:

$$C_{1,AD} = C^*_{1,AD} \tag{3.85}$$

$$C_{2,AD} = C^*_{3,AD} \tag{3.86}$$

$$C_{3,AD} = C^*_{2,AD} + C^*_{4,AD} \tag{3.87}$$

and finally we can relate it to the conduction and the valence band, in the n-type semiconductor case, as:

$$\Delta E_{\mathrm{C}} = C^*_{1,AD}\left(\frac{N_D}{10^{18}}\right)^{1/3} + C^*_{2,AD}\left(\frac{N_D}{10^{18}}\right)^{1/2} \tag{3.88}$$

$$\Delta E_{\mathrm{V}} = C^*_{3,AD}\left(\frac{N_D}{10^{18}}\right)^{1/4} + C^*_{4,AD}\left(\frac{N_D}{10^{18}}\right)^{1/2} \tag{3.89}$$

and in the p-type semiconductor as:

$$\Delta E_{\mathrm{C}} = C^*_{3,AD}\left(\frac{N_D}{10^{18}}\right)^{1/4} + C^*_{4,AD}\left(\frac{N_D}{10^{18}}\right)^{1/2} \tag{3.90}$$

$$\Delta E_{\mathrm{V}} = C^*_{1,AD}\left(\frac{N_D}{10^{18}}\right)^{1/3} + C^*_{2,AD}\left(\frac{N_D}{10^{18}}\right)^{1/2} \tag{3.91}$$

$$\tag{3.92}$$

Tab. 3.7 reports the parameters of eq. 3.90 for relaxed Silicon.

3.8 Non-local phonon-assisted BtBT model calibration for strained Silicon and application to the simulation of a strained nanowire TFET

In 2013 Knoll et al. [39] have presented very promising results regarding a Ω-gated nanowire TFET with a strained Silicon channel. The device was fabricated on a SSOI wafer with a biaxial tensile strain $\epsilon = 0.8\%$ that correspond to a stress $T \approx 1.3$GPa and in fig. 3.10 the TEM image of the cross section is reported. The nanowire is oriented in the [110] direction

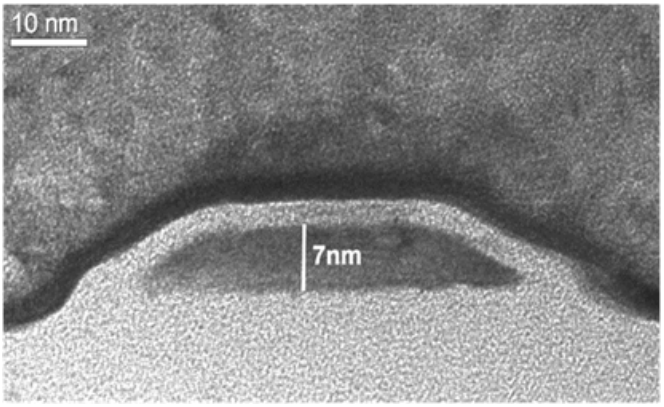

Figure 3.10: TEM image of the cross section of the Ω-gated nanowire TFET proposed in [39]. Courtesy of Forschungszentrum Jülich GmbH.

and after the etching the strain in the transverse direction is relaxed leaving only the uniaxial strain in the [110] direction [40]. This TFET design is subjected to dopant segregation during the silicidation of source and drain and a very high and sharp doping profile is expected.

As pointed out in [41, 42] the presence of acute angles at the corners of the cross section of a multi-gate device (such as FinFETs, Ω gated nanowire, GAA nanowire etc.) implies the presence of a volume inversion due to the size- and bias-quantization effect. By reducing the corner angle three effects take place, namely an increased electrostatic control that increase the density of the inversion charge when a gate biasing is applied, and an increased volume inversion effect (figs. 1 and 2 in [41]) and the distance of the maximum of the inversion charge is increased (indicating a stronger quantization effect). The increased quantization effect should imply also a widening of the actual band gap that reduces the tunneling probability, but, to have a correct estimation of this band gap widening, the solution in the cross section of the 2D Schrödinger equation with closed boundaries coupled with the 2D Poisson is required.

Fig. 3.11 reports the corresponding simulation domain structure, characterized by an isosceles trapezoidal cross section where the larger base and the narrower base width are $W_1 = 50$nm and $W_2 = 25$nm, respectively, and the height of the semiconductor is T_{sc}=7nm. The lateral acute angles are equal to $\alpha = 30$. The oxide is HfO_2 with an oxide thickness $T_{\text{ox}} = 3$nm. To model the effect of dopant segregation due to silicidation in the TFET of [39] in the simulation domain the source acceptor doping density has been set to the Boron solubility limit in Silicon $N_A = 3.3 \cdot 10^{20}\text{cm}^{-3}$ with abrupt doping profile. To avoid ambipolarity leakage in the simulation results, the drain donor doping has been set to the value of $N_D = 10^{18}\text{cm}^{-3}$. The effect of the doping density on the band gaps in the different regions of the device has been considered using the Jain Roulston model with the parameters reported in tab. 3.6.

The application of strain deforms the band structure of the material, breaking the degeneracy between the light and the heavy holes at the Γ and between the Δ valleys in the conduction band. Therefore it changes the energy gap between the valence and the conduction band valleys in a way that is different from the relaxed nominal and that is, in principle, different for each distinct couple of valence and conduction band valleys.

Tabs. 3.8 and 3.9 reports the band gaps and the effective masses of holes and electrons for the transition between all the possible transitions between the light and heavy hole valence band valleys and the Δ valleys in the conduction band, for the simulation of the TFET in fig. 3.11. They have been extrapolated by the band structure calculated with the 30 bands k·p provided with the strain profile of the Knoll's nanowire [39] (uniaxial strain along [110] $T = 1.3$GPa) using the procedure reported in sec. 3.7.1.

The same approach for the parameter choice proposed in 3.7.1 for the simulation of strained

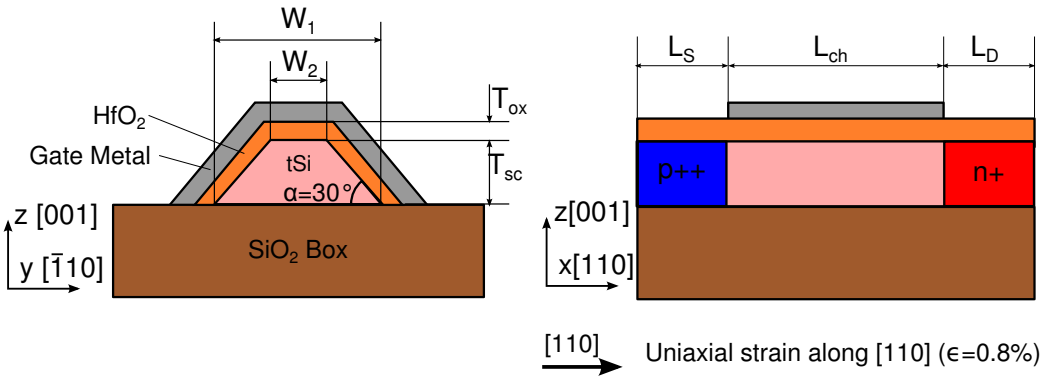

Figure 3.11: Simulated nanowire structure simulated emulating the device presented in [39]. The width is W=50nm, the semiconductor thickness is T_{sc}=7nm. The channel length is L_{ch}=60nm. L_S = 20nm and L_D=40nm. $N_A = 3.3 \cdot 10^{20}\text{cm}^{-3}$, $N_D = 10^{18}\text{cm}^{-3}$. The doping profiles are abrupt and the gate edges are perfectly aligned with the source and drain junctions.

Table 3.8: Effective masses extracted from the 30 bands k·p for the the silicon strained in [110] direction ($\varepsilon = 0.8\%$). The electron effective masses have been evaluated in the [110] direction.

Transition in tSi	m_v $[m_0]$	$m_{c,x}$ $[m_0]$	m_r $[m_0]$	$m_{c,d}$ $[m_0]$	E_{G} source [eV]	E_{G} channel [eV]	E_{G} drain [eV]
$\Gamma_{lh} \rightarrow \Delta_{100}$	0.26	0.32	0.14	0.33	0.925	1.159	1.132
$\Gamma_{lh} \rightarrow \Delta_{010}$	0.26	0.32	0.14	0.33	0.925	1.159	1.132
$\Gamma_{lh} \rightarrow \Delta_{001}$	0.26	0.17	0.10	0.33	0.860	1.094	1.067
$\Gamma_{hh} \rightarrow \Delta_{100}$	0.23	0.32	0.13	0.33	0.899	1.133	1.106
$\Gamma_{hh} \rightarrow \Delta_{010}$	0.23	0.32	0.13	0.33	0.899	1.133	1.106
$\Gamma_{hh} \rightarrow \Delta_{001}$	0.23	0.17	0.096	0.33	0.834	1.068	1.042

Table 3.9: Valence DoS effective mass computed for the regions of the TFET of fig. 3.11 implemented with uniaxially tensile strained Silicon using the procedure proposed in sec. 3.7.1

	Source	Channel	Drain
$m_{v,d}[m_0]$	0.38	0.30	0.30

Table 3.10: Effective masses extracted from the 30 bands k·p for the relaxed silicon. The electron effective masses have been evaluated in the [110] direction.

Transition in tSi	m_v [m_0]	$m_{c,x}$ [m_0]	m_r [m_0]	$m_{c,d}$ [m_0]	E_G source [eV]	E_G channel [eV]	E_G drain [eV]
$\Gamma_{lh} \rightarrow \Delta_{100}$	0.15	0.32	0.10	0.33	0.895	1.128	1.102
$\Gamma_{lh} \rightarrow \Delta_{010}$	0.15	0.32	0.10	0.33	0.895	1.128	1.102
$\Gamma_{lh} \rightarrow \Delta_{001}$	0.15	0.18	0.083	0.33	0.895	1.128	1.102
$\Gamma_{hh} \rightarrow \Delta_{100}$	0.48	0.32	0.19	0.33	0.895	1.128	1.102
$\Gamma_{hh} \rightarrow \Delta_{010}$	0.48	0.32	0.19	0.33	0.895	1.128	1.102
$\Gamma_{hh} \rightarrow \Delta_{001}$	0.48	0.18	0.13	0.33	0.895	1.128	1.102

Table 3.11: Parameters of the phonon assisted BtBT non-local dynamic model, derived from the effective mass and band gap values reported in tab. 3.8 and used in the simulation of the structure of fig. 3.11.

	Source		Channel		Drain	
	A	B	A	B	A	B
Transition	[10^{14}cm^{-3}s^{-1}]	[MV/cm]	[10^{14}cm^{-3}s^{-1}]	[MV/cm]	[10^{14}cm^{-3}s^{-1}]	[MV/cm]
$\Gamma_{lh} \rightarrow \Delta_{100}$	7.12	23.06	3.29	32.14	3.43	31.05
$\Gamma_{lh} \rightarrow \Delta_{010}$	7.12	23.06	3.29	32.14	3.43	31.05
$\Gamma_{lh} \rightarrow \Delta_{001}$	12.68	17.39	5.71	24.79	5.96	23.90
$\Gamma_{hh} \rightarrow \Delta_{100}$	8.16	21.34	3.73	30.00	3.89	28.96
$\Gamma_{hh} \rightarrow \Delta_{010}$	8.16	21.34	3.73	30.00	3.89	28.96
$\Gamma_{hh} \rightarrow \Delta_{001}$	14.23	16.21	6.34	23.33	6.62	22.47

Si TFET in fig. 3.11, is also used for the computation of the parameters of Si considering [110] as the transport direction. Since in relaxed Silicon the valence bands are degenerate in the Γ point, the valence band DoS effective mass is equal to $m_{v,d} = (0.16^{3/2} + 0.49^{3/2})^{3/2} m_0 = 0.55 m_0$.

With the intent of maintaining a link with the Hurkx and Kane models, the non-local direct and phonon-assisted models implemented in Sentaurus Device are calibrated using the A, B and the band gap parameters (eq. 3.40 and 3.61 for the direct and the phonon-assisted models, respectively) therefore for each transition between different pairs of valence/conduction band valleys the user specifies the A, B parameters and the Band Gap (together with the phonon energy ε_{op} for the Phonon Assisted model and the ratio between m_c and m_v). Eqs. 3.39 and 3.60 highlight how a large A and a smaller B value correspond to higher G_{bbt} and therefore to higher BtBT currents.

Tabs. 3.11 and 3.12 report A and B parameters for all the BtBT transitions of interest in strained and relaxed Silicon, respectively, between the valence and the conduction band valleys, whereas fig. 3.12 shows the trans-characteristics of the TFET of fig. 3.11 in strained (plot a) and relaxed (plot b) Silicon. All the BtBT transition between different pairs of valence/conduction band valleys have been separately taken into account and the total BtBT current is compared with the measurements reported in [39]

The obtained results indicates a clear discrepancy between the simulation and the experimental results: the simulated current for the strained Silicon case not only is lower than the measurements but also with respect to one of the relaxed case. Fig. 3.13 helps to understand the reason for these results: plot a) reports the DoS effective masses versus the applied strain whereas plot b) shows the band gap corresponding to the transitions between the valence light or heavy hole valleys and the conduction valleys Δ . The conduction effective mass $m_{c,x}$ refers to the Δ_{001} valley which gives the most significant contribution to BtBT. As known the conduction band effective masses does not significantly depend on the strain level [33]. On the

Table 3.12: Parameters of the phonon assisted BtBT non-local dynamic model used in the simulation of the structure of fig. 3.11 implemented with relaxed Silicon.

	Source		Channel		Drain	
Transition	A $[10^{14}\text{cm}^{-3}\text{s}^{-1}]$	B [MV/cm]	A $[10^{14}\text{cm}^{-3}\text{s}^{-1}]$	B [MV/cm]	A $[10^{14}\text{cm}^{-3}\text{s}^{-1}]$	B [MV/cm]
$\Gamma_{lh} \rightarrow \Delta_{100}$	19.04	18.55	12.77	26.11	13.31	25.34
$\Gamma_{lh} \rightarrow \Delta_{010}$	19.04	18.55	12.77	26.11	13.31	25.34
$\Gamma_{lh} \rightarrow \Delta_{001}$	24.97	16.64	16.75	23.43	17.46	22.73
$\Gamma_{hh} \rightarrow \Delta_{100}$	8.72	25.36	5.85	35.70	6.09	34.46
$\Gamma_{hh} \rightarrow \Delta_{010}$	8.72	25.36	5.85	35.70	6.09	34.46
$\Gamma_{hh} \rightarrow \Delta_{001}$	13.89	21.04	9.32	29.70	9.71	28.60

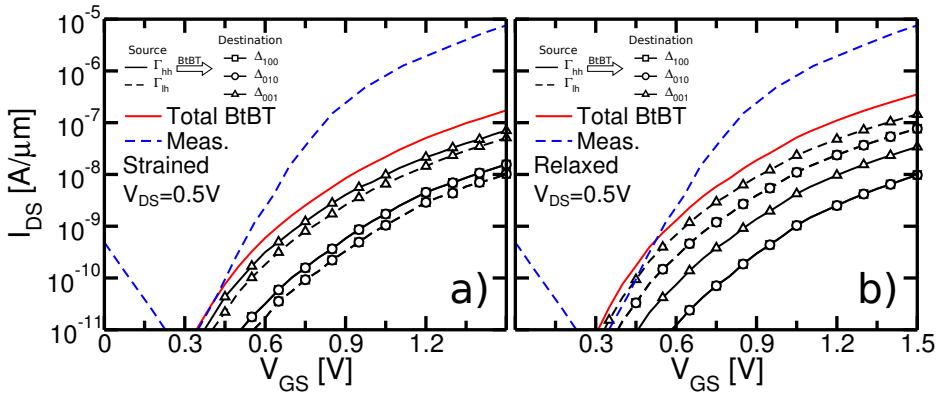

Figure 3.12: Plot a) trans-characteristics of the Nanowire TFET sketched in fig. 3.11, simulated with Sentaurus SDevice using the Non Local Dynamic Model calibrated procedure reported in sec. 3.7.1 (parameters in tabs. 3.8, 3.11). Plot b) trans-characteristics of the same structure implemented with relaxed silicon (parameters). BtBT currents related to the different transitions between the valence and the conduction band valleys have been computed separately. The sum of all the components is compared with the measurements reported in [39].

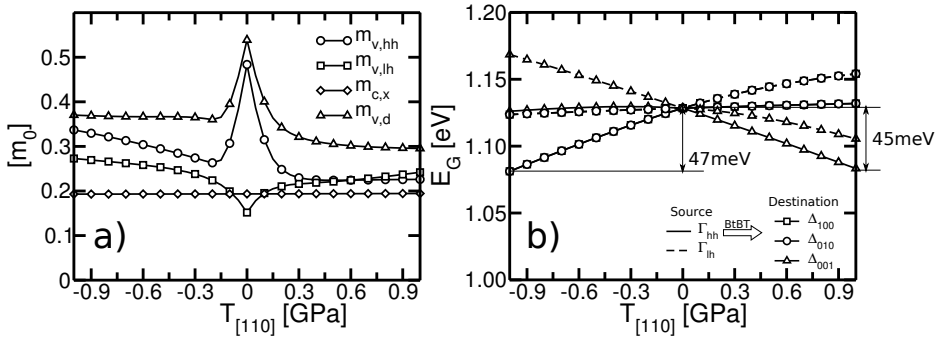

Figure 3.13: Plot a) Effective masses involved in the computation of BtBT in Silicon versus the stress along the [110] direction. Plot b) Band gap corresponding to the various transition between the valence light and heavy hole band valleys and the conduction Δ valleys.

other hand fig. 3.13-a shows how light and heavy hole DoS effective masses change with the strain level and highlight that the smallest mass is found for the light hole valley in the relaxed case. Moreover also the whole valence DoS effective mass $m_{v,d}$ decreases with the strain, and this correspond to a reduction of DoS of the valence and hence of the BtBT generation rate. Therefore when strain is applied we see a reduction of the DoS and an increase of the effective mass that correspond to a reduction of the total BtBT rate. Fig. 3.13-b confirms this conclusion showing the band gap between the minimum of valence and conduction band valleys and some transitions see a reduction of the band gap when strain is applied with respect to the relaxed case, but the same transitions are characterized by a lower DoS (smaller $m_{v,d}$) and by a larger value of the minimum reduced mass that correspond to a reduced BtBT generation rate, and therefore to a reduced BtBT current.

These conclusions are further confirmed by fig. 3.14 that plots the BtBT parameters A and B versus the applied stress $T_{[110]}$ along the [110] direction. A (plot a) and B (plot b) find their maximum and minimum, respectively, in the relaxed case considering the BtBT transition from the light hole valley Γ_{lh} to the conduction band valley Δ_{001}. Since in tensile strained case the minimum value of B is larger and maximum value of A is smaller than in the relaxed case a reduction of the BtBT current is expected.

The comparison of the results in fig. 3.12-a and -b with the experimental results in [39] therefore reveals that the proposed approach for the BtBT parameter choice in presence of strain is not capable to reproduce the current found in the experimental results. Moreover considering the idealizations imposed in the simulation (no quantization effect, very high source doping, abrupt doping profiles), in presence of a correct modeling of the BtBT generation mechanism, the total current should be significantly higher than the experimental one.

Nevertheless the proposed methodology for the BtBT parameter choice is accurate when applied to the case of the relaxed Silicon in UTB FD-SOI TFETs, and some final remarks can be pointed out to contextualize the results:

- The experimental device structure is not completely known and therefore some fundamental aspects could be neglected in the simulation domain definition, spoiling the accuracy of the simulations.

- At our knowledge in the literature the dependence of the phonon properties in strained indirect band gap materials is not deeply investigated and it is not possible to find an estimation of phonon energy and of the deformation potential values for tensile strained silicon. Using the relaxed silicon phonon parameters could result in a underestimation of the actual BtBT current.

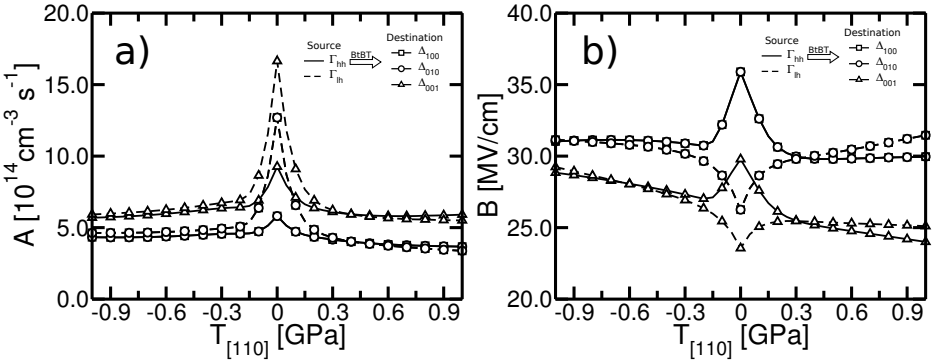

Figure 3.14: A (plot a) and B (plot b) parameters versus the amount of stress along the [110] direction $T_{[110]}$.

- Ohashi et al. measured the acoustic phonon deformation potential in UTB FDSOI structures [43, 44], demonstrating that it becomes larger in structure with thin semiconductor layer $T_{\mathrm{Si}} < 10$nm. The larger value of the deformation potential may have a significant effect on the band structure and on BtBT in presence of strain and deserves to be investigated.

- In presence of strain the non-local phonon-assisted BtBT model may not be sufficiently accurate and more fundamental approaches, as those reported in [22, 45] may be necessary.

In conclusion to improve the understanding of the physical mechanisms operating inside the TFETs in presence of strain, a further characterization work is required to investigate the actual strain profile found inside the TFET channel and its effect on the device performance. A further modeling work is also required to overcome the limitations illustrated above, to investigate phonon properties in presence of strain and to apply more fundamental BtBT models to the simulation of the TFETs implemented in strained indirect band gap material.

3.9 Summary

In this chapter the most common semi classical local and non-local models for Direct and Phonon Assisted BtBT of free carriers have been presented, pointing out the limitations of the Local models [14] the simulation of Tunnel FETs and of tunneling devices. Non Local models on the other hand are more accurate since they consider the whole potential profile along the tunneling path.

If the electron gas is quantized at first order we expect a reduction of the BtBT generation rate because the splitting of the subbands makes the tunneling longer and increases the band gap. To overcome these limitations Vandenberghe et al. proposed a full quantum phonon-assisted BtBT model that naturally accounts for size- and bias-induced quantization but on the other hand represents a heavier computational burden with respect to semi-classical non-local phonon assisted BtBT model.

A calibration of the BtBT Models has been presented which is based on data presented by Kao et. al [29] for SiGe alloys and which has been confirmed by original 30 band k·p calculations. Model parameters for strained SiGe (not reported by Kao) have also been computed using the same 30 bands k·p [32, 33]. In particular we extracted the effective masses and the band gaps for the valence and the conduction band valleys. By using these values as an input for the non-local phonon-assisted BtBT model implemented in the Sentaurus SDevice the simulation of a nanowire structure similar to the one proposed in [39] and the results have been compared with

the experimental data. In the comparison between the measurements and the simulation results a significant discrepancy have been found and it cannot simply be attributed to limitations of the BtBT model, even if there are some aspects, as the phonon parameter dependence on strain or on semiconductor thickness in UTB SOI structure, that are not fully investigated and that may give a significant contribution in enhancing the accuracy of the BtBT generation rate estimation. It is also possible that the phonon-assisted non-local BtBT model is not sufficiently accurate considering strained indirect band gap materials and that a more fundamental approach is required to investigate the problem.

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Chapter 4

Multi Subband Monte Carlo simulation approach for TFETs

In this chapter we describe the development of a Multi-Subband Monte Carlo (MSMC) simulator for planar Tunnel FETs. The choice of this modelling approach is justified by considerations that range from the fact that techniques based on MSMC have been extensively developed in recent years for nanoscale MOSFETs [1, 2] and the fact that they represent a good compromise, in terms of efficiency and physical content, between commercial TCAD software and full quantum transport simulators. MSMC models can handle all transport regimes from diffusive to purely ballistic and it is relatively easy to add new physics (scattering mechanisms) introduced by the use of technology boosters as those envisioned to improve the performance of nanoscale devices. In fact, MSMC simulators already include the effect of many technology boosters (strain, high-k, Schottky barrier, alternative channel materials) [3, 4, 5]. Quantization in the confinement direction is properly taken into account by solving the Schrödinger equation (SE) in the vertical direction (as in full-quantum approaches) at a number of sections in the channel. Introducing a pure quantum mechanical effect such as BtBT into a MSMC simulator is however a challenging task. In fact semi-classical transport is inherently based on a particle-like or charged carriers view and on the solution of the Boltzmann transport equation. Carrier injection into the channel of a conventional MOSFET is treated as a thermionic process and source to drain tunneling effects are normally neglected. However, these quantum effects along the transport direction can be handled by a corrected potential, in conventional MOSFETs these become important only for L_{G} lower than approximately 6nm [6].

In order to introduce BtBT in a MSMC transport model we considered BtBT as a generation/recombination mechanism, as in commercial TCAD [7]. This choice has non trivial implication on the stability of the self consistent Poisson-Monte Carlo loop. To assess the model limits we investigated the sensitivity of simulation results to different formulations of the BTBT generation rate and to the adapted modeling approximations.

In addition, in order to account for the impact of subband splitting on carrier confinement in the vertical direction, an empirical correction of the band structure is proposed and calibrated against the results of more fundamental modeling approaches. The modified MSMC simulator thus obtained combines all the advantages of conventional MSMC codes for nano MOSFETs with the ability to tackle difficult problems in the optimization of TFETs. One in particular concerns the role of scattering and carrier velocity profiles in the TFET performance. In fact carrier injection in the channel is limited by BtBT mechanism which should be insensitive to scattering. On the other hand we know from nanoscale MOSFETs studies that even a few scattering events in the channel can affect the electrostatics and can appreciably reduce the current compared to the ballistic limit [4, 5]. In addiction high-κ material related scattering mechanism can severely degrade the mobility and high-κ gate stacks are important to achieve an adequate gate coupling in TFETs. The MSMC approach thus offers unique opportunities to investigate non trivial physical effects in MOSFETs as well as in TFETs.

The choice for the BtBT model has fallen on the phonon assisted and direct dynamic non-local models [7] since they represent a good trade-off between good accuracy, acceptable computation burden and compatibility with the internal mechanism of a MSMC simulator, briefly described later. The local models, like the Kane's and Keldysh's ones, are very simple to implement and their computational burden is reduced but, considering the electrostatic profile that characterizes the TFET they are not sufficiently accurate. In fact the approximation of constant field is not acceptable (especially in the sub-threshold region) and brings to severe over-estimation of BtBT generation rate [8]. On the other hand, full quantum models like the one proposed in [9, 10] based on the EMA Hamiltonian, or more fundamental ones based on k·p or tight-binding Hamiltonians, like those proposed in [11, 12], are characterized by a very good accuracy but at the cost of an increase of the computational burden. As demonstrated in appendix A the 2D Quantum model presented in [10] requires the computation of a large number of 1D Schrödinger with closed and open boundary conditions, that represent a significant computational burden that is further increased considering k·p or atomistic full quantum simulators. The latter can be applied only on domains reduced to few nanometers and therefore

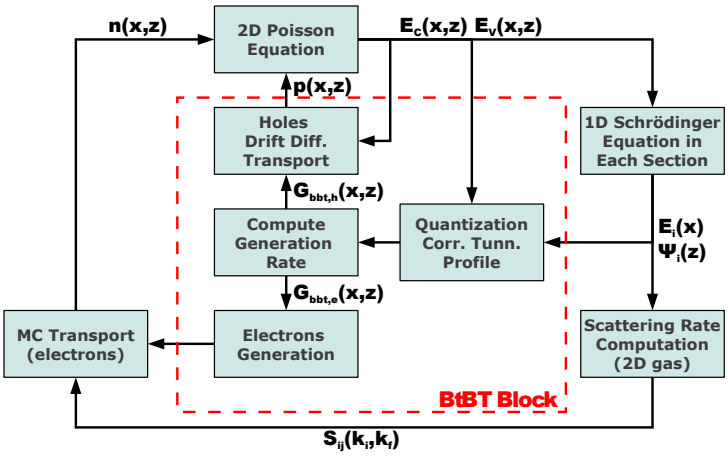

Figure 4.1: Flowchart of the MSMC simulator including BtBT generation. $\hat{x}$ is the transport direction, $\hat{z}$ the quantization direction. $G_{\mathrm{bbt,e}}(x,z)$ and $G_{\mathrm{bbt,h}}(x,z)$ are the electron and hole BtBT generation rates respectively. $E_{\mathrm{i}}(x)$ are the subband energies, Ψ_{i} the subband eigenfunctions. S_{ij} are the scattering rates, whereas $n(x,z)$ and $p(x,z)$ are the density of electrons and holes respectively.

on a limited field of application of nanowire devices with reduced cross section area and very short length.

As said above the dynamic non-local models hold for a gas of free electrons, but with a semi-empirical correction, presented in sec. 4.1.4, we were able to account effectively for the quantization usually found in planar UTB FD-SOI devices.

The following results concentrate on n-type TFETs where conduction occurs due to valence to conduction band tunneling of electrons at the source side of the devices.

4.1 Model Description

Fig. 4.1 reports the flowchart of the modified MSMC simulator for TFET simulation developed in this work. In this model a 2D domain is divided in slices parallel to the vertical direction, denoted in the following as "quantization direction" where the carriers are confined and therefore subject to quantization. For each slice, given the conduction band profile, the Schrödinger solver block computes the subband energies and the corresponding wave-functions for the conduction band valleys, the latter are then used for the evaluation of the scattering rates. In the following step the transport is computed through the Monte Carlo block. The last step is the 2D non-linear Poisson solver that couples the transport with the electrostatics and computes the potential and band profiles that will be used in the next iteration. A more exhaustive analysis of the blocks of the MSMC necessary for the simulation of conventional MOSFETs, is beyond the aim of this thesis and can be found in [13].

The dashed line in fig. 4.1 encircles the additional blocks specifically needed to account for BtBT generation. We incorporate BtBT as a generation/recombination mechanism, as in commercial TCAD software [7], but we also introduce a correction to the conduction and valence band profiles in order to account to the first order for carrier quantization in the channel.

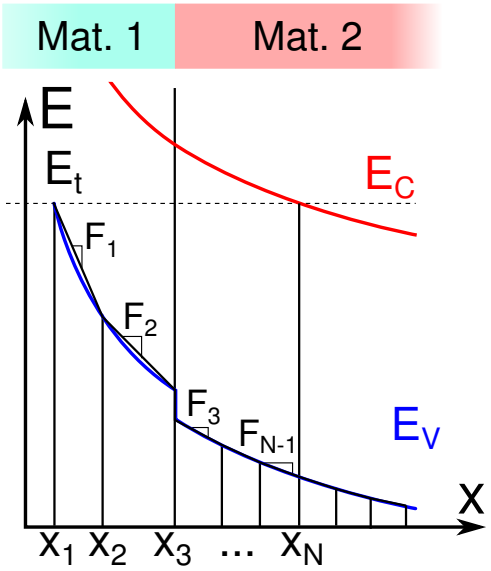

Figure 4.2: Schematic representation of the discretization of the tunneling path in N-1 bins. The amplitude Δx_n is not fixed and can change from bin to bin. The n-th bin is limited between x_n and x_{n+1} and it is characterized by a constant electric field F_n. The potential energy is therefore approximated by a piecewise linear curve.

4.1.1 Calculation of the BtBT Generation Rate

The direct and phonon-assisted BtBT generation rates are calculated according to the corresponding dynamic non-local models (eqs. 3.58, 3.67, and 3.68 in section 3.4 and 3.6 of chapter 3) using the potential gradient rule for the determination of the tunneling path in section 3.5. In the following sections we describe the discretization of the tunneling path and the computation of the integrals of the dispersion relation along the tunneling path.

Numerical solution of the integral terms in homo- and hetero-junctions for the Non Local Direct BtBT Model

The integrals in eq. 3.58 cannot be calculated in a closed form because the potential profile along the tunneling path is not known analytically; thus, a numerical approximation is required. The trapezoid method cannot be used for the terms $\int k_t^{-1}(x)dx$, the integrand being a singular function at the beginning and at the end of the tunneling path (the classical turning points). To overcome this limitation we follow the approach illustrated in fig. 4.2 for the discretization of the tunneling path. The latter is divided in $N-1$ non uniform bins of width Δx_n between the coordinates x_n and x_{n+1}. Inside each bin the electric field is assumed constant and the potential energy along the tunneling path is therefore a piecewise linear curve. For the sake of generality, fig. 4.2 shows that the tunneling path crosses the interface between two semiconductor materials with different physical properties, in particular: the reduced mass m_r, the band gap E_G and the electron affinity χ. The generic n-th bin of the tunneling path is homogeneous and therefore characterized by a single reduced mass $m_{r,n}$, band gap $E_{G,n}$ and affinity χ_n. Under these

assumptions we can write:

$$\int_{x_i}^{x_f} k_t(x)dx = \sum_{n=1}^{N-1} \int_{x_n}^{x_{n+1}} k_t(x)dx = \sum_{n=1}^{N-1} \int_{x_n}^{x_{n+1}} \frac{1}{\hbar}\sqrt{m_{r,n}E_{\mathrm{G},n}(1-\alpha_n^2(E_\mathrm{t},x))}dx \tag{4.1}$$

$$\int_{x_i}^{x_f} k_t^{-1}(x)dx = \sum_{n=1}^{N-1} \int_{x_n}^{x_{n+1}} k_t(x)^{-1}dx = \sum_{n=1}^{N-1} \int_{x_n}^{x_{n+1}} \frac{\hbar dx}{\sqrt{m_{r,n}E_{\mathrm{G},n}(1-\alpha_n^2(E_\mathrm{t},x))}} \tag{4.2}$$

$$\tag{4.3}$$

where

$$\alpha_n(E_\mathrm{t},x,E_{\mathrm{G},n}) = -\frac{m_0}{2m_{r,n}} + 2\sqrt{\frac{m_0}{2m_{r,n}}\left(\frac{E_\mathrm{t}-E_{\mathrm{V,n}}+F_n(x-x_n)}{E_{\mathrm{G},n}}-\frac{1}{2}\right)+\frac{m_0^2}{16m_{r,n}^2}+\frac{1}{4}} \tag{4.4}$$

with $E_{\mathrm{V},n} = E_\mathrm{V}(x_n)$. To change the variable from x to α_n the following derivative is required:

$$\frac{d\alpha_n}{dx} = \frac{1}{\alpha_n + \frac{m_0}{2m_{r,n}}}\frac{m_0qF_n}{E_{\mathrm{G},n}} \tag{4.5}$$

The integral 4.1 can thus be rewritten as:

$$\int_{x_i}^{x_f} k_t(x)dx = \sum_{n=1}^{N-1} \frac{\sqrt{m_{r,n}}E_{\mathrm{G},n}^{3/2}}{\hbar m_0 qF_n} \int_{\alpha_n(x_n)}^{\alpha_n(x_{n+1})} \left(\alpha_n + \frac{m_0}{2m_{r,n}}\right)\sqrt{(1-\alpha_n^2)}d\alpha_n \tag{4.6}$$

Considering the two terms inside the round brackets the integral is divided in two terms that can be integrated as:

$$I_{n,1} = \int_{\alpha_n(x_n)}^{\alpha_n(x_{n+1})} \alpha_n\sqrt{(1-\alpha_n^2)}d\alpha_n = \left.\frac{(1+\alpha_n^2)^{3/2}}{3}\right|_{\alpha_n(x_n)}^{\alpha_n(x_{n+1})} \tag{4.7}$$

$$I_{n,2} = \frac{m_0}{2m_{r,n}}\int_{\alpha_n(x_n)}^{\alpha_n(x_{n+1})} \sqrt{(1-\alpha_n^2)}d\alpha_n = \frac{m_0}{2m_{r,n}}\left.\left(\alpha_n\sqrt{1-\alpha_n^2}+\sin^{-1}(\alpha_n^2)\right)\right|_{\alpha_n(x_n)}^{\alpha_n(x_{n+1})} \tag{4.8}$$

We can then numerically compute:

$$\int_{x_i}^{x_f} k_t(x)dx = \sum_{n=1}^{N-1} \frac{\sqrt{m_{r,n}}E_{\mathrm{G},n}^{3/2}}{\hbar m_0 qF_n}(I_{n,1}+I_{n,2}) \tag{4.9}$$

For the integral $\int k_t^{-1}(x)dx$ we can use the same approach presented above. It follows

$$\int_{x_i}^{x_f} k_t^{-1}(x)dx = \sum_{n=1}^{N-1} \frac{\hbar}{m_0qF_n}\sqrt{\frac{E_{\mathrm{G},n}}{m_{r,n}}}\int_{\alpha_n(x_n)}^{\alpha_n(x_{n+1})} \frac{\alpha_n+\frac{m_0}{2m_{r,n}}}{\sqrt{(1-\alpha_n^2)}}d\alpha_n \tag{4.10}$$

The two terms of the sum are calculated one by one as:

$$I_{n,3} = \int_{\alpha_n(x_n)}^{\alpha_n(x_{n+1})} \frac{\alpha_n}{\sqrt{(1-\alpha_n^2)}}d\alpha_n = \left.\sqrt{1-\alpha_n^2}\right|_{\alpha_n(x_n)}^{\alpha_n(x_{n+1})} \tag{4.11}$$

$$I_{n,4} = \frac{m_0}{2m_{r,n}}\int_{\alpha_n(x_n)}^{\alpha_n(x_{n+1})} \frac{1}{\sqrt{(1-\alpha_n^2)}}d\alpha_n = \frac{m_0}{2m_{r,n}}\left.\sin^{-1}(\alpha_n)\right|_{\alpha_n(x_n)}^{\alpha_n(x_{n+1})} \tag{4.12}$$

The desired path integral is then numerically calculated as :

$$\int_{x_i}^{x_f} k_t^{-1}(x)dx = \sum_{n=1}^{N-1} \frac{\hbar}{m_0qF_n}\sqrt{\frac{E_{\mathrm{G},n}}{m_{r,n}}}\,(I_{n,3}+I_{n,4}) \tag{4.13}$$

Numerical solution of the integrals $\int k dl$ and $\int k^{-1} dl$ for the phonon-assisted non-local BtBT model

The implementation of the non-local phonon assisted BtBT model requires the numerical evaluation of the integral terms included in eq. 3.67 and 3.68. If the simulation domain presents only one semiconductor material the first integral term in eq. 3.68 is a constant multiplied by the tunneling length L. On the other hand, in the presence of a hetero-junction in the channel, the material properties change along the tunneling path.

Following the same discretization approach for the tunneling path presented in fig.4.2, we have that the generic n-th bin of length Δx_n will be associated to one material only. Let us denote $m_{c,n}$ and $m_{v,n}$ its electron and hole effective masses respectively, and $E_{\mathrm{G},n}$ its band gap. As stated above, the trapezoidal method for the numerical integration of the terms $\int_{x_i}^{x_0} k^{-1} dl$ is not a viable solution due to the singularity of k_v and k_c at the beginning and at the end of the tunneling path, respectively. The profile of the Keldysh dispersion relation (eq. 3.69) inside the n-th bin can be written as:

$$k_c(x) = \sqrt{\frac{2m_{c,n}}{\hbar^2}(E_{\mathrm{C}}(x_n) + F_n(x - x_n) - E_{\mathrm{t}})} \quad \text{with } x \in \Delta x_n \tag{4.14}$$

$$k_v(x) = \sqrt{\frac{2m_{v,n}}{\hbar^2}(E_{\mathrm{t}} - E_{\mathrm{V}}(x_n) - F_n(x - x_n))} \quad \text{with } x \in \Delta x_n \tag{4.15}$$

By denoting $x_0 = x_{n0}$ the coordinate of the turning point between the conduction and valence branches of the dispersion relation in the band gap, the integral $\int_{x_0}^{x_f} k_c dx$ can be written as:

$$\int_{x_0}^{x_f} k_c dx = \sum_{n=n_0}^{N-1} \sqrt{\frac{2m_{c,n}}{\hbar^2}(E_{\mathrm{C},n} - E_{\mathrm{t}})} \int_{x_n}^{x_{n+1}} \sqrt{1 + \alpha(x)} dx \tag{4.16}$$

where $E_{\mathrm{C},n} = E_{\mathrm{C}}(x_n)$ and

$$\alpha(x) = \frac{(x - x_n)F_n}{E_{\mathrm{C},n} - E_{\mathrm{t}}} \tag{4.17}$$

$$\frac{d\alpha(x)}{dx} = \frac{F_n}{E_{\mathrm{C},n} - E_{\mathrm{t}}} \tag{4.18}$$

We perform a variable change from x to α obtaining the expression:

$$\int_{x_0}^{x_f} k_c dx = \sum_{n=n_0}^{N-1} \frac{2}{3F_n} \sqrt{\frac{2m_{c,n}}{\hbar^2}} \left[(E_{\mathrm{C},n} - E_{\mathrm{t}})^{3/2} - (E_{\mathrm{C},n} - E_{\mathrm{t}})^{3/2} \right] \tag{4.19}$$

Following the same approach, the integral $\int_{x_0}^{x_f} k_c^{-1} dx$ can be numerically evaluated as:

$$\int_{x_0}^{x_f} k_c^{-1} dx \approx \sum_{n=n_0}^{N-1} \frac{1}{2F_n} \sqrt{\frac{\hbar^2}{2m_{c,n}}} \left[\sqrt{E_{\mathrm{C},n} - E_{\mathrm{t}}} - \sqrt{E_{\mathrm{C},n} - E_{\mathrm{t}}} \right] \tag{4.20}$$

For the solution of the integrals over the valence band branch of the dispersion relation, we take the same approach and approximate the solution as:

$$\int_{x_i}^{x_0} k_v dx \approx \sum_{n=1}^{n_0-1} \frac{2}{3F_n} \sqrt{\frac{2m_{v,n}}{\hbar^2}} \left[(E_{\mathrm{t}} - E_{\mathrm{V},n})^{3/2} - (E_{\mathrm{t}} - E_{\mathrm{V},n})^{3/2} \right] \tag{4.21}$$

$$\int_{x_i}^{x_0} k_v^{-1} dx \approx \sum_{n=1}^{n_0-1} \frac{1}{2F_n} \sqrt{\frac{\hbar^2}{2m_{v,n}}} \left[\sqrt{E_{\mathrm{t}} - E_{\mathrm{V},n}} - \sqrt{E_{\mathrm{t}} - E_{\mathrm{V},n}} \right] \tag{4.22}$$

$$\tag{4.23}$$

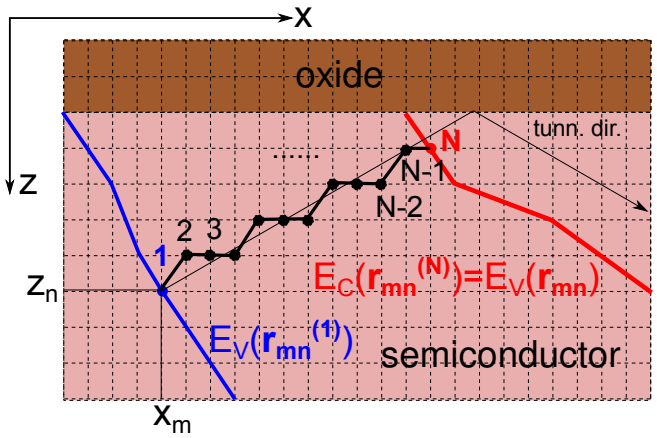

Figure 4.3: Sketch of the algorithm for the determination of the tunneling path on the interpolated discretization mesh of the MSMC model domain.

Choice of the Tunneling Path

The simulation domain in the MSMC simulator is rectangular and discretized in N_x and N_z points along the transport direction $\hat{x}$ and the quantization direction $\hat{z}$, respectively. In each point (x_m, z_n) of the simulation domain the tunneling direction $\hat{l}_{nm}$ is chosen using the opposite of the valence band gradient rule presented in section 3.5. The next step is the identification of the points of the rectangular mesh that belong to the tunneling path. Fig. 4.3 illustrates the algorithm used to determine the tunneling path for the generic starting point $\mathbf{r_{mn}} = (x_m, z_n)$ (blue dot). The gradient of the valence band is approximated using centered finite difference:

$$\nabla E_{\mathrm{V}}(\mathbf{r_{mn}}) \approx \left(\frac{E_{\mathrm{V}}(x_{m+1}, z_n) - E_{\mathrm{V}}(x_{m-1}, z_n)}{x_{m+1} - x_{m-1}}, \frac{E_{\mathrm{V}}(x_m, z_{n+1}) - E_{\mathrm{V}}(x_m, z_{n-1})}{z_{n+1} - z_{n-1}} \right) \tag{4.24}$$

The opposite of the gradient direction is then chosen as tunneling direction. The tunneling direction identifies a piecewise linear curve l passing through the starting point $\mathbf{r_{nm}}$ with direction determined by the opposite of the valence band gradient in $\mathbf{r_{nm}}$ that is specularly reflected when the path crosses a semiconductor/oxide interface. The selection of the discretization points for the tunneling path is an iterative operation: starting from the point $\mathbf{r}_{\mathbf{mn}}^{(\mathbf{1})}$, at the generic l-th step we select the point $\mathbf{r}_{\mathbf{mn}}^{(\mathbf{l+1})}$ between the first neighbors of the point $\mathbf{r}_{\mathbf{mn}}^{(\mathbf{l})}$ that minimize the distance from the piecewise linear curve l. This operation is iterated until the first point where $E_{\mathrm{C}}(\mathbf{r}) \leq E_{\mathrm{V}}(\mathbf{r_{mn}})$ if found and considered as the ending point of the tunneling path $\mathbf{r}_{\mathbf{mn}}^{(\mathbf{N})}$. With this procedure a certain error in energy and a little overestimation of the tunneling path length is expected. With a sufficiently fine mesh ($\Delta x \approx \Delta z < 1$Å) this error becomes negligible, but at this levels of refinement if the mesh is the same used for the numerical solution of the Poisson's problem the computational burden becomes unbearable considering devices with deca-nanometer channel length. To overcome this limitation, for the computation of the tunneling rate, a separate much refined mesh with respect to the one used for the modeling of the transport is implemented. The user can specify the extension of the refined mesh, that can cover a part or the whole simulation domain representing the device and at each iteration the potential and therefore the band profiles are linearly interpolated on the new refined mesh using the coarser one on which the numerical solution of the Poisson problem is carried out. In the following all the BtBT currents, if not otherwise specified, have been computed with the MSMC using a refined mesh with square elements and $\Delta x = \Delta z = 0.5$Å.

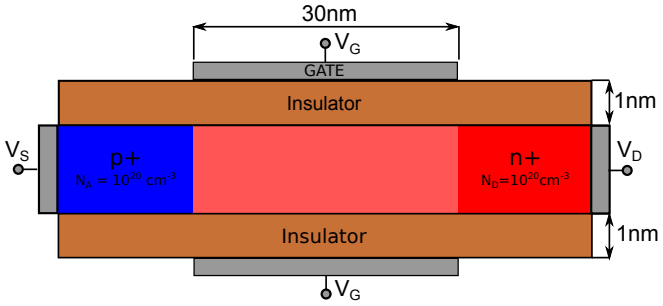

Figure 4.4: Sketch of an idealized double gate TFET template structure $N_{\mathrm{A,s}} = N_{\mathrm{D,d}} = 10^{20}\mathrm{cm}^{-3}$, EOT = 1nm, L_{G}=30nm and gate metal work-function E_{wf}=4.05eV, T_{sc}=10nm. Abrupt doping profiles. The device was simulated as a homo-junction and as a hetero-junction with Si or Ge materials in the source, in the channel and in the drain. The hetero-junction, if present, is located at the source-channel interface.

Validation of the BtBT model implementation

At this stage the implemented BtBT models are essentially the same of the TCAD software Synopsys Sentaurus SDevice. Therefore the implementation of eqs. 3.58 and 3.67 has been validated by direct comparison with TCAD on a variety of tunnel-diodes and TFETs. In section 4.1.4 we will discuss in detail how the model has been extended to account for vertical quantization effects.

Fig. 4.5 shows a representative result, namely: the MSMC and the TCAD simulation of the trans-characteristic of the device in fig. 4.4 considered both as a Si or Ge homo-junction Double Gate TFET or as a hetero-junction DG TFET with Ge source and Si channel and drain. The simulation results for the homo-junction as well as of the hetero-junction devices are obtained using the same set of defaults parameters for the non-local phonon-assisted BtBT model specified in [7]. The computation of the BtBT generation rate and current by the MSMC has been carried out using the same frozen potential profile provided by Sentaurus Device simulation of the same structure. As expected the difference between the MSMC and TCAD results is extremely small.

With the intent of maintaining a link with the Hurkx and Kane models, the non-local direct and phonon-assisted models implemented in Sentaurus Device are calibrated using the A, B and the band gap parameters (eq. 3.40 and 3.61 for the direct and the phonon-assisted models, respectively). To ease the comparison with Sentaurus, we have done the same choice in our implementation; namely: the user specifies the A, B parameters and the Band Gap (together with $\varepsilon_{\mathrm{op}}$ for the Phonon Assisted model and the ratio between m_c and m_v) for each material. These values allow us to derive the effective masses for the computation of the generation rates by inverting the eqs. 3.40 and 3.61 for the direct and the phonon-assisted models respectively. This approach makes the comparison with Sentaurus easy, but since A and B depend on the band gap, hence on the amount of band gap narrowing (BGN), when the band gap changes from the nominal value, e.g. because of high doping, the value of A and B must be recomputed. In Sentaurus as well as in the MSMC, this operation is not automatic. The user must specify the correct parameters given the band gap narrowing. This operation can be done only if the doping is abrupt and it is possible to identify regions with constant doping, constant BGN and therefore constant BtBT parameters.

4.1.2 Hole BtBT generation rate and hole transport

In order to account for the non-negligible contribution of holes generated by the BtBT process to the space charge density, a solver for the hole transport has been implemented. In n-type

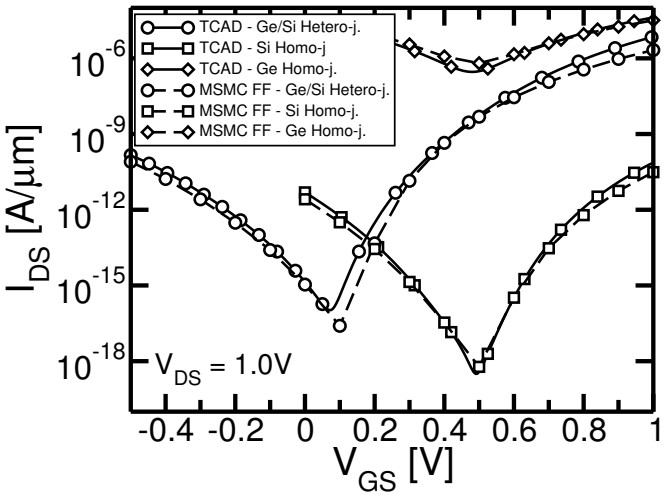

Figure 4.5: Simulated trans-characteristic of the template structure in fig. 4.4 considered as a Si or a Ge homo-junction DG device or as a hetero-junction double gate TFET with Ge source and Si channel and drain. Simulations have been carried out with the MSMC model in frozen field configuration using the potential profile provided by the TCAD [7] and with the TCAD software Sentaurus SDevice using the same set of parameters for the non-local phonon assisted BtBT model. $A = 4 \cdot 10^{14}\mathrm{cm}^{-3}\mathrm{s}^{-1}$ and $B = 1.9 \cdot 10^{7}\mathrm{V/cm}$ for the Silicon regions and $A = 9.1 \cdot 10^{16}\mathrm{cm}^{-3}\mathrm{s}^{-1}$ and $B = 4.9 \cdot 10^{6}\mathrm{V/cm}$ for the Germanium region.

TFETs holes travel mostly in the low field source region so that a simple drift diffusion approach is adequate to the purpose. Accordingly, holes are not treated like single particles (as electrons in the MSMC) but as a continuous charge distribution with concentration $p(x,z)$ derived from the hole generation rate $G_{\mathrm{bbt,h}}(x,z)$. The following equations have been implemented employing the Scharfetter-Gummel discretization scheme [14]:

$$\nabla \cdot \mathbf{J}_p = qG_{\mathrm{bbt,h}}(x,z) \tag{4.25}$$

$$\mathbf{J}_p(x,z) = -qp(x,z)\mu_p(x,z)\nabla E_{\mathrm{V}} - qD_p(x,z)\nabla p \tag{4.26}$$

where all symbols take their usual meaning. Hole velocity saturation is included in the hole mobility model as [15]:

$$\mu_p(x,z) = \frac{\mu_{p,0}}{\left[1 + \left(\frac{\mu_{p,0}|\mathbf{F}_{\mathrm{el}}|}{v_{\mathrm{sat}}}\right)^{1/\beta}\right]^{\beta}} \tag{4.27}$$

.

Considering the double gate TFET in fig. 4.4 implemented as Si homo-junction the profile of the hole density along the transport direction at the vertical center of the channel in the source/channel junction is reported in fig. 4.6. Reference results from Sentaurus Device (black curve) agree fairly well with those of our MSMC model with (dashed red curve) and without (solid red curve) activating the velocity saturation. The agreement between Sentaurus and the MSMC simulations is more than satisfactory. Residual discrepancies are due to the fact that Sentaurus and MSMC model have slightly different electrostatic potential profiles due to vertical quantization that is not included in Sentaurus calculations.

4.1.3 BtBT particle generation in the MC gas

Once the generation rate has been computed in the whole domain, the simulator generates a fixed number of electrons N_e at each time step Δt. The position of these particles in the

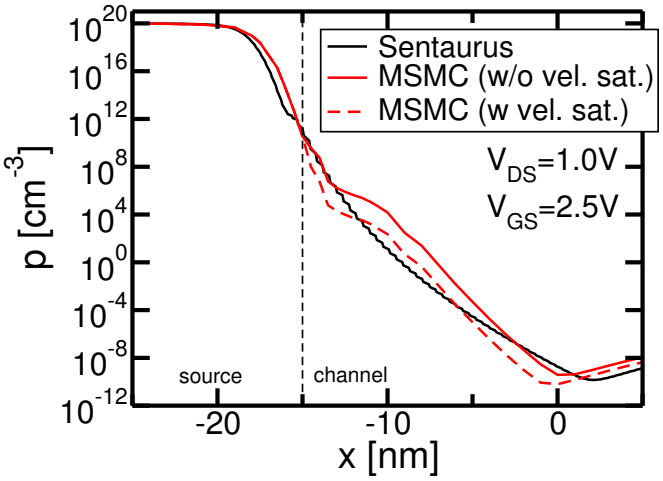

Figure 4.6: Hole concentration in the middle of the semiconductor film across the source/channel junction of the device in fig. 4.4.

simulation domain is chosen randomly with probability distribution

$$P(x) = \frac{\int G_{\mathrm{bbt,e}}(x,z)dz}{\iint G_{\mathrm{bbt,e}}(x,z)dxdz} \tag{4.28}$$

Given a semiconductor thickness T_{sc}, the generated particles must have a statistical weight

$$w = \frac{W\Delta t}{N_e} \iint_0^{T_{\mathrm{sc}}} G_{\mathrm{bbt,e}}(x,z)dxdz \tag{4.29}$$

to obtain the correct value for the current per unit of width

$$\frac{I_{\mathrm{DS}}}{W} = q \iint G_{\mathrm{bbt,e}}(x,z)dxdz \tag{4.30}$$

Following this approach the user has direct control on the number of BtBT-generated particles N_e (whose weight depends on $G_{\mathrm{bbt,e}}(x,z)$), hence some degree of control on the statistical robustness of the simulation. In fact the particles flow in the channel, and grant an accurate statistical estimation of the electron density n and of the drain current I_{DS}. Fig. 4.7, reports the current estimated using eq. 4.30 (solid line) and the spatial average of the electron current along the channel from the point of maximum BtBT generation to the beginning of the drain extension on a large number of time steps Δt chosen after the initial time transient has expired. Fig. 4.7 shows that the two drain current estimators are essentially noise-free and in very good agreement even in the subthreshold region. This is an obvious but critical result to ensure the usability of statistical MC techniques for the simulation of low currents devices such as the TFETs. We emphasize that in order to obtain a good resilience of the estimator to statistical noise it is sufficient to impose an adequately high number of generated particle N_e (i.e $N_e \approx 50$/fs for a Si TFET). All these particles contributes to the I_{DS} estimator, in fact in conventional MOSFET case even if the total number of particles in the simulation domain is large, most of them are located in the source and in the drain region; only very few of them overcome the source barrier and are eventually found moving in the channel. Therefore, for a given current and a given total number of particles, the statistical noise in the MOSFET under subthreshold bias will be significantly larger than in the TFET case. Alternatively for the same degree of accuracy of the estimator a much smaller number of particle and computational burden is required in the TFET case than in the MOSFET one.

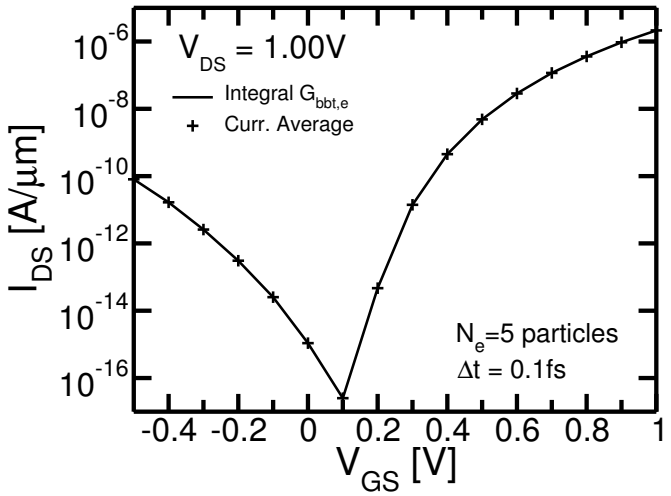

Figure 4.7: Simulated trans-characteristic for the same idealized double gate hetero-junction TFET reported in fig. 4.4. The results reported with the solid line are estimated using eq. 4.30 while the results reported with crosses are estimated averaging the current along the channel for 15000 Δt.

4.1.4 Quantum corrections

As stated in the previous chapter the implemented non-local models apply to a gas of free (3D) gas of carriers and does not take into account quantization. Accordingly, particles should be generated as free electrons with almost zero kinetic energy[1], and the z coordinate should be set randomly following the statistical distribution:

$$P_x(z) = \frac{G_{\mathrm{bbt,e}}(x,z)}{\int_0^{T_{\mathrm{sc}}} G_{\mathrm{bbt,e}}(x,z)dz} \tag{4.31}$$

The total energy of the generated particle will be $E_{3D} = E_{\mathrm{C}}(x,z)$. This is for instance the algorithm used in a 3D free carrier gas MC simulator such as [17]. However, quantization modulates the effective band gap and changes the tunneling path in inversion layers and Ultra Thin Body devices. Carrier confinement is naturally accounted for in MSMC simulators where the carriers belong to subbands and, at given x, their position distribution in z is given by the solution of the one dimensional Schrödinger equation (SE) along z [13]. Thus, a procedure to map the 3D generation rate into subbands is necessary. To this purpose, the carriers generated at position x according to the probability density $P(x)$ (eq. 4.28) are associated to one of the subbands obtained solving the SE at the nearest x node. This methodology, was originally proposed in [1] to map the free electrons in the source and drain of conventional MOSFETs into the quantized electron states in the channel. In our case we search for the i-th subband that minimizes the difference between the eigenvalue energy $\varepsilon_{\mathrm{C,i}}(x)$ and $E_{3D}(x,z)$.

Strictly speaking this procedure implies a violation of the energy conservation principle as schematically sketched in fig. 4.8. The E_{C} profile is drawn along the quantization direction $\hat{z}$, with the corresponding eigenvalues $\varepsilon_{\mathrm{C,i}}$ in the generic slice with x coordinate x^*. In this slice a particle is generated in the point (x^*, z^*) where z^* is randomly chosen using the procedure presented in sec. 4.1.3 and this point is characterized by an energy $E^*_{3D} = E_{\mathrm{C}}(x^*, z^*)$. This energy E_{3D} is generic and can be significantly different for the value of the actual subband

[1]The kinetic energy along the tunneling direction should be null, whereas different wave-vectors normal to the tunneling path contribute to the BtBT rate, but the smallest k values (i.e. the low kinetic energy ones) are the most effective [16]

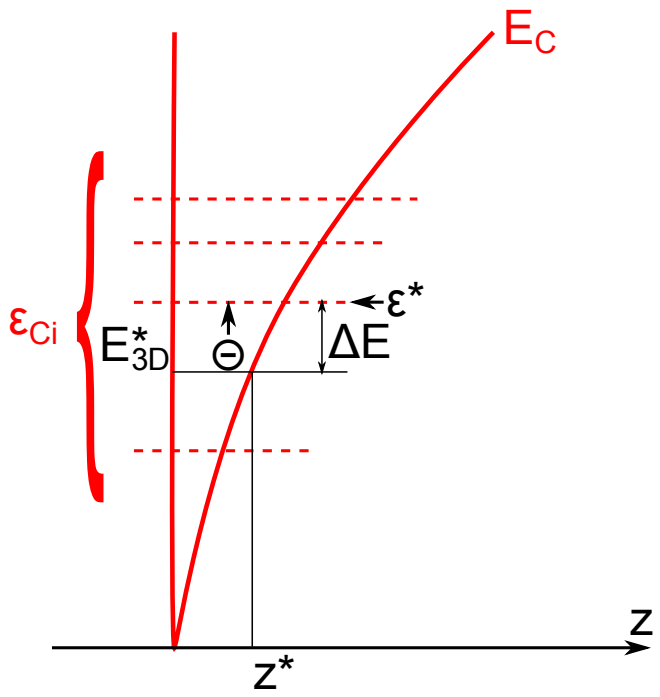

Figure 4.8: Sketch of the procedure used to determine the subband where, for each Δt, the BtBT particle must be generated in the MSMC gas and of the corresponding energy error ΔE.

energies. At this point the selected subband where the particle is generated is the one nearest to E_{3D} that is $\varepsilon^*_{\mathrm{C},}$ in the sketch and this correspond to an energy error ΔE.

To reduce the energy error and, at the same time, account for the effect of quantization on the actual energy gap, we modify the band profiles as shown in the fig. 4.9. For the conduction band at all points where $E_{\mathrm{C}}(x,z) < \varepsilon_{\mathrm{C},0}(x)$ we set $E_{\mathrm{C}}(x,z) = \varepsilon_{\mathrm{C},0}(x)$ where $\varepsilon_{\mathrm{C},0}(x)$ is the lowest subband energy at the position x. A similar procedure is followed for the valence band via the solution of the 1D SE for holes at each node of the grid along x using the EMA Hamiltonian and the DoS effective masses. The highest valence band $\varepsilon_{\mathrm{V},0}(x)$ is selected and used to limit $E_{\mathrm{V}}(x,z)$. The correction method has been implemented allowing the user to specify the quantization mass for the valence band. In Silicon the dominant BtBT transitions are those starting from the light hole valley, and therefore as quantization mass the DoS effective mass for the light hole has been used.

At this time the MSMC simulator can handle only a single set of parameters corresponding to the transition between a single pair of valence and conduction band valleys. An improvement of the next version of the simulator will be the possibility to specify different sets of parameters, for different transitions between different couples of valence and conduction valleys, that will be computed on the same conduction and valence band profile iteration after iteration. Nevertheless in this work to evaluate the effect of the BtBT transitions between different valence and conduction valleys we have launched separated simulations with specified the corresponding BtBT parameter sets. This is possible because for the TFET devices, as reported in chapter 5, at the V_{GS} and V_{DS} potentials of interest, the currents found are low ($< 10\mu\mathrm{A}/\mu\mathrm{m}$) and therefore their effect on the electrostatic and on the band profiles can be neglected. Consequently the total BtBT current can be computed as sum of the currents corresponding to all the possible transitions between the valence and conduction band valleys.

A clear advantage of this procedure, hereafter denoted *Quantum Corrected Tunneling Profile (QCTP)*, is that it drastically reduces the energy conservation error associated to the mapping

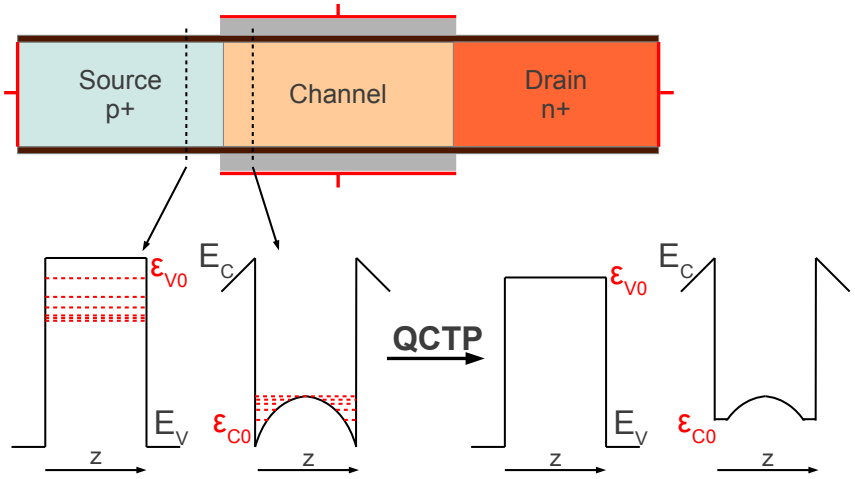

Figure 4.9: Sketch of the QCTP procedure, see text for the full description

between free (3D) and bound (2D) particles, as can be seen in fig. 4.10 reporting the average energy error in the particle generation obtained in the simulation of a InAs SOI TFET with different T_{sc} using or the QCTP.

The QCTP accounts for the increase of the energy gap induced by quantization hence for the impact of the reduced density of states on the tunneling rates. Such an effect is presently neglected by commercial TCAD models even when the density gradient correction is used, whereas it is naturally accounted for by full quantum models, with no possibility to switch it off. Therefore the proposed QCTP correction appears as a useful tool to assess the relative importance of band gap correction on the tunneling rates.

Fig. 4.11 compares MSMC results with and without QCTP activated with those reported in [9]. As throughly described in the previous chapter, the Vandenberghe's model [10] is a 2D Full Quantum Model for phonon assisted BtBT that provides the most accurate results for UTB devices. The small difference between the dynamic non-local model in [7] and the MSMC w/o QCTP is due to the effect of residual size- and bias-induced quantization of the electron energy levels, that, differently from the TCAD, is taken into account by MSMC simulation and that is not completely negligible with a semiconductor thickness of 10nm. Due to this effect, the electrostatic potential profile in the MSMC differs from the one calculated by Sentaurus and, consequently, the calculated BtBT generation rate is slightly different. In the case with QCTP, instead, a remarkable agreement with the quantum 2D model is observed, considering that our model implements carrier quantization as a correction to a free electron BtBT model. Besides the mutual agreement between models we observe that quantization is responsible for a remarkable reduction of the tunneling current, consistently with the results in [9].

4.2 Summary

In this chapter we have presented the implementation of the blocks required to simulate TFETs in the framework of a Multi Subband Monte Carlo transport model. BtBT is modeled as a generation rate that is computed using the dynamic non-local models presented in chapter 3 both for direct and phonon-assisted tunneling. The transport of the holes generated by BtBT is modeled using a Drift Diffusion solver. A quantum correction scheme is then proposed to take into account the effect of the size- and bias-induced quantization present in UTB TFETs on the BtBT since the implemented non-local models hold considering a gas of free electrons. The results from the MSMC with the correction scheme are compared with the results produced by

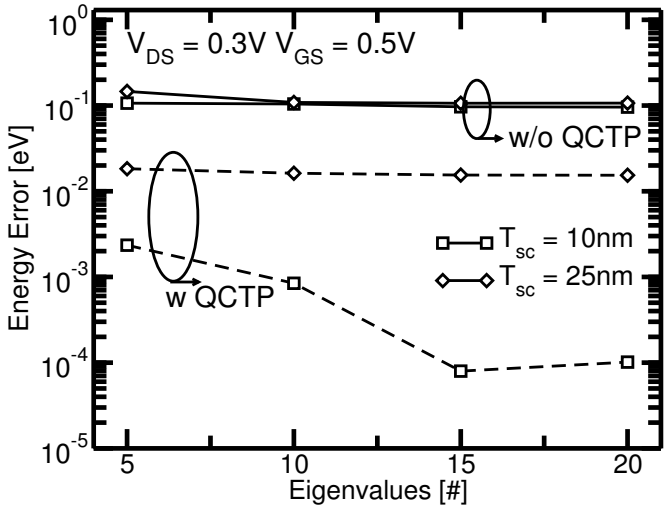

Figure 4.10: Energy conservation error, averaged over 1000 generated particles, due to 3D to 2D mapping of the generated electrons as a function of the number of subbands in the MSMC, with or without QCTP. The simulation has been performed on a SOI TFET with InAs channel. The semiconductor thickness is T_{sc}=10nm or T_{sc}=25nm. The drain doping is $N_{\mathrm{D}=}5\cdot10^{19}\mathrm{cm}^{-3}$. EOT=1.45nm for the device with T_{sc}=25nm. EOT=0.7 for the device with T_{sc}=10nm. The metal gate work-function is E_{wf}=4.97eV.

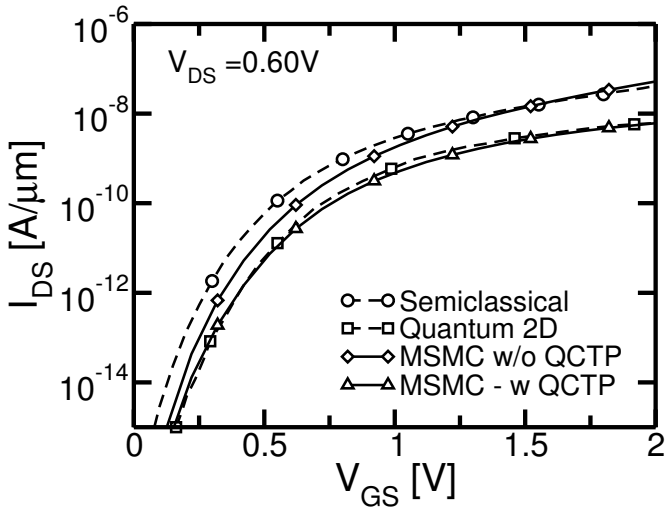

Figure 4.11: Transfer characteristic of the device considered in [9] (double gate SOI with T_{sc}=10nm and EOT=3nm) compared to the results of our MSMC model with and without the Quantum Corrected Tunneling Profile QCTP.

the Full Quantum model in [10, 9] with a very satisfying agreement. In the next chapter a set of case studies will be presented where the MSMC model is used to evaluate the performance of homo-junction and hetero-junction devices implemented with SiGe alloys or III-V, with the aim of evaluating the effect of the variation of particular geometrical parameters like the gate extension or the semiconductor thickness on the device performances or to find an optimized alignment between the hetero-junction, the doping junction and gate edges.

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Chapter 5

Analysis of a study of SiGe and III-V compound semiconductor TFETs

In this chapter we present case studies of the use of the MSMC transport model for TFET to evaluate the dependence of the performance of specific Semiconductor on Insulator (ScOI) TFETs on design parameters such as semiconductor thickness, EOT or channel length. The choice is restricted to Double or Single Gate ScOI architectures because, as explained in sec. 1.2 subthreshold slope is improved in presence of a strong coupling between the gate and the channel. Such a good electrostatic control cannot be achieved in bulk structures but only in ScOI or DG structures. The impact of technology boosters such as strain and new materials is also evaluated.

The first case study concerns the effect of vertical scaling on a Silicon planar homo-junction FD-SOI TFET. The model calibration was carried out by means of comparison to the measurements of tunneling diodes reported in [1] and Sentaurus Device simulations of the same tunneling junction. The advantage of using the data of [1] is that arsenic and boron doping density profiles have been reported in [1] and used in the definition of the tunneling junction simulation domain. [1] reports the value for the equivalent band gap E_G extracted from C-V measurements. The calibration has then been validated with a further comparison between the experiments reported in [2] and the MSMC simulations of a template structure similar to the measured one. The parameters A and B have been extracted from the comparison between measurements and simulation, that have been carried out with the nominal value of band gap in silicon $E_G = 1.12$eV. These BtBT parameter values thus obtained refer to effective masses and phonon deformation potential values (eq. 3.61) that are considerably different from those found in literature (Kao et al. [3]).

The second case study deals with the choice of the design parameters for an unstrained $Si/Si_{0.5}Ge_{0.5}$ hetero-junction planar Double Gate (DG) TFET and has been carried out using the calibration provided by Kao et al. [3] and considering the Band Gap Narrowing effect through the Jain-Roulston model [4] as described in the previous chapter.

The third case study regards the analysis of an idealized homo-junction implemented in InAs or $In_{0.53}Ga_{0.47}As$ and resembling the 3D MESA device proposed by Dewey in [5]. The analysis concerns the scaling of the semiconductor thickness, of the channel length, the effect of the gate/channel overlap and the effect of source doping density.

In the fourth and last case study, we investigate a complex $In_{0.53}Ga_{0.47}As/In_{0.7}Ga_{0.3}As/In_{0.53}Ga_{0.47}As$ hetero-junction device derived from the one proposed in [5]. The analysis is carried out considering the Band Gap Narrowing and the effect of strain induced on the $In_{0.7}Ga_{0.3}As$ layer by the relaxed $In_{0.53}Ga_{0.47}As$ layers in the source and in the channel and drain. The effect of the thickness of the $In_{0.7}Ga_{0.3}As$ film was investigated to identify the possible existence of an optimum length of the low band gap region.

In all the case studies, except for the first, BGN effect has been taken into account in simulation not only for what concerns the band profiles, but also for the calculation of the BtBT parameters A and B that significantly depends on E_G.

5.1 Planar homo-junction silicon TFET device

5.1.1 Calibration of the phonon assisted model for Silicon

To calibrate the model for Si, we have taken as a reference the measurements of a n+/p tunnel diode (denominated Q5) in the work of Solomon et al. [1]. The measured I_D/V_D curve and also the doping profile along the device are provided in [1]. These have been used to simulate the diode with Sentaurus Device using the dynamic non-local phonon-assisted BtBT model. The parameters A and B (denoted `Apath1` and `Bpath1` in Sentaurus Device) have been adjusted to find the best fit to the measurements. The tunneling diode has been simulated also considering BGN using the Bennett-Wilson model [6] and using the BtBT model parameters (`Apath1`, `Bpath1` and `Ppath1`) reported in [3] or computed using the band gap and effective masses extracted from the 30 band k·p band structure calculation [7, 8]. In tab. 5.1 the parameters of

Table 5.1: Non-local phonon-assisted BtBT model parameters. First row reports those extracted by numerical fit of Sentaurus SDevice simulations without considering BGN (E_G = 1.12eV) the to the measurements in [1]; second row: those provided in [3]; third row: those computed using the effective masses and the band gap extracted by 30 bands k·p calculations using the methodology explained in chapter 3.

	`Apath1` $[10^{14}\text{cm}^{-3}s{-}1]$	`Bpath11` [MV/cm]	ε_{op} [meV]	E_G [eV]
Numerical fit	3.7	12.6	30	1.12
Kao [3]	32.9	23.8	19	0.93
30 bands k·p	25.6	17.8	19	0.93

the non-local phonon-assisted BtBT use for the simulation of the tunneling diode are reported.

Fig. 5.1 compares the measurements and the simulation results. If we examine the measurements at low V_n and the simulations obtained with `Apath1` and `Bpath1` computed using the masses and band gaps from the literature or the k·p model, we observe that the latter systematically predict a steeper characteristic than the measurements. To understand if measurements are affected by additional injection mechanisms we repeated the simulation including the dynamic non-local Trap Assisted Tunnel (TAT) model [9] with the default parameters for the dynamic non-local TAT model. A complete description of the Sentaurus Device TAT model is beyond the objectives of this thesis work and can be found in [9]. The results (see inset), show that the inclusion of the TAT mechanism yields an $I_n - V_n$ curve that, especially at low voltage, is closer to the measurements. These results justify the difference that we see in tab. 5.1 between the BtBT parameters obtained through numerical fit case and those reported in [3] and those computed with the 30 bands k·p model. In the first case we have that A and B account for three different mechanisms: the BGN (since the band gap was fixed at $E_G = 1.12$eV), the BtBT and the TAT. The phonon energy was fixed to 30meV, which is the default value used in Sentaurus Device. In the latter two cases, on the contrary, the BGN is taken into account using the band gap energy specified in [1] ($E_G = 0.93$eV) extracted from C-V measurements carried out on the diode, and only the BtBT transition is considered whereas TAT is accounted with a dedicated non-local model.

These results provided a first calibrated set of model parameters for predictive simulations. At the same time, they show that even in very simple experiments on essentially one dimensional junctions the tunneling current may be affected by additional parasitic generation mechanisms as TAT. The presence of traps yields a degraded slope of the $I_n - V_n$ curves which may jeopardize the ability to achieve less than 60mV/dec slope at 300K in complete FET devices. This effect will be extensively discussed in chapter 6, dealing with experiments on SiGe based devices.

Comparison between MSMC simulation results and experimental Si TFETs

To further validate the parameter set obtained with the numerical fit of tunnel junctions $I_n - V_n$ curves, we have considered as a reference also the measurements reported in [2] regarding a planar FD-SOI TFET with HfO_2/SiO_2 gate stack and with EOT=2.2nm, T_{Si}=20nm, L_G=400nm, $N_{D,d} = 10^{18}\text{cm}^{-3}$, $N_{A,s} = 10^{20}\text{cm}^{-3}$. We have then simulated the FD-SOI template structure reported in fig. 5.2-a that is a good approximation of the one proposed in [2]. The device parameters are the same of the experimental samples except for $L_G = 100$nm. In fact, knowing that L_G has a weak effect on the TFET performance when $L_G >$30nm [10], the gate length is kept shorter to reduce the computation burden.

The simulations have been carried out using the MSMC model and the parameter set obtained by numerical fit of Solomon's measurements without BGN ($E_G = 1.12$eV). Fig. 5.2-b compares the measurements (circles) with the MSMC simulation results (squares) and demonstrates reasonable mutual agreement, suggesting that the MSMC is a fairly accurate model and

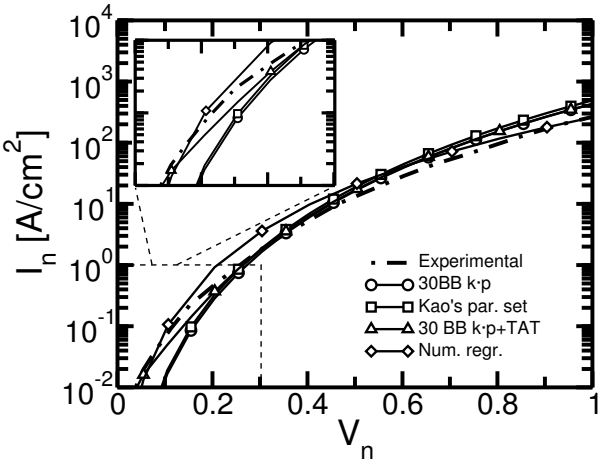

Figure 5.1: Comparison between the measurements (dot-dashed line) of the n+/p tunnel diode Q5 in [1] and Sentaurus Device simulation using the BtBT model parameters obtained by numerical fit (diamonds) or those provided in [3] (squares) or calculated using the effective masses and band gap extracted from 30 bands k·p model [7, 8]. The latter simulation has been launched including (triangles) or not (circles) the dynamic non-local TAT model [9]. The inset zooms on the low-voltage/low-current region.

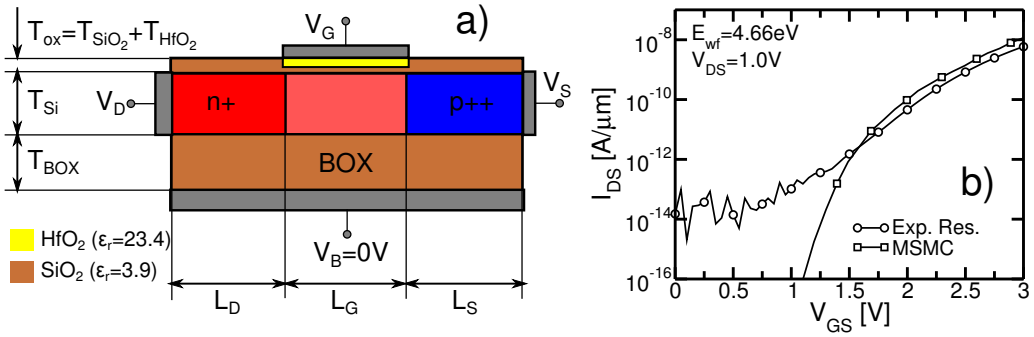

Figure 5.2: Plot a) sketch of the considered FD-SOI structure. The device is similar to the one with HfO_2/SiO_2 gate stack (EOT=2.2nm) presented in fig. 3 (red curve) of [2]. Plot b) compares the simulation results with the measurements in [2].

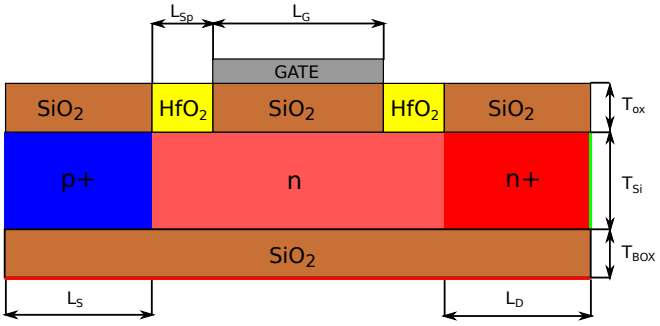

Figure 5.3: Sketch of the template Silicon FD-SOI structure. T_{ox}=1.1nm, L_{sp}=2nm, T_{BOX}=45nm, L_G=30nm, L_S=L_D=60nm, gate metal work function E_{wf}=4.1eV. $N_{A,s}$=10^{20}cm^{-3}, $N_{D,d}$=10^{17}cm^{-3}. ε_{HfO_2}=25ε_0, ε_{SiO_2}=3.9ε_0. Abrupt doping profiles have been assumed.

Table 5.2: Subthreshold swing at V_{GS}=0.0V for the device of fig. 5.4-a

T_{Si} [nm]	EOT [nm]	SS [mV/dec]
3	0.7	21
5	0.9	23
10	1.1	44

the calibration against the Solomon's measurements is reasonably robust against changes in the device structures. We note that also in this case the current at low V_{GS} exhibits a pronounced tail, likely due to additional leakage mechanisms such as TAT and instrument noise.

5.1.2 Vertical Scaling of a UTB FD-SOI TFET with HfO_2 spacers

Fig. 5.3 sketches the Silicon TFET structure that will be analyzed in this case study. It is a UTB FD-SOI TFET with SiO_2 gate oxide, a gate underlap and HfO_2 spacers to increase gate-junction coupling as proposed in [11].

We observe in fig. 5.4-a that, since small T_{Si} corresponds to increased effective gap (due to carrier confinement and energy quantization), the advantages in terms of electrostatic control are dominant and the drain current is improved for decreasing T_{Si} values even when considering subband splitting and the QCTP. Simulations with and without the QCTP indicate that carrier confinement reduces the current by almost a factor of 10. The T_{Si} reduction improves the electrostatic control and reduces the SS as reported in table 5.2.

The simulated on-state drain current for the Silicon TFET in fig. 5.4 is very low for the device to be of practical usefulness ($\approx$nA/μm at V_{GS} = V_{DS} = 1V). This result is consistent with both TCAD and quantum simulation [12, 13] and with experiments as well [14]. Larger currents are obtained in [15] but with V_{DS} = V_{GS} = 3V instead of 1V as in fig. 5.4. Such a large V_{DS} = V_{GS} however is of limited practical usefulness because conventional CMOS transistors offer much better performance at lower V_{DS} than the TFET. TFETs seems to have a chance to become competitive only at very small $V_{DS} \leq$ 0.3V as will be shown in the following of this dissertation. Since I_{DS} is very low, the contribution of the generated carriers to the total charge in the device is very small. Consequently the potential profile with and without BtBT generation is essentially the same and the BtBT current could be calculated as a post processing of an essentially purely electrostatic simulation considering only the cold carriers in the device. A non trivial consequence of this observation is also that as far as the current is small, carrier scattering in the channel will not modulate the potential profile and the tunneling barrier. Consequently it is expected that far from equilibrium transport in the channel may not be so

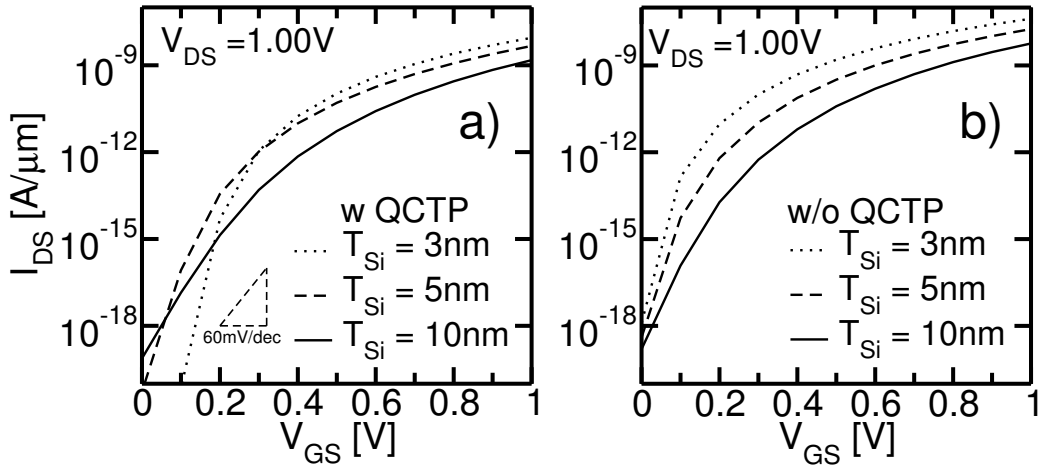

Figure 5.4: Simulated trans-characteristic of the device in fig. 5.3 considering different oxide thickness T_{Si} and EOT (1.1nm, 0.9nm and 0.7 for T_{Si}=10nm, 5nm, 3nm) either activating (plot a) or disabling (plot b) the QCTP correction. Results accounting for QCTP show the expected reduction of the current and a shift of the threshold voltage with respect to the results of simulations without QCTP.

relevant for the purpose of estimating TFET currents as it is for MOSFETs [16, 17].

5.2 Optimization of a $Si_{0.5}Ge_{0.5}$/Si double-gate hetero-junction TFET

Fig. 5.5 sketches the template device investigated in this second case study. It is a $Si_{0.5}Ge_{0.5}$/Si DG hetero-junction TFET with an aggressive vertical scaling (EOT=0.7nm and T_{sc}=5nm). Different positions of the $Si_{0.5}Ge_{0.5}$/Si abrupt hetero-junction (x_{SiGe}) and of the abrupt junction between the acceptor doped source and the intrinsic channel (x_{Dop}) have been explored. Abrupt junctions have been considered because they are the most favorable to achieve high field at the tunneling junction, hence high BtBT rates.

$Si_{0.5}Ge_{0.5}$ has been considered since a Ge molar fraction x=0.5 is high enough to provide a significant reduction of the band gap (E_{G}=0.92eV without BGN) while its manufacturability and co-integration in state-of-the-art CMOS technology have been proven [18, 19]. If not otherwise specified, the metal work-function E_{wf} has been set in order to have $I_{\mathrm{off}} = 1\mathrm{pA}/\mu\mathrm{m}$ at $V_{\mathrm{DS}} = 0.5\mathrm{V}$ and $V_{\mathrm{GS}} = 0.0\mathrm{V}$. The source doping level ($N_{\mathrm{A,s}} = 10^{20}\mathrm{cm}^{-3}$) corresponds to limited source degeneracy as it is necessary to avoid excessively large drain turn-on voltages [20, 21], degraded output characteristics and degraded SS. The dielectric constant for $Si_{0.5}Ge_{0.5}$ is obtained by linear interpolation of the Si and Ge values, therefore $\varepsilon_{\mathrm{Si_{0.5}Ge_{0.5}}} = 14.2\varepsilon_0$.

5.2.1 Model Calibration

If not otherwise specified all the simulations have been carried out using the MSMC with the QCTP. This is a mandatory ingredient for the simulation of such a thin SiGe layer. The parameters for indirect BtBT have been taken from [3] and verified with the 30 bands k·p model [7, 8] (tab. 5.3) as explained in section 3.7. The source region is heavily doped and significant BGN is expected. The Bennett-Wilson BGN model [6] has been adopted, with the silicon parameters, and consistently the actual band gap of $Si_{0.5}Ge_{0.5}$ is estimated to be 0.81eV for the $Si_{0.5}Ge_{0.5}$ source region at the acceptor doping level of $10^{20}\mathrm{cm}^{-3}$ and 1.01eV for Si at the

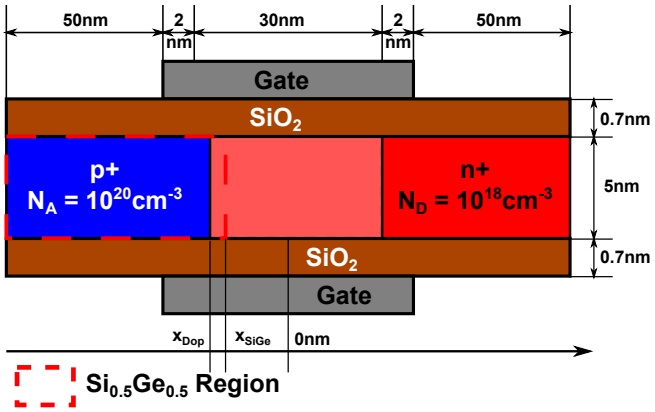

Figure 5.5: Sketch of the $Si_{0.5}Ge_{0.5}$/Si hetero-junction double-gate device. x_{Dop} is the coordinate of the doping boundary between source and channel. x_{SiGe} is the coordinate of the hetero-junction between the $Si_{0.5}Ge_{0.5}$ region and the Si region. The x_{Dop} and x_{SiGe} coordinates are referred to the zero at the center of the gate. The doping profiles are assumed abrupt. The transport direction and the wafer plane are [100]/(001). No strain is considered.

Table 5.3: Band to Band Tunneling model parameters for indirect band gap materials considered in this work accounting for (2^{nd} and 3^{rd} column) and neglecting (4^{th} and 5^{th} column) the significant Band Gap Narrowing effect in the source region.

Parameters	$Si_{0.5}Ge_{0.5}$ BGN	Si BGN	$Si_{0.5}Ge_{0.5}$	Si
Apath [$10^{15}\mathrm{cm}^{-3}\mathrm{s}^{-1}$]	2.81	3.91	2.27	3.29
Bpath [MV/cm]	12.9	20.5	15.5	23.8
ε_{op} [meV]	13.8	19	13.8	19
E_{G} [eV]	0.81	1.01	0.92	1.12
χ [eV]	4.025	4.05	4.025	4.05

same doping level. Since `Apath1` and `Bpath1` parameters are band gap dependent (eqs. 3.61), they have been recomputed to the values reported in tab. 5.3. In Si as well as in $Si_{0.5}Ge_{0.5}$ the direct band gap is more than 1eV higher than the indirect one. Thus only phonon assisted BtBT has been considered in these simulations.

5.2.2 Simulation Results

As first step we simulated homo-junction versions of the device in fig. 5.5 entirely made in Silicon and in $Si_{0.5}Ge_{0.5}$. Then the hetero-junction structure has been simulated changing the values of x_{Dop} (in order to move the junction from the left to the right of the gate edge) and changing the misalignment $\Delta x_{\mathrm{SiGe}} = x_{\mathrm{SiGe}} - x_{\mathrm{Dop}}$ from negative to positive values. Fig. 5.6 reports the SS at $I_{\mathrm{DS}} = I_{\mathrm{off}} = 1\mathrm{pA}/\mu\mathrm{m}$ and the I_{on} at V_{GS}=0.5V for different pairs (x_{Dop},Δx_{SiGe}). The relative doping and hetero-junction positions that optimize SS and I_{on} are those when the source junction and the gate edge are aligned (x_{Dop}=-17nm) and the hetero-junction is slightly (1nm) at the right of the source junction (x_{SiGe}=-16nm).

To evaluate the effect of material choice and of size- and bias-induced quantization in the different materials we have compared the optimal hetero-junction to the homo-junction devices by means of both MSMC and Sentaurus Device (fig. 5.7).

As already mentioned the SDevice results neglect the impact of size- and bias-induced quantization on the BtBT rates. For the hetero-junction TFET SDevice predicts better electrostatic control resulting in higher currents and lower SS with respect to the SiGe homo-junction device.

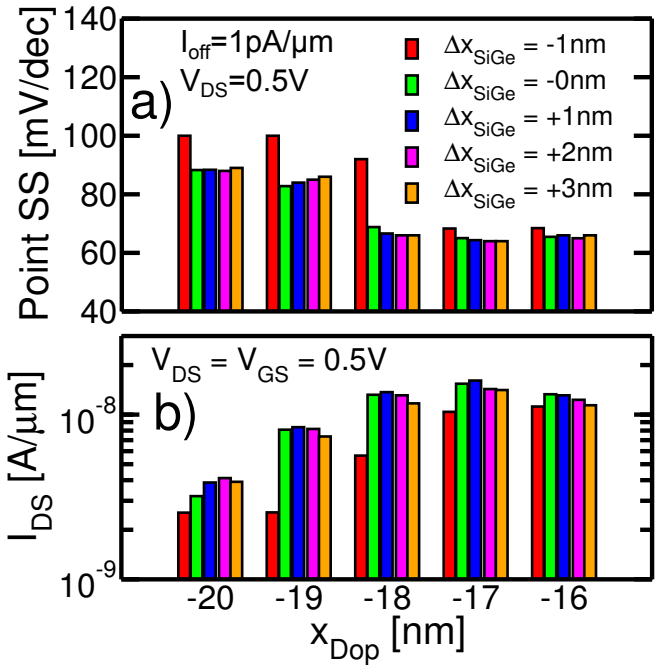

Figure 5.6: Bar chart summarizing the performance of the device in fig. 5.5 for different pairs $(x_{\mathrm{Dop}}, x_{\mathrm{SiGe}})$. Plot a) reports the point SS at I_{DS}=I_{off}=1pA/μm. Plot b) reports the I_{on}=I_{DS}@V_{GS}=0.5V.

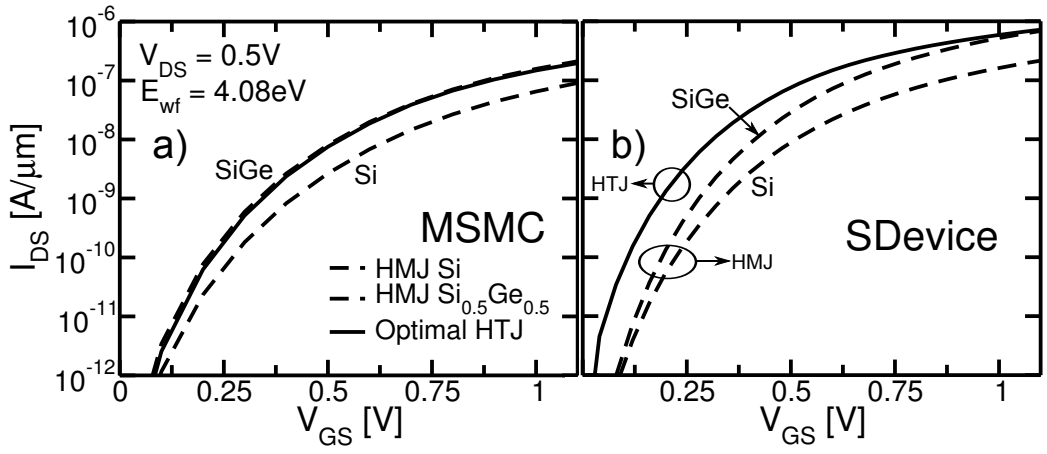

Figure 5.7: Trans-characteristics of the optimal SiGe/Si hetero-junction (HTJ) device (x_{Dop}=-17nm, x_{SiGe}=-16nm) and of the Si and SiGe homo-junction (HMJ) devices simulated using the MSMC (plot a) and the Sentaurus tools (plot b).

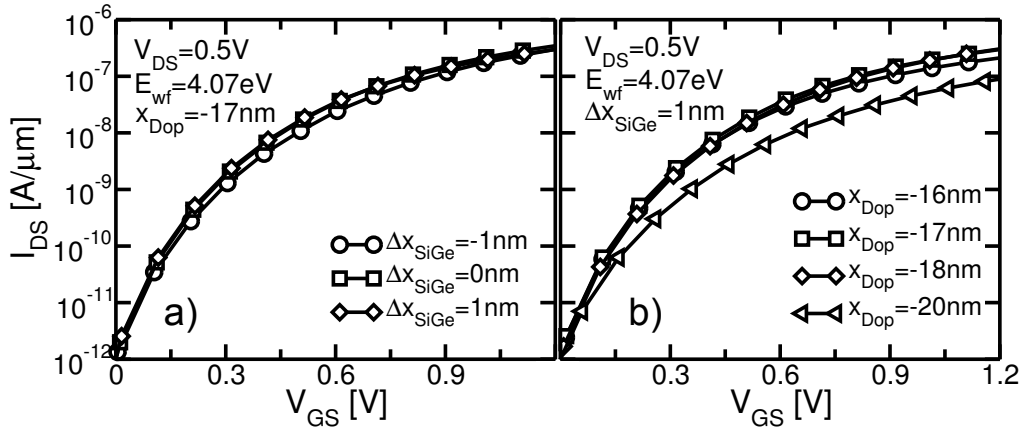

Figure 5.8: Trans-characteristics of the device of fig. 5.5 for different Δx_{SiGe} at fixed x_{Dop}=-17nm (plot a) and for different x_{Dop} at fixed Δx_{SiGe} (plot b).

On the other hand when we include quantization effects via our MSMC model with QCTP the effect of vertical component of electric field on BtBT is reduced due to the limitation imposed to the valence and to the conduction bands (sec. 4.1.4); this results in a lower BtBT generation rate spatially located toward the center of the semiconductor layer rather than near the semiconductor/oxide interfaces.

The hetero-junction and the SiGe homo-junction trans-characteristics, as computed by MSMC, are quite quite similar, whereas the SDevice simulations report a higher current and steeper SS for the hetero-junction device. This can be explained considering that the quantization changes the position and length of the tunneling path, as shown also in fig. 5.16. Since the SiGe homo-junction and the hetero-junction trans-characteristics are similar in the MSMC simulations, it follows that holes and electrons are generated in the source that is characterized by the same material ($Si_{0.5}Ge_{0.5}$) in both the structures. This implies also that the shortest tunneling path that gives the most significant contribution to the BtBT current, when quantization is taken into account, is moved toward the source in both the structures, with a similar electrostatic.

To evaluate the sensitivity of the BtBT current to the change of x_{Dop} and x_{SiGe} we report in fig. 5.8 the trans-characteristics at either different Δx_{SiGe} having the source junction aligned with the gate edge (fig. 5.8-a) or at different x_{Dop} when the optimum misalignment Δx_{SiGe}=1nm is chosen (fig. 5.8-b). In the former case (plot a) the curves are very similar to each other except at $V_{\mathrm{GS}} \approx 0.5$V where the devices with Δx_{SiGe}=0nm and 1nm show a higher current than the one for Δx_{SiGe}=-1nm. This can be explained by the fact that at low V_{GS} BtBT takes place mostly in the low E_{G} region (SiGe), and for the optimum alignment case ($\Delta x_{\mathrm{SiGe}} \geq 0$nm) the BtBT moves from the Si channel region to the SiGe region when V_{GS} is increased. Consequently the current is increased, and therefore the SS improved. On the other hand x_{Dop} changes have a limited effect on the curves when the I_{off} is fixed, unless the source junction is largely misaligned from the gate edge (plot b). The best I_{on} ($\approx$10nA/μm) and SS (64mV/dec), correspond to an $I_{\mathrm{on}}/I_{\mathrm{off}}$ ratio of $\approx 10^4$ and it is obtained when the source junction and the gate edge are aligned (x_{Dop}=-17nm). The Si and $Si_{0.5}Ge_{0.5}$ homo-junction device simulations (fig. 5.7) are consistent with the measurements in [14] where passing from pure Si to a $Si_{0.7}Ge_{0.3}$ alloy the homo-junction device I_{on} increases approximately by an order of magnitude.

Fig. 5.9 reports the generation rate and the band profiles along the channel considering x_{Dop} ranging from -20nm and -16nm and Δx_{SiGe} from -1nm and 3nm. Consistently with the results reported in 5.6 the sensitivity of the generation rate profile (and therefore of the I_{on}) on x_{Dop} is not significant when x_{Dop} is near the gate edge coordinate at the source ($x = -17$nm).

On the other hand, for $x_{\mathrm{Dop}} = 20$nm we see a reduction of almost a order of magnitude of the maximum generation rate that is consistent with the reduction of a order of magnitude in the current. When the junction is under the gate ($x_{\mathrm{Dop}} > -17$nm) the maximum of the hole generation rate is found near the coordinate of the gate edge. For $x_{\mathrm{Dop}} < -17$nm instead, the maximum is found near the junction doping. The dependence on the hetero-junction coordinate x_{SiGe} is almost negligible, whereas only for $x_{\mathrm{Dop}} = -20$nm to larger Δx_{SiGe} corresponds a knee of the hole generation rate profile at the right of the junction coordinate x_{Dop}, that nevertheless does not contribute significantly to the total current.

5.3 Analysis of a III-V compound planar homo-junction TFET

In this case study we analyze a homo-junction TFET with the channel formed by different III-V compound semiconductors such as $In_{0.53}Ga_{0.47}As$ or InAs and two different vertical architectures (T_{sc}=25nm, EOT=1.45nm and T_{sc}=10nm EOT=0.7nm). Fig. 5.11 sketches the simulation template that captures the key features of the homo-junction device proposed in [5] including the published doping profiles, and a T_{sc} large enough to emulate the behavior of the large MESA structure reported in [5]. The gate material work-function E_{wf} has been adjusted to improve the threshold voltage match between our simulations and experiments. An ideal tunnel junction free of gap states has been assumed. The MSMC simulation are self-consistent. Many scattering mechanisms may be relevant in III-V devices [5, 22]. We follow here a simplified approach similar to [23] and include elastic and inelastic isotropic phonons mimicking the effect of polar optical phonons. A more accurate setup including local and remote polar phonons as well as surface roughness may be possible but would require a more refined model calibration. However, since the I_{on} of this device remains low compared to MOSFETs in spite of the reduced band gap of $In_{0.53}Ga_{0.47}As$, we expect the scattering to have a modest effect on the drain current similarly to the previous observations on Si and SiGe TFETs. Fig. 5.10 compares the current the long channel (L_{ch}=100nm) homo-junction device of fig. 5.11 when scattering is included or not in the transport calculation. The relative error ε between the two curve is defined as:

$$\varepsilon = \left| \frac{I_{\mathrm{DS,ball}} - I_{\mathrm{DS,scatt}}}{I_{\mathrm{DS,scatt}}} \right| \tag{5.1}$$

As shown in fig. 5.10 ε is not significant with a peak value of almost 15% that seems to be more related to noise in the current estimation than to the effective difference in the electrostatics. In fact as V_{GS} increases the current and total number of scattering events becomes larger a stronger effect of scattering on the total current should be expected. At high V_{GS} where the difference between the curves should be higher ε is reduced to few percentage points, confirming the fact that the effect of scattering can be neglected.

5.3.1 Vertical scaling effect on InGaAs and InAs TFET devices

Simulations have been carried out using the MSMC with the non-local direct BtBT model calibrated using the band gaps and the effective masses provided in [24, 25, 26]. These parameters are reported in tab. 5.4 with the corresponding direct BtBT parameters `Apath1` and `Bpath1` computed considering only the transition between the light hole valence band valley and the Γ conduction band valley. This choice is motivated by the fact that the much larger heavy hole effective mass which causes a severe reduction of the probability for the transition from the heavy hole valley. The transition probability can be thus considered essentially negligible. The BGN has not been considered in this first set of simulations. The BGN issue is examined in more detail in section 5.3.2.

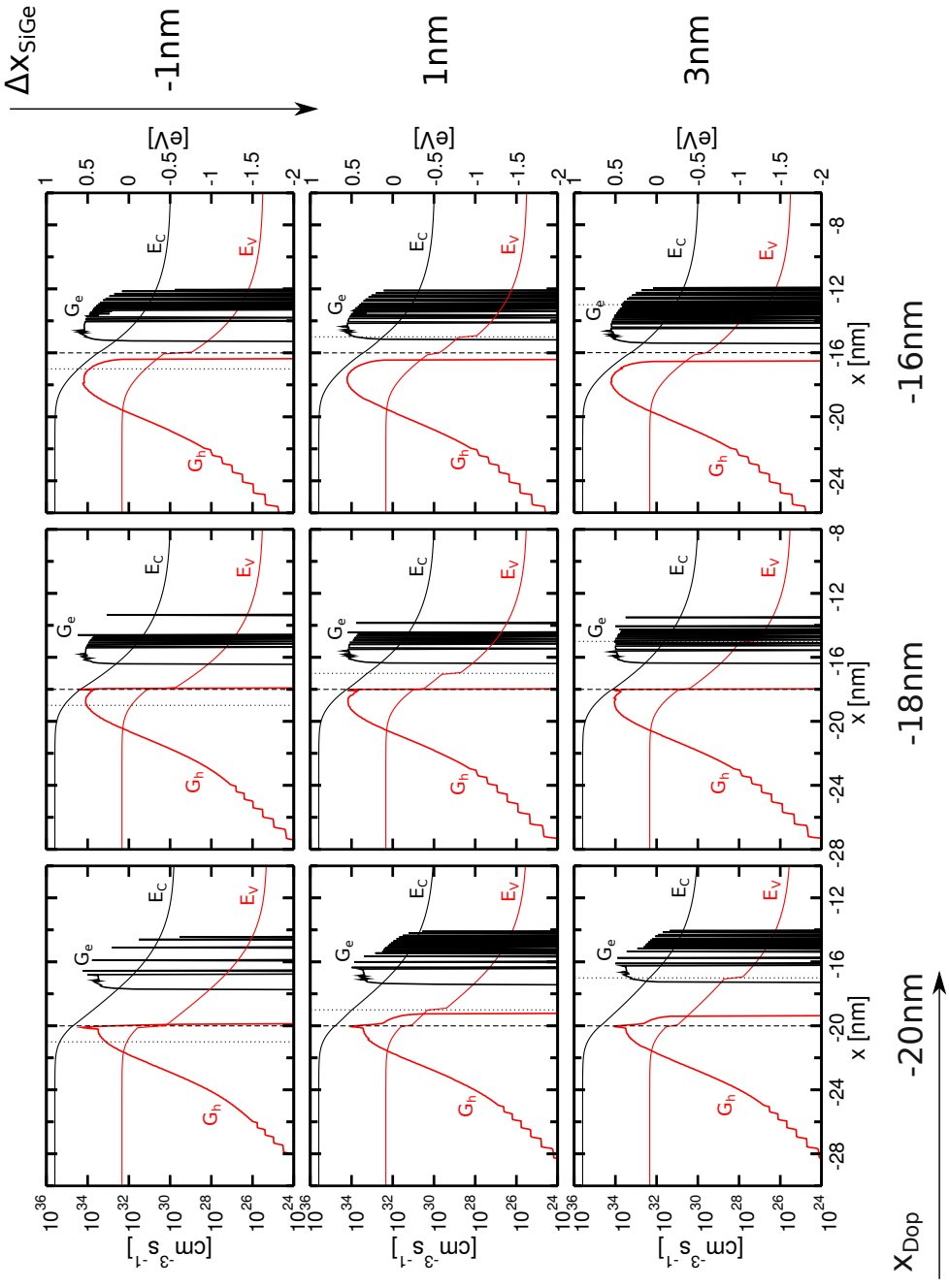

Figure 5.9: Profiles along the transport direction of the conduction and valence bands and of the electron and hole BtBT generation rate at the channel center. The profiles concern devices with different x_{Dop} and Δx_{SiGe} ranging from -20nm to -16nm and from -1nm to 3nm, respectively and biased with $V_{\mathrm{DS}} = 0.5V$ and $V_{\mathrm{GS}} - V_{\mathrm{GS,off}} = 0.5V$, where $V_{\mathrm{GS,off}}$ is the V_{GS} at which $I_{\mathrm{DS}} = 1\mathrm{pA}/\mu\mathrm{m}$. For all the considered x_{Dop} and x_{SiGe} combinations the gate edge at the source side is located at the coordinate $x = -17\mathrm{nm}$. The coordinates of the doping junction and of the hetero-junction coordinate are marked by the dashed and dotted vertical lines, respectively.

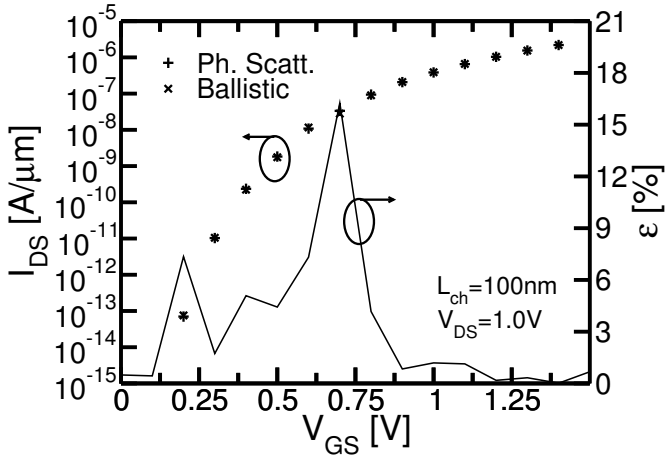

Figure 5.10: Comparison of the simulated current for the TFET of fig. 5.11 with $L_G = 100$nm if the transport is ballistic (×) or not (+).

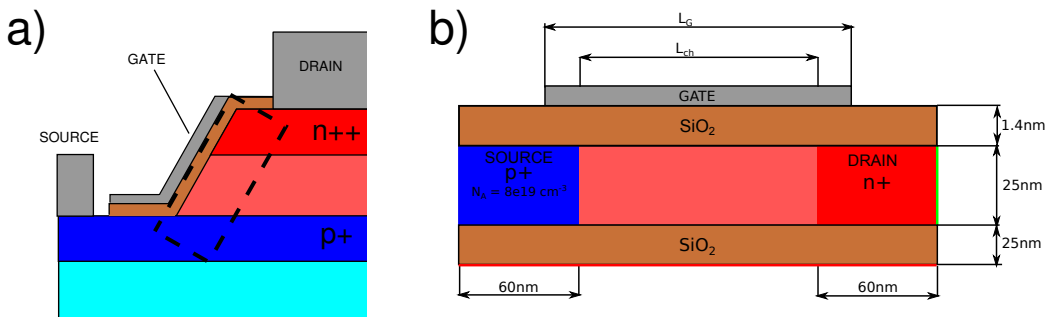

Figure 5.11: Sketch of the cross section of the MESA $In_{0.53}Ga_{0.47}As$ homo-junction TFET proposed in [5] (plot a). We considered the area of the cross section included in the rectangle and we derivated a planar ScOI device sketched in plot b). L_G is the gate length while L_{ch} is the channel length. Abrupt doping profile have been assumed. The L_G is considered variable to study the effect of gate extension on the device performances.

Table 5.4: Parameters used in the direct BtBT model for the simulation of the device in fig. 5.11 implemented in $In_{0.53}Ga_{0.47}As$ and InAs

Material	`Apath1` $[10^{20}cm^{-3}s^{-1}]$	`Bpath1` [MV/cm]	E_G [eV]	m_r $[m_0]$	$m_{v,lh}$ $[m_0]$	$m_{v,hh}$ $[m_0]$	$m_{c,\Gamma}$ $[m_0]$
$In_{0.53}Ga_{0.47}As$	1.73	5.5	0.73	0.023	0.052	0.457	0.043
InAs	1.86	1.36	0.35	0.013	0.026	0.41	0.026

Table 5.5: Subthreshold slope at $V_{\rm GS}$=0V for the device of fig. 5.11 and fig. 5.12.

Material	T_s [nm]	EOT [nm]	SS [mV/dec]	$N_{\rm D,d}$ [cm^{-3}]	$E_{\rm wf}$ [eV]
InAs	10	0.7	20	4.84	10^{18}
InAs	25	1.45	42	4.93	10^{18}
InGaAs	10	0.7	45	4.42	$5 \cdot 10^{19}$
InGaAs	25	1.45	67	4.29	$5 \cdot 10^{19}$

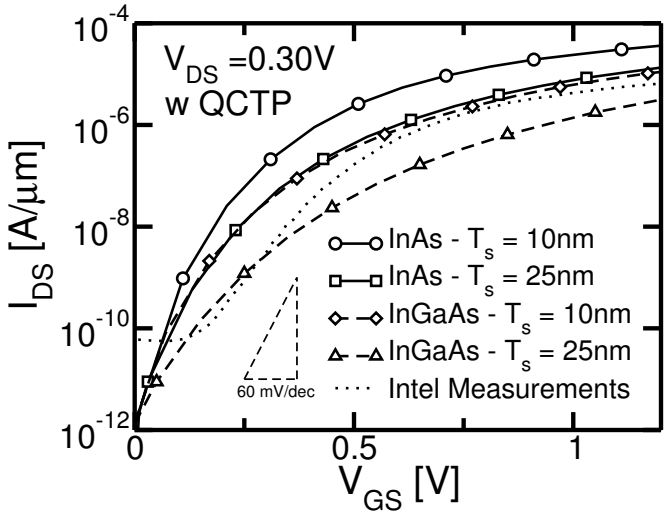

Figure 5.12: Simulated trans-characteristic of the template device in fig. 5.11 considering $In_{0.53}Ga_{0.47}As$ and InAs channels. The $E_{\rm wf}$ has been adjusted to achieve $I_{\rm off}$ = 1pA/μm. The values are reported in tab. 5.5. The devices with 10nm thickness have EOT=0.7nm, whereas the ones with 25nm thickness have EOT=1.45nm as in [5]. Experiments from [5] are also shown (dotted line). The source doping is $N_{\rm A,s} = 8{\cdot}10^{19}$cm^{-3}. The drain doping is $N_{\rm D,d} = 5{\cdot}10^{19}$cm^{-3} for the $In_{0.53}Ga_{0.47}As$ devices and 10^{18}cm^{-3} for the InAs devices.

Fig. 5.12 reports the trans-characteristics of the simulated $In_{0.53}Ga_{0.47}As$ and InAs devices. The source doping density for both InGaAs and InAs devices is $N_{\rm A,s} = 8 \cdot 10^{19}$cm^{-3}. The doping of the drain region is equal to $N_{\rm D,d} = 5 \cdot 10^{19}$cm^{-3} for the InGaAs devices, whereas it is set to $N_{\rm D,d} = 1 \cdot 10^{18}$cm^{-3} for the InAs ones, in order to suppress the ambipolar leakage current that stems from the reduced band gap (as shown in the I-V curve of fig. 5.13). The dotted line reports the measurements in [5], and it is qualitatively matched by the results of the simulated $In_{0.53}Ga_{0.47}As$ device with $T_{\rm sc}$=25nm. Although quantitative discrepancies remain which can be up to a factor of 10x at high $V_{\rm GS}$ this is not surprising given the structural difference between the idealized device in fig. 5.11 and the real and partly unknown measured transistor. The figure also shows that reducing the semiconductor film thickness to 10nm and the EOT to 0.7nm (diamond symbols) significantly increases the current drive and reduces the SS (tab. 5.5).

The static current is further improved if the InGaAs channel material is replaced with InAs (circle and square symbols). The source doping is kept at a moderately high value $N_{\rm A,s} = 8 \cdot 10^{19}$cm^{-3}. It should be noticed that in fig. 5.12 we observe currents as high as 100μA/μm, but only for $V_{\rm GS}$ higher than 1V. Nevertheless on-currents above 1μA/μm at $V_{\rm DS} = V_{\rm GS} = 0.5$V seems to be possible with these material. For $V_{\rm GS} = V_{\rm DS} = 0.3$V that is a reasonable voltage at which the TFET becomes interesting as a CMOS replacement for Ultra-Low-Power applications, the on-current is not higher than 0.5μA/μm. That is due to the fact that the steep subthreshold slope is obtained only close to $V_{\rm GS} = 0$V, whereas the average slope is much lower. These results

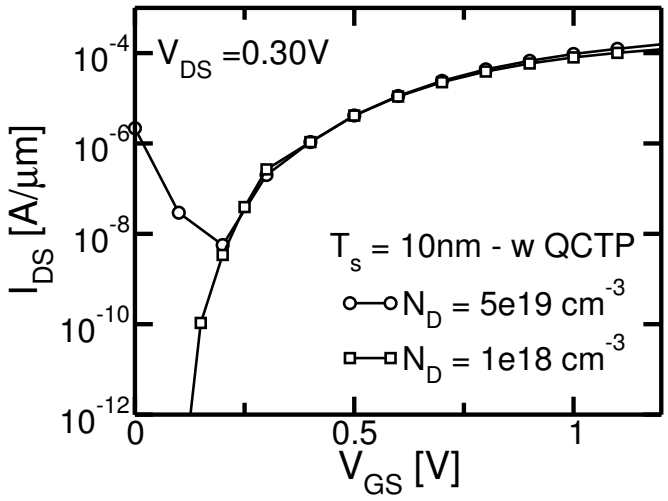

Figure 5.13: Simulated trans-characteristic of the template device of fig. 5.11 considering InAs as the channel material and a semiconductor thickness T_{sc}=10nm. The device with drain doping $N_{\mathrm{D,d}} = 5 \cdot 10^{19}\mathrm{cm}^{-3}$ (circles) exhibits a stronger ambipolar behavior with respect to the device with $N_{\mathrm{D,d}} = 10^{18}\mathrm{cm}^{-3}$ (squares). An increased drain resistance may correspond to this reduced drain doping but this effect is not taken into account here because, given the low current density, the parasitic voltage drop is likely to be negligible.

Table 5.6: Parameters for the Jain Roulston BGN model for $In_{0.53}Ga_{0.47}As$[27]

	n-type semiconductor	p-type semiconductor
C_1 [meV]	4.8	11.3
C_2 [meV]	0	0.23
C_3 [meV]	3.2	9.2
C_4 [meV]	0	3.4

suggest that even for deeply scaled geometries and advanced low band gap materials, relaxed planar homo-junction TFETs may hardly reach I_{on} specs of interest for mainstream CMOS applications.

5.3.2 Band Gap narrowing effect on the I-V curves

In the following, the BGN effect will be examined using the Jain Roulston Model [4] with parameters for $In_{0.53}Ga_{0.47}As$ taken from [27]. In [27] the parameters of the Jain Roulston model are calculated considering separately the BGN narrowing contribution given by the lowering of the conduction band edge ΔE_{C} and by the increase of the valence band edge ΔE_{V}. Hence $\Delta E_{\mathrm{G}} = \Delta E_{\mathrm{V}} + \Delta E_{\mathrm{C}}$ with:

$$\Delta E_{\mathrm{C}} = C_1\left(\frac{N}{10^{18}}\right)^{1/3} + C_2\left(\frac{N}{10^{18}}\right)^{1/2} \tag{5.2}$$

$$\Delta E_{\mathrm{V}} = C_3\left(\frac{N}{10^{18}}\right)^{1/4} + C_4\left(\frac{N}{10^{18}}\right)^{1/2} \tag{5.3}$$

where N is the doping density (acceptor or donor). The parameters $C_1, \ldots, C_4$ are different for acceptor or donor doped $In_{0.53}Ga_{0.47}As$ and are reported in tab. 5.6. The electron affinity of

Table 5.7: Parameters of the dynamic non-local direct BtBT model for the different regions of the $In_{0.53}Ga_{0.47}As$ device in fig. 5.11

	Source $[N_{A,s} = 8 \cdot 10^{19}cm^{-3}]$	Channel [Intrinsic]	Drain $[N_{D,d} = 4 \cdot 10^{19}cm^{-3}]$
m_r $[m_0]$	0.023	0.023	0.023
Nominal			
E_G [eV]	0.73	0.73	0.73
χ [eV]	4.51	4.51	4.51
`Apath1` $[10^{20}cm^{-3}s^{-1}]$	1.73	1.73	1.73
`Bpath1` [MV/cm]	5.52	5.52	5.52
with BGN			
E_G [eV]	0.61	0.73	0.54
χ [eV]	4.55	4.51	4.72
`Apath1` $[10^{20}cm^{-3}s^{-1}]$	1.91	1.73	2.02
`Bpath1` [MV/cm]	4.16	5.52	3.46

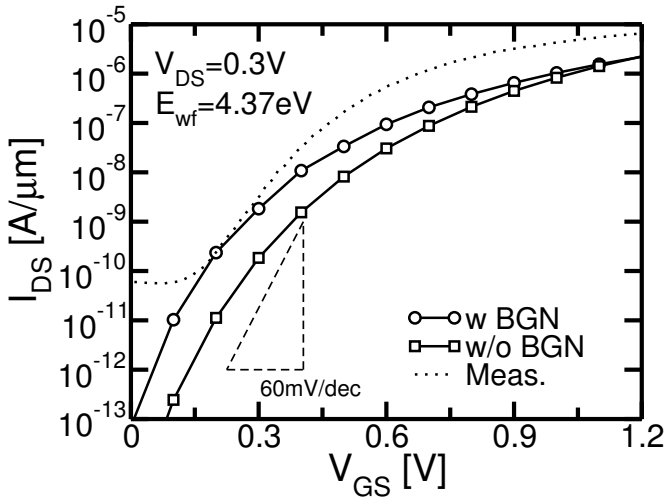

Figure 5.14: Simulated trans-characteristic of the template device of fig. 5.11 considering a semiconductor thickness $T_{sc} = 25nm$, including (circles) or not (squares) the BGN effect.

the doped $In_{0.53}Ga_{0.47}As$ can be written as:

$$\chi(N) = \chi(N = 0) + \Delta E_C(N) \tag{5.4}$$

where again N is the doping density.

Tab. 5.7 reports the E_G and the reduced mass m_r in the different parts of the channel considering the actual doping density therein.

Fig. 5.14 compares the trans-characteristics of the homo-junction $In_{0.53}Ga_{0.47}As$ device with T_{sc}=25nm, when the BGN is considered (circles) and when it is not (squares). The measurements from [5] are also reported as a reference. The results show that the band gap reduction which occurs mostly in the source increases the current at low V_{GS} thus causing a reduction of the SS from 72mV/dec (without BGN) to 62mV/dec (with BGN). Such effect has not been shown before to our knowledge.

Given the need to design the source with a relatively high doping level for high field in the BtBT region, it appears that BGN effects are quantitatively important and cannot be neglected as instead it is most often the case in the literature.

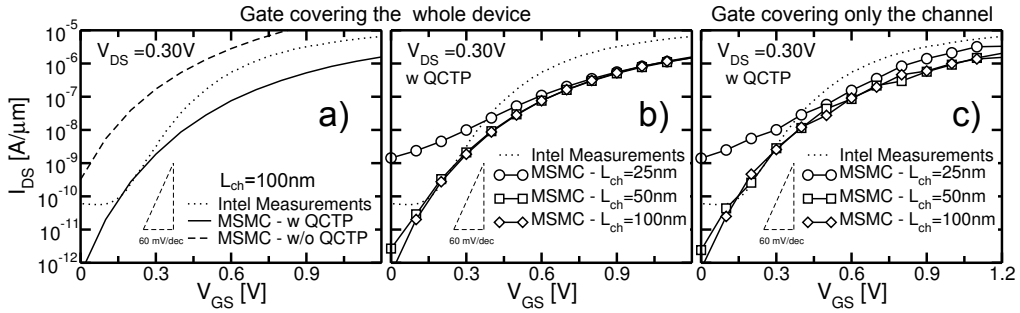

Figure 5.15: Simulated trans-characteristics of the $In_{0.53}Ga_{0.47}As$ device with the gate covering the whole device from source to drain (plot a and b) and the gate covering only the channel (plot c) together with the measurements from [5]. Plot a) reports the trans-characteristic computed by means of the MSMC model with L_{ch}=100nm using or not the QCTP, while plot b) and c) reports the trans-characteristics considering different values of L_{ch}. All devices have a gate metal work-function E_{wf}=4.27eV.

5.3.3 Gate extension and channel length effect on the $In_{0.53}Ga_{0.47}As$ device

In the following we investigate the dependence of the $In_{0.53}Ga_{0.47}As$ device characteristics on the gate/channel overlap and the channel length. BGN is accounted for using the Jain Roulston model as specified in the previous section. Fig. 5.15 reports the trans-characteristics for the device in fig. 5.11 with and without QCTP (plot a) and with L_{ch}=100nm and the gate that covers completely the device. This is the geometry of the prototypical devices in [5]. Figs. 5.15-b and 5.15-c report the trans-characteristics obtained with different channel length (L_{ch}=100nm, 50nm and 25nm) considering again the gate that covers the whole device (plot b) or only the channel, plus a 2nm overlap on the source and on the drain side (plot c).

The current is essentially independent of channel length (as expected for TFET devices [10]) unless L_{ch} becomes extremely short ($L_{ch} \approx T_{sc}$ in our case). At that stage we observe that a reduction of the channel length contributes to make the barrier thinner and to increase the ambipolarity. Restricting the gate extension only to the channel does not have any significant effect on the static trans-characteristic provided a small overlap remains, as it is the case here. However, such a reduction is expected to be highly beneficial to a reduced gate/drain capacitance which is known to cause undesiderable anomalies in the switching behavior of TFETs.

Consistently with what has been shown in the previous sections of this chapter, fig. 5.15-a shows that the current decreases by more than an order of magnitude if vertical quantization is accounted for.

In planar nTFET devices the BtBT generation profile is peaked in a very small region. Fig. 5.16 shows the cross-section of the device of fig. 5.11 near the source junction and highlights the position of the maximum generation rate for electrons and holes computed with and without QCTP. With QCTP the average vertical component of the band profile gradient is reduced, moving the maximum of the generation rates for both electrons and holes from the oxide/semiconductor interface toward the center of the channel (fig. 5.16-a). This implies longer tunneling paths and, thus, a significant reduction of the BtBT probability. The effect is early visible in fig. 5.16-b and 5.16-c, where we report the generation rate profile for electrons and holes along the x direction and at the z coordinate at which they attain the maximum value.

These plots explain the low sensitivity of the trans-characteristic in fig. 5.15-b and 5.15-c to the gate extension: indeed the latter controls mostly the vertical field in the device changing

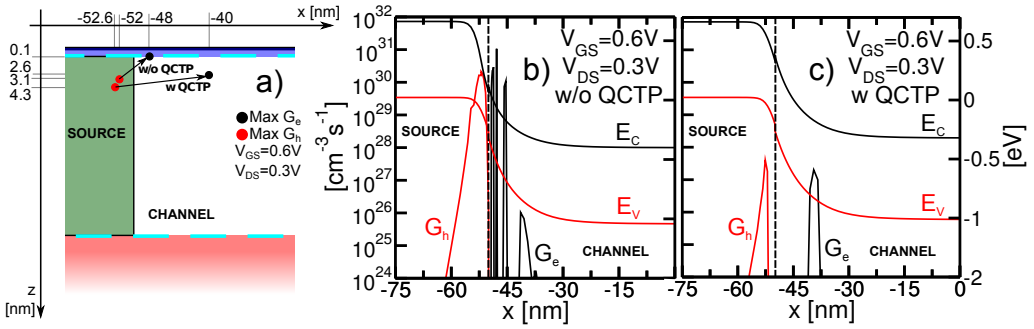

Figure 5.16: Map of the device of fig. 5.11 near the source junction, indicating the position of the maximum generation rate of holes and electrons computed using or not the QCTP (plot a). The generation rates and band profiles are also shown along the x direction at the z coordinate of maximum $G_{\mathrm{bbt,e}}$ (for the conduction band E_{C} and $G_{\mathrm{bbt,e}}$) and of maximum $G_{\mathrm{bbt,h}}$ (for the valence band E_{V} and for $G_{\mathrm{bbt,h}}$).

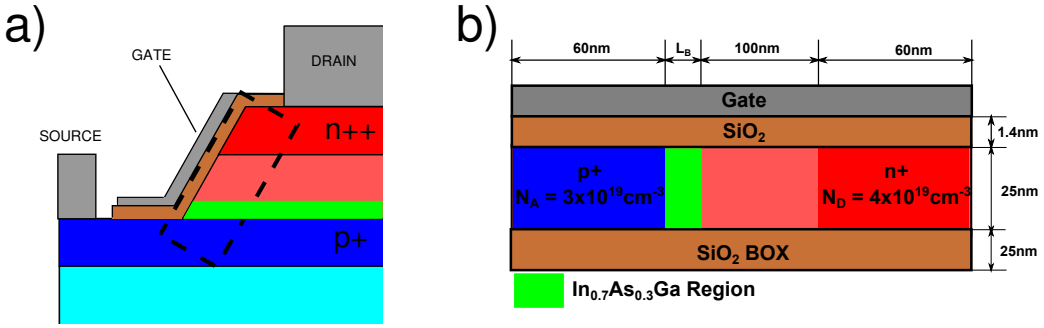

Figure 5.17: Sketch of the cross section of the MESA $In_{0.53}Ga_{0.47}As/In_{0.7}Ga_{0.3}As/In_{0.53}Ga_{0.47}As$ hetero-junction TFET presented in [5] (plot a). The rectangle includes the area that has been taken into account in the definition of the planar hetero-junction TFET sketched in plot b). L_{B} is the length of the small E_{G} $In_{0.7}Ga_{0.3}As$ region. The transport and the wafer plane directions are $< 100 > /(001)$.

the electrostatics, but quantization, as said above, makes the BtBT less sensitive to the electric field at the interface, thus reducing the effect of the gate extension in the source region.

5.4 Analysis of a III-V compound semiconductor planar hetero-junction TFET

In this case study we report the analysis of a planar hetero-junction TFET template (fig. 5.17) derived from the $In_{0.53}Ga_{0.47}As$ hetero-junction TFET device with a thin $In_{0.7}Ga_{0.3}As$ layer (featuring a lower E_{G}) inserted in the middle of the tunneling region. In the planar template the $In_{0.7}Ga_{0.3}As$ region between the channel and the source has a nominal length L_{B}=6nm and the gate covers the whole device from source to drain with the purpose of direct comparison with the experiments in [5].

Table 5.8: List of the parameters for GaAs, InAs and compressively strained $In_{0.7}Ga_{0.3}As$ ($cIn_{0.7}Ga_{0.3}As$) [**?**, 29] (10^{12}dyne/cm^2=100GPa)

Parameters	InAs	GaAs	$cIn_{0.7}Ga_{0.3}As$
ϵ[%]	0	0	1.16
C_{11} [10^{12} dyne cm^{-2}]	0.87	1.19	0.941
C_{12} [10^{12} dyne cm^{-2}]	0.49	0.54	0.478
Ξ [eV]	6.0	8.2	6.66
b [eV]	1.8	2.0	1.86
$E_{G,hh}$ [eV]	0.35	1.424	0.61
$E_{G,lh}$ [eV]	0.35	1.424	0.67

5.4.1 Computation of the strain effect on the band gap

The $In_{0.7}Ga_{0.3}As$ is placed between two $In_{0.53}Ga_{0.47}As$ regions and thus subject to a compressive strain that splits the valleys of light and heavy holes and changes the band gap. These band modifications have been computed considering the model reported in [28]. The light and the heavy hole valence band edge in presence of biaxial strain increase according to the relations:

$$\Delta E_{hh} = -2\Xi\epsilon\left(\frac{C_{11}-C12}{C_{11}}\right) + b\epsilon\left(\frac{C_{11}+C_{12}}{C_{11}}\right) \tag{5.5}$$

$$\Delta E_{lh} = -2\Xi\epsilon\left(\frac{C_{11}-C12}{C_{11}}\right) + b\epsilon\left(\frac{C_{11}+2C_{12}}{C_{11}}\right) \tag{5.6}$$

where C_{11} and C_{12} are the elastic coefficients, Ξ is the hydrostatic deformation potential, b the shear deformation potential and ϵ is the strain computed as:

$$\epsilon = \frac{a_{\text{str}}}{a_0} \tag{5.7}$$

where a_{str} and a_0 are the lattice constants of the in-plane strained and relaxed material respectively. In tab. 5.8 the parameters for the compressively strained $In_{0.7}Ga_{0.3}As$ used for the computation of ΔE_{hh} and ΔE_{lh} are reported and have been extracted as linear interpolation between the parameters of GaAs and InAs.

Using the eqs. 5.5-5.7 we obtain ΔE_{lh}=120meV and ΔE_{hh}=44meV. The band gap for the light holes and the heavy holes can be computed as:

$$E_{G,hh} = E_{G,\text{rel}} + \Delta E_{hh} = 0.61\text{eV} \tag{5.8}$$

$$E_{G,lh} = E_{G,\text{rel}} + \Delta E_{lh} = 0.67\text{eV} \tag{5.9}$$

where $E_{G,hh}$ and $E_{G,lh}$ are the $cIn_{0.7}Ga_{0.3}As$ band gaps between the conduction band and the heavy hole valence band and the light hole respectively, and $E_{G,\text{rel}}$ is the band gap for the relaxed material. The light and heavy hole valley has been moved down in energy increasing the band gaps between the conduction band and the light and heavy holes valence bands as qualitatively sketched in fig. 5.18.

To compute the variation of the electron affinity in $cIn_{0.7}Ga_{0.3}As$ in [28] the following approach is followed [28]:

$$\frac{\Delta E_C}{\Delta E_G} = \frac{E_C(In_{0.53}Ga_{0.47}As) - E_C(cIn_{0.53}Ga_{0.47}As)}{E_G(In_{0.53}Ga_{0.47}As) - E_{G,hh}(cIn_{0.53}Ga_{0.47}As)} = 0.65 \tag{5.10}$$

Therefore the electron affinity χ of $cIn_{0.7}Ga_{0.3}As$ can be estimated as:

$$\chi(cIn_{0.7}Ga_{0.3}As) = \chi(In_{0.53}Ga_{0.47}As) + 0.65\Delta E_G \tag{5.11}$$

$$= 4.51\text{eV} + 0.08\text{eV} = 4.59\text{eV} \tag{5.12}$$

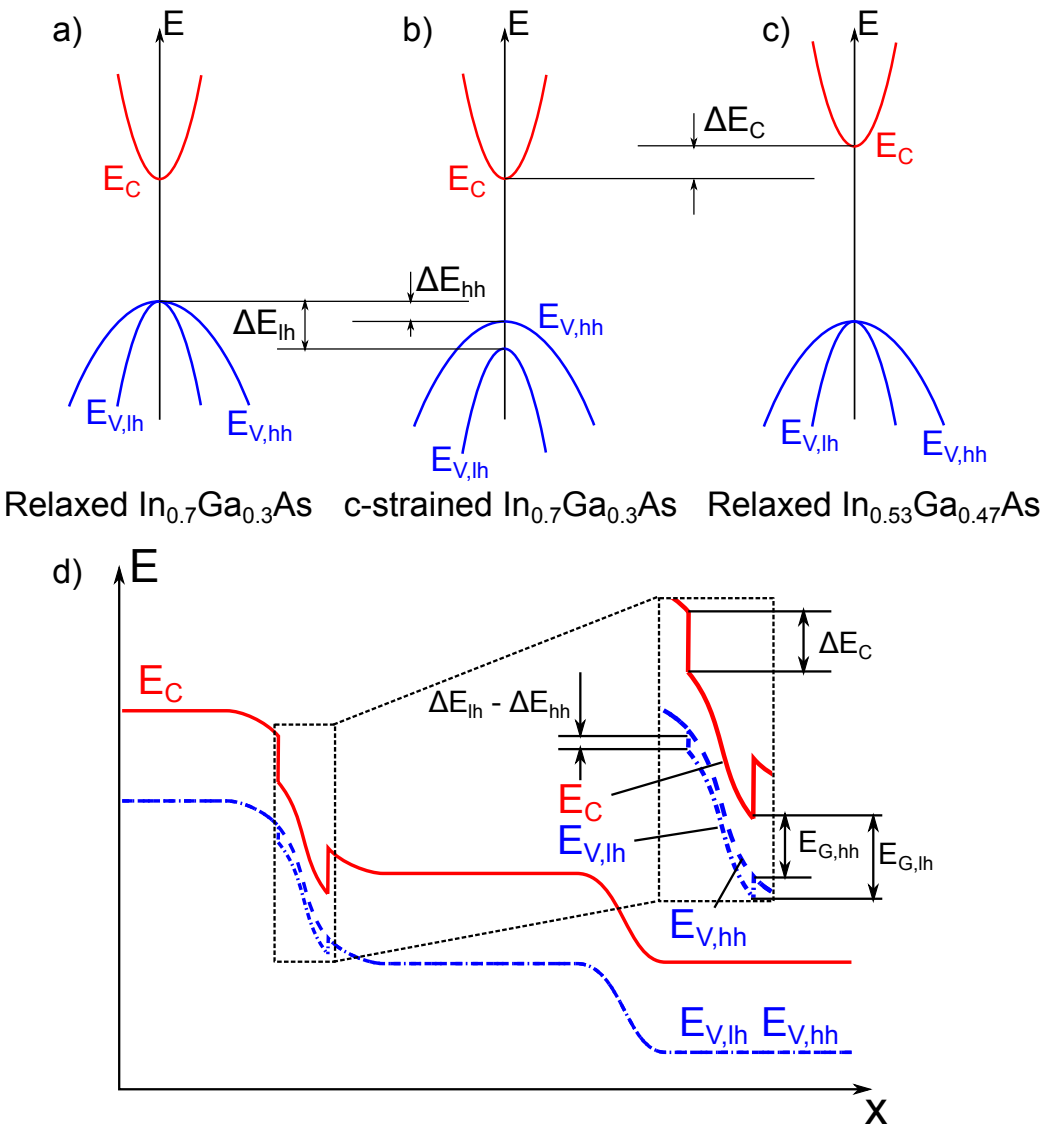

Figure 5.18: Qualitative sketch of the bands for a relaxed $In_{0.7}Ga_{0.3}As$ compound (plot a), for compressively strained $In_{0.7}Ga_{0.3}As$ layer (plot b) that is strained by a relaxed $In_{0.53}Ga_{0.47}As$ layer whose bands are sketched in plot c). ΔE_{hh} and ΔE_{lh} definitions have as reference the valence band edge of the relaxed $In_{0.7}Ga_{0.3}As$ compound bands whereas the ΔE_C one has as reference the conduction band edge of the relaxed $In_{0.53}Ga_{0.47}As$. Plot d) qualitatively sketch the band profiles along the transport direction for the device in fig. 5.17-b (without including BGN), and how the value of ΔE_C, ΔE_{hh}, and ΔE_{lh} reflect on the band profiles (inset).

Table 5.9: List of the BtBT parameters for the transition starting from the light hole valence band ($\Gamma_{v,lh} \rightarrow \Gamma_c$,) and of the transition starting from the heavy hole valence band ($\Gamma_{v,hh} \rightarrow \Gamma_c$) in the different regions of the device. BGN for the source and the drain $In_{0.53}Ga_{0.47}As$ region is already accounted using the Jain Roulston model [4] and the parameters in [27].

BtBT transition $\Gamma_{v,lh} \rightarrow \Gamma_c$				
Parameters	Source $N_{A,s} = 4 \cdot 10^{19}cm^{-3}$	Low E_G region intrinsic	Channel intrinsic	Drain $N_{D,d} = 4 \cdot 10^{19}cm^{-3}$
`Apath1` $[10^{20}cm^{-3}s^{-1}]$	1.87	1.65	1.76	2.01
`Bpath1` [MV/cm]	4.42	4.45	5.31	3.53
E_G [eV]	0.63	0.67	0.71	0.54
m_c $[m_0]$	0.043	0.036	0.043	0.043
$m_{v,lh}$ $[m_0]$	0.053	0.043	0.053	0.053
m_r $[m_0]$	0.023	0.019	0.023	0.023
χ [eV]	4.54	4.59	4.51	4.67
BtBT transition $\Gamma_{v,hh} \rightarrow \Gamma_c$				
Parameters	Source $N_{A,s} = 4 \cdot 10^{19}cm^{-3}$	Low E_G region intrinsic	Channel intrinsic	Drain $N_{D,d} = 4 \cdot 10^{19}cm^{-3}$
`Apath1` $[10^{20}cm^{-3}s^{-1}]$	2.42	2.29	2.27	2.60
`Bpath1` [MV/cm]	5.70	4.86	6.85	4.56
E_G [eV]	0.63	0.60	0.71	0.54
m_c $[m_0]$	0.043	0.036	0.043	0.043
$m_{v,hh}$ $[m_0]$	0.452	0.440	0.452	0.452
m_r $[m_0]$	0.039	0.033	0.039	0.039
χ [eV]	4.54	4.59	4.51	4.67

No information were found in literature about strain effect on the effective masses of III-V compounds, so we choose to use the relaxed material effective masses for the light and heavy holes and for the electrons that are provided in [24] ($m_{v,lh} = 0.043m_0$, $m_{c,hh} = 0.44m_0$ and $m_e = 0.036m_0$) and give reduced masses equal to $m_{r,lh} = 0.019m_0$ and $m_{r,hh} = 0.034m_0$ for BtBT transition starting from the light and heavy hole valence band, respectively. Using these data we can now compute the parameters for the non-local direct BtBT model for both the transitions starting from the light and heavy hole bands that are reported in tab. 5.9.

Considering the homo-junction case, investigated in the previous section, the probability of the transition starting from the heavy hole valence band was negligible with respect to the one starting from the light hole one due to the heavier reduced mass.

In the case of the hetero-junction device treated here, the strain in the $cIn_{0.7}Ga_{0.3}As$ region makes the band gap starting from the heavy hole valence band narrower than the one concerning the transition from the light hole valence band. This makes both the transitions that start from the heavy and from the light hole valence band equally significant on the drain current, and the simulation must account for both of them.

5.4.2 Simulation results

The Band Gap Narrowing in the heavily doped source and drain regions, is described using the same approach proposed in section 5.3.2, that is the Jain Roulston model and the parameters provided in [27]. The parameters for the dynamic non-local direct BtBT model for the various regions of the device are reported in tab. 5.9.

Fig. 5.19 compares the measured trans-characteristic of ref. [5] to the simulated one accounting for both the direct BtBT transitions that start from the light and heavy hole valence bands, and give rise to two different current components that are reported together with their sum. The simulations have been carried out with and without the QCTP. For the simulations without QCTP only the total current is shown. For all the V_{GS} the current that stems from

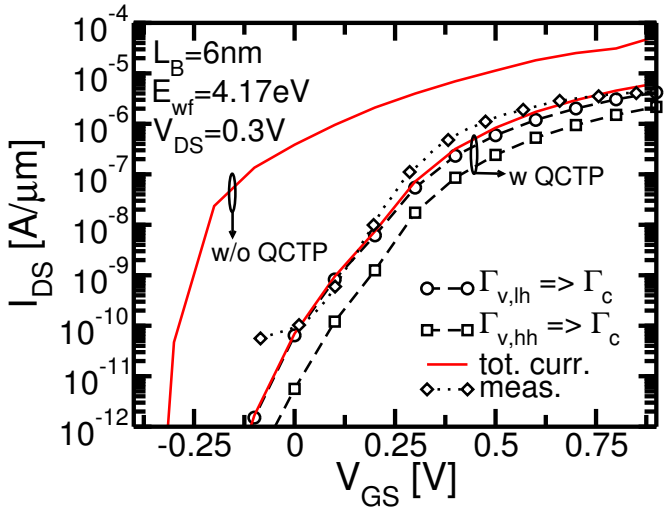

Figure 5.19: Comparison between the simulated trans-characteristics of the hetero-junction device reported in fig. 5.17 computed considering both the current components generated from the direct BtBT transitions starting from light (circles) and heavy (squares) hole valence bands together with their sum (red solid line). The measurements reported in [5] are also reported as a reference. The MSMC simulations have been carried out with and without QCTP, but in the latter case only the total current is reported.

the direct BtBT transition starting from the light hole valence band is higher than the one from the heavy hole valence band, but the difference is reduced as V_{GS} increases and it is never significant enough to allow to neglect the heavy hole BtBT current. The qualitative agreement of the total current computed with the quantum corrected model with measurement is more than satisfactory as was the case for the homo-junction device. If we consider that the reference device in [5] has a bulk MESA structure whereas the device in fig. 5.17 is a ScOI. This is partly due to the relatively thin surface region where BtBT occurs which is weakly affected by the actual total layer thickness.

Next we investigate the width of the low band gap region that maximizes the I_{on} and minimizes the SS. To this purpose, L_B has been systematically changed in the range from 3nm to 18nm with step 3nm. I_{on} is taken as the I_{DS} current at $V_{DS} = 0.3$V and V_{GS}=0.3V. The I_{DS} at $V_{DS} = 0.3$V and $V_{GS} = 0.5$V and the same I_{off} is also recorded. Fig. 5.20 shows that the maximum I_{on} is obtained at $L_B = 12$nm for V_{GS}=0.3V and at $L_B = 9$nm for $V_{GS} = 0.5$V. For L_B longer than 6nm, SS decreases from a value higher than 60mV/dec to the minimum value of 40mV/dec with $L_B = 12$nm. It thus appears that the thin barrier layer can be further engineered to improve the performance beyond what was reported in [5].

The reason for this behavior is explained by fig. 5.21 where, considering only the dominant current component due to direct BtBT transition from the light hole valence band valley to the conduction band, we show the bands profile and the generation rate for electrons ($G_{bbt,e}$) and for holes ($G_{bbt,h}$) along the x direction for $L_B = 6$nm, 12nm and 15nm at $V_{DS} = V_{GS} = 0.3V$ having fixed $I_{off} = 1$pA/μm. If, upon increase of V_{GS}, the point of maximum generation rate of electrons ($G_{bbt,e}$) moves into the low band gap region, then $G_{bbt,e}$ has a sudden boost which contributes to both reduced SS and increased I_{DS}. The widening of L_B does not affect significantly the position of the maximum $G_{bbt,e}$ and $G_{bbt,h}$ with respect to the left edge of the low band gap ($In_{0.7}Ga_{0.53}As$) region; on the contrary the position of maximum $G_{bbt,e}$ is mostly controlled by the V_{GS} potential. At $V_{GS} = 0.3$V we do not see an increase of the maximum $G_{bbt,e}$ with a L_B longer than 12nm, and this is consistent with fig. 5.20 that reports the maximum of the I_{on} for $L_B = 12$nm, while at $V_{GS} = 0.5$V the optimum L_B is smaller.

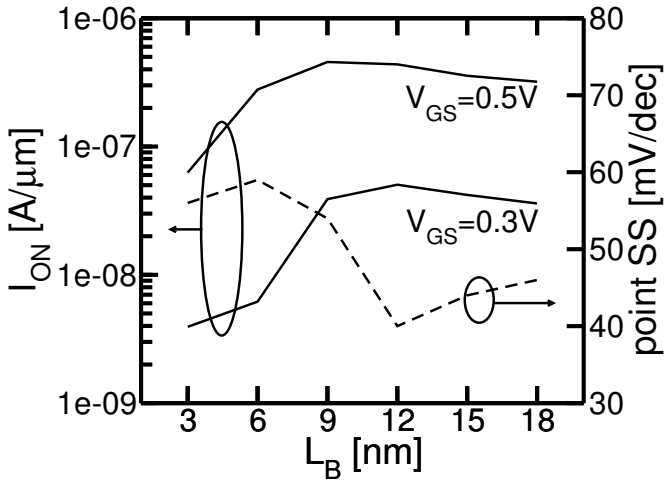

Figure 5.20: I_{on} at $V_{\mathrm{GS}} = 0.3\mathrm{V}$ and $0.5\mathrm{V}$ (being $V_{\mathrm{DS}} = 0.3\mathrm{V}$ and $I_{\mathrm{DS}} = I_{\mathrm{off}} = 1\mu\mathrm{A}/\mu\mathrm{m}$ at $V_{\mathrm{GS}} = 0.0\mathrm{V}$) and point SS at $I_{\mathrm{DS}} = I_{\mathrm{off}}$ for different values of L_{B}.

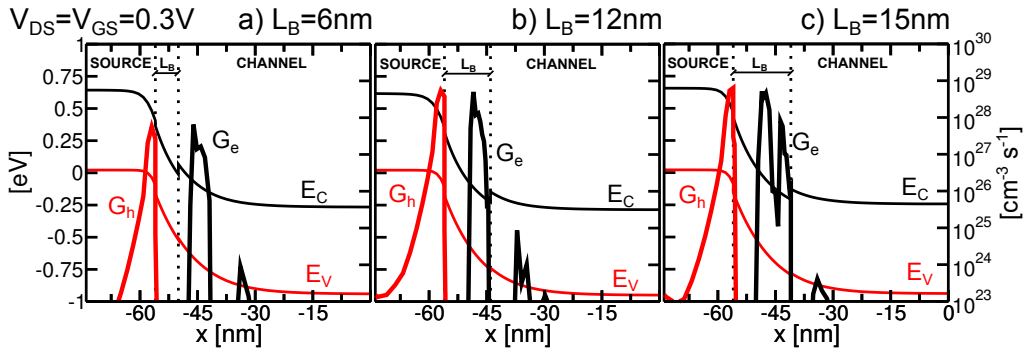

Figure 5.21: Energy bands and generation profile for L_{B}=6nm (plot a) and 12nm (plot b) and 15nm (plot c) at $V_{\mathrm{DS}} = V_{\mathrm{GS}} = 0.3\mathrm{V}$ with I_{off}=1pA/μA. E_{V} and $G_{\mathrm{bbt,h}}$ curves are plotted along the x direction at the y coordinate of maximum $G_{\mathrm{bbt,h}}$; E_{C} and $G_{\mathrm{bbt,e}}$ are plotted at the y coordinate of maximum $G_{\mathrm{bbt,e}}$.

5.5 Summary and Conclusions

In this chapter a wide spectrum of TFET case studies has been analyzed by means of MSMC simulation using the dynamic non-local direct and phonon-assisted BtBT models with the QCTP. By means of comparison with experimental results found in the literature, we show that the MSMC is an accurate and reliable model for the simulation of planar Si and III-V compound UTB TFET devices and that the presence of size- and bias-induced quantization cannot be neglected. We also demonstrate that the vertical scaling allows us to achieve current enhancements due to the improved electrostatics.

The analysis of the SiGe device and the search for the optimum alignment of the $Si_{0.5}Ge_{0.5}$/Si hetero-junction DG TFET has shown that, even if the device is aggressively scaled, it is unlikely to attain adequate specs for digital ultra low power application ($V_{DD} < 0.5$V, I_{off}=10pA/μm, $I_{on} > 10\mu$A/μm). Perhaps further technology boosters and/or nanowire device architectures could help meet these goals. Indeed in published experimental works significant current improvements are attributed to strain for SiGe hetero-junction TFET devices [30, 31].

The planar $In_{0.53}Ga_{0.47}As/In_{0.7}Ga_{0.3}As/In_{0.53}Ga_{0.47}As$ hetero-junction device in this work exhibits promising I_{on} in the order of 0.1μA/μm SS=40mV/dec at V_{DS}=0.3V. We expect that improved electrostatic achieved via a better vertical scaling or nanowire architecture might also improve the I_{on} and the SS of III-V hetero-junction devices presented in this chapter. It has also been shown that the on-current is limited by the small tunneling area of a planar TFET architecture. A few TFET concepts where the tunneling current might scale with area have been proposed which could possibly help to overcome the current limitations of the TFETs devices [32, 33, 34] and are experimentally investigated in chapter 7.

Tab. 5.10 summarizes the major outcomes obtained from the analysis of the device template whose simulation results have been reported in this chapter.

Table 5.10: Summary of the major outcomes obtained from the study of the different template structures reported in this chapter

Template	Biasing	Outcomes
Planar Silicon Homo-junction Sec. 5.1.1	V_{DS} 1.0V V_{GS} 0V → 3.0V	BtBT parameters extracted from Solomon diodes data [1] → Simulations using only the BtBT model account also for TAT and BGN BtBT parameters from 30 bands k.p [7,8] → Simulations using only the BtBT model account only for BtBT Comparison of MSMC and experimental results [2] with good agreement I_{on}=10nA/μm SS=191mV/dec
Planar Silicon Homo-junction Sec. 5.1.2	V_{DS} 1.0V V_{GS} 0V → 1.0V	MSMC simulation with and without QCTP has shown: → detrimental effect of quantum carrier confinement → vertical scaling enhance the performance through electrostatic control more than it degrade it through heavier quantization effects. I_{on}=9nA/μm SS=87mV/dec
Planar $Si_{0.5}Ge_{0.5}$/Si Hetero-junction Sec. 5.1.3	V_{DS} 0.5V V_{GS} 0V → 1.2V	MSMC used to tailor the device trans-characteristics, changing the doping and hetero-junction alignment. → a local optimum for SS and I_{on} has been found → SiGe/Si hetero-junction simulations without accounting for strain show little performance improvement with respect to Si homo-junction I_{on}=10nA/μm SS=63mV/dec
Planar $In_{0.53}Ga_{0.47}As$ Homo-junction Sec. 5.1.4	V_{DS} 0.3V V_{GS} 0V → 1.2V	MSMC simulations investigated various aspects of the considered design: → Vertical scaling improves the device performances → Dependence of the trans-characteristics on $N_{D,d}$ → Strong Dependence of BtBT on BGN with better Ion and SS → Good agreement with the experimental results in [5] → Quantum carrier confinement effect on BtBT generation rate profiles → Negligible performance dependence on the metal gate extension over the channel I_{on}=1μA/μm SS=73mV/dec
Planar InGaAs Hetero-junction Sec. 5.1.5	V_{DS} 0.3V V_{GS} 0V → 1.2V	MSMC simulations accounting for BGN and strain effect on perfomance investigated various aspects of the considered design: → Tailoring of the length of the low band gap region for optimizing current and SS →Ion=5μA/μm SS=40mV/dec → In the nominal case with L_B=6nm very good agreement is found between simulation and measurements results in [5]

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Chapter 6

Characterization of SiGe and Si homo- and hetero-junction TFETs

In this chapter we present the room and low temperature characterization of planar hetero-junction SiGe/Si on Insulator TFETs fabricated in the CEA-LETI research center clean room in Grenoble. The goal is to investigate the injection mechanism from the source to the channel inside the devices. As a reference we also measured the characteristics of MOSFETs fabricated with state-of-the-art CEA-LETI silicon FD-SOI CMOS technology (denoted lot 1) and the planar SiGe/Si hetero-junction TFETs whose room temperature characteristics were already presented in [1] (denoted lot 2). A second third batch of wafers has been measured, denoted lot 3. Lot 3 has been fabricated with a mask set and process allowing for small geometrical dimensions ($L_G = 30$nm) and Ω-gated devices. Further measurements were carried out on two other lots denoted lot 4 and lot 5. The former presents TFET devices with the same structure of those of lot 3 but without the Boron in-situ doping in the N++ region that affects the TFET of lot 3. Lot 5 has been fabricated with the same mask of lots 3 and 4 but with the device channel implemented in $Si_{0.7}Ge_{0.3}$ obtained with the Germanium enrichment procedure [2]. In order to better understand the injection mechanism we also simulated simple FD-SOI nMOSFET and nTFET templates to investigate the effect of temperature considering pure thermionic emission (nMOSFET) and pure BtBT injection (nTFET), and compared the simulation results with the experimental evidences.

6.1 Temperature dependence of TFET and MOSFET trans-characteristics

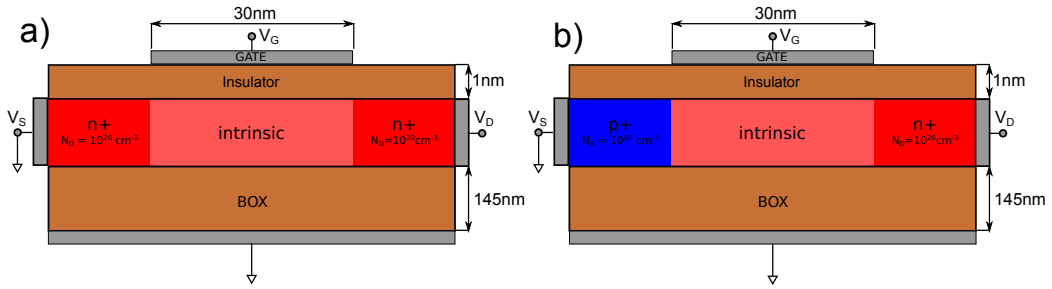

Figure 6.1: Sketch of the planar FD-SOI nMOSFET (plot a) and nTFET (plot b) templates simulated with the MSMC model. $T_{Si} = 10$nm, EOT=1nm, $T_{BOX} = 145$nm. The only difference between the two templates is the dopant of the source region, that changes from donor (nMOSFET) to acceptor (nTFET). The doping profiles are abrupt.

We simulated with our MSMC the planar Silicon FD-SOI nMOSFET and the nTFET sketched in fig. 6.1 to determine the expected temperature dependence of pure thermionic emission (nMOSFET) and of pure BtBT (nTFET) injection mechanisms. The parameters for the non-local phonon-assisted BtBT for Silicon have been calculated using the tunneling masses reported in the literature [3]. The Band Gap dependence on temperature in Silicon is described as [4]:

$$E_G(T) = 1.17 - 4.73 \cdot 10^{-4} \cdot T^2/(T + 636) \tag{6.1}$$

and accounting for the BGN with the Jain Roulston model [5] presented in section 3.7. The SS of the MOSFET trans-characteristics is reduced at low temperatures, while the trans-characteristics of the TFET do not show an appreciable dependence on the temperature. At high temperature the band gap is reduced and therefore the current is slightly increased, but the overall change is modest compared to that of the MOSFET (fig. 6.2).

Fig. 6.3 reports the SS vs I_D curve for the nMOSFET (plot a) and the nTFET (plot b) simulated with the MSMC at the temperature T=150K, 300K, 450K. The MOSFET shows that SS

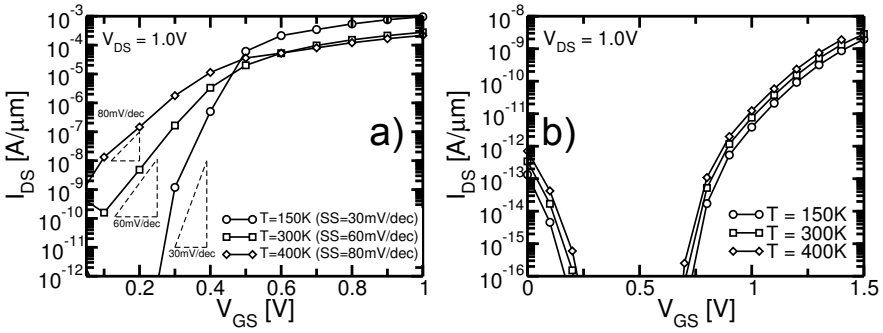

Figure 6.2: Trans-characteristics of the nMOSFET (plot a) and of the nTFET (plot b) simulated with the MSMC at the temperature T=150K, 300K, 450K.

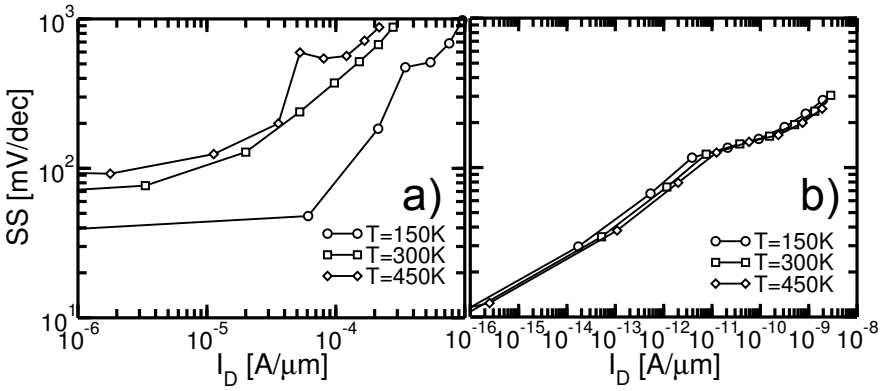

Figure 6.3: SS on I_{D} of the nMOSFET (plot a) and of the nTFET (plot b) simulated with the MSMC at the temperature T=150K, 300K, 450K.

is almost constant for low I_{D} levels, and a lower SS is obtained at lower temperatures. The low I_{D} limits of SS are in good agreement with theoretical expectations (SS=30mV/dec @ T=150K and SS=90meV @ T=450K). On the other hand, the TFET curves are almost independent of temperature and two regions can be recognized: a first region for $I_{\mathrm{D}} < 100\mathrm{pA}/\mu\mathrm{m}$ where the curves (in logarithmic scale) can be approximated with a straight line and a second region for $I_{\mathrm{D}} > 100\mathrm{pA}/\mu\mathrm{m}$ where the curves are super-linear. The reason for the different behavior at low and high I_{D} can be explained by the fact that higher currents correspond to higher electric field in the device. In presence of high fields the current in the tunneling junction can be well approximated by the Kane model in constant field. On the other hand low I_{D} corresponds to low V_{GS} and low electric field, and in this range the SS trend is different.

6.2 Reference MOSFET characterization at low temperature (lot 1)

Fig. 6.4 sketches the planar Silicon FD-SOI MOSFET device presented in [1] which is here taken as a reference.

Fig. 6.5 reports the FD-SOI nMOSFET (plot a) and the pMOSFET (plot c) trans-characteristics measured at various temperatures ranging from T=77K to T=294K for a device with $L_{\mathrm{G}} =$ 80nm, $W = 10\mu$m. Plots b) and d) report the SS vs. I_{D} characteristics. At low current (subthreshold region) the SS remains almost constant and this is typical for a MOSFET where the

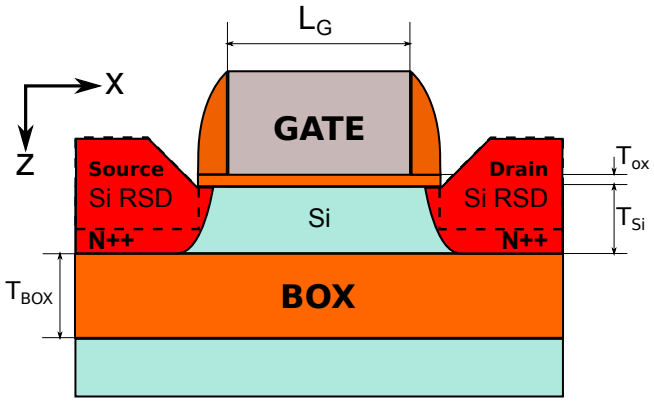

Figure 6.4: Sketch of the planar Silicon FD-SOI MOSFET devices presented in [1]. $T_{Si} \approx$ 6.3nm, EOT≈1.2nm and T_{BOX}=145nm, L_G = 80nm.

SS is limited by the theoretical limit of the thermionic emission. The curves reported in plots b) and d) present a trend that is similar to the one found in simulation and reported in fig. 6.3-a.

The Si FD-SOI TFETs fabricated in this lot has not been considered for this characterization work since their I_{on} and SS performance are significantly inferior if compared with the devices of the lot 2, whose results are reported in the next section.

The dependence of SS on temperature is shown in fig. 6.6. The measured SS follows the linear trend predicted by MOSFET theory with small discrepancy due to the non-perfect coupling between the gate and the channel.

6.3 Reference TFET characterization at low temperature (lot 2)

Fig. 6.7 sketches the structure of the planar hetero-junction TFET device fabricated in lot 2 and presented in [1]. The Raised Source and Drain are in $Si_{0.7}Ge_{0.3}$, and a $Si_{0.85}Ge_{0.15}$ layer is interposed between two Silicon layers.

Fig. 6.8 reports the trans-characteristics of the TFETs of different geometries biased with the p-type configuration at different temperatures ranging from T=77K to T=294K. Differently from the MOSFET case, we consider the drain current $I_D = I_p$ since the drain region in the pTFET correspond to the p++ region. As illustrated in fig. 6.9 in TFETs the gate leakage current flows from the channel to the n++ region and will sum with the BtBT current. However, considering both the n-type and the p-type configuration, the particles can flow only in direction of the N++ region that for the nTFET is the drain and for the pTFET is the source. Indeed the band diagram in both cases is the one of a p-i-n diode where the gate current can flow only toward the N++ region where the gate current I_G sums with the injection current from the source I_{BtBT}. On the contrary, in the P++ region only the BtBT current can be found. In this work we are interested in the injection current behavior at low temperature and therefore we consider only the P++ current I_p, where only the BtBT component is found, that is the source current I_S for the nTFET or the drain current I_D for the pTFET.

The temperature dependence of the curves suggests that there are two injection mechanism occurring at the source/channel junction: the BtBT that dominates at low temperature and a concurrent temperature dependent mechanism that dominates at low V_{GS} and high temperature. Although the mechanism is not unambiguously identified, it is likely to be Trap Assisted Tunneling (TAT) at the hetero-junction interface where a significant number of defects and

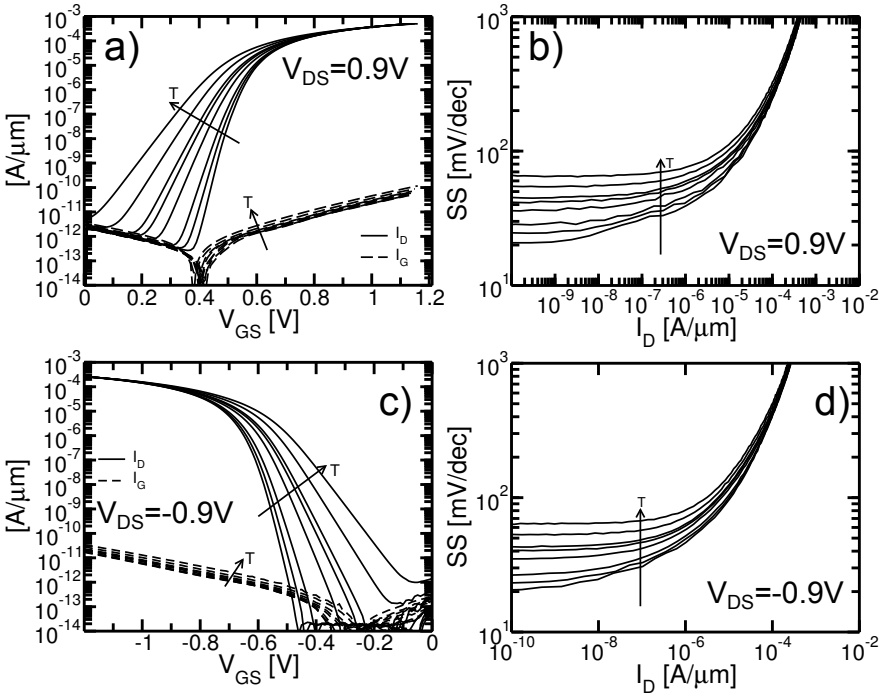

Figure 6.5: FD-SOI nMOSFET (plot a) and pMOSFET (plot c)trans-characteristics measured at temperature T=77K, 100K, 130K, 150K, 180K, 210K, 250K, 294K. L=80nm, W=10μm. Plots b) and d) report the SS vs I_D characteristic for nMOSFET and pMOSFET respectively.

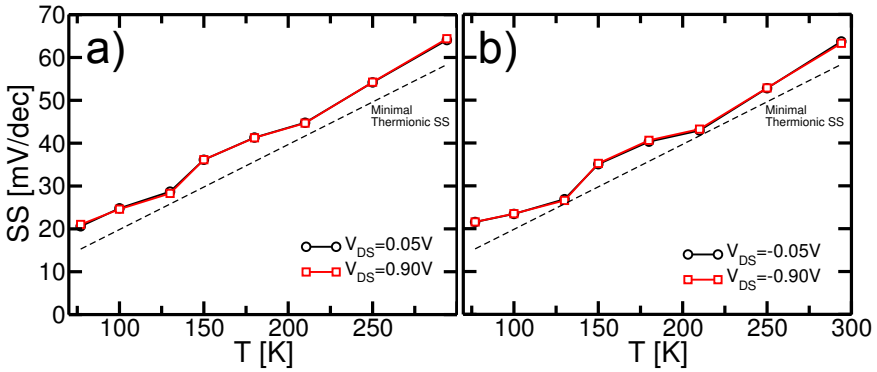

Figure 6.6: SS measured at I_D = 10pA/μm vs. T for the nMOSFET (plot a) and pMOSFET (plot b) of fig. 6.5. The SS follows the expected linear trend versus temperature with a slightly larger value that is due to the non perfect coupling between the gate and the channel.

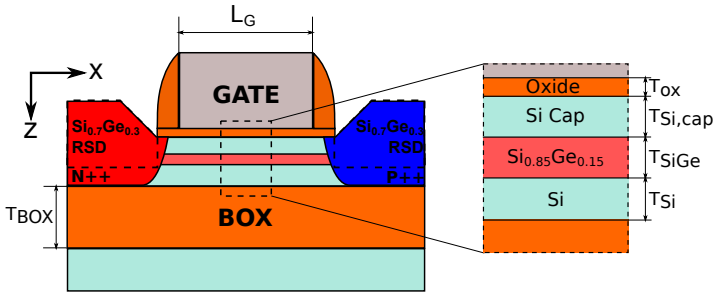

Figure 6.7: Sketch of the planar hetero-junction TFET device presented in [1] and measured at low temperature. The Raised Source and Drain are in $Si_{0.7}Ge_{0.3}$, and a $Si_{0.85}Ge_{0.15}$ layer is interposed between two Silicon layers in the channel. $T_{Si} \approx 3.5$nm, $T_{SiGe} \approx 6$nm, $T_{Si,cap} \approx 1.5$nm, EOT$\approx$1.2nm and T_{BOX}=145nm.

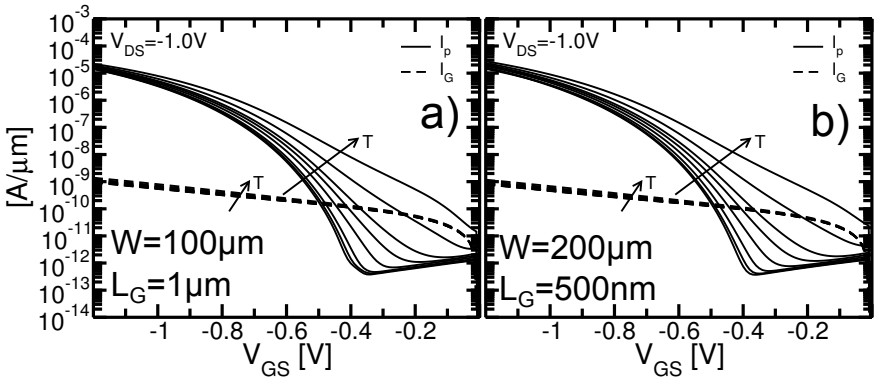

Figure 6.8: Trans-characteristics of the TFETs of different geometries measured in p-type configuration at temperature T=77K, 100K, 130K, 150K, 180K, 210K, 250K, 294K.

dislocations can be found. TAT is a temperature dependent mechanism that is remarkably reduced at low temperature [6].

Fig. 6.10 reports the SS vs. I_p of the TFETs for two different geometries measured in p-type configuration at temperatures that range from T=77K to T=20K. At low temperature ($T \leq 130$K) the curves are almost independent of temperature. Two regions are visible: for $I_p > 1\mu A/\mu m$ the current is a independent of temperature while for $10pA/\mu m < I_p < 1\mu A/\mu m$ no dependence is found on temperature only for $T < 130$K and where a linear trend can be found. The experimental curves are qualitatively similar to the one computed with the MSMC simulator (fig. 6.3-d).

Fig. 6.11 reports the SS measured at $I_D = 100pA/\mu m$ as a function of the temperature for the TFETs of fig. 6.7. The SS does not go below the thermionic limit at low temperature for both the devices with $L_G = 1\mu m$ and with $L_G = 500$nm, but for low temperatures $T < 130$K SS does not show a significant dependence on temperature. The results shown in figs. 6.8, 6.10 and 6.11 suggest that the parasitic conduction at low temperature may not be due to a parasitic MOSFET in parallel to the TFET but rather to a Trap Assisted Tunneling (TAT) mechanism.

Tab. 6.1 reports a summary of the injection mechanisms that presumably occur in the measured devices of lot 2.

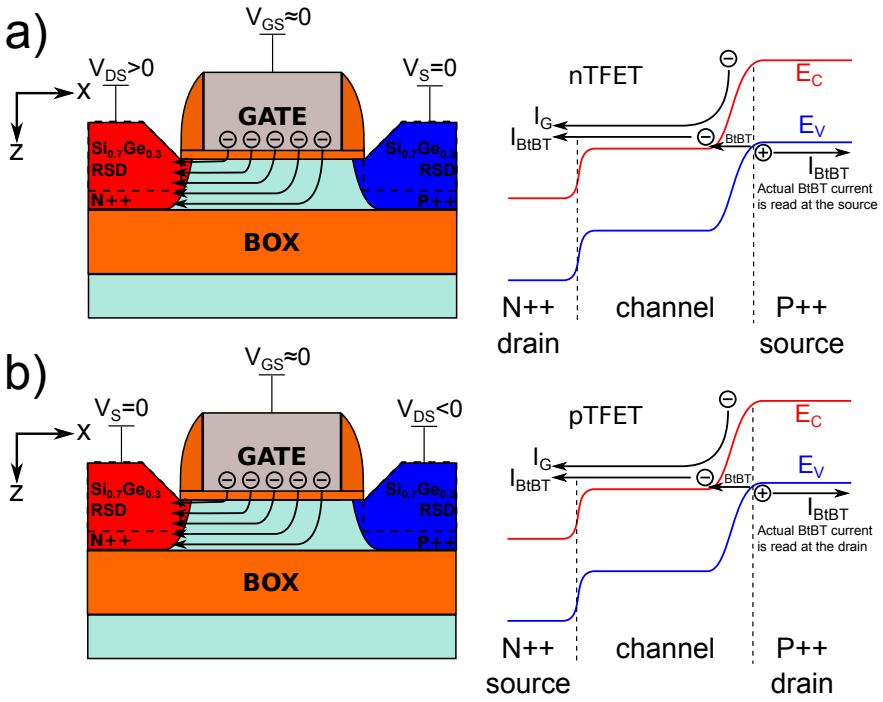

Figure 6.9: Qualitative sketch of the bands for an nTFET (plot a) and for a pTFET (plot b) at low V_{GS}.

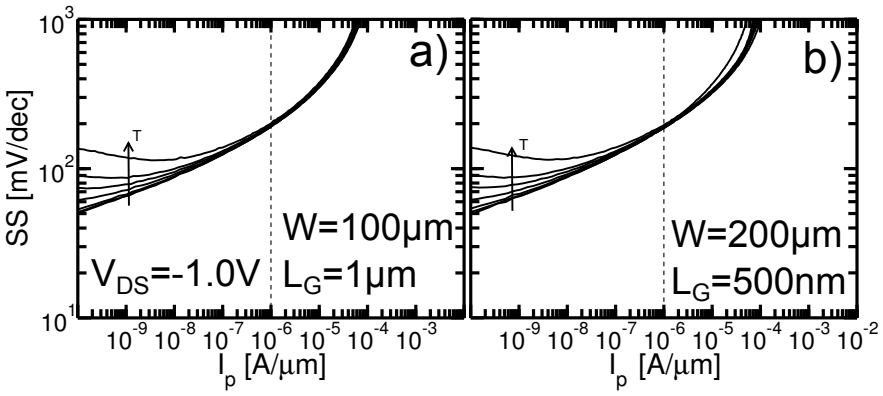

Figure 6.10: SS vs. I_p of the p-type TFETs for two different geometries at temperature T=77K, 100K, 130K, 150K, 180K, 210K, 250K.

Table 6.1: Summary table reporting the injection mechanism occurring in the tunneling junctions of the TFET devices of lot 2 as suggested by the measurements reported in this section.

TFET Lot 2 (reference)				
L [μm]	W [μm]	Junction	Temperature	Inject. Mach.
1	100	N++/channel	low	BtBT
1	100	N++/channel	high	BtBT+TAT
0.5	200	N++/channel	low	BtBT
0.5	200	N++/channel	high	BtBT+TAT

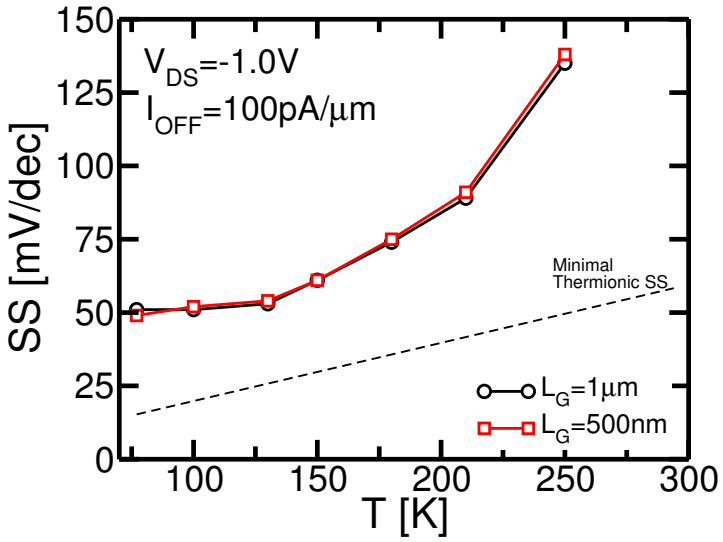

Figure 6.11: SS measured at I_D = 100pA/μm for the TFETs of fig. 6.7 whose transcharacteristics are reported in fig. 6.8.

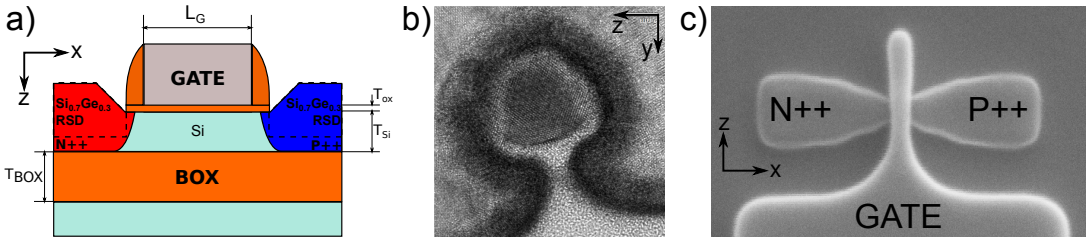

Figure 6.12: Sketch of the $Si_{0.3}Ge_{0.7}$/Si on Insulator hetero-junction planar TFET device fabricated in the second batch using an alternative mask set (plot a). $T_{Si} \approx 12$nm, EOT=1.42nm, T_{BOX}=145nm. The TFET device is an Ω-gated nanowire as visible in the TEM images of plots b) and c). The images in plot b) and c) are courtesy of CEA-LETI research center of Grenoble.

6.4 TFET characterization at low temperature (lot 3)

Fig. 6.12 sketches the $Si_{0.7}Ge_{0.3}$/Si on insulator hetero-junction TFET devices of lot 3 fabricated with the mask set denominated as "Snow Mask". The TFET device has an nanowire/nanoribbon Ω-gate that should improve the electrostatic control especially for narrow devices ($W \approx$ 30nm).

Fig. 6.13 reports the trans-characteristics of three TFET devices of fig. 6.12 biased in p-type configuration (plots a, c and e) and in n-type configuration (plots b, d and f) at different temperatures that range from T=77K to T=250K. The width $W = 2\mu$m is the same for all devices whereas the gate length is $L_G = 1\mu$m, 250nm and 100nm. The trans-characteristics show almost no dependence on gate length consistently with theoretical expectations [7]. A significant difference is instead found between the p-type TFET trans-characteristic and the n-type one, mainly concerning the dependence on temperature. The nTFET I-V curves show a temperature dependence only for T>150K whereas the p-TFET ones are sensitive to temperature even at T=77K. This suggests that the injection mechanism found in the source/channel and in the channel/drain junction is not the same, moreover also the gate leakage current does not flow in direction of the N++ region (as should be in a typical TFET) but partly in direction of the P++ region. The p-type trans-characteristics are quite similar to those of a MOSFET (fig. 6.5) with respect to the ones of a TFET (fig. 6.8), and at higher temperatures a parasitic injection mechanism takes place in the P++/channel junction.

Fig. 6.14 reports the SS versus I_n curve for the TFET device in fig. 6.12 biased in the p-type (plot a) or the n-type (plot b) configuration. The pTFET curves are similar to those of the pMOSFETs (fig. 6.5-d). This suggest that in the p-type configuration the current at the source/channel junction is the sum of a parasitic thermionic emission and BtBT components. The former may be justified by the presence of a parasitic pMOSFET in parallel with the TFET. On the other hand fig. 6.14-b shows a curve set similar to the one presented in fig. 6.10 suggesting that in the n-type configuration the main injection mechanism at the source/channel junction, at low temperatures, is BtBT.

Fig. 6.15 reports SS versus temperature curves for different gate lengths. The SS is computed at $I_p = I_{off} = 1$nA/μm for the devices of fig. 6.12. The figure shows the curves for the TFETs biased in the p-type configuration (plot a) or in the n-type configuration (plot b). For the p-type configuration (therefore considering the injection mechanism occurring at the N++/channel junction) the curve of the long device shows a linear trend of the SS for T<180K whereas for higher temperatures the SS becomes independent on temperature. For the device with $L_G = 100$nm the SS dependence of temperature follows a linear trend that has a slope quite similar to the one given by the theoretical limit of the thermionic emission confirming that the N++/channel junction is not working as a tunneling junction. The experimental results presented in fig. 6.15 and 6.14-b suggest that a thermionic mechanism is taking place in the N++/channel junction. On the other hand for the n-type configuration (injection at the P++/channel junction) the value of SS is higher than the one of the p-type configuration. This is due to a non perfect electrostatic control of the gate on the channel and the limited dependence of the curves on L_G and on temperature, consistently with the results presented in fig. 6.14-b suggests that the injection mechanism occurring in the P++/channel junction is BtBT.

The assessment that the injection mechanism is different between the N++/channel and the P++/channel junctions is further confirmed by the results in fig. 6.16 where I_{on} versus temperature curves of the TFET device of fig. 6.12 is reported for a few gate lengths. The I_{on} is extracted at $|V_{DS}| = 1.0$V and $|V_{GS}| = 2.0$V. Plot a) shows the curves for the p-type devices and plot b) the ones for the n-type devices. The pTFET current is higher by an order of magnitude than the one of nTFETs. Moreover they have a weak dependence on the temperature and the current is doubled passing from $L_G = 1\mu$m to 250nm and 100nm. On the other hand plot b) shows a clear dependence of I_{on} on the temperature and a weak dependence on the gate length

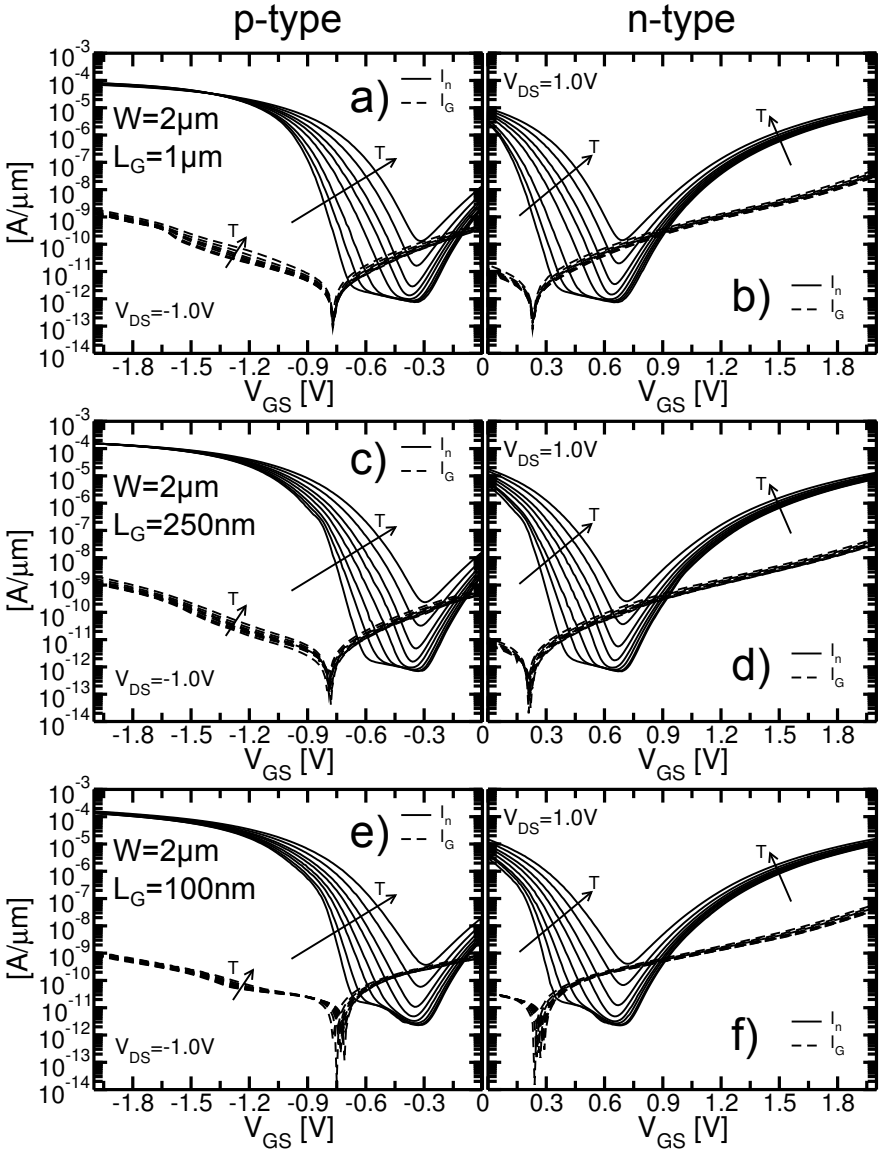

Figure 6.13: Trans-characteristics of three of the TFET devices in fig. 6.12 biased p-type (plots a, c and e) and in n-type mode (plots b, d and f) at the temperatures T=77K, 100K, 130K, 150K, 180K, 210K, 230K, 250K. The width $W = 2\mu$m is the same for all devices whereas the gate length $L_{\mathrm{G}} = 1\mu\mathrm{m}, 250\mathrm{nm}, 100\mathrm{nm}$.

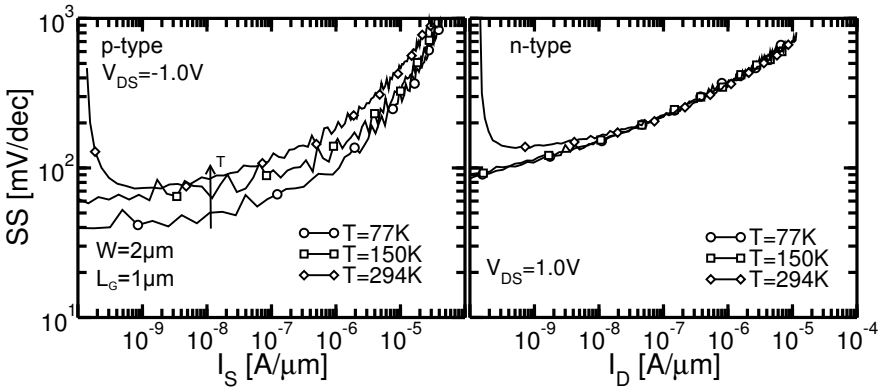

Figure 6.14: SS versus $I_{\rm n}$ curve for the TFET device in fig. 6.12 (whose trans-characteristics are reported in figs. 6.13-a and 6.13-b) biased in the p-type (plot a) or the n-type (plot b) configuration.

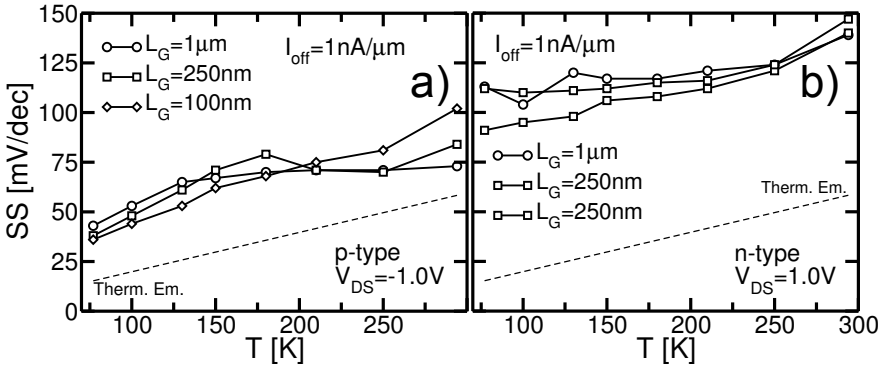

Figure 6.15: SS versus temperature curves for different gate lengths. The SS is computed at $I_{\rm p} = I_{\rm off} = 1{\rm nA}/\mu{\rm m}$ for the devices of fig. 6.12.

that increases by a factor x1.5 moving from 1μm to 100nm.

A further analysis of the device fabrication process carried out by CEA-LETI pointed out that in lot 3 the parasitic effect is due to a non-optimized fabrication process of the wafer. In fact it has been found that the raised N++ region is in-situ doped with Boron which should not be the case. In a following process step the source region has been donor doped via Arsenic implantation and then activated with annealing as sketched in fig. 6.17-a. Fig. 6.17-b qualitatively sketches the resulting band diagram just below the upper semiconductor/oxide interface, with the device biased in the p-type configuration. The band diagram refers to a Silicon homo-junction device, for the sake of simplicity, but the effect of hetero-junction does not change the validity of the analysis. At the source and at the drain there is a reservoir of holes, and this is the first requirement for having a thermionic injection for a p-type device. The N++ region forms a potential barrier for the holes in the parasitic p-type source that is modulated by the gate potential. As $V_{\rm GS}$ becomes more negative the barrier is lowered and the holes can flow in the device.

To evaluate the effectiveness of the Ω-gate in improving the electrostatics for a narrow W we have also measured a device with $W = 30$nm. Fig. 6.18 reports the trans-characteristics of the TFET devices of fig. 6.12 biased in p-type configuration (plot a) and in n-type configuration (plots b) at various temperatures ranging from $T = 77$K to $T = 294$K. The channel length and width are $L_{\rm G} = 50$nm and $W = 30\mu$m, respectively. The trans-characteristics match those

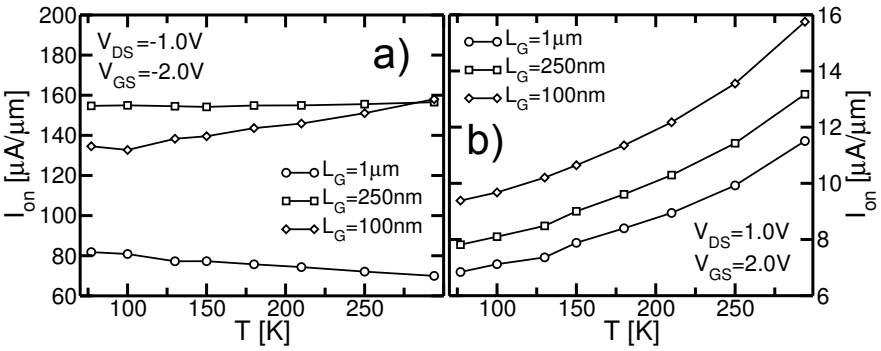

Figure 6.16: I_{on} versus temperature of the TFET devices of fig. 6.12 for different gate lengths. The I_{on} is computed at $|V_{DS}| = 1.0$V and $|V_{GS}| = 2.0$V. Plot a) and plot b) report the curves for the p-type and the n-type devices, respectively.

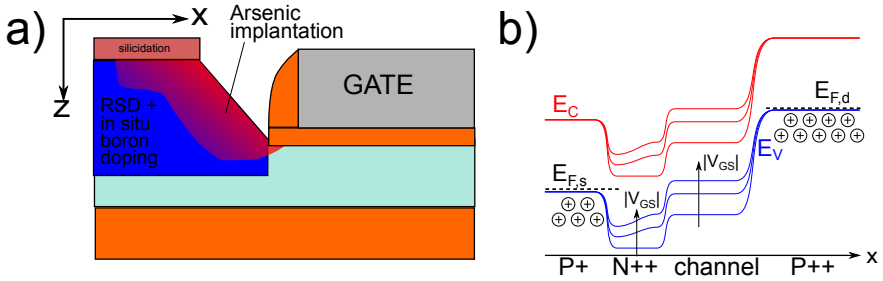

Figure 6.17: Qualitative sketch of the actual doping profile of the N++ region found in the TFET device of lot 2 (plot a) and the corresponding band diagram just below the upper semiconductor/oxide interface, for the TFET device biased in p-type configuration.

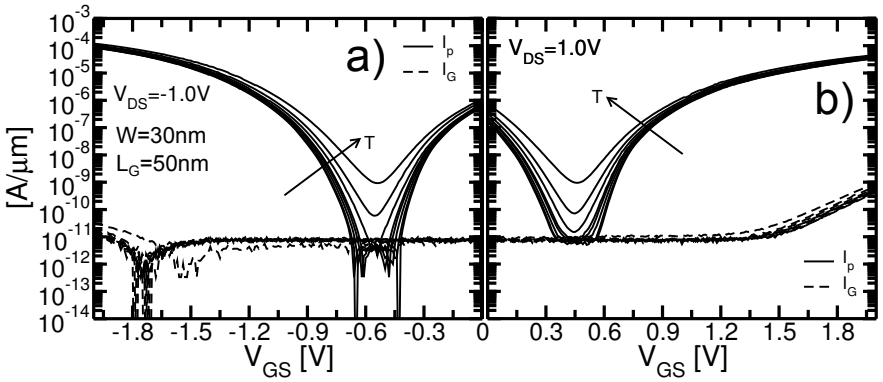

Figure 6.18: Trans-characteristics of the TFET devices of fig. 6.12 in p-type mode (plot a) and in n-type mode (plots b) at the temperature T=77K, 100K, 130K, 150K, 180K, 210K, 230K, 250K, 294K. $W = 30\mu$m and $L_G = 50nm$. The trans-characteristics of this device biased are typical of a TFET (fig. 6.8) in both pTFET and a nTFET mode.

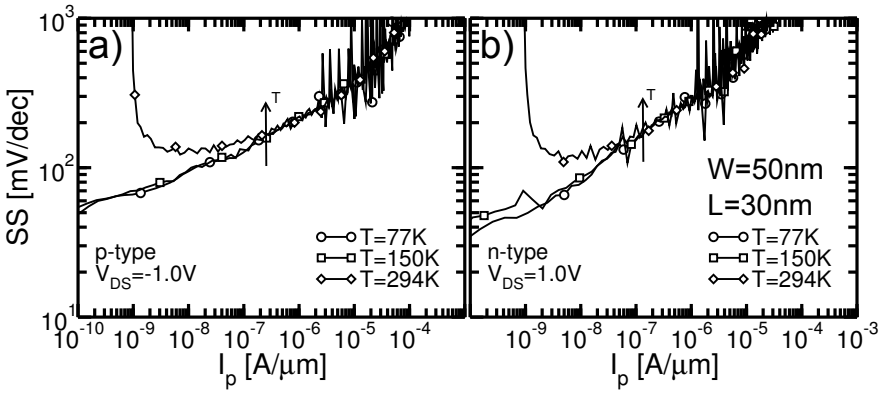

Figure 6.19: SS on I_p for the device of fig. 6.12 whose trans-characteristics are reported in fig. 6.18. Plot a) reports the curve for the pTFET biasing of the device whereas plot b) for the nTFET biasing. A weak dependence of the curves on the temperature is found and the curves are typical of a device where the main injection mechanism is BtBT both for the pTFET as for the nTFET biasing configurations.

expected from TFETs in both n-type and p-type configuration (figs. 6.8) Differently from the devices presented in fig. 6.13 at both the source and the drain tunneling junctions the carrier injection mechanism seems to be due to the same given the symmetrical behavior of the curve in the p-type and in the n-type mode. At low temperature a negligible dependence on the temperature is observed, whereas at higher temperature a more pronounced dependence takes place, possibly due to Trap Assisted Tunneling. This symmetrical behavior of the drain and source junction is further confirmed by fig. 6.19, where both n-type and p-type configuration behave as expected for a BtBT injection mechanism (fig. 6.3). This conclusion is confirmed by fig. 6.20, that reports the SS measured at $I_p = 100$pA/μm (plot a) and the I_{on} current measured at $|V_D| = 1V$ and $|V_{GS}| = 2$ (plot b) versus the temperature. For p-type and n-type configuration the SS and the I_{on} show a negligible dependence on temperature at low temperature (T<200K).

It is not clear to explain why the in-situ acceptor doping found in the N++ region of larger device seems not to affect the narrow device ($W = 30$nm) biased as a pTFET. The reported

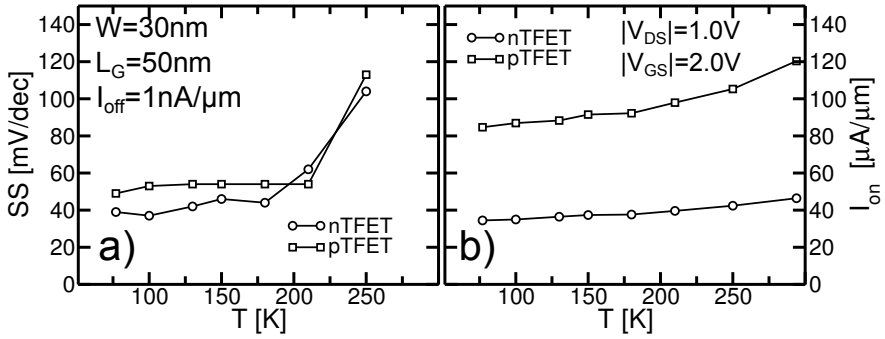

Figure 6.20: SS and I_{on} versus temperature for the devices of fig. 6.12 whose trans-characteristics are reported in fig. 6.18. Plot a) reports the SS computed at $I_{\text{p}} = 100\text{pA}/\mu\text{m}$ for the n-type and p-type biasing configuration of the device. Plot b) the I_{on} measured at $|V_{\text{DS}}| = 1.0V$ and $|V_{\text{GS}}| = 2.0V$.

measurements regard a single device and could not be repeated on other dies. It is therefore possible that the selected device represents a "lucky" sample and is not statistically meaningful. It is apparent however that, on the measured device, the evidence of a electron reservoir at the source exists whereas it cannot be found at the drain, where on the other hand evidence of a hole reservoir exists. Consistently the measured trans-characteristics, both for the p-type and n-type configurations, match those expected for a TFET, at low as well as at room temperature.

Tab. 6.2 reports a summary of the injection mechanisms that occurs in the measured devices of lot 3.

6.5 TFET characterization at low temperature (lot 4)

In this section we present the measurements concerning the TFET devices of a further batch fabricated by CEA-LETI research center in Grenoble. In this additional lot the the Boron in-situ doping in both the raised source and drain regions has been eliminated. The structure of the devices is the same presented in fig. 6.12.

Fig. 6.21 reports the trans-characteristics of the TFET devices of lot 4 having W=2μm and $L_{\text{G}} = 500\text{nm}$, 250nm and 100nm. We immediately see that the devices in n-type mode do not work properly since they have a tunneling current that is lower than the gate current and an unacceptably high SS. On the other hand the p-type configuration works well and demonstrates an $I_{\text{on}} \approx 10\mu\text{A}/\mu\text{m}$. Figs. 6.22 confirms a low dependence of SS on T and a low temperature behavior that matches the one expected if BtBT is the main injection mechanism.

Considering devices with a smaller W, given the Ω-gate configuration a better electrostatic control is expected. Fig. 6.23 reports the trans-characteristics of two devices of the lot 4 biased in p-type and n-type mode. The gate length is $L_{\text{G}} = 100\text{nm}$; the widths are $W = 50\text{nm}$ and $W = 30\text{nm}$, respectively. These results together with those of fig. 6.21, confirm that the reduction of the W in conjunction with the Ω-gated nanowire geometry improves the performances of the device.

We see in fig. 6.24-c that at low currents and low temperature ($I_{\text{p}} < 1\text{nA}/\mu\text{m}$ and T<130K) the SS is significantly reduced. Similar results are visible in fig. 6.24-b, where a reduction of the SS is observed for $I_{\text{p}} < 1\text{nA}/\mu\text{m}$. The reason for this behavior is not clear but it could be due to the fact that the maximum of the BtBT generation rate for electrons moves from the channel region in strained Si to the source region in SiGe in analogy with what exhibited by the Si/InAs nanowire TFET presented by Tomioka [8]. Additional experiments would be necessary to assess the actual reason for this change in the SS other experiments aimed at the

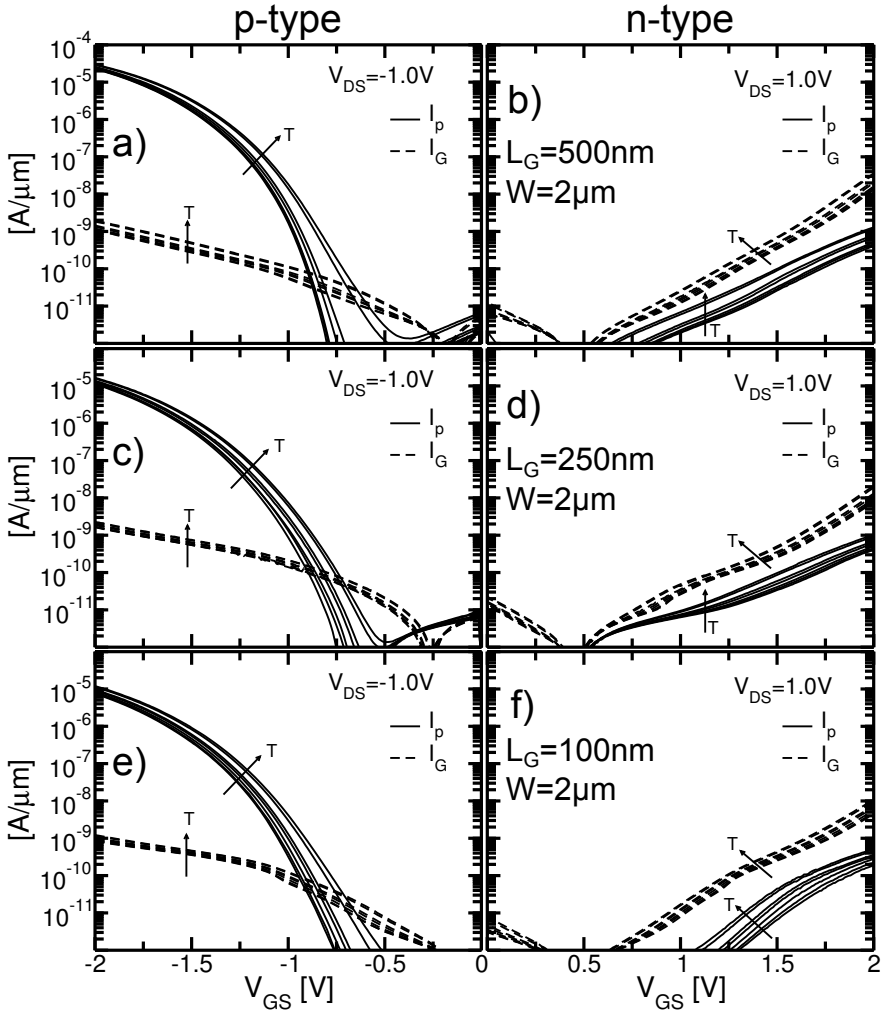

Figure 6.21: Trans-characteristics of three TFET devices of fig. 6.12 biased in p-type mode (plots a, c and e) and in n-type mode (plots b, d and f) at the temperature T=77K, 110K, 150K, 190K, 230K, 270K and 300K. The width $W = 2\mu$m is the same for all devices whereas the gate length $L_{\mathrm{G}} = 500\mathrm{nm}, 250\mathrm{nm}, 100\mathrm{nm}$.

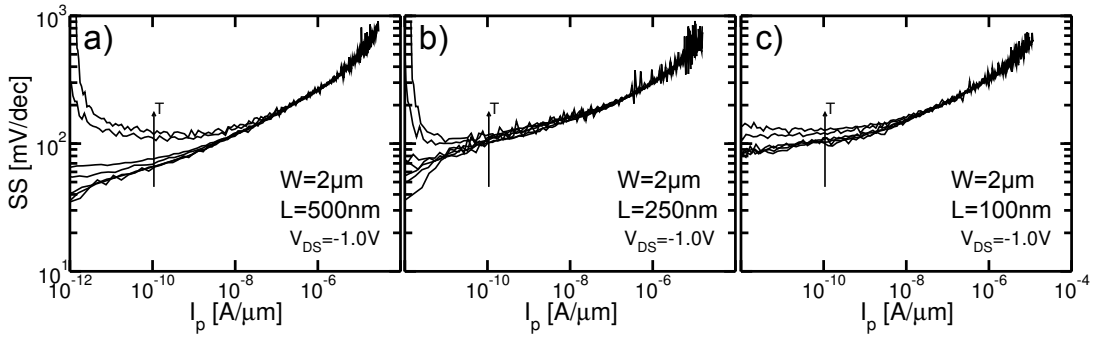

Figure 6.22: SS versus I_{D} curves for three TFET devices of lot 4, biased in p-type configuration at T=77K, 110K, 150K, 190K, 230K, 270K and 300K. The width $W = 2\mu$m is the same for all devices whereas the gate length is $L_{\mathrm{G}} = 500\mathrm{nm}, 250\mathrm{nm}, 100\mathrm{nm}$.

Table 6.2: Summary table reporting the injection mechanism occurring in the tunneling junctions of the TFET devices of lot 3 as suggested by the measurements reported in this section.

TFET Lot 3				
L [μm]	W [μm]	Junction	Temperature	Inject. Mech.
1	2	N++/channel	low	Therm. Em.
1	2	N++/channel	high	Therm. Em.
1	2	P++/channel	low	BtBT
1	2	P++/channel	high	BtBT+TAT
0.25	2	N++/channel	low	Therm. Em.
0.25	2	N++/channel	high	Therm. Em.
0.25	2	P++/channel	low	BtBT
0.25	2	P++/channel	high	BtBT+TAT
0.1	2	N++/channel	low	Therm. Em.
0.1	2	N++/channel	high	Therm. Em.
0.1	2	P++/channel	low	BtBT
0.1	2	P++/channel	high	BtBT+TAT
0.05	0.03	N++/channel	low	BtBT
0.05	0.03	N++/channel	high	BtBT+TAT
0.05	0.03	P++/channel	low	BtBT
0.05	0.03	P++/channel	high	BtBT+TAT

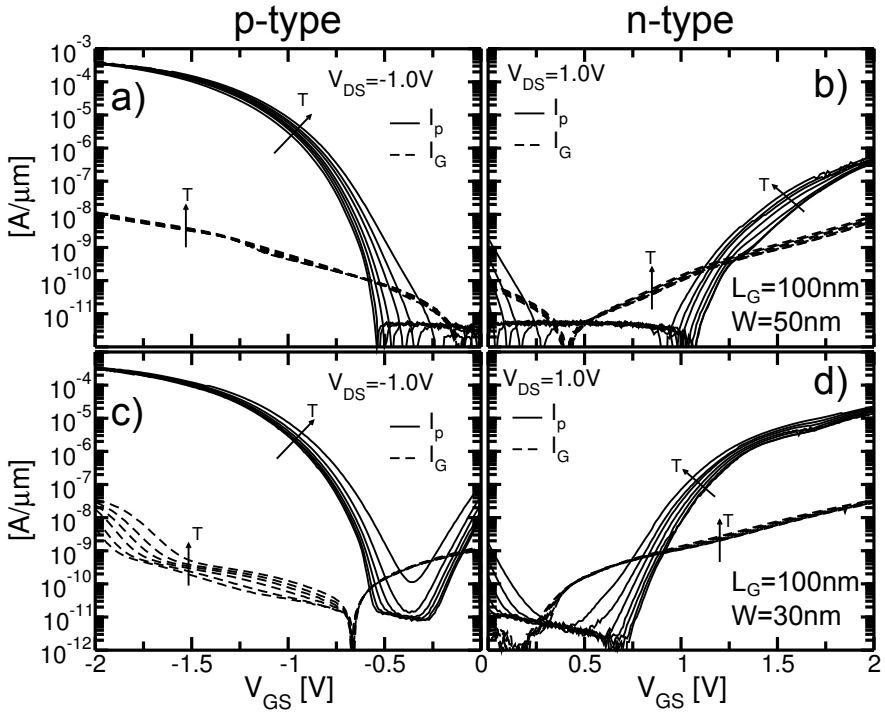

Figure 6.23: Trans-characteristics of two TFET devices of fig. 6.12 biased in p-type (plots a and c) and in n-type mode (plots b and d) at the temperature T=77K, 110K, 150K, 190K, 230K, 270K and 300K. The gate length is the same for both the (L_G = 100nm) whereas the width is equal to W = 50nm and W = 30nm respectively.

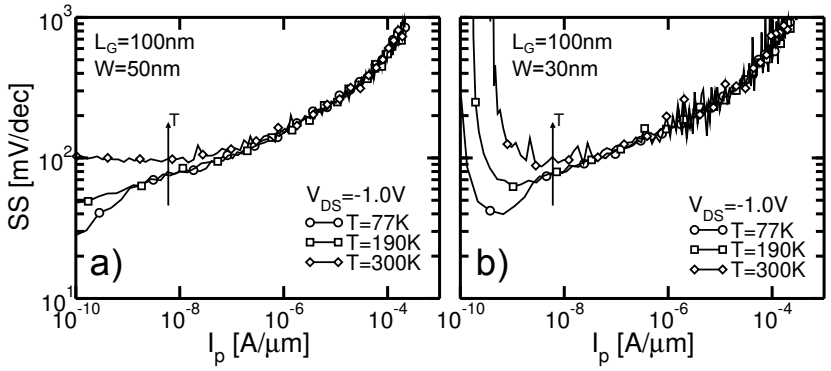

Figure 6.24: SS versus $I_{\rm p}$ curve for the TFET device in p-type mode of lot 4 with $L_{\rm G} = 100$nm and $W = 50$nm (plot a) and $W = 30$nm (plot b). $V_{\rm DS} = -1.0$V and the temperature is T=77K, 190K, 300K.

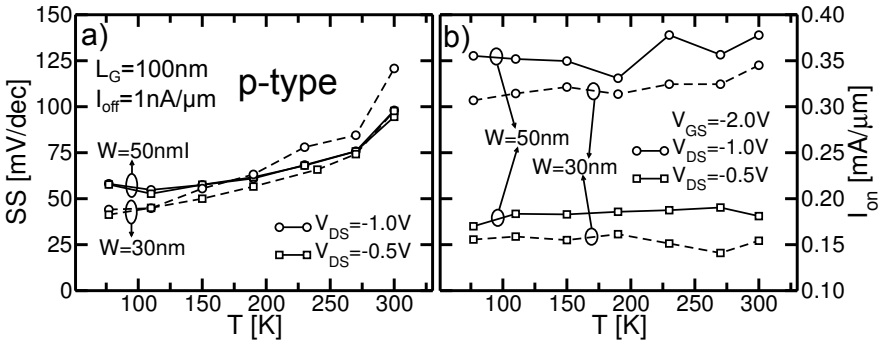

Figure 6.25: SS measured at $I_{\rm D} = 1$nA/μm (plot a) and $I_{\rm on} = I_{\rm D}$ measured at the $V_{\rm GS} = -2.0$V (plot b) over T. The measurements are reported for both the device with $W = 30$nm and $W = 50$nm considering $V_{\rm DS} = -1.0$V (circles) and $V_{\rm DS} = -0.5$ (squares).

determination of the actual position of the source/channel hetero-junction and doping junction and of the typology and amount of strain in the channel and the source region.

Fig. 6.25 summarizes the SS and $I_{\rm on}$ performance of lot 4 devices with $L_{\rm G} = 100$nm and $W = 50$nm and $W = 30$nm biased as p-type TFETs. The SS is measured at $I_{\rm p} = I_{\rm off} = 1$nA/$\mu$m with $V_{\rm DS} = -0.5V$ and $V_{\rm DS} = -1.0V$. For both the devices at low temperature ($T < 150$K) the dependence of SS on T is negligible. On the other hand for $T > 150$K the SS increases with an exponential trend, confirming again that at higher temperatures an additional injection mechanism sensitive to temperature occurs. Fig. 6.25-b reports $I_{\rm on}$ measured at $V_{\rm GS} = -2.0$V and $V_{\rm DS} = -0.5$V and $V_{\rm DS} = -1.0$V. Clearly the curves for $V_{\rm DS} = -0.5V$ are lower but for both the devices $I_{\rm on}$ clearly does not depend on temperature, suggesting that at high temperatures and with strong gate potential the main injection mechanism is indeed BtBT.

To analyze in more detail the effect of the width of the nanowire we have considered multi-channel TFET devices for different values of the single channel width. Fig. 6.26 reports the trans-characteristics of three devices with 75 channels of width $W = 60$nm, 50nm and 40nm and channel length $L_{\rm G} = 500$nm. The p-type devices are not significantly affected by the reduction of W. On the other hand when biased in n-type mode the reduction of the W remarkably improves the characteristics, making devices more symmetrical.

A possible explanation for the improved performance of small W device in n-type configuration is related to the doping profile of the p++ region. Ion implantation is performed to

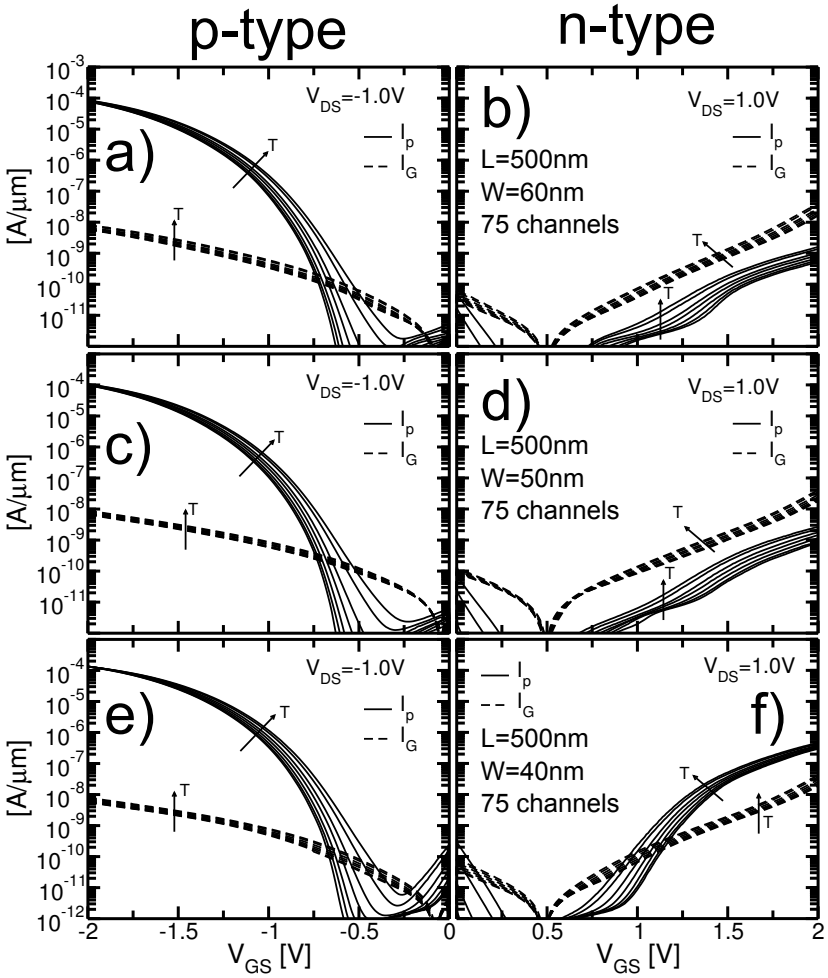

Figure 6.26: Trans-characteristics of three multi-channel TFET from lot 4 biased in p-type (plots a, c and e) and in n-type mode (plots b, d and f) at the temperature T=77K, 110K, 150K, 190K, 230K, 270K and 300K. $L_G = 500$nm. The number of channels is 75, whereas the width of the single channel is $W = 60$nm, $W = 50$nm, $W = 40$nm.

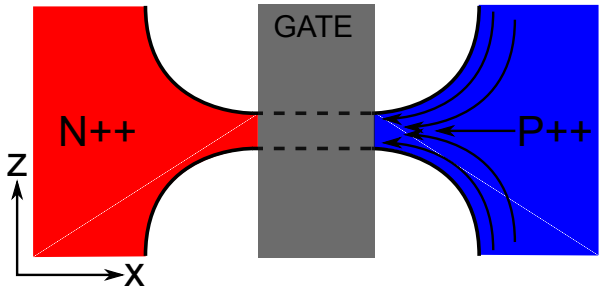

Figure 6.27: Schematic representation of the acceptor dopant diffusion during the annealing that follows the ion implantation step.

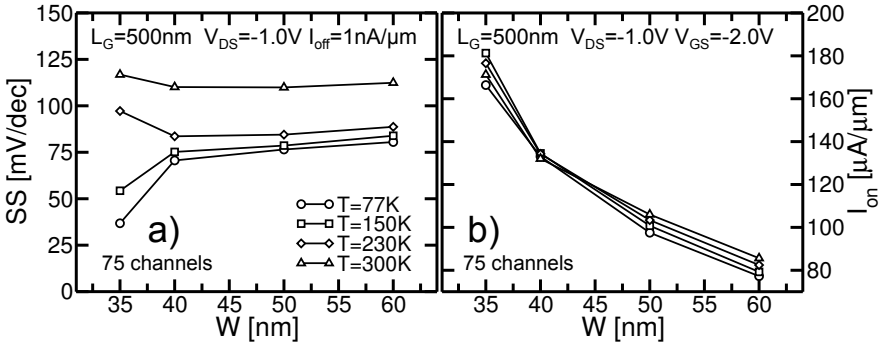

Figure 6.28: SS and I_{on} over the width W of the single channel considering multi-channel devices of lot 4. SS is measured at $I_{\text{D}} = I_{\text{p}} = I_{\text{off}} = 1\text{nA}/\mu\text{m}$ with $V_{\text{DS}} = -1.0\text{V}$ and the I_{on} is measured at $V_{\text{GS}} = -2.0\text{V}$ and $V_{\text{DS}} = -1.0V$.

create the N++ and P++ after the raised source and drain epitaxial growth. During the following annealing step many physical effects modify the doping profile in n-type and p-type semiconductor regions, such as the diffusion of the acceptor (Boron) and the donor (Arsenic) in the semiconductor lattice with different velocities [9, 10, 11, 12]. A possible explanation for the different performance of the wider and narrower devices is given by the fact that, as represented in fig. 6.27, in narrow nanowire devices the doping atoms during the annealing diffuse and tend to concentrate in the region near the channel, making the doping profile sharper at both junctions. A comparison between the n-type trans-characteristics in figs. 6.13 and 6.21 suggests that the Boron in-situ doping of the p++ region followed by Boron ion implantation (lot 3) allows for better performance of the n-type configuration with respect to the devices of lot 4 where the $Si_{0.7}Ge_{0.3}$ raised source and drain regions are grown undoped and the p++ region is doped by Boron ion implantation. This is also confirmed by results in fig. 6.18 where p-type and n-type configurations show almost symmetrical behavior. However a clearer picture of the structure of the devices requires other experiments, not-so-easy measurements of the the profiles at the junctions as well as the strain profile measurements. These experiments go far beyond the aim of this thesis work.

6.6 TFET characterization at low temperature (lot 5)

The characterization work has eventually focused on a lot of TFET devices with $Si_{0.7}Ge_{0.3}$ raised source and drain and compressively strained $Si_{0.8}Ge_{0.2}$ channel obtained through Germanium enrichment of a Silicon layer, as schematically represented in fig. 6.29 [2]. These devices have

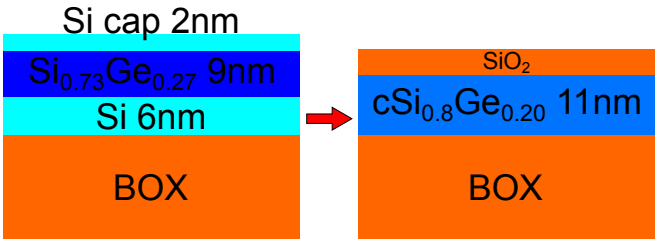

Figure 6.29: Schematic representation of the Germanium Enrichment process used to fabricate a single layer of compressively strained $Si_{0.8}Ge_{0.2}$ over Insulator starting from a layer of $Si_{0.7}Ge_{0.3}$ between two layers of Silicon.

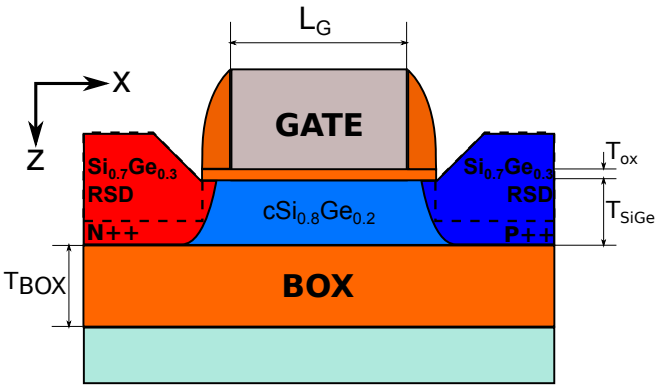

Figure 6.30: Sketch of the FD-SOI TFET devices of lot 5. $T_{ox} \approx 1.42$nm, $T_{BOX} = 145$nm, $T_{SiGe} \approx 12$nm.

a nanowire Ω-gate geometry (as those of lot 4) and they are sketched in fig. 6.30.

Fig. 6.31 reports the trans-characteristics of three lot 5 TFETs, with $W = 2\mu$m and $L_G = 500$nm, 250nm and 100nm with a temperature that ranges from 77K to 300K. Comparing these measurements to those of lot 4 (fig. 6.21) a significant reduction of the on-state current (≈ 10nA/μm) is found for the p-type configuration. On the other hand the n-type configuration in figs. 6.21 and 6.31 shows a BtBT current that is lower or of the same order of magnitude of the gate current.

Lot 5 demonstrated a much lower yield than the one of lot 4, especially for narrow width devices ($W < 70$nm) featuring single or multiple channels. The only device that we found fully operational is a single channel one with a nominal width $W = 30$nm. The trans-characteristics of this sample in p-type and n-type configurations are reported in fig. 6.32 and show the record current performances for the p-type configuration with $I_{on} \approx 600\mu$A/μm.

For the same device fig. 6.33 reports the SS vs. I_p curve in p-type mode at $V_{DS} = -1.0$V for T=77K, 230K and 300K. At low temperature the device demonstrates very promising SS values (SS≈20mV/dec), but differently from the results in fig. 6.24 at low I_p a flat trend of the curves can be found, with a behavior similar to the one reported in fig. 6.3-a and typical of a MOSFET. This suggests that a the performance is spoiled by a parasitic MOSFET

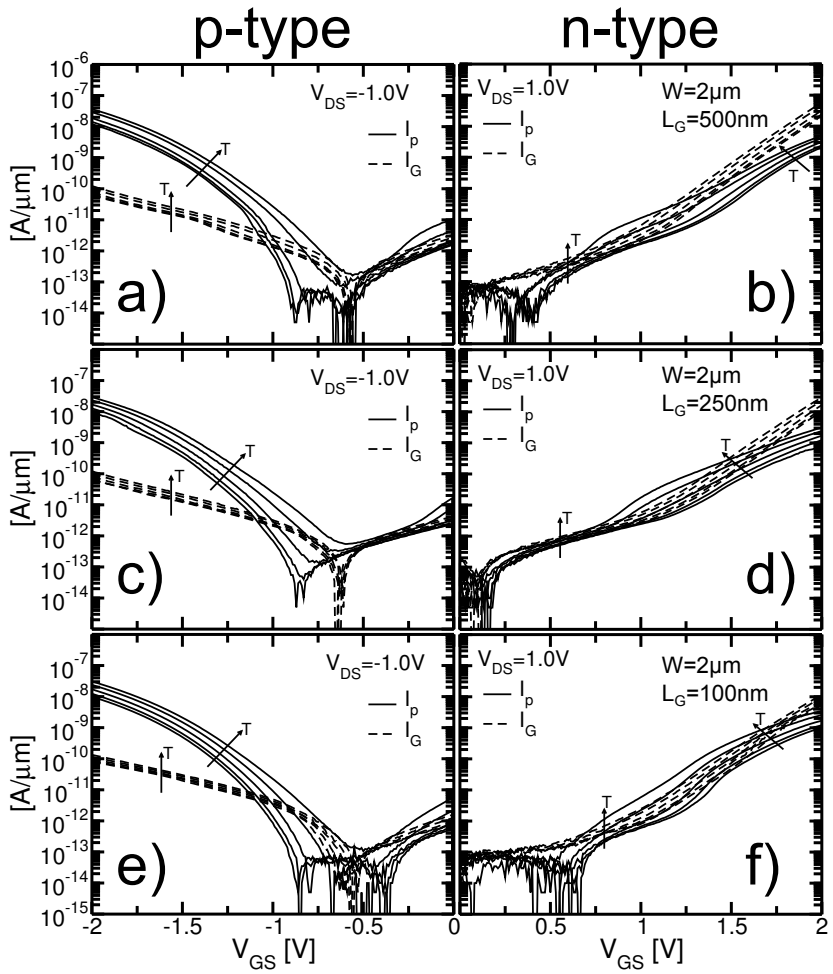

Figure 6.31: Trans-characteristics of three TFET devices of fig. 6.30 biased is p-type (plots a, c and e) and in n-type mode (plots b, d and f) at the temperature T=77K, 130K, 190K, 250K, and 300K. The width $W = 2\mu$m is the same for all devices whereas the gate length is different and equal to $L_{\rm G} = 500\text{nm}, 250\text{nm}, 100\text{nm}$.

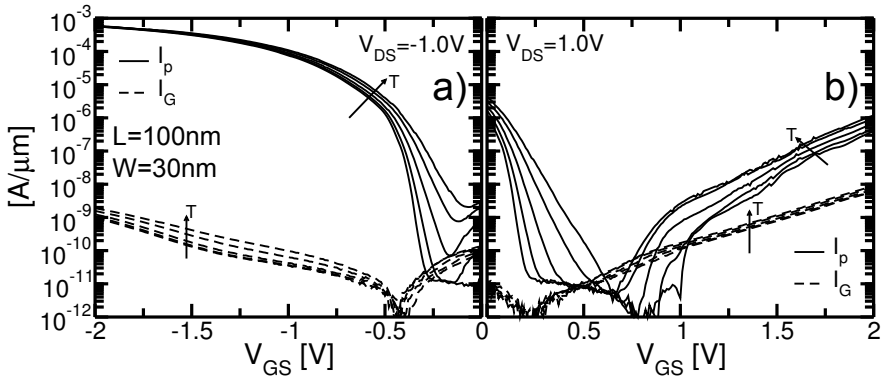

Figure 6.32: Trans-characteristics of the single channel TFET device in fig. 6.30, $L_{\rm G} = 100$nm and $W = 30$nm in p-type configuration (plot a) and n-type configuration (plot b). T=77K, 130K, 190K, 250K, and 300K.

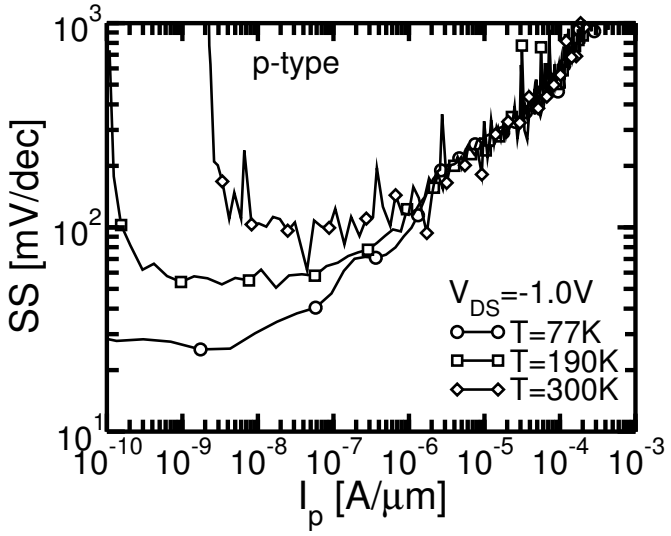

Figure 6.33: SS on I_p curve for the device of fig. 6.30 with $L_G = 100$nm and $W = 30$nm at $V_{DS} = -1.0$V for T=77K, 190K, and 300K.

In conclusion fig. 6.34 reports a comparison between lot 4 and 5 TFETs, in particular the I_{on} and SS performance of single channel device ($L_G = 100$nm and $W = 30$nm). This is the TFET with the best performance for both lots. The SS is measured at $I_D = 1\text{nA}/\mu\text{m}$ and $V_{DS} = -0.5V$ and the I_{on} at $V_{DS} = -1.0$V and $V_{GS} = -2.0$V. The SS has an exponential dependence on temperature, indicating the possible presence of a temperature dependent injection mechanism (e.g. TAT) in addition to BtBT. On the other hand for both lots, the I_{on} shows no significant dependence on temperature confirming that the BtBT is the dominant injection mechanism at higher voltages. As said above the yield of lot 5 is very low but fig. 6.34 shows that both the SS and the I_{on} are improved with respect to those exhibited by lot 4 TFETs.

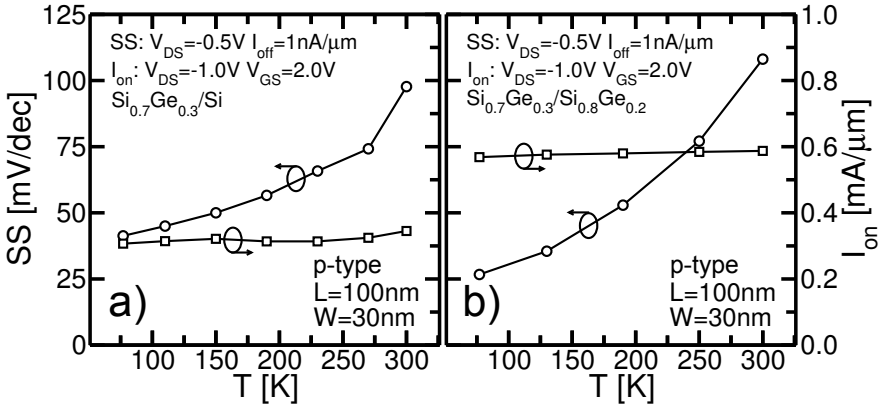

Figure 6.34: Comparison between the I_{on} and SS performance obtained by the device of lot 4 (plot a) and 5 (plot b) with single channel $L_G = 100$nm and $W = 30$nm.

6.7 Summary and Conclusions

In this chapter we have reported the experimental results obtained by measuring the low temperature trans-characteristics of planar FD-SOI MOSFETs and of planar hetero-junction TFETs

fabricated in five lots with two different mask. The measurements of MOSFETs and the TFETs from lot 1 and 2, respectively, have been taken as a reference. The measurements point out that for the large TFET devices of the lot 3 the N++/channel and the P++/channel junctions different injection mechanism can be found. In the former thermionic emission is the main injection mechanism suggesting the presence of a parasitic MOSFET in the device structure that is due to the presence of Boron in-situ doping in the epitaxially raised region in the side of the device that should be only donor doped.

On the other hand for the P++/channel tunneling junction the BtBT is the main injection mechanism. Scaling the width to $W = 30$nm improves the I_{on} and the SS performance.

Lot 4 TFETs have the exact structure of those of lot 3, but without in-situ Boron doped raised regions. These devices demonstrate the same injection mechanism in both the junctions.

Lot 5 TFETs have an hetero-structure with Ge enriched $Si_{0.8}Ge_{0.2}$ subjected to compressive strain and raised $Si_{0.7}Ge_{0.3}$ source and drain. Our measurements demonstrate that the introduction of the $cSi_{0.8}Ge_{0.2}$ channel entails an improvement of the I_{on} and SS performance.

However for all the measured TFET devices, at room temperatures, TAT seems to be the main parasitic effect that degrades the SS at low $|V_{\text{GS}}|$, but being a physical effect that strongly depends on temperature at low temperature it tends to switch off and only the BtBT current remains with steeper SS.

The measured I_{on} is quite high (0.6mA/μm at V_{DS}=1V and V_{GS}=2V) but the SS however never falls below the values for a conventional MOSFET at the same temperature, and this points out the necessity for a further research work focused on the electrostatic control improvement of planar TFETs and on the reduction of the defects and dislocations density that have a severe detrimental effect on the trans-characteristics and on the SS at low V_{GS}.

These conclusions are confirmed by the measurements on lot 4 and 5 TFETs that exhibit very interesting I_{on} for the p-type device but with a SS degraded by the presence of other generation mechanisms as the TAT. On the other hand n-type TFETs present very poor BtBT currents that are even inferior to the gate leakage currents, especially for the wider devices ($W > 100$nm). Considering lot 3 n-type TFETs their BtBT currents do not match those found in the pTFETs of lots 4 and 5 pTFET I_{on} but that are significantly better of those found for the nTFET of lots 4 and 5. This suggested that the P++ region in-situ Boron doping before the ionic implantation in the devices of lot 3 may have a beneficial effect on the performances of the n-type TFETs, because it probably makes the acceptor doping profile sharper in the nTFET source/channel junction.

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Chapter 7

Investigation on Electron Hole Bilayer TFET (EHB-TFET) through I-V measurements and simulations

In this chapter we will report a further experimental investigation carried out on planar UTB FD-SOI TFETs fabricated by the CEA-LETI research center in Grenoble with a strong bias applied on the back of the wafer. The goal of the experimental work is to analyze experimentally the idea proposed by Lattanzio et al. [1] to overcome this limitation, boosting the I_{on}. The idea is to replace the small horizontal tunnelling region at the source/channel junction with a vertical tunnelling region that covers the whole transistor body. The alignment of tunnelling direction and vertical electric field is achieved by back-gate biasing. In a double-gate TFET, the front and back gates can be biased with opposite polarities such as to induce an electron-hole bilayer in the channel area under the front gate, effectively extending the physical N^+ and P^+ source and drain terminals into the channel (see Fig. 7.1). In the resulting EHB-TFET, BTBT occurs vertically between the virtual bias-induced terminals. The clear advantage is that the tunneling surface becomes as large as the front gate area.

A series of articles reported the concept and predicted performance of Si and Ge EHB-TFETs obtained from extensive semi-classical simulations [2, 1, 3]. A later paper [4], based on a more refined Schrödinger-Poisson simulator coupled with a full quantum BTBT model, concluded that earlier expectations for I_{on} were overestimated by 2–3 orders of magnitude. On the other hand, Teherani *et al.* examined the details of band alignment and raised fundamental questions about the practicality of the EHB-TFET [5]. They argued that, due to size- and bias-induced quantization, prohibitively high gate voltages would be required, causing oxide reliability concerns.

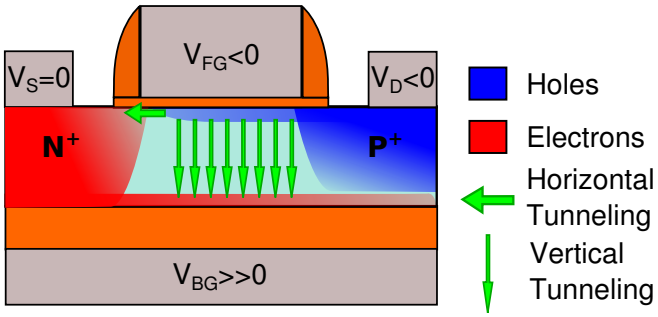

Figure 7.1: Sketch of the TFET biased with opposite potentials at the front gate and at the back gate (substrate) to form electron and hole layers. The arrows indicate the horizontal and the expected vertical BTBT transitions.

For BTBT to occur in TFETs several conditions need to be fulfilled:

i simultaneous formation of the proper band alignment and of the electron and hole layers in the channel,

ii strong vertical electric field leading to short tunneling distance,

iii significant overlap of the electron and hole wave-functions in the vertical direction.

Condition (ii) implies ultra thin film, which in turn affects requirements (i) and (iii). Semi-classical models, based on WKB approach [6], indicate that the BTBT generation rate increases exponentially in thinner films. However, in a strong vertical field, size- and field-induced quantization leads to the splitting of the valence and conduction bands into well-resolved subbands at energies above the band extrema $E_{C,min}$ and $E_{V,max}$, making band alignment more difficult to achieve, as shown schematically in Fig. 7.2. Furthermore, the lowest subband energies $E_{e,0}$ and $E_{h,0}$ are determined by the heaviest effective masses in the vertical direction, but this impedes (iii). A direct consequence is that semi-classical models are not fully reliable for modeling EHB-TFETs and more advanced approaches are requested, such as those reported in [7, 8].

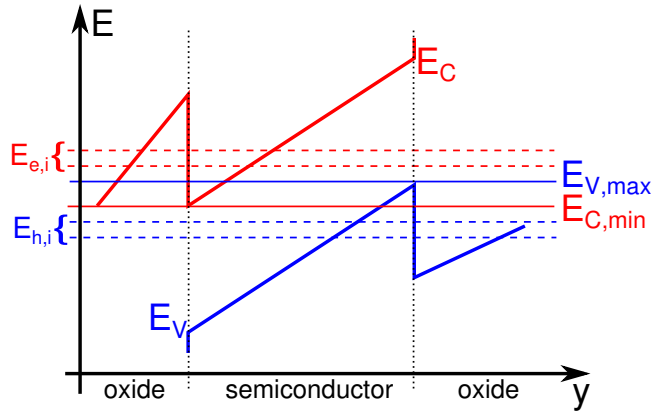

Figure 7.2: Splitting of the conduction and valence band in sub-bands in a double-gate (DG) structure with an opposite biasing of the front and the back gates. While the edges of conduction and valence bands are favorably aligned ($E_{\mathrm{V,max}} > E_{\mathrm{C,min}}$) the lowest valence subband $E_{\mathrm{h},0}$ still lays below the lowest conduction subband $E_{\mathrm{e},0}$, hence BTBT cannot take place.

Band alignment can eventually be achieved by increasing the vertical field (*i.e.*, the voltage drop V_{B} across the body). The efficiency of this method is modest, because the bias-induced quantization further separates the $E_{\mathrm{e},0}$ and $E_{\mathrm{h},0}$ subbands. In addition, a change in body voltage ΔV_{B} requires a much higher difference $\Delta V_{\mathrm{G,fb}}$ between the front and back gate voltages. Below 10 nm thickness, the efficiency rate $\Delta V_{\mathrm{B}}/\Delta V_{\mathrm{G,fb}}$ drops severely which means that higher gate voltages are needed [5]. This is not an option for several reasons: (i) it negates the main advantage of TFETs, which is low supply voltage operation, (ii) it increases significantly the gate tunneling current, which jeopardizes the SS and I_{off}, and (iii) it may even cause oxide breakdown.

Furthermore, the formation of the electron and hole bilayers in ultra thin films faces the 'supercoupling'effect [9]. Below a critical thickness, it is impossible to induce accumulation and inversion layers facing each other. One of the gates dominates and either electrons or holes fill the body, leading to volume inversion or volume accumulation. Supercoupling is a general size effect governed by the film thickness. Changing the materials, gate bias or buried oxide thickness only modifies the critical thickness by a few nm.

On the experimental side, given the significant research effort devoted to TFETs in recent years, it is troubling that no experimental confirmation for EHB-TFET operation has been reported to date. The aim of our work is to fill the experimental gap by measuring the vertical tunneling in several types of Si/SiGe fully-depleted SOI (FD-SOI) TFET devices. The experimental conditions are given in Section II and the measurements are reported in Section III, with no effective vertical BTBT current observed for any combination of front and back gate biasing. In view of the results obtained, we performed self-consistent quantum simulations to revisit the conditions needed for EHB-TFET operation. These results are discussed in Section IV.

7.1 Devices and measurement setup

Measurements have been carried out on three recent runs of FD-SOI TFETs, fabricated at LETI-CEA, which showed some of the best TFET performance reported to date.

The first variant (Design 1) has an ultra thin channel entirely composed of silicon with a thickness T_{Si}=6.3nm.

Designs 2 and 3 feature three-layer composite channels, as illustrated in Fig. 7.3: a lower Si

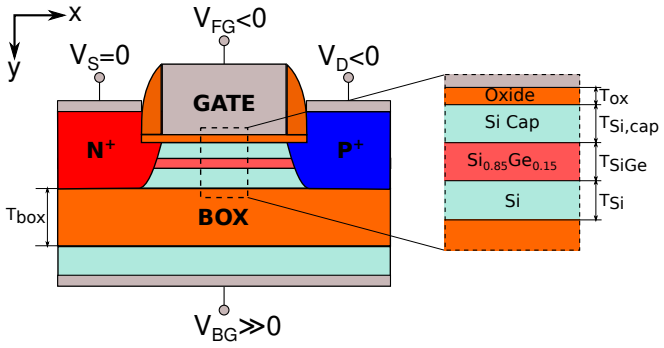

Figure 7.3: Sketch of the TFET structures tested in this work.

Table 7.1: Thickness of the material layers for the three considered TFET designs.

	EOT	T_{BOX}	T_{Si}	T_{SiGe}	$T_{\mathrm{Si,cap}}$
Design 1	≈1.2nm	145nm	≈6.3nm	0nm	0nm
Design 2	≈1.2nm	145nm	≈3.5nm	≈1.7nm	≈1.5nm
Design 3	≈1.2nm	145nm	≈3.5nm	≈9.6nm	≈1.5nm

layer of thickness T_{Si}=3.5 nm, a central compressively strained $Si_{0.85}Ge_{0.15}$ layer of thickness T_{SiGe} and an upper Si cap of $T_{\mathrm{Si,cap}}$ = 1.5 nm. The buffer Si serves for epitaxial growth of strained SiGe, whereas the Si cap achieves improved interface quality with the gate oxide. Designs 2 and 3 differ in the T_{SiGe} layer thickness, 1.7 nm and 9.6 nm, respectively.

For all designs, the gate dielectric is HfO_2 with an EOT≈1.2nm and the SiO_2 buried oxide is 145nm thick. The thicknesses of the various layers are reported in Table 7.1. Devices made from the three designs all had the same range of geometric dimensions W (gate width), L (gate length), and numbers of fingers, as reported in Table 7.2. We have chosen these FD-SOI devices because of their record I_{on} performance in TFET mode, reported in [10] and of their structure that permits to create an electron inversion channel at the back interface using a large V_{BG}, allowing us to study them in a EHB-TFET working mode.

The first Design is representative of a state-of-the-art Si FD-SOI technology. The introduction of the SiGe in Designs 2 and 3 results in enhanced BTBT given its reduced band gap and the highest I_{on} ever obtained for a Si/SiGe hetero-junction TFET.

The measurements have been performed using the semiconductor parametric analyzer HP4155A with a Karl Suss probe station. The devices have been biased in p-mode configuration: the N^+ region is considered as the TFET source (grounded) while the P^+ terminal is the drain biased with $V_{\mathrm{D}} < 0$. The front gate bias is negative $V_{\mathrm{FG}} \leq$0V. For the electrical field in the channel to have the dominant component in the vertical direction, needed for EHB-TFETs, a positive back-bias V_{BG} has been applied to the substrate.

Table 7.2: Geometric dimensions of the tested devices for all the three designs.

	L [μm]	W [μm]	Fingers	Ch. Area [μm^2]
Device 1	1	10	10	100
Device 2	0.5	10	20	100
Device 3	0.2	10	50	100
Device 4	0.1	10	10	10
Device 5	0.2	10	1	2
Device 6	0.15	10	1	1.5

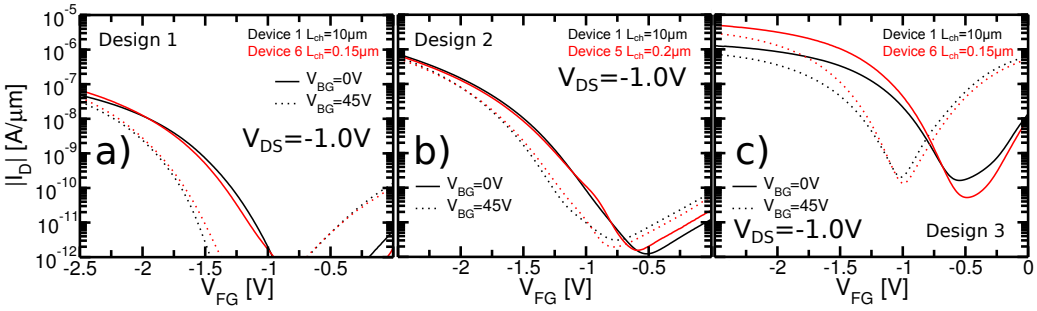

Figure 7.4: Trans-characteristics of small area ($A_{\mathrm{ch}} \approx 1.5\mu\mathrm{m}^2$) and large area ($A_{\mathrm{ch}}$=100$\mu$m^2) TFETs for all the three designs with back-gate biasing (V_{BG}=45V) and without.

7.2 Experimental results

Representative trans-characteristics for the 3 families of TFETs are shown in Fig. 7.4. Our goal is to identify the origin of the tunneling current. The sketch in Fig. 7.1 qualitatively illustrates the two possible BTBT mechanisms. Horizontal BTBT takes place from the source terminal to the channel region, whereas vertical BTBT occurs between the virtual accumulation and inversion layers of the EHB-TFET. Only the vertical BTBT requires back-gate biasing.

We first discuss the case of grounded substrate (V_{BG}=0V) for horizontal tunneling, which is the conventional mechanism in planar TFETs. The $I_{\mathrm{D}}(V_{\mathrm{FG}})$ curves in Fig. 7.4 are normally behaved. On the technology side, they confirm the advantage of SiGe channel for boosting the I_{on} and of ultra thin channel for reducing the OFF current. No significant impact of gate length is observed, except in Design 3 where the shorter TFET performs better, as explained by the potential drop in the lateral MOSFET channel at high current [11].

When a high positive V_{BG}= +45V bias is applied to the back gate, we simply note a lateral shift of the characteristics to the left. This effect is well known in FD SOI MOSFETs as interface coupling [12]: a positive V_{BG} increases the threshold voltage of the hole channel at the front interface V_{FT} by $\Delta V_{\mathrm{FT}}/\Delta V_{\mathrm{BG}} \simeq \mathrm{EOT}/T_{\mathrm{BOX}}$. In our case ($\mathrm{EOT}/T_{\mathrm{BOX}} \simeq 0.08$), the calculated shift is 350 mV, in good agreement with Fig. 7.4.

Another argument against vertical BTBT is given by the comparison of devices with very different channel (gate) area A_{ch}. Figure 7.4 shows characteristics for TFETs with A_{ch} changed by two orders of magnitude. Since the vertical BTBT scales with the channel area, the current in Device 1 (with A_{ch}=100μm^2) should be significantly higher than the one of Devices 5 or 6 ($A_{\mathrm{ch}} \approx 1.5\mu m^2$). For fair comparison of the different devices, we have considered a unique criterion of leakage current, I_{off}=6nA/μm, and measured the corresponding gate voltage $V_{\mathrm{FG}} = V_{\mathrm{FG,off}}$. We defined the ON current I_{on} for 1V voltage swing at $V_{\mathrm{FG,on}} = V_{\mathrm{FG,off}} - 1\mathrm{V}$. Figure 7.5 shows the normalized I_{on} current (accounting for gate width and number of fingers) measured for all designs, with and without positive back-gate biasing, as a function of gate area. In presence of a noticeable vertical BTBT current at V_{BG}=45V, the I_{on} should have increased linearly with the channel area. However, the curves in Fig. 7.5 are quite flat. These results suggest that vertical EHB current is completely absent or negligible with respect to the horizontal BTBT current between the source and the channel.

In order to maximize the possibility of observing vertical BTBT, we measured Design 3 TFETs at an even higher V_{BG}, up to 80V. Figure 7.6 shows the resulting transfer curves. Again, increasing V_{BG} even far beyond the threshold of forming an electron layer at the back interface does not lead to a higher I_{on}. Furthermore, the V_{BG} = 80V curve is smooth, whereas the combination of lateral and vertical BTBT would presumably lead to a kink in subthreshold characteristics, as schematically illustrated in the inset of Fig. 7.6 since the two tunneling mech-

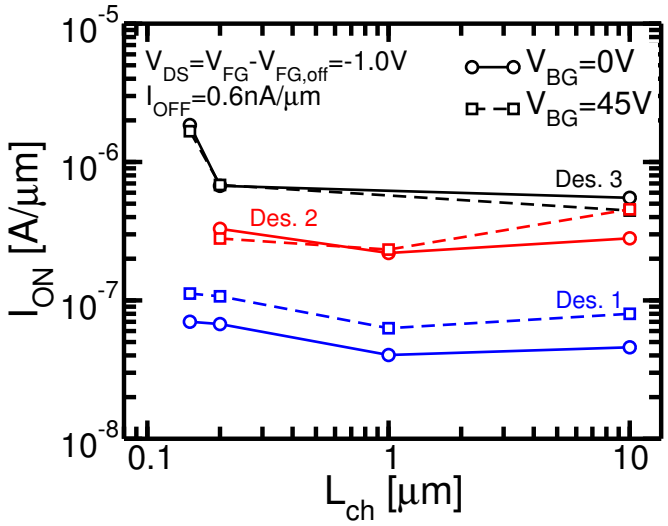

Figure 7.5: I_{on} current (per unit width) defined as $I_{\text{D}}(V_{\text{FG}} = V_{\text{FG,off}} - 1\text{V})$, where $V_{\text{FG,off}}$ is the V_{FG} voltage at which I_{D}=I_{off}=6nA/μm. Measurements with back-bias (dashed line) and without back-bias application (solid line) are compared.

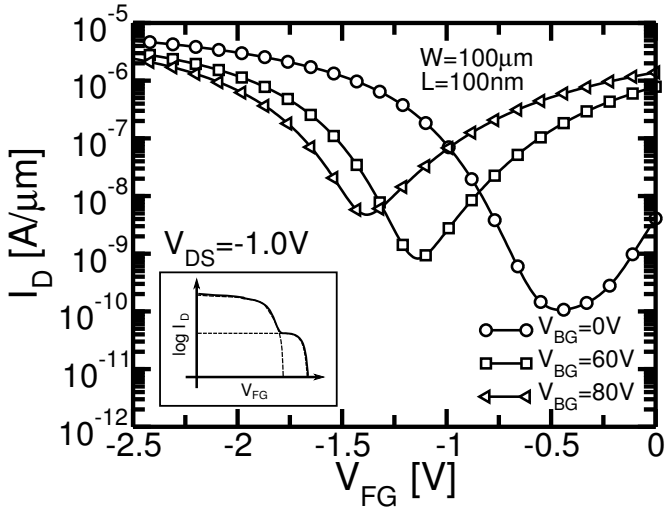

Figure 7.6: Trans-characteristics of Design 3 TFET measured at very high back-gate bias. For $V_{\text{BG}} = 80$ V the ON-current is smaller than for $V_{\text{BG}} = 0$V showing the absence of vertical tunneling. The inset shows schematically the kink in I-V curves expected from the transition from lateral to vertical tunneling.

anisms have different parameters. Moreover, quantization has different effect on the horizontal tunneling component with respect to the vertical one [13, 7, 4]. Due to effective mass quantization and strain, the valence band is split into multiple subbands and in presence of a strong contribution of a strong contribution of the vertical BTBT this should lead to the possible appearance of multiple kinks in the I_D-V_{FG}, reflecting the sequential alignment of the conduction and valence subbands as V_{FG} increases [14]. The smooth I_D-V_{FG}, even for V_{BG}=80V, indicates that the current is dominated by the horizontal BTBT near the source/channel junction.

7.3 Simulation results

A self-consistent 1D Schrödinger-Poisson simulator has been used to simulate the subband splitting in the vertical quantization direction of the multi-layer stack. The computation of the Schrödinger problem requires specifying the effective mass of electrons and holes, the band gap and the affinity of the materials. The vertical profiles of electrons and holes have been computed self-consistently with the wave-functions and the Fermi-Dirac statistics for 2D quantized gases [14]. These simulations give insight on the fulfillment or violation of the conditions for vertical BTBT. In this regard, a 1D approach is sufficient, since the electric field in the device is maximum in the vertical direction and almost constant over the entire channel area. Moreover since the EHB-TFET requires large channel area, and therefore large L_{ch} and W_{ch}, the quantization and corner effects in the plane normal to the tunneling direction can be neglected.

Alignment of the valence and conduction subbands. The simulations for Design 1 and 2 structures, given their thin channel thicknesses, show no possible alignment of the lowest conduction and valence subbands even when biasing the front and back gates with very high, unrealistic voltages (V_{BG}=100V). An example is given in Fig. 7.7 where only the band profiles (best case) are reported. Even ignoring quantization effects there is no chance of EHB tunneling in Design 1 (Fig. 7.7,e) or Design 2 (similar curves, not shown), since E_C at the back interface lies above E_V at the front interface. On the other hand, considering the lowest electron and hole subband for Design 3 for $V_{BG} \leq 60$V (Fig. 7.9,a) there is no intersection between the hole and the electron subbands for any potential V_{FG} between 0V and -2.5V. On the other hand, if $V_{BG} > 60$V a favorable alignment of the subbands can take place at $|V_{FG}| < 2.5$V, as discussed later. Regarding the bias conditions, it has been shown that the front-gate voltage can be reduced by tuning of the work-function [1]. The back-gate bias is of serious concern: even with very thin 25 nm BOX, V_{BG} will be in the 10V range, too high for practical applications. TFETs with FinFET structure and independent lateral gates may be a solution that requires experimental confirmation.

Existence of electron-hole bilayer reservoirs. The right panels in Fig. 7.7 show the carrier profiles computed with the Schrödinger-Poisson simulator along the quantization direction, at mid-distance between source and drain. The biasing potentials are V_{DS}=-1V, V_{FG}=-2.5V (strong accumulation of holes) and V_{BG}=50V and 80V. In Design 3*, which is identical to Design 3 but with thicker T_{sc} = 30nm (Fig. 7.7,b), there is clear formation of opposite layers of electrons and holes with very high concentrations ($\geq 10^{19}$cm^{-3}). For the experimental thickness of 15 nm in Design 3 (Fig. 7.7,d), the peak electron concentration barely reaches the intrinsic concentration in Si (10^{10}cm^{-3}). Even more dramatic is the case of ultra thin Designs 1 and 2 (Fig. 7.7,f), where the electrons vanish from the body and the holes spread along the whole channel thickness. These simulations confirm the so called "supercoupling" effect, first discussed by Eminente *et al.* [9]. For given gate biases, there is a critical film thickness below which electrons and holes cannot be accommodated together. The stronger gate bias imposes the body to host either electrons or holes. The bilayer simply transforms into a mono-layer excluding any vertical EHB tunneling.

Vertical electric field. Figure 7.8 shows the variation of the average value of the vertical field F_{av} with increasing back-gate bias, for V_{DS}=-1V, V_{FG}=-2.5V. In a thick film (T_{sc}=30nm, diamond symbols), the average field saturates as soon as the electron layer is formed at the

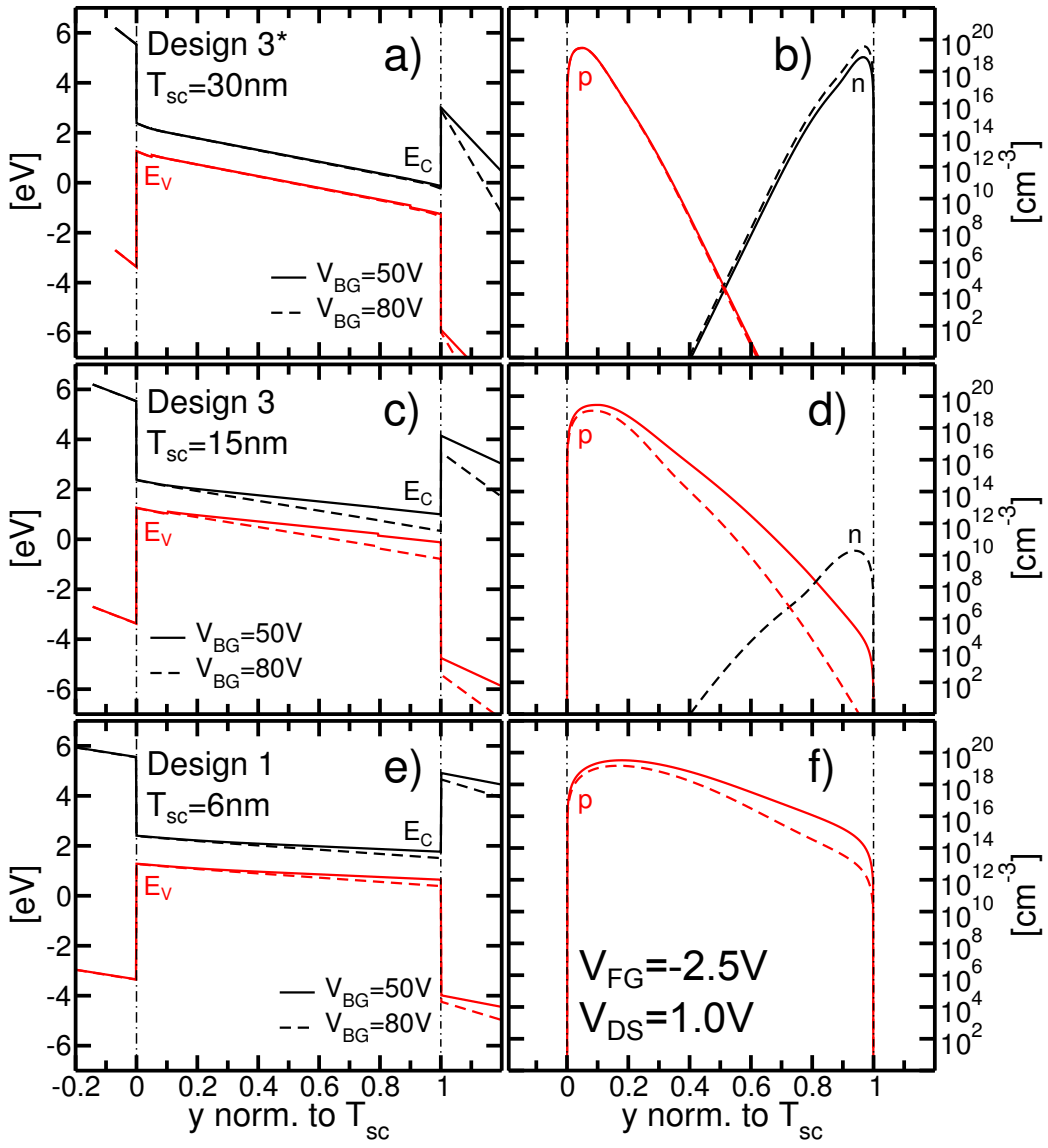

Figure 7.7: (Left panels a, c, e) Vertical profiles of the conduction E_C and valence band E_V along the quantization direction at the mid-point between source and drain. (Right panels b, d, f) Corresponding concentrations of holes p and electrons n versus normalized distance across the film. First row considers a variant of Design 3, (denoted Design 3*) with thicker semiconductor stack (T_{sc}=30nm). Second row corresponds to Design 3 with T_{sc}=15nm. The last row corresponds to Design 1 and encompasses the case of Design 2.

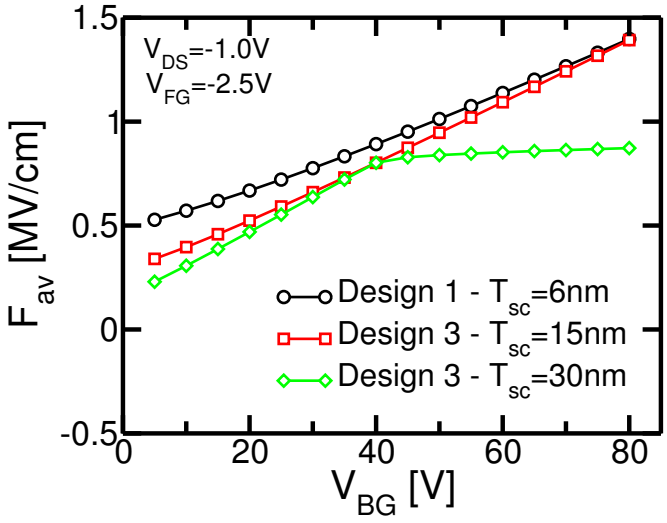

Figure 7.8: Average electric field along the quantization direction at mid-distance between source and drain for TFETs with Design 1 and Design 3 (with $T_{\rm sc}$=15nm and $T_{\rm sc}$=30nm).

back interface ($V_{\rm BG} > 40$V). There is no field saturation in the thinner structure ($T_{\rm sc}$=15nm, square symbols) because the super-coupling effect prevents the formation of the electron layer. The linear increase of the field with $V_{\rm BG}$ reflects a stronger bias-induced quantization and therefore a more pronounced subband splitting [5]. For $V_{\rm BG} = 80$V, the average field reaches $F_{\rm av} = 1.35$MV/cm which is of concern for device reliability.

BTBT, wave-function overlap and effective mass anisotropy. Effective BTBT requires strong overlap of the electron-hole wave-functions, in other words a short tunneling distance. According to Vandenberghe *et al.* [7], in indirect band gap semiconductors, the probability for transition between the l-th valence subband and the k-th conduction subband T_{lk} is proportional to the wave-function overlap I_{lk} as follow:

$$T_{lk} \propto \begin{cases} I_{lk} & \text{if } E_{\rm h,l} > E_{\rm e,k} \\ 0 & \text{otherwise} \end{cases} \tag{7.1}$$

with

$$I_{lk} = \int_0^{T_{\rm Si}} dy |\Psi_{h,l}(y)|^2 |\Psi_{e,k}(y)|^2 \tag{7.2}$$

where $\Psi_{h,l}$ and $\Psi_{e,k}$ are the normalized wave-functions of the l-th valence and of the k-th conduction subbands, respectively, and $E_{\rm h,l}$ and $E_{\rm e,k}$ are the corresponding subband energies (neglecting the phonon energies in phonon-assisted BTBT).

In order to estimate the probability for vertical BTBT, we focus on the transition between the lowest valence $E_{\rm h,0}$ and conduction $E_{\rm e,0}$ subbands. Figure 7.9,a shows the energy levels for same TFET structures as in Fig. 7.8. The value for $E_{\rm h,0}$ is fully governed by the strong accumulation condition at the front interface ($V_{\rm FG}$= -2.5V) and is practically insensitive to back-gate bias and film thickness. The decrease in electron subband energy with $V_{\rm BG}$ reflects the buildup of the electron charge [14]. For $T_{\rm sc}$=30nm, the inversion layer forms rapidly at the back interface and $E_{\rm e,0}(V_{\rm BG})$ variation has a steep slope $A_e = dE_{\rm e,0}/dV_{\rm BG} = 0.048$eV/V. This variation stops when the back electron channel reaches strong inversion ($V_{\rm BG}$=40). In thinner films, the buildup of the electron layer is slowed down by supercoupling (see also Fig.7.7d,f), reducing the rate at which the conduction subbands drop with $V_{\rm BG}$ ($A_e = 0.018$ for $T_{\rm sc}$=15nm and $A_e = 0.004$ for $T_{\rm sc}$=6nm). Note that slope A_e has a similar meaning as the efficiency

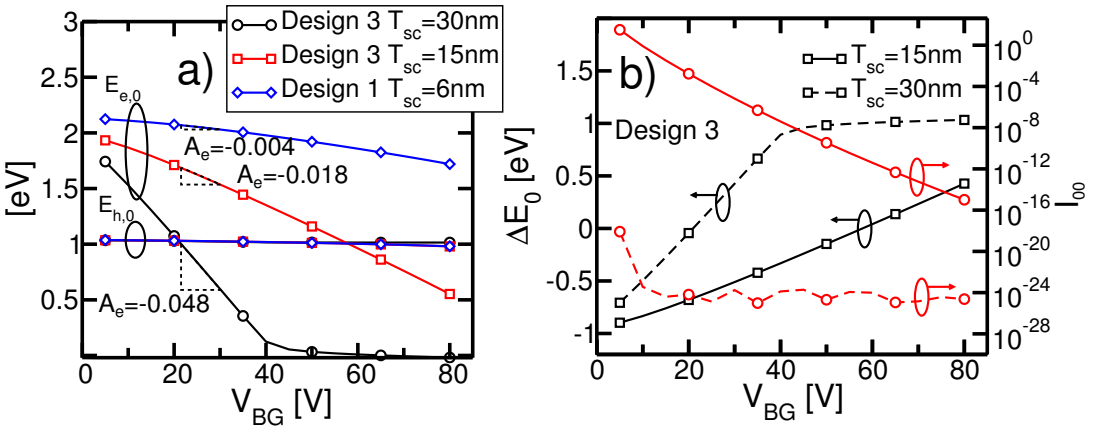

Figure 7.9: Influence of back-gate voltage on (a) energy levels of the highest valence subband $E_{\mathrm{h},0}$ and the lowest conduction $E_{\mathrm{e},0}$ subband and (b) energy difference $\Delta E_0 = E_{\mathrm{h},0} - E_{\mathrm{e},0}$ (square symbols) and overlap integral I_{00} (circle symbols). Various TFET designs, V_{DS}=-1.0V, V_{FG}=-2.5V.

rate $\Delta V_{\mathrm{B}}/\Delta V_{\mathrm{G,fb}}$ defined by Teherani *et al.* [5]. It follows that the presence of the bilayer is a necessary condition for vertical BTBT because it is the strong electron inversion and hole accumulation that allows the conduction and valence subbands to reach alignment.

Figure 7.9 shows the impact of the back-gate bias on the energy difference $\Delta E_0 = E_{\mathrm{h},0} - E_{\mathrm{e},0}$ (square symbols) and on the overlap integral I_{00} (circle symbols) for TFETs with Design 3 and 3* (best case). The transition between these two subbands is possible when $\Delta E_0 \geq 0$. (For large ΔE_0, other transitions between additional valence and conduction subbands with higher energy become also possible.) In the thicker Design 3* device (T_{sc}=30nm, dashed lines), favorable band alignment ($\Delta E_0 \geq 0$) is easily secured for V_{BG} ≥20V and due to the saturation of the accumulation layer at the back-gate ($V_{\mathrm{BG}} > 40$V) the value of $E_{\mathrm{h},0}$ cannot descend further. Unfortunately, the transition probability is negligible because of the insufficient overlap integral value I_{00} between the two wave-functions. This probability is higher by many orders of magnitude in the thinner TFET (T_{sc}=15nm, plain lines) at low carrier confinement, and decreases exponentially with the vertical field and V_{BG}. Since the band alignment is achieved at much higher voltage (V_{BG} ≥60V), the overlap integral I_{00}, and therefore, the transition probability becomes modest again. Additional simulations demonstrate very high overlap integral in ultra thin films (sub-10 nm thick as in Designs 1 and 2) but without the necessary band alignment for effective BTBT.

To rule out the possibility that it is the thick buried oxide that is responsible for the insufficient electron inversion layer at the back interface, we have simulated the exact Ge-channel structure proposed by Lattanzio et al. [2] at the mid-point between the source and drain. Figure 7.10,a shows the electron and hole densities in the vertical direction as a function of V_{FG} in the n-type configuration proposed in [2]. It has the same EOT=0.46nm for both front and back gate oxides, but we observe that as we increase $V_{\mathrm{FG}} > 0$V and, therefore, the electron inversion layer density is enhanced, at the same time the hole accumulation layer is reduced. This confirms that the super-coupling effect occurs in any ultra thin semiconductor channel, where one of the gates comes to dominate the other [9]. Additional confirmation is shown in Fig. 7.10,b, where we plot the lowest electron and hole subband energies as a function of increasing V_{FG}. For $V_{\mathrm{FG}} < 1$V both subband energies decrease, whereas for $V_{\mathrm{FG}} > 1$V the electron layer saturates and the subbands begin to approach each other, but even at $V_{\mathrm{FG}} = 2.5$V a favorable BTBT subband alignment is not achieved. Similar simulations for Si-channel TFET with symmetrical gate oxides reveal far more unfavorable conditions than for Ge-channel.

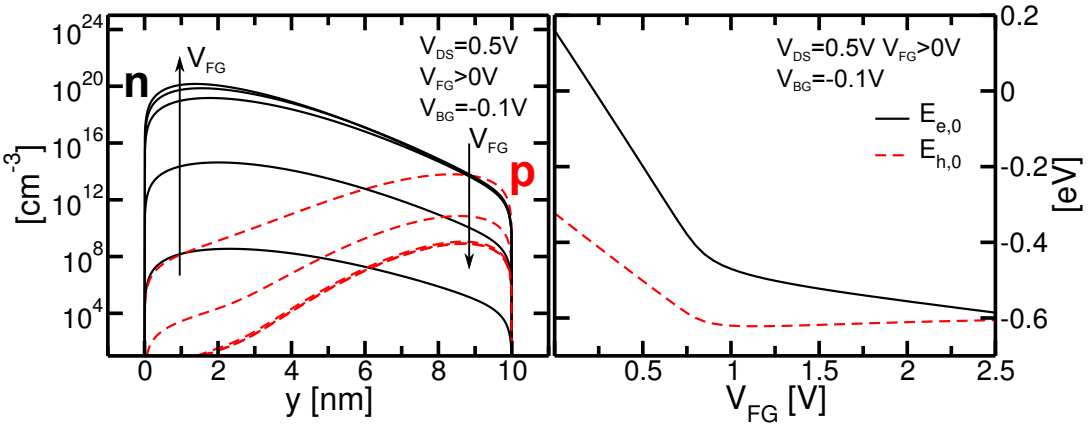

Figure 7.10: Plot (a) In-depth profiles of electrons (full lines) and holes (dashed) at the midpoint between source and drain for the symmetrical Ge TFET presented in [2] biased in n-type configuration. (b) Dependence of the lowest electron and hole subband energies. V_{DS}=0.5V, V_{BG}=-0.1V, EOT=0.46nm, $E_{\mathrm{wf,FG}}$=3.8eV, $E_{\mathrm{wf,BG}}$=4.64eV.

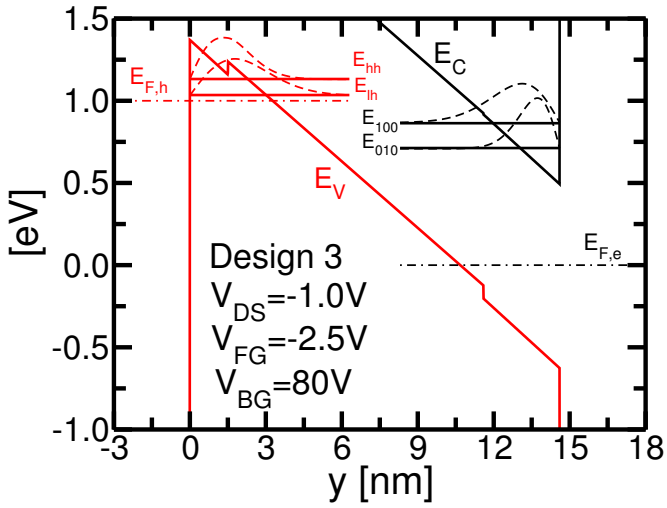

Figure 7.11: Profile of the valence and conduction band with V_{DS}=-1.0V, V_{FG}=-2.5V and V_{BG}=80V. The lowest subbands are computed for the light- and heavy-hole valence band valleys and for the Δ_{100} and Δ_{010} conduction band valleys. The corresponding wave-functions are also shown (dashed lines). For the wave-function the vertical scale is arbitrary but the horizontal scale is the same of the bands profile. The electron Fermi level is set as the zero of energy $E_{\mathrm{F,e}}$=0eV.

Another element that impedes the operation of the EHB-TFET device is the effect of the effective mass in the vertical quantization direction. The lighter the vertical effective mass, the larger the splitting of the subband energies and more difficult the alignment between valence and conduction subbands. Therefore a heavier mass is favorable for the subband alignment. On the other hand, heavy effective mass in the quantization direction reduces the penetration of the wave-function into the channel [15], and hence the wave-function overlap in Eq. 7.2. Figure 7.11 shows the profile of the valence and conduction bands and of the lowest light- and heavy-hole valley subbands together with the Δ_{100} and Δ_{010} conduction valley subbands

(ignoring the second eigen-energy of the heavier longitudinal electron effective mass for clarity). The corresponding wave-functions are also shown. The light hole mass is $m_{lh} = 0.16m_0$ and the heavy hole mass is $m_{hh} = 0.49m_0$. Considering [010] to be the quantization direction, Δ_{100} has the quantization effective mass $m_{c,y} = m_t = 0.19m_0$, whereas the Δ_{010} has $m_{c,y} = m_l = 0.91m_0$. The wave-functions corresponding to the heavier quantization masses form the ground state, but have the lowest overlap integral in eq. 7.2. The simultaneous fulfillment of both subband energy alignment and strong overlap of the wave-functions is therefore problematic.

7.4 Conclusions

Extensive measurements in TFETs with variable front gate area and channel architecture demonstrate that EHB vertical tunneling in ultra thin Si or Si/SiGe TFETs is difficult to achieve. The main experimental argument is the lack of scalability of the tunneling current with the gate area and the absence of kinks in the current-voltage characteristics.

Numerical simulations confirm the experimental conclusion and explain the reasons. It turns out that EHB tunneling is a complex problem with many competing issues. In principle, an ultra thin body is suited for achieving a narrow tunneling barrier and high tunnel current. This condition adversely affects the subband alignment due to size-quantization. The formation of the bilayer structure is also difficult without violating the super-coupling effect. Increasing the gate bias has a beneficial effect on the band alignment, but at the expense of very high, impractical vertical electric field. Furthermore, the effective mass anisotropy in Si and SiGe works against the wave-function overlap between the lowest energy subbands that determines the vertical BTBT. Thus, we believe that SOI or SGOI EHB-TFETs cannot work because the conditions for vertical BTBT cannot be fulfilled simultaneously. A design window may open in semiconductors with a lower band gap only if the key requirements (band alignment, ultra thin tunneling barrier, bilayer buildup, low vertical effective mass for both electrons and holes and reasonable fields) can intersect. Perhaps the problem does not have a solution. For example, in III-V compound semiconductor with a low band gap (e.g. InGaAs, InAs) the quantization effect is exacerbated by the small electron effective mass, making band alignment more difficult to achieve.

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Appendix A

2D full quantum phonon-assisted BtBT of UTB FD-SOI TFETs

A.1 Adaptation of 2D quantum model to FD-SOI TFETs

In this section we adapt the 2D full quantum phonon-assisted BtBT model of [1] to the special case of planar UTB FD-SOI TFETs where strong quantization effects occur in the vertical direction and carrier transport is possible only in the wafer plane. Considering a planar UTB FD-SOI TFET the BtBT transition is driven by the x component of the electric field $\mathbf{F}_{\mathrm{el},\mathbf{x}}(x,y,z)$ along the transport direction $\hat{x}$ that in the solution of the Schrödinger equation is characterized by open boundaries. We assume $\hat{z}$ as the quantization direction that is characterized by a narrow potential well. $\hat{y}$ is a direction of zero field and homogeneous conditions. Under these conditions according to the Effective Mass Approximation (EMA), the Schrödinger Equation for a particle with total energy E and a kinetic energy in the $\hat{y}$ direction $\hbar^2 k_y^2/2m_y$ can be written as:

$$\mathcal{H}_{\mathrm{c,v}}(k_y)\Psi_{k_y} = -\frac{\hbar^2}{2m_x}\frac{\partial^2\Psi_{k_y}}{\partial x^2} - \frac{\hbar^2}{2m_z}\frac{\partial^2\Psi_{k_y}}{\partial z^2} + U(x,z)\Psi_{k_y} = \left(E - \frac{\hbar^2 k_y^2}{2m_y}\right)\Psi_{k_y} \tag{A.1}$$

We search a solution by variable separation, i.e. we write Ψ_{k_y} as:

$$\Psi_{k_y}(x,z) = \Psi_{k_y,x}(x)\Psi_{k_y,xz}(x,z) \tag{A.2}$$

In a planar UTB device the potential $U(x,z)$ changes rapidly in the $\hat{z}$ direction and gradually in the $\hat{x}$ direction. Under these assumption eq. A.1 can be rewritten as:

$$\frac{\partial^2\Psi_{k_y,x}}{\partial x^2} + \frac{\partial^2\Psi_{k_y,xz}}{\partial z^2} \gg \frac{\partial^2\Psi_{k_y,xz}}{\partial x^2} + 2\frac{\partial\Psi_{k_y,xz}}{\partial x}\frac{\partial\Psi_{k_y,xz}}{\partial x} \tag{A.3}$$

Under these assumptions eq. A.1 can be rewritten as:

$$-\frac{1}{\Psi_{k_y,x}}\frac{\hbar^2}{2m_x}\frac{\partial^2\Psi_{k_y,x}}{\partial x^2} + \left[-\frac{1}{\Psi_{k_y,xz}}\frac{\hbar^2}{2m_z}\frac{\partial^2\Psi_{k_y,xz}}{\partial z^2} + U(x,z)\right] + \frac{\hbar^2 k_y^2}{2m_y} - E = 0 \tag{A.4}$$

The term between the square brackets can be integrated in z with closed boundary conditions thus obtaining:

$$-\frac{\hbar^2}{2m_z}\frac{\partial^2\Psi_{xz,l}}{\partial z^2} + U(x,z) = \varepsilon_l(x)\Psi_{xz,l} \tag{A.5}$$

and it yields an infinite number of eigenfunctions $\Psi_{xz,l}(x,z)$ with a corresponding infinite number of eigenvalues $\varepsilon_l(x)$ that have different values for each point x along the transport direction, but that do not depend on the value of k_y and of E. Consequently the eq. A.1 can be rewritten as:

$$\frac{\hbar^2}{2m_x}\frac{\partial^2\Psi_{k_y,x,l}(x;E)}{\partial x^2} + \varepsilon_l(x)\Psi_{k_y,x,l}(x;E) + \left(\frac{\hbar^2 k_y^2}{2m_y} - E\right)\Psi_{k_y,x,l}(x;E) = 0 \tag{A.6}$$

That must be solved for each value of E, k_y and l imposing open boundary conditions. The solution of eq. A.1 for the generic l-th subband can be approximated by:

$$\Psi_{k_y,l}(x,y;E) = \Psi_{k_y,x,l}(x;E)\Psi_{xz,l}(x,z;E) \tag{A.7}$$

We denote the diagonal part of the spectral function, for either the valence and conduction band, as $\tilde{A}(x,z,E) = A(\mathbf{r},\mathbf{r},E)$ with $\mathbf{r} = (x,z)$ and using eq. A.7 we can write:

$$\tilde{A}(x,z;E) = \sum_{k_y}\sum_{l}|\Psi_{k_y,x,l}(x;)\Psi_{k_y,xy,l}(x,z;E)|^2 \tag{A.8}$$

$$\approx \frac{W}{2\pi}\sum_{l}\int_0^{+\infty} dk_y|\Psi_{k_y,x,l}(E;x)\Psi_{xz,l}(E;x,z)|^2 \tag{A.9}$$

To compute the diagonal part of the spectral function for the valence band states $\tilde{A}_v(x,z;E)$, the effective masses $(-m_x,-m_y,-m_z)$ (negative) are set equal to the effective masses at the Γ point of the dispersion relation and the confining potential is $U(x,z)=E_{\mathrm{V}}(x,z)$, while for the diagonal part of the spectral function of the conduction band $\tilde{A}_c$ the effective masses are positive and correspond to the value for the destination valley whereas $U(x,z)=E_{\mathrm{C}}(x,z)$. The spectral function are strictly related to the Density of States (DoS) and can be used to calculate the charge density $\rho(\mathbf{r})$. In the case of a planar device $\rho(\mathbf{r})$ can be written as:

$$\rho(x,z)=\frac{qn_{\mathrm{sp}}}{W}\int\left[\tilde{A}_v(x,z;E)(1-f_v(E-E_{\mathrm{F,h}}))+\tilde{A}_c(x,z;E)f_c(E-E_{\mathrm{F,e}})\right]dE \tag{A.10}$$

The transmission probability is computed as:

$$T(E)=\Omega|M_{\mathbf{k_0}}|^2\iiint dxdydzA_{\mathrm{v}}(E;x,z)A_{\mathrm{c}}(x,z;E\pm\varepsilon_{\mathrm{op}}) \tag{A.11}$$

that can finally be rewritten as:

$$T(E)=|M_{\mathbf{k_0}}|^2\frac{\Omega W}{2\pi}\iint dxdz\int_0^{+\infty}dk_y\sum_l|\Psi^{(v)}_{k_y,l}(E;x)|^2|\Psi^{(c)}_{k_yl}(E\pm\varepsilon_{\mathrm{op}};x)|^2 \tag{A.12}$$

By the application of the Landauer formula it is eventually possible to obtain the expression of the Generation Rate:

$$\begin{aligned}G_{\mathrm{bbt}}(\mathbf{r})=&\frac{|\nabla E_{\mathrm{V}}(\mathbf{r})|}{\pi\hbar}\cdot\\&\cdot\left[\frac{|M_{\mathbf{k_0}}|^2\Omega WN_{\mathrm{op}}}{2\pi}\iint dxdz\int_0^{+\infty}dk_y\sum_l|\Psi^{(v)}_{k_y,l}(E_{\mathrm{V}}(\mathbf{r});x)|^2|\Psi^{(c)}_{k_yl}(E_{\mathrm{V}}(\mathbf{r})+\varepsilon_{\mathrm{op}};x)|^2\right]\cdot\\&\cdot\left[f_v\left(\frac{E_{\mathrm{V}}(r)-E_{\mathrm{F,h}}}{k_{\mathrm{B}}T}\right)-f_c\left(\frac{E_{\mathrm{V}}(\mathbf{r})-E_{\mathrm{F,e}}}{k_{\mathrm{B}}T}\right)\right]\end{aligned} \tag{A.13}$$

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Concluding remarks and future developments

This PhD thesis dealt with the modeling simulation and characterization of new TFET device for low power electronics. As a first step we have examined in detail existing BtBT models and we have adapted a Multi Subband Monte Carlo (MSMC) transport model for nanoscale MOSFETs to the simulation of TFETs with planar geometry by implementing the state-of-the-art semi-classical non-local models for phonon-assisted and direct Band to Band Tunneling (BtBT) generation mechanisms. A heuristic correction has been implemented to account for the significant quantum mechanical effects due to confinement that are expected to occur in UTB FD-SOI devices and that, if neglected, would result in a severe overestimation of the BtBT current flowing in the device.

The MSMC model has been extensively used to investigate a variety of UTB FD-SOI TFETs designs in Si, SiGe and III-V compound Semiconductor on Insulator (ScOI) TFETs. Special care has been given to the needs of an adequately accurate model calibration, including the often neglected band gap narrowing effects. This investigation puts in evidence that vertical scaling is effective in enhancing the on-state current of homo-junction and hetero-junction TFETs, due to the better electrostatic control that overtakes the negative impact of the carrier quantization. This holds for Si, Ge and SiGe alloys and in III-V compounds such as InAs and $In_{0.53}Ga_{0.47}As$ homo- and hetero-junction TFETs.

We also used the MSMC model to investigate a few device designs (a SiGe/Si FD-SOI hetero-junction TFETs and of a $In_{0.53}Ga_{0.47}As/In_{0.7}Ga_{0.3}As/In_{0.53}Ga_{0.47}As$ hetero-junction TFET) and to select the parameter values that optimize their performance. In the case of the InGaAs hetero-junction device also the strain effect on the band gap has been considered by a careful modeling of the band structure.

The second part of this thesis deals with the low temperature characterization of Si and SiGe homo- and hetero-junction devices fabricated by the french research center CEA-LETI. The experiments highlighted the effect of additional parasitic generation mechanisms in TFETs such as Trap Assisted Tunneling (TAT) that strongly limit the reduction of the subthreshold swing. Therefore strategies for the reduction of the defect density in the band gap, at the source junction, must be devised to improve the SS performance of the TFETs. Temperature measurements allowed us to discriminate if the dominant active injection mechanism working is indeed BtBT rather than thermionic emission.

We evaluated the advantages and the drawbacks of a new EHB-TFET device, by means of modeling and characterization of UTB FD-SOI TFET operated in double gate mode, with the two gates biased with opposite potentials. This work aimed to understand if the EHB-TFET concept was actually able to improved performance with respect to the planar TFET. Unfortunately our measurements and simulations demonstrate that performance improvement is really difficult to achieve for this device, due to the conflicting design requirements necessary on the one hand to reduce quantized subband splitting and on the other hand to attain strong wave-function overlap since both are needed for BtBT to occur.

The state-of-the-art of TFET fabrication and modeling was significantly improved in the last years through the work of many research groups leading to enhanced on-state current and with promising reduction of the measured subthreshold swing SS. Thanks to these efforts TFET is still the most promising candidate for replacing the traditional MOSFET at supply voltages $V_{DD} < 0.5$V. In fact, in this V_{DD} range it can exceed the power consumption performance of conventional CMOS devices in ultra low power applications provided SS < 60mV/dec at room temperature. Experimental TFET I_{on} and the SS are still far from the values required real competition with CMOS in for this application domain, but the results obtained with SiGe

hetero-junction and III-V compound TFETs are nevertheless promising.

From the experimental point of view, the most significant problem found in the fabricated TFETs, once that a high I_{on} has been achieved, is the TAT and efforts should be focused to improve the quality of the hetero-junction and to avoid as much as possible defect and dislocations at the interface between the two semiconductors. Alternatively also the reduction of the cross sectional area of the hetero-junction nanowire TFETs proved to be a viable strategy for the reduction of the TAT impact on TFET SS performance. Characterization effort aimed to the accurate estimation of the number of defects at the hetero-junction interface will be necessary to evaluate the effectiveness of the selected solutions to reduce the TAT rate.

From the modeling point of view instead, this thesis has demonstrated a good accuracy of the non-local BtBT models with a simple correction for the quantum carrier confinement in reproducing the performance of homo-junction and hetero-junction TFETs fabricated in III-V compound semiconductors and of Si homo-junction TFETs. Nevertheless, additional modeling work is required to better investigate TAT effect on SiGe hetero-junction TFET designs and to correctly reproduce BtBT in SiGe hetero-junction TFETs subject to strain, since there are still many physical aspects that are not perfectly understood in presence of strain such as, e.g. the variation of phonon energy and the deformation potential or the impact of the larger value of deformation potential in UTB FD-SOI device on BtBT, and that require to be investigated. Moreover it could be necessary to apply more fundamental approaches in modeling the BtBT in strained indirect band gap semiconductors.

It is also important to remember that even if a hypothetical TFET will reach $I_{on} > 10\mu A/\mu m$ and SS < 60mV/dec, variability will still be a serious concern for a device where any non-ideality entails an exponential effect on the I-V curves. Therefore it will be mandatory to control the TFET device variability. It will be another significant effort that the scientific community will have to face to bring the TFET concept to be an industrial standard.

In conclusion, the work carried out for this PhD thesis convinced the author that the state-of-the-art of the TFET is at a mid-point, where the first truly promising results have been recently shown demonstrating that this device is more than an interesting concept for ultra low power application. Nevertheless, there are still many physical aspects (TAT, Strain, etc.) that need to be clarified and investigated to achieve a clear picture of the TFET operation and to make this device a viable option available to the microelectronic industry to address the needs of ultra low power applications.

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