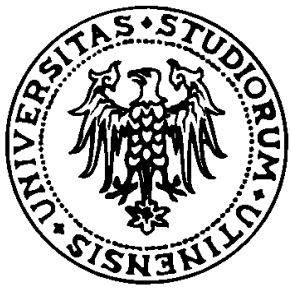

University of Udine

INDUSTRIAL AND INFORMATION ENGINEERING PHD PROGRAM

Doctoral Dissertation

Digital Control of Power Converters and Drives for Hybrid Traction and Wireless Charging

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Prof. Roberto Petrella

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Accademic Year 2014/2015

"*HARD WORK BEATS TALENT WHEN TALENT DOESN'T WORK HARD."*
(cit. KD)

Alla mia famiglia che mi ha sempre spronato a dare il meglio e alle persone che hanno sempre creduto in me.

ABSTRACT

In the last years environmental issues and constant increase of fuel and energy cost have been incentivizing the development of low emission and high efficiency systems, either in traction field or in distributed generation systems from renewable energy sources.

In the automotive industry, alternative solutions to the standard internal combustion engine (ICE) adopted in the conventional vehicles have been developed, i.e. fuel cell electric vehicles (FCEVs), hybrid electric vehicles (HEVs), plug-in hybrid electric vehicles (PHEV) or pure electric vehicles (EVs), also referred as battery powered electric vehicles (BEV).

Both academic and industry researchers all over the world are still facing several technical development areas concerning HEV components, system topologies, power converters and control strategies. Efficiency, lifetime, stability and volume issues have moved the attention on a number of bidirectional conversion solutions, both for the energy transfer to/from the storage element and to/from the electric machine side.

Moreover, along with the fast growing interest in EVs and PHEVs, wireless charging, as a new way of charging batteries, has drawn the attention of researchers, car manufacturers, and customers recently. Compared to conductive power transfer (usually plug-in), wireless power transfer (WPT) is more convenient, weather proof, and electric shock protected. However, there is still more research work needs to be done to optimize efficiency, cost, increase misalignment tolerance, and reduce size of the WPT chargers.

The proposed dissertation describes the work from 2012 to 2014, during the PhD course at the Electric Drives Laboratory of the University of Udine and during my six months visiting scholarship at the University of Michigan in Dearborn. The topics studied are related to power conversion and digital control of converters and drives suitable for hybrid/electric traction, generation from renewable energy sources and wireless charging applications. From the theoretical point of view, multilevel and multiphase DC/AC and DC/DC converters are discussed here, focusing on design issues, optimization (especially from the efficiency point-of-view) and advantages. Some novel modulation algorithms for the neutral-point clamped three-level inverter are presented here as well as a new multiphase proposal for a three-level buck converter. In addition, a new active torque damping technique in order to reduce torque oscillations in internal combustion engines is proposed here.

Mainly, two practical implementations are considered in this dissertation, i.e. an original two-stage bi-directional converter for mild hybrid traction and a wireless charger for electric vehicles fast charge.

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LIST OF ABBREVIATIONS AND ACRONYMS

ICE = Internal Combustion Engine

FCEV = Fuel Cell Electric Vehicle

HEV = Hybrid Electric Vehicle

PHEV = Plug-in Hybrid Electric Vehicle

EV = Electric Vehicle

BEV= Battery powered Electric Vehicle

DG = Distributed Generation

DER = Distributed Energy Resources

NP = Neutral Point

PWM = Pulse Width Modulation

SVM = Space Vector Modulation

SPWM = Sinusoidal Pulse Width Modulation

DSPWM = Double Signal Pulse Width Modulation

HPWM = Hybrid Pulse Width Modulation

DHPWM = Discontinuous Hybrid Pulse Width Modulation

IntPWM = Interleaved Pulse Width Modulation

FEM = Finite Element Method

DSP = Digital Signal Processor

1 INTRODUCTION

In this Section, firstly an overview of the background behind this dissertation and the main original contributions of that are given. Then, the contents of each chapter of the thesis are briefly described. Finally, a list of the author's publications is reported.

1.1 Background

In the last 10 years, the increasing cost of oil, consequently affecting the price per liter of fuel as clearly shown by **Fig. 1.1**, and Earth global warming due to greenhouse gases have incentivized the academic research, the authorities and thus the market in the development of higher efficiency and lower emission systems, in order to reduce the total fuel consumption and therefore its associated emissions of CO_2.

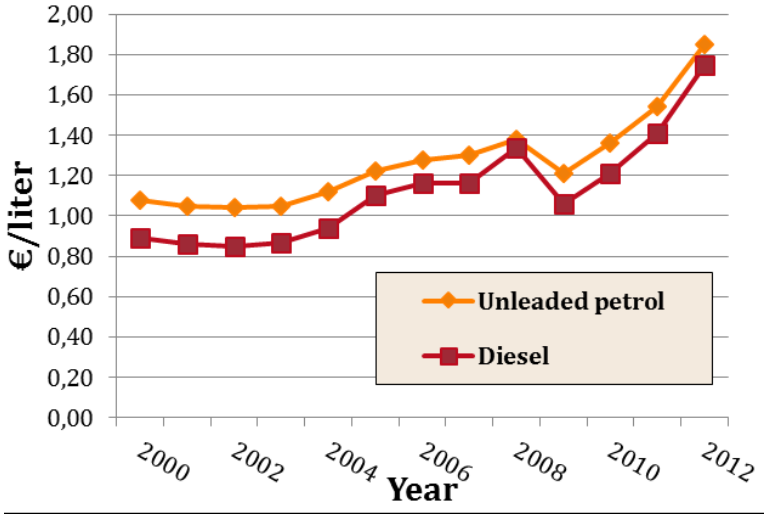


Fig. 1.1: Last 12-years average retail price chart in Italy (Source: www.economyonline.it).

Actually, the most involved fields by this technological revolution are the electricity generation systems and the field of transportation and mobility.

These two sectors are the main accountable of CO_2 global emission that are associated for about 45% to electricity generation and for about 30% to transport. Moreover, it should be noted that although the oil is not a renewable energy source, currently about 40% of the production world energy depends on oil and the level of dependence rises to about 80% in the transportation sector where the majority of vehicles is powered by an engine fueled by oil derivatives. In **Fig. 1.2** the distribution of CO_2 emissions in Europe during 2012 is presented. Germany leads this particular ranking with 23% of carbon dioxide emissions, followed by UK and Italy with 15% and 12 % respectively.

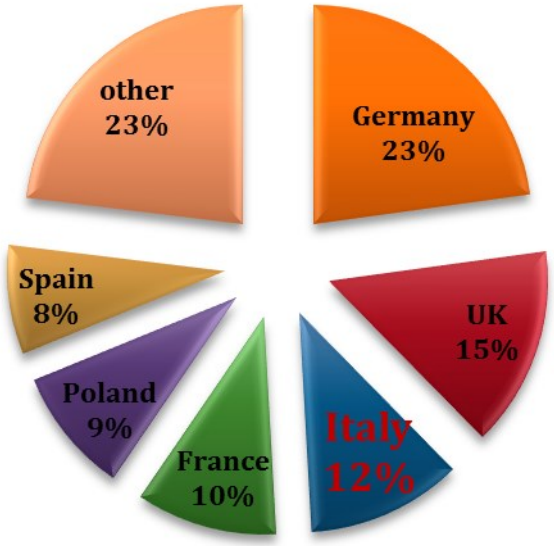


Fig. 1.2: 2012 European countries C02 emissions distribution (Source: Eurostat).

Talking about distribution of electricity, conventional power stations, such as coal-fired, gas and nuclear powered plants, as well as hydroelectric dams and large-scale solar power stations, are centralized and often require electricity to be transmitted over long distances, affecting overall efficiency and reliability. More recently, distributed generation (DG) has been growing up very fast. Decentralized energy is generated or stored by a variety of small, grid-connected devices referred to as distributed energy resources (DER) or distributed energy resource systems. DER systems are decentralized, modular and more flexible technologies that are located close to the load they serve, albeit having capacities of only 10 megawatts (MW) or less. DER systems typically use renewable energy sources, including, but not limited to, small hydro, biomass, biogas, solar power, wind power, geothermal power and increasingly play an important role for the electric power distribution system.

In the automotive industry, alternative solutions to the standard internal combustion engine (ICE) adopted in the conventional vehicles have been developed, i.e. fuel cell electric vehicles (FCEVs), hybrid electric vehicles (HEVs), plug-in hybrid electric vehicles (PHEV) or pure electric vehicles (EVs), also referred as battery powered electric vehicles (BEV), as presented in the classification of **Fig. 1.3**.

Both academic and industry researchers all over the world are still facing several technical development areas concerning HEV components, system topologies and control strategies. Efficiency, lifetime, stability and volume issues have moved the attention on a number of bidirectional conversion solutions, both for the energy transfer to/from the storage element and to/from the electric machine side.

Moreover, along with the fast growing interest in EVs and plug-in hybrid electric vehicles (PHEVs), wireless charging, as a new way of charging batteries, has drawn the attention of researchers, car manufacturers, and customers recently. Compared to conductive power transfer (usually plug-in), wireless power transfer (WPT) is more convenient, weather proof, and electric shock protected. However, there is still more research work needs to be done to optimize efficiency, cost, increase misalignment tolerance, and reduce size of the WPT chargers.

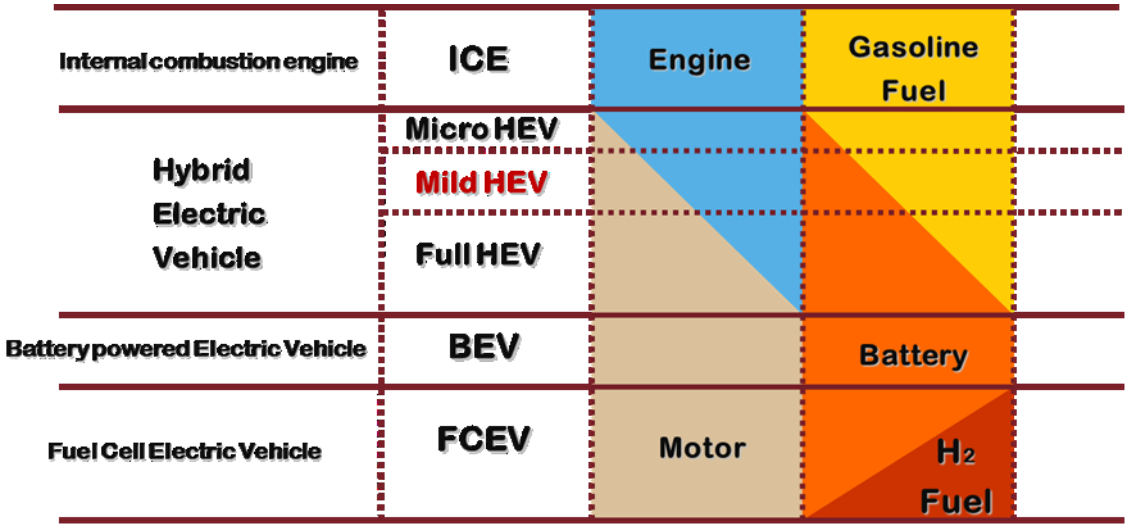


Fig. 1.3: Transition from ICE to EV chart.

1.1 Contribution of this work

The author's doctoral dissertation has been carried out at the Electric Drives Laboratory of the University of Udine from 2012 to 2014, during his PhD course. In addition, the author spent about six months as a visiting scholar at the University of Michigan in Dearborn, where he followed a specific project about wireless power transfer.

The topics discussed in this dissertation are related to power conversion and digital control of converters and drives suitable for hybrid/electric traction, generation from renewable energy sources and wireless charging applications. From the theoretical point of view, multilevel and multiphase DC/AC and DC/DC converters are presented here, focusing on design issues, optimization (especially from the efficiency point-of-view) and advantages. Some novel modulation algorithms for the neutral-point clamped three-level inverter are presented here as well as a new multiphase proposal for a three-level buck converter. . In addition, a new active torque damping technique in order to reduce torque oscillations in internal combustion engines is proposed here.

Mainly, two practical implementations are considered in this dissertation, i.e. an original two-stage bi-directional converter for mild hybrid traction and a wireless charger for electric vehicles fast charge.

1.2 Outline of the thesis

Hereafter, the contents of the each Chapter of the thesis are briefly described.

Chapter 2 illustrates the basic features of the 3-level neutral-point-clamped inverter, presents a review of the modulation strategies in literature and proposes some original algorithms. Furthermore, an accurate modeling and compensation of the dead time is presented as well as an analytical approach to loss calculation based on fundamental equations and power device datasheets.

Chapter 3 presents some non-isolated DC/DC converter topologies, in particular bidirectional and multilevel approaches. A novel multiphase three-level buck converter is proposed by the author.

Chapter 4 reports the description, implementation and prototype development of a two stage bi-directional converter suitable for battery charging and mild hybrid traction systems.

Finally, **Chapter 5** illustrates the basics of the inductive power transfer and presents the design of a 22 kW wireless charger for electric vehicles fast charge.

1.3 List of publications

Several parts of the work reported in this thesis have been published in the proceeding of well-known conferences. Hereafter, a list of these academic papers has been reported in chronological order.

[1] Bolognani, M.Morandin, R.Petrella, A.Pevere, S. Calligaro "Mild-Hybrid Traction System Based on a Bidirectional Half-Bridge Interleaved Converter and an SPM Motor Drive Fed by a 3-Level Active NPC Inverter," in *Proceedings of the Applied Power Electronics Conference and Exposition (APEC)*, Orlando (FL), USA, 02/2012.

[2] A.Pevere , R.Petrella , F. Pasut, S. Calligaro "Modulation techniques for three-phase three-level NPC inverters: A review and a novel solution for switching losses reduction and optimal neutral-point balancing in photovoltaic applications," in Proceedings of the IEEE Applied Power Electronics Conference and Exposition (APEC), Long Beach (CA), USA, 03/2013.

[3] A.Pevere , R.Petrella, S. Calligaro "Hybrid Modulation and Oprimal Neutral-Point Voltage Control for Three-Level NPC Inverters", in Proceedings of the Power Conversion and Intelligent Motion Conference (PCIM), Nuremberg (D), 05/2013.

[4] A.Pevere , R.Petrella "Discontinuous Hybrid Modulation Technique for Three-Phase Three-Level Neutral Point Clamped Inverters", in Proceeding of the IEEE energy Conversion Conference and Expo (ECCE), Denver (CO), USA, 09/2013.

[5] S.Bolognani, M.Morandin, R.Petrella, A.Pevere, S. Calligaro “Bidirectional PMSM Drive Employing a Three Level ANPC Inverter and a Multi-Phase Interleaved DC/DC Converter for Hybrid Electric Vehicles," in Proceedings of the IEEE Applied Power Electronics Conference and Exposition (APEC), Fort Worth (TX), USA, 03/2014.

[6] A.Pevere , R.Petrella "Interleaved Carrier-Based Modulations for Reducing Low-Frequency Neutral Point Voltage Ripple in the Three-Phase Neutral Point Clamped Inverter", in Proceedings of the IEEE Applied Power Electronics Conference and Exposition (APEC), Fort Worth (TX), USA, 03/2014.

[7] A.Pevere , R.Petrella, S. Zhou, C. C. Mi, "Design of a high efficiency 22 kW wireless power transfer system for EVs fast contactless charging stations", in Proceedings of the IEEE International Electric Vehicle Conference (IEVC), Florence (I), 12/2014.

[8] A.Pevere , R.Petrella, S. Zhou, C. C. Mi, "Novel Multiphase Interleaved Proposal for a Three Level Neutral Point Clamped Buck Converter", in Proceedings of the IEEE Applied Power Electronics Conference and Exposition (APEC), Charlotte (NC), USA, 03/2015.

2 THREE-LEVEL NPC INVERTER

2.1 Introduction

In many industrial applications higher power equipment has begun to be required in the last two decades. Some medium voltage motor drives and utility applications require medium voltage and megawatt power level. For a medium voltage grid, it is troublesome to connect only one power semiconductor switch directly. As a result, a multilevel power converter structure has been introduced as an alternative in high power and medium voltage situations. A multilevel converter not only achieves high power ratings in existing industrial systems, but in some cases also enables the use of renewable energy sources. Renewable energy sources such as photovoltaic, wind, and fuel cells can be easily interfaced to a multilevel converter system for a high power application.

Moreover, the latest progress in research and development of low-voltage power semiconductors, e.g. Silicon Carbide (SiC), Gallium Nitride (GaN), leads to extension of multilevel inverters from the medium to the low voltage range applications [4]. In-fact, in the low voltage range a lot of optimized switches are available. Therefore multilevel topologies could outperform the classical two-level inverter with fewer losses and higher virtual switching frequency, improving both efficiency and harmonic content.

Multilevel topologies, modulation and control strategies have been extensively researched in literature [1]-[47]. In the next subsections, firstly a brief history and a general presentation of the multilevel converter will be reported. After that, the three main multilevel topologies will be described, including main advantages and drawbacks of each one. Then, the dissertation will go more into detail about one of those three structures, i.e. neutral point clamped three level inverter, presenting a review and some original proposals for the NPC inverter modulation. Finally, an analytical approach for loss estimation and dead time compensation will be presented as well.

2.2 Multilevel converter history

The concept of multilevel converters has been introduced since 1975 [1]. The term multilevel began with the three-level converter [2]. Subsequently, several multilevel converter

topologies have been developed [1]-[47]. However, the elementary concept of a multilevel converter to achieve higher power is to use a series of power semiconductor switches with several lower voltage dc sources to perform the power conversion by synthesizing a staircase voltage waveform. Capacitors, batteries, and renewable energy voltage sources can be used as the multiple dc voltage sources. The commutation of the power switches aggregate these multiple dc sources in order to achieve high voltage at the output; however, the rated voltage of the power semiconductor switches depends only upon the rating of the dc voltage sources to which they are connected.

A multilevel converter has several advantages over a conventional two-level converter that uses high switching frequency pulse width modulation (PWM). The attractive features of multilevel converters can be briefly summarized as follows.

- They use switching devices at lower blocking voltage.
- They can reach higher efficiency.
- They can generate output voltages with extremely low distortion and lower dv/dt.
- They draw input current with very low distortion.
- They generate smaller common-mode (CM) voltage, thus reducing the stress in the motor bearings. If using advanced modulation strategies, CM voltages can be even eliminated.
- They can operate with a lower switching frequency.

2.3 Multilevel structures

Three main multilevel inverter structures have been applied in industrial applications, i.e. cascaded multi-cell converter with separate dc sources, diode clamped and flying capacitor configurations. Before examining in depth each multilevel structure, it should be mentioned that the term multilevel converter is utilized to refer to a power electronic circuit that could operate both in an inverter or rectifier mode. The multilevel inverter structures are the focus of in this chapter; however, the illustrated structures can be implemented for rectifying operation as well.

2.3.1 Cascaded multi-cells

The series H-bridge inverter appeared in 1975 [3], but several recent patents have been obtained for this topology as well [5]-[7]. Since this topology consist of several power conversion cells in series, the voltage and power level may be easily scaled. An evident disadvantage of this topology is the large number of isolated voltages required to supply each

cell. **Fig. 2.1** shows a general single-phase m-levels cascaded inverter, where every cell has been realized by a simple full-bridge converter with separate dc-link input source.

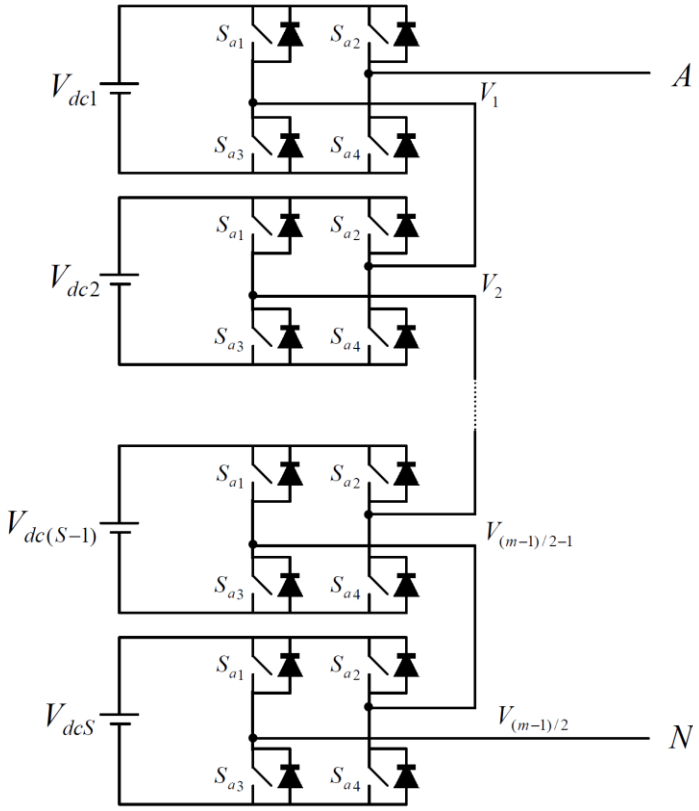


Fig. 2.1: Single-phase example of a multilevel cascaded inverter with m-levels.

However, the cells can be supplied by phase-shifted transformers in medium-voltage systems in order to provide high power quality at the utility connection [5].

Manjrekar has proposed a cascade topology that uses multiple dc levels, which instead of being identical in value are multiples of each other [8]-[9]. He also uses a combination of fundamental frequency switching for some of the levels and PWM switching for part of the levels to achieve the output voltage waveform. This approach enables a wider diversity of output voltage magnitudes; however, it also results in unequal voltage and current ratings for each of the levels and loses the advantage of being able to use identical, modular units for each level. The main advantages and disadvantages of multilevel cascaded H-bridge converters are as follows.

Advantages

- The number of possible output voltage levels is more than twice the number of dc sources ($m = 2s + 1$).
- The series of full-bridges makes for modularized layout and packaging. This will enable the manufacturing process to be done more quickly and cheaply.

Drawbacks

- Separate dc sources are required for each of the H-bridges. This will limit its application to products that already have multiple SDCSs readily available.

Recently, a modular multilevel converter (MMC) was proposed for HVDC applications. Instead of using full-bridge inverter units in the cascaded multilevel inverters, this new converter uses the P2 cells as the basic building block, same as the generalized multilevel topology in [11]. Therefore, MMC can naturally be derived from the generalized multilevel topology by removing the top part of the structure. Similar to the cascade multilevel inverters, the MMC cannot balance the capacitor voltage automatically when active-power is involved. Complicated control methods have to be used to balance the capacitor voltage.

2.3.2 Flying capacitor

Meynard and Foch introduced a flying-capacitor-based inverter in 1992 [10]. The structure of this inverter is similar to that of the diode-clamped inverter (described in the next subsection) except that instead of using clamping diodes, the inverter uses capacitors in their place. This topology has a ladder structure of dc side capacitors, where the voltage on each capacitor differs from that of the next capacitor. In **Fig. 2.2** a 4-level flying capacitor single-phase inverter topology has been depicted.

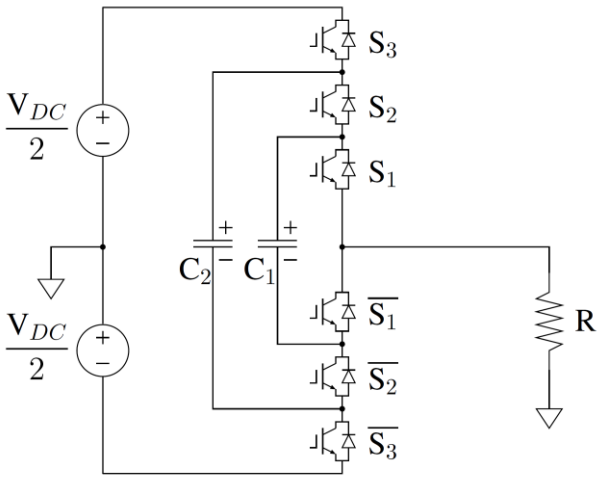


Fig. 2.2: Single-phase example of a flying capacitor inverter with 4-levels.

The voltage increment between two adjacent capacitor legs gives the size of the voltage steps in the output waveform.

One advantage of the flying-capacitor-based inverter is that it has redundancies for inner voltage levels; in other words, two or more valid switch combinations can synthesize an output voltage. Unlike the diode-clamped inverter, the flying-capacitor inverter does not require all of the switches that are on (conducting) be in a consecutive series. Moreover, the

flying-capacitor inverter has phase redundancies, whereas the diode-clamped inverter has only line-line redundancies [12]. These redundancies allow a choice of charging/discharging specific capacitors and can be incorporated in the control system for balancing the voltages across the various levels. In addition to the $(m-1)$ dc-link capacitors, the m-level flying-capacitor multilevel inverter will require $(m-1) \times \frac{m-2}{2}$ auxiliary capacitors per phase if the voltage rating of the capacitors is identical to that of the main switches. One application proposed in the literature for the multilevel flying capacitor is static-var generation [3]-[13]. The main advantages and disadvantages of multilevel flying capacitor converters are as follows.

Advantages:

- Phase redundancies are available for balancing the voltage levels of the capacitors.
- Real and reactive power flow can be controlled.
- The large number of capacitors enables the inverter to ride through short duration outages and deep voltage sags.

Disadvantages:

- Control is complicated to track the voltage levels for all of the capacitors. Also, pre-charging all of the capacitors to the same voltage level and startup are complex.
- Switching utilization and efficiency are poor for real power transmission.
- The large numbers of capacitors are both more expensive and bulky than clamping diodes in multilevel diode-clamped converters.
- Packaging is also more difficult in inverters with a high number of levels.

2.3.3 Neutral-point clamped

The first three-level diode-clamped inverter was proposed by Nabae, Takahashi and Akagi in 1981 [2]. Since the 90s several researchers published papers showing analytical studies and experimental results for three-, four-, five-, and six-level diode-clamped converters for applications such as static var compensation, variable speed motor drives, and high-voltage system interconnections. A three-phase three-level neutral point clamped (NPC) inverter is shown in **Fig. 2.3**. Each of the three phases of the inverter shares a common dc-link, which has been split by two input capacitors. The voltage across each capacitor is $\frac{V_{dc}}{2}$ and the voltage stress across each switching device is also limited to $\frac{V_{dc}}{2}$ through the clamping diodes.

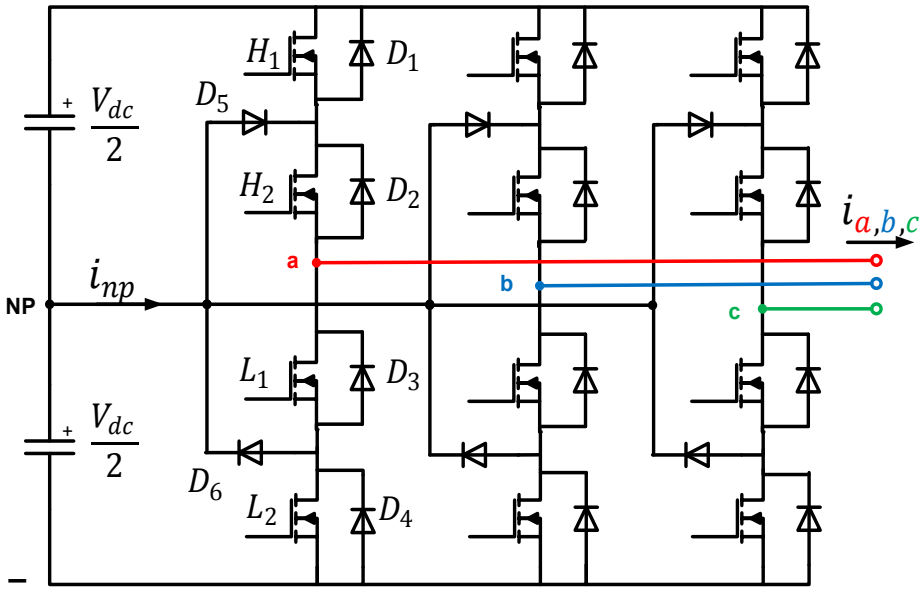


Fig. 2.3: Three-phase three-level NPC inverter.

General issues of multilevel NPC inverters are related but not limited to total harmonic distortion (THD) of the output current, neutral-point voltage unbalance compensation (AC and DC), ability to operate with any power factor, stability, high efficiency, size and lifetime of the converter.

Control of the neutral point voltage is a fundamental task of the modulation algorithm as it affects performance, reliability and cost of the inverter, as dc-link capacitors should normally be oversized to withstand any voltage unbalance condition.

Advantages:

- All of the phases share a common dc bus, which minimizes the capacitance requirements of the converter. For this reason, a back-to-back topology is not only possible but also practical for uses such as a high-voltage back-to-back inter-connection or an adjustable speed drive.
- The capacitors can be pre-charged as a group.
- Efficiency is high for fundamental frequency switching.

Disadvantages:

- Real power flow is difficult for a single inverter because the intermediate dc levels will tend to overcharge or discharge without precise monitoring and control.
- The number of clamping diodes required is quadratic to the number of levels, which can be cumbersome for units with a high number of levels.

2.4 NPC control strategies

Hereafter, only the control strategies associated with the neutral point clamped structure will be considered.

Various modulation schemes have been studied and developed for 3-level inverters, with neutral point voltage balancing scheme. They can be classified into three categories namely, Selective Harmonic Elimination (SHE), Carrier-Based PWM (CB-PWM) and Space-Vector Pulse-Width Modulation (SV-PWM).

2.4.1 Space vector modulations (SVM)

The SV-PWM converts the three voltage control references in complex (α–β) space in order to generate a vector reference by selecting a proper sequence of active vectors.

The active vectors are determined by the switches combination of each inverter leg. The operating status of the switches in the NPC inverter can be represented by the switching states shown in **Tab. 2.1**. Switching state 'P' denotes that the upper two switches in one of the inverter legs (for example A-leg) are ON and the inverter pole voltage V_a, is ideally equal to $+\frac{V_{dc}}{2}$, whereas 'N' indicates that the lower two switches conduct, leading to $V_a = -\frac{V_{dc}}{2}$.

Tab. 2.1 Conversion space vectors switches

	H1	H2	L1	L2	Voltage
P	1	1	0	0	$\frac{V_{dc}}{2}$
O	0	1	1	0	V_{np}
N	0	0	1	1	$-\frac{V_{dc}}{2}$

Switching state 'O' means that the inner two switches H2 and L1 are ON and V_a is clamped to zero through the clamping diodes. Depending on the direction of the load current i_a, one of the two clamping diodes is turned ON. For instance, a positive load current ($i_a > 0$) forces D1 to turn on, and the terminal 'a' is connected to the neutral point 'NP' through the conduction of D5 and H2. The switches H1 and L1 operate in a complementary manner similar to switches H2 and L2. As indicated earlier, the neutral-point voltage V_{np} varies with the operating condition of the NPC inverter. If the neutral-point voltage deviates too far, an uneven voltage distribution takes place, which may lead to premature failure of the switching devices and cause an increase in the harmonic of the inverter output voltage.

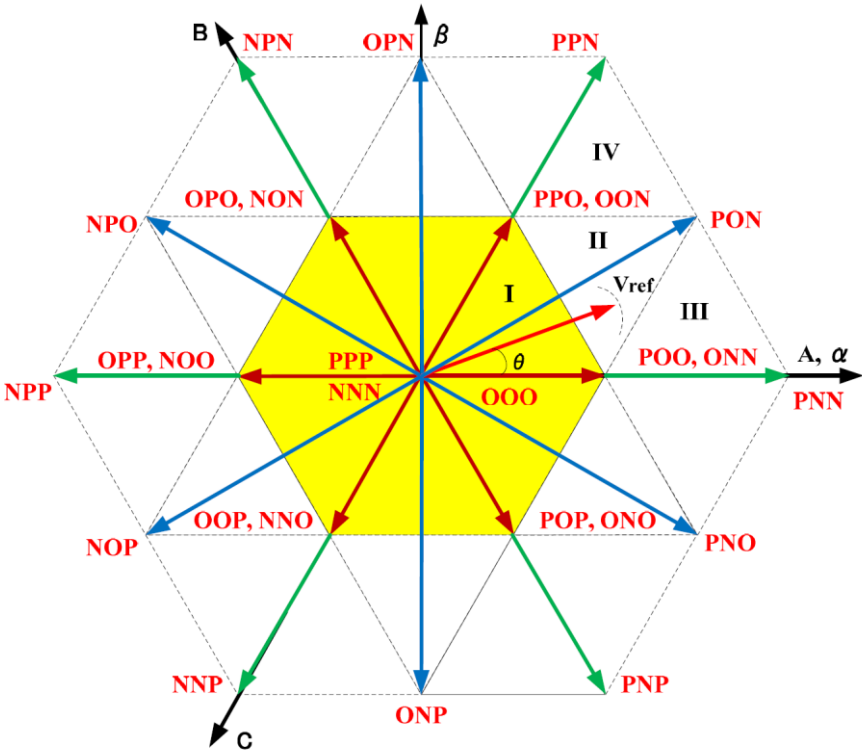


Fig. 2.4: Space vector diagram for a three-level inverter.

As already mentioned, the operation of each inverter phase lag can be represented by three switching states P, O, and N. Considering all the three phases together, the inverter has a total of 27 possible combinations of switching states. **Fig. 2.4** shows the space vector diagram of total 27 switching states (highlighted in red) corresponding to 19 voltage vectors for three-level NPC inverter.

Based on magnitude, the voltage vectors can be divided into four groups: *Zero vector* ($\boldsymbol{u_o}$), *Small vector* ($\boldsymbol{u_s}$), *Medium vector* ($\boldsymbol{u_m}$), and *Large vectors* ($\boldsymbol{u_l}$). All zero vectors (PPP, OOO and NNN) have zero magnitude, small vectors (perimeter of the yellow inner hexagon of **Fig. 2.4**) have a magnitude of $\frac{V_{dc}}{3}$, medium vectors have magnitude of $\frac{V_{dc}}{\sqrt{3}}$ and large vectors (perimeter of the external hexagon) have magnitude of $\frac{2}{3}V_{dc}$. Each small vector has two switching states, one containing P and other containing N, and therefore can be further classified into a P-type or N-type vector. Generally, the SV-PWM methods select the nearest three vectors to perform modulation, so this approach is known as nearest three vector (NTV) scheme.

Effect of the switching states on the NP

The effect of switching states on neutral voltage deviation is well illustrated by **Fig. 2.5**. When the inverter is operated with switching state [PPP] of zero vector $\boldsymbol{u_o}$, the upper two switches

in each of the three inverter legs are turned on, connecting the inverter terminals a, b, and c to the positive dc-link as shown in **Fig. 2.5a**. Since the neutral point NP is left unconnected, this switching state does not affect V_{np}. Similarly, the other zero switching states [OOO] and [NNN] do not cause V_{np} to shift either. **Fig. 2.5b** shows the inverter operation with P-type switching state [POO] of small vector $\boldsymbol{u_{S_p}}$. Since the three-phase load is connected between the positive DC bus and neutral point NP, the neutral current i_n flows in NP, causing V_{np} to increase. On the contrary, the N-type switching state [ONN] of small vector $\boldsymbol{u_{S_n}}$ makes V_{np} to decrease as shown in **Fig. 2.5c.** For medium vector $\boldsymbol{u_m}$ with switching state [PON] in **Fig. 2.5d,** load terminals a, b, and c are connected to the positive bus, the neutral point, and the negative bus, respectively. Depending on the inverter operating conditions, the neutral-point voltage V_{np} may rise or drop. Finally, considering a large vector $\boldsymbol{u_l}$ with switching state [PNN] as shown in **Fig. 2.5e,** the load terminals are connected between the positive and negative dc-links. The neutral point NP is left unconnected and thus the neutral voltage is not perturbed.

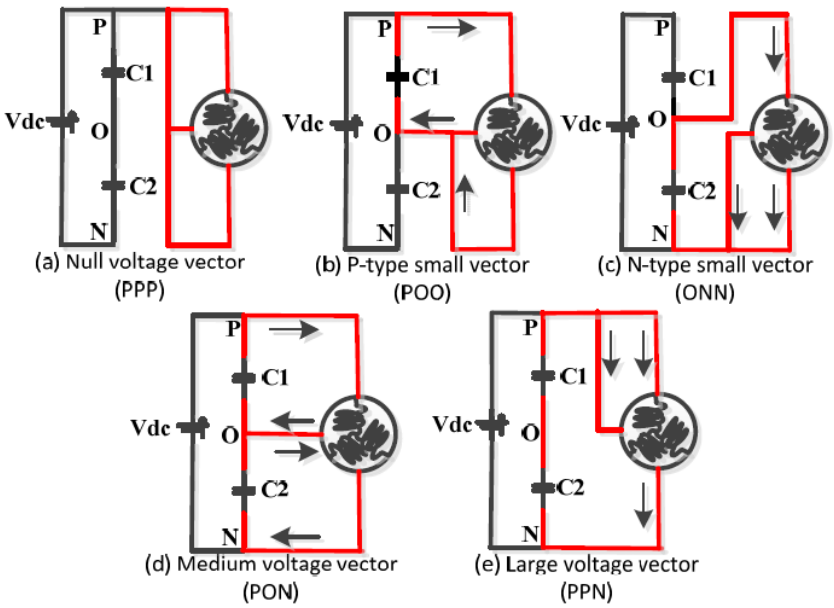


Fig. 2.5: Effects of the different vector types on the NP.

5-segments NTV

The considered SVM algorithm [18] is based on a 5-segment pattern and it utilizes only one redundant state per switching period. Each sextant of the space vector hexagon is divided into six regions (**Fig. 2.6**), containing only one redundant vector. These redundant states have opposite effects on the DC-link capacitor voltages, although they generate the same output line-to-line voltage. So, alternate use of these switching states is desirable for DC-link capacitor voltage balancing control. Effective utilization of redundant switching states

eliminates the need of extra hardware for the capacitor voltage balancing, without affecting the dwell timing of space vector over switching period. Using the proposed 5-segment SVM, every switching period one phase is clamped to reduce significantly the number of commutations with respect to the standard SPWM (1/3 less commutations). In **Tab. 2.2**, the sequences of vectors in function of the triangle and the redundant vector for the first sector is reported. It can be clearly seen that one leg is always clamped to "P",O" or N". In fact each switch transition has been highlighted by a corresponding change of color in **Tab. 2.2**.

Tab. 2.2 Sequences of vector s in the first sextant for 5-segment NTV

Triangle	Redundant sequences									
	"1"					"0"				
1	P	P	P	P	P	O	P	P	P	O
	N	O	O	O	N	N	N	O	N	N
	N	N	O	N	N	N	N	N	N	N
2	P	P	P	P	P	O	P	P	P	O
	O	P	P	P	O	O	O	P	O	O
	N	N	O	N	N	N	N	N	N	N
3	O	P	P	P	O	O	O	P	O	O
	O	O	O	O	O	N	O	O	O	N
	N	N	O	N	N	N	N	N	N	N
4	P	P	P	P	P	O	P	P	P	O
	O	O	P	O	O	O	O	O	O	O
	N	O	O	O	N	N	N	O	N	N
5	O	O	P	O	O	O	O	O	O	O
	O	O	O	O	O	N	O	O	O	N
	N	O	O	O	N	N	N	O	N	N
6	O	P	P	P	O	O	O	P	O	O
	O	O	P	O	O	O	O	O	O	O
	O	O	O	O	O	N	O	O	O	N

Symmetric

Symmetric modulation is characterized by the use of four vectors per modulation sequence. This modulation is very similar to previous 5-segment NTV, but it presents a 7-segment pattern due to the use of an extra vector. The new vector added to the sequence is the other redundant vector that was not selected using the other strategy. Thanks to this, the duty cycles

are basically calculated by the same process, with the only difference being that the duty cycle applied in NTV to only one of the double vectors is now shared between both of them.

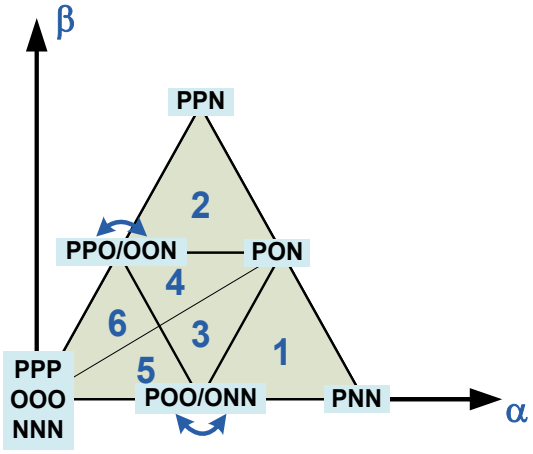


Fig. 2.6: Vectors placement for SVM in the first sextant.

2.4.2 Neutral-point balancing in SVM

In the 5-segment NTV SVM, the NP voltage "DC" balance effect is intrinsic to this modulation and is made by the proper choice of the redundant vector according to the sign of ΔV_c and the sign of the phase currents (**Fig. 2.7**). This control algorithm is based on the instant sign measure of currents and voltage, then a steady-state compensation is made leading to more ripple with respect to the PI based control loop [30].

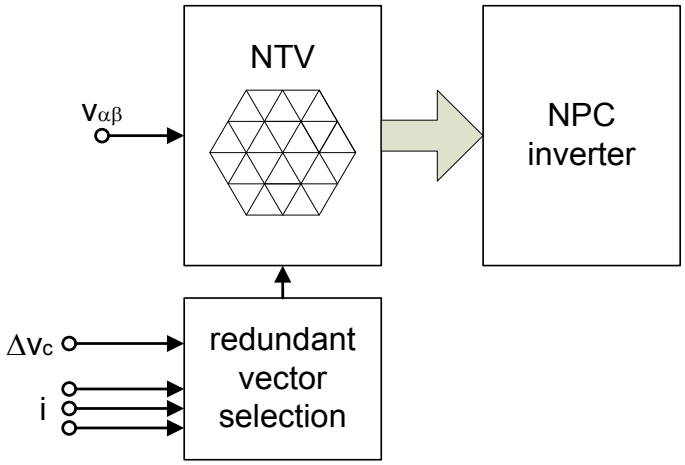


Fig. 2.7: Redundant selection scheme for the NTV SV-PWM.

In symmetric modulation, in order to satisfy the zero-NP-current condition, the duty cycle calculated for the couple of redundant vectors should now be properly shared between them. This duty cycle can be distributed according to a variable α, generated from an opportune PI regulator (**Fig. 2.8**). In steady-state condition, α is equal to 0,5 so the two redundant states are applied for an equal interval of time during the switching period.

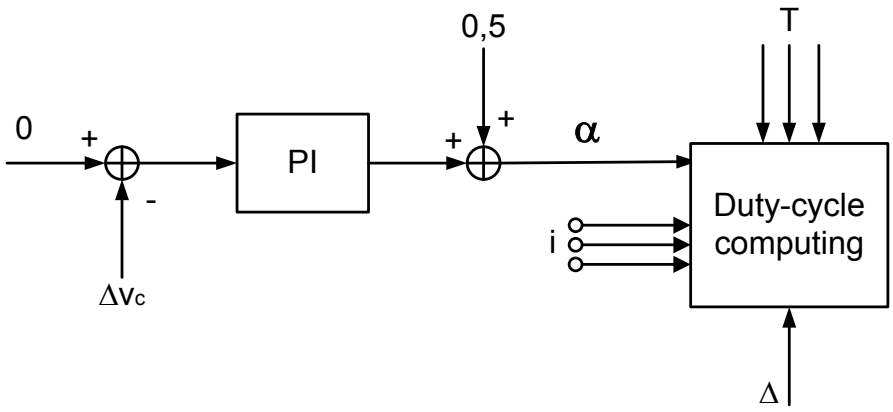


Fig. 2.8: ***Calculation of parameter α in symmetric modulation.***

2.4.3 Carrier-based modulations (CBM)

Carrier based modulation (CBM) is the simplest method to be implemented. It directly generates the duty cycles for the switches from the reference-voltage vector, instead of sector identification and extensive numeric calculations of the switching period, as in case of the classic SVM strategy. Moreover, this reduces the total computation time of the controller, which in turn allows increase in system switching frequency. It can be also demonstrated that every SVM technique can be reproduced with a carrier-based one, by adopting a modulating signal with the proper zero signal injection.

Recently proposed modulation techniques, normally addressed as double-signal modulation (DSPWM) modulation, adopt two modulation signals per phase, one positive and one negative and allows to reduce or eliminate low-frequency voltage oscillations of the neutral point, [14][26], but they increase significantly the switching losses of the converter as compared to other modulation techniques, such as standard sinusoidal pulse-width modulation (SPWM) or nearest-three-vector (NTV) space vector modulation (SVM), [18]. Sinusoidal modulations, on the other hand, exhibit a strong low-frequency content of the NP voltage ripple, that depends on both load power angle and converter modulation index.

The trade-off between the NP voltage ripple produced by sinusoidal strategies on one hand, and the increment of switching losses and output voltage harmonic distortion caused by double signal strategies on the other, gave birth to hybrid [15] or, more recently, interleaved modulation strategies [45].

Hybrid modulation approaches belong to the double signal modulation class and are based on clamping modulation signals for some time during the non-common intervals. As the modulation signals are clamped to zero for an additional time, this leads to the switching frequency of the power switches being reduced, i.e. their switching losses also decrease. The

exact combination is chosen by a sharing variable D, which can take values within the interval [0,1].

In [31] a carrier-based DC-link voltage balancing strategy, based on neutral point current, is derived. Although, results show desired steady-state performance, the proposed system is complicated for hardware implementation, since it requires intense mathematical computation.

A Carrier based PWM strategy based on reduced switching losses is proposed in [32]. In this strategy, one of the phases is clamped to positive, negative, or neutral point of the inverter, depending on the two capacitor voltages. Though experimental results show a reduction in the capacitor voltage difference, detailed transient performance is not carried out. Moreover, the DC-link capacitor voltage is also kept low, which makes the capacitor voltage difference low. A double carrier based DC-link voltage balancing strategy is shown in [33]. An optimum value of DC-offset value is also analytically derived. However, results show a lot of neutral point voltage ripple and no transients results are shown to verify the efficacy of the system with transient load variations. A similar voltage balancing strategy based on neutral point current is proposed in [14], [16]. Although an expression for optimum value of a DC-offset value is derived, no transient simulation or experimental results are shown.

Another single carrier based voltage balancing scheme, with 6^{th} order voltage harmonic addition with DC-offset voltage is shown in [34]. Although, results showed convergence of the two DC-link capacitor voltages, it takes a considerable time to balance the capacitor voltages even with passive load. Hence, with system with much more transients like for electric vehicle, it might not be a best solution.

Sinusoidal PWM

The sinusoidal pulse width modulation (SPWM) is still a reference modulation technique in many applications due to easy implementation and acceptable performances. When using SPWM to control a three phase three level NPC inverter, each phase is controlled by one sinusoidal reference signal at the modulation frequency that is compared with two carriers of half unitary amplitude at the switching frequency producing the gate control signals.

In order to achieve a linear operating range equivalent to that of space vector modulation, the original sinusoidal references (v_a, v_b, v_c) are modified by injecting a proper zero sequence v_o, as follows:

$$\begin{cases} v'_a = v_a - v_o \\ v'_b = v_b - v_o \\ v'_c = v_c - v_o \end{cases} \quad (1)$$

$$v_o = \frac{max(v_a, v_b, v_c) + min(v_a, v_b, v_c)}{2}$$

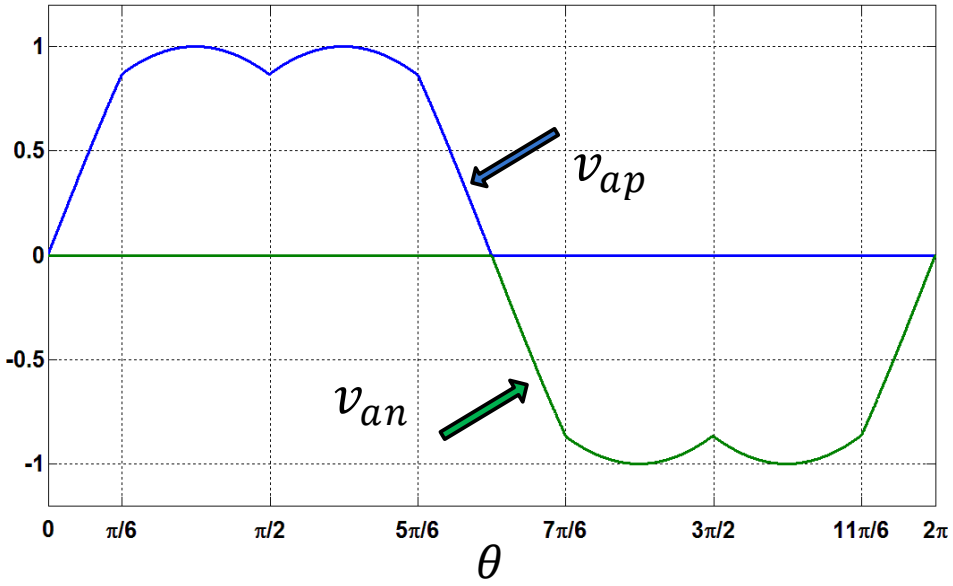


Fig. 2.9: Modulation signals for SPWM.

Each phase modulation signal can be divided in two signals as shown in **Fig. 2.9**. Obviously, the sums of these modulation signals have to be equal to the (1), so that:

$$\begin{cases} v'_a = v_{ap} + v_{an} \\ v'_b = v_{bp} + v_{bn} \\ v'_c = v_{cp} + v_{cn} \end{cases} \quad (2)$$

where $v_{ip} \geq 0$ and $v_{in} \leq 0$, with $i = \{a, b, c\}$. The signals with subscript p will only cross the positive carrier $v^p_{carrier} \epsilon [0,1]$ and the signals with subscript n will only cross the negative carrier $v^n_{carrier} \epsilon [-1,0]$.

When one inverter phase leg of is clamped to the NP, its output current is injected into that point and NP current i_{np} can be expressed as follows:

$$i_{np}(t) = s_{a0}(t) i_a(t) + s_{b0}(t) i_b(t) + s_{c0}(t) i_c(t) \quad (3)$$

where s_{i0} $(i = a, b, c)$ is a binary function being unity value when output phase i is connected to NP or zero otherwise.

Neutral point voltage ripple can be calculated by averaging NP current over the modulation period T_{sw} adopting a moving average operator, i.e.:

$$\bar{\imath}_{np}(t) = \frac{1}{T_{sw}} \int_{t-T_{sw}}^{t} i_{np}(\tau) d\tau \tag{4}$$

Applying expression (3) inside the integral (4), one obtains the following:

$$\bar{\imath}_{np} = d_{a0}\bar{\imath}_a + d_{b0}\bar{\imath}_b + d_{c0}\bar{\imath}_c \tag{5}$$

in which $d_{i0} = \bar{s}_{i0}$. Since the carrier/switching frequency is much higher than the frequency of the modulation signals (i.e. fundamental frequency of the output voltage), the duty cycles can be expressed as follows [14]:

$$d_{i0} = \left|1 + v_{in} - v_{ip}\right| \tag{6}$$

The modulus operator in (6) can be removed when the inverter works in linear operator range since the difference $\left(v_{in} - v_{ip}\right)$ will never be less than negative one.

As a result, the expression (5) can be rewritten with the following:

$$\bar{\imath}_{np} = \sum_{i=a,b,c} \left(1 + v_{in} - v_{ip}\right) \cdot \bar{\imath}_i \tag{7}$$

Considering the analytical expressions of v_{in}, v_{ip} and $\bar{\imath}_i$ for this conventional SPWM technique, it is possible to determine the exact behavior of the NP current during a fundamental period.

Hereafter, for simplicity only the values for the phase A, i.e. v_{ap}, v_{an} and $\bar{\imath}_a$, will be reported.

$$v_{ap} = \begin{cases} \frac{3}{2} m \cdot cos\left(\theta - \frac{\pi}{2}\right) & --\rightarrow 0 \le \theta \le \frac{\pi}{6} \\ \frac{\sqrt{3}}{2} m \cdot cos\left(\theta - \frac{\pi}{3}\right) & --\rightarrow \frac{\pi}{6} \le \theta \le \frac{\pi}{2} \\ \frac{\sqrt{3}}{2} m \cdot cos\left(\theta - \frac{2\pi}{3}\right) & --\rightarrow \frac{\pi}{2} \le \theta \le \frac{5\pi}{6} \\ \frac{3}{2} m \cdot cos\left(\theta - \frac{\pi}{2}\right) & --\rightarrow \frac{5\pi}{6} \le \theta \le \pi \\ 0 & --\rightarrow \pi \le \theta \le 2\pi \end{cases} \tag{8}$$

$$v_{an} = \begin{cases} 0 & --\rightarrow 0 \le \theta \le \pi \\ \frac{3}{2} m \cdot cos\left(\theta - \frac{\pi}{2}\right) & --\rightarrow \pi \le \theta \le \frac{7\pi}{6} \\ \frac{\sqrt{3}}{2} m \cdot cos\left(\theta - \frac{\pi}{3}\right) & --\rightarrow \frac{7\pi}{6} \le \theta \le \frac{3\pi}{2} \\ \frac{\sqrt{3}}{2} m \cdot cos\left(\theta - \frac{2\pi}{3}\right) & --\rightarrow \frac{3\pi}{2} \le \theta \le \frac{11\pi}{6} \\ \frac{3}{2} m \cdot cos\left(\theta - \frac{\pi}{2}\right) & --\rightarrow \frac{11\pi}{6} \le \theta \le 2\pi \end{cases} \tag{9}$$

$$\bar{\imath}_a = \boldsymbol{sin}(\boldsymbol{\theta} + \boldsymbol{\alpha}_{vi}) \quad \textbf{(10)}$$

where α_{vi} is the phase delay between the output voltage and current at the considered load and m is the modulation index.

The behavior of $\bar{\imath}_{np}(t)$ for SPWM within a modulating period T_m is shown in **Fig. 2.10**. In this case, the value of α_{vi} has been fixed to 50 degrees. One can notice that this neutral point current is a periodic signal with a frequency three times the fundamental one As a consequence, a low-frequency oscillation is induced in the neutral point voltage. The amplitude of these voltage oscillations are proportional to the neutral point current ripple. Also it can be highlighted that the RMS value of the instantaneous NP current is quite high, leading to high losses in the dc bus capacitors.

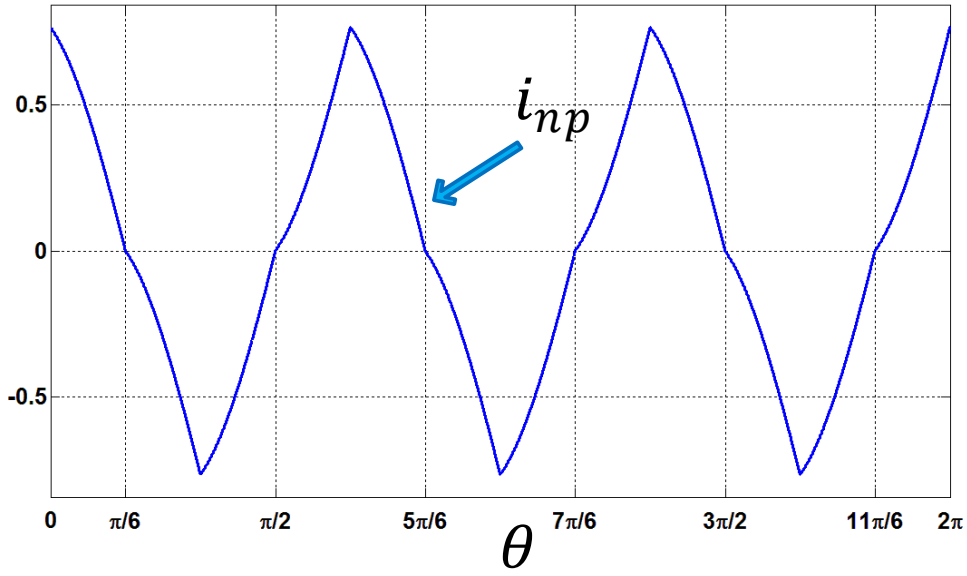


Fig. 2.10: NP current average value within a fundamental period for SPWM with $\alpha_{vi} = 50°$.

Fig. 2.11 shows the NP current behavior depending on the value of the load phase angle α_{vi}. One can notice that the minimum amplitude values correspond to $\alpha_{vi} = 0°$ and $\alpha_{vi} = 180°$, on the other hand the maximum occurs for $\alpha_{vi} = 90°$.

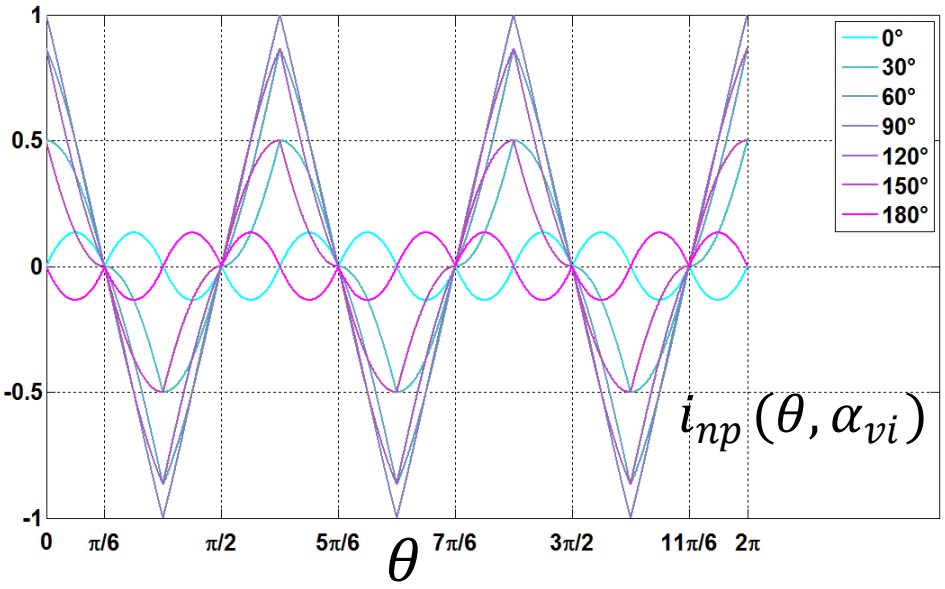


Fig. 2.11 NP average current waveform within a fundamental period for SPWM at different values of α_{vi}.

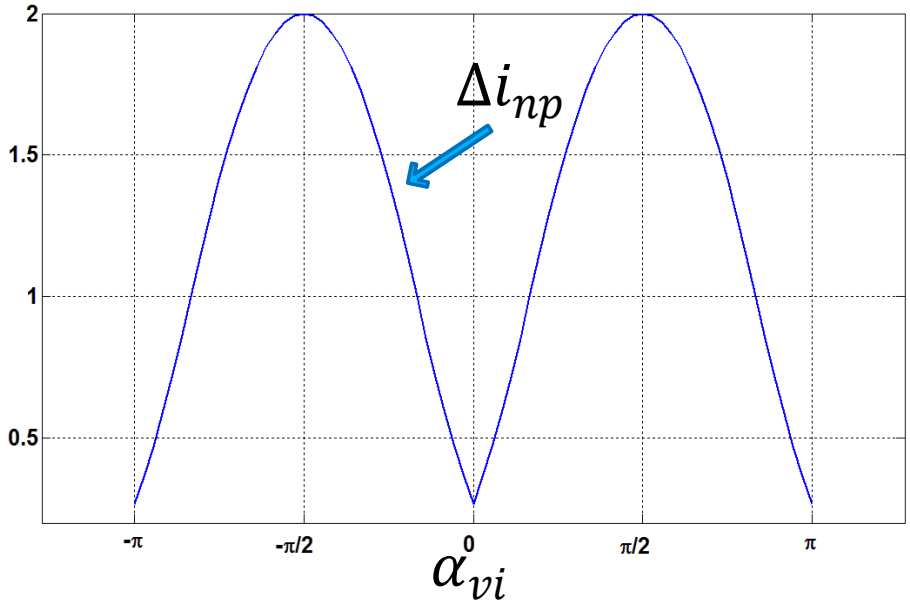


Fig. 2.12: NP current ripple for SPWM as a function of load phase angle α_{vi}.

Double signal PWM

The fast-processing modulation, [14], also referred as double signal pulse width modulation (DSPWM), is able to completely remove low-frequency oscillations at the expenses of significant increase of switching losses in the converter with respect to previous section conventional SPWM.

In order to preserve NP voltage balancing, the locally averaged NP current (5) must be zero, i.e.

$$\bar{\boldsymbol{i}}_{\boldsymbol{np}} = \boldsymbol{d}_{\boldsymbol{a0}}\bar{\boldsymbol{i}}_{\boldsymbol{a}} + \boldsymbol{d}_{\boldsymbol{b0}}\bar{\boldsymbol{i}}_{\boldsymbol{b}} + \boldsymbol{d}_{\boldsymbol{c0}}\bar{\boldsymbol{i}}_{\boldsymbol{c}} = \mathbf{0} \tag{11}$$

If we find a value of v_x such as:

$$\boldsymbol{v}_{\boldsymbol{an}} - \boldsymbol{v}_{\boldsymbol{ap}} = \boldsymbol{v}_{\boldsymbol{bn}} - \boldsymbol{v}_{\boldsymbol{bp}} = \boldsymbol{v}_{\boldsymbol{cn}} - \boldsymbol{v}_{\boldsymbol{cp}} = \boldsymbol{v}_{\boldsymbol{x}} \tag{12}$$

then the expression (7) would be:

$$\bar{\boldsymbol{i}}_{\boldsymbol{np}} = (\mathbf{1} + \boldsymbol{v}_{\boldsymbol{x}}) \cdot \sum_{\boldsymbol{i=a,b,c}} \bar{\boldsymbol{\imath}}_{\boldsymbol{i}} \tag{13}$$

Since the neutral of the load is open or is just a triangle-connected load, there is no zero sequence in the current. Subsequently, the sum of the output currents is always zero

$$\bar{\boldsymbol{i}}_{\boldsymbol{a}} + \bar{\boldsymbol{i}}_{\boldsymbol{b}} + \bar{\boldsymbol{i}}_{\boldsymbol{c}} = \mathbf{0} \tag{14}$$

hence, $\bar{i}_{np}$ becomes equal to zero.

The problem of maintaining the locally averaged voltages on the dc-link capacitors constant is reduced to find a proper value for v_x in (13). An infinite number of solutions can be found; however, one particularly interesting solution can achieve minimum switching frequencies in the devices of the converter. This solution is found by forcing variables v_{ip} and v_{in} in to be zero for the maximum time possible since, when these signals are zero, some of the transistors do not switch (none of the modulation signals cross a carrier signal). Regarding this restriction and relationships (1), (2), and (9), the following solution is obtained [14]:

$$\begin{cases} \boldsymbol{v}_{\boldsymbol{ip}} = \dfrac{\boldsymbol{v}_{\boldsymbol{i}} - \boldsymbol{min}(\boldsymbol{v}_{\boldsymbol{a}}, \boldsymbol{v}_{\boldsymbol{b}}, \boldsymbol{v}_{\boldsymbol{c}})}{\mathbf{2}} \\ \boldsymbol{v}_{\boldsymbol{in}} = \dfrac{\boldsymbol{v}_{\boldsymbol{i}} - \boldsymbol{max}(\boldsymbol{v}_{\boldsymbol{a}}, \boldsymbol{v}_{\boldsymbol{b}}, \boldsymbol{v}_{\boldsymbol{c}})}{\mathbf{2}} \end{cases} \tag{15}$$

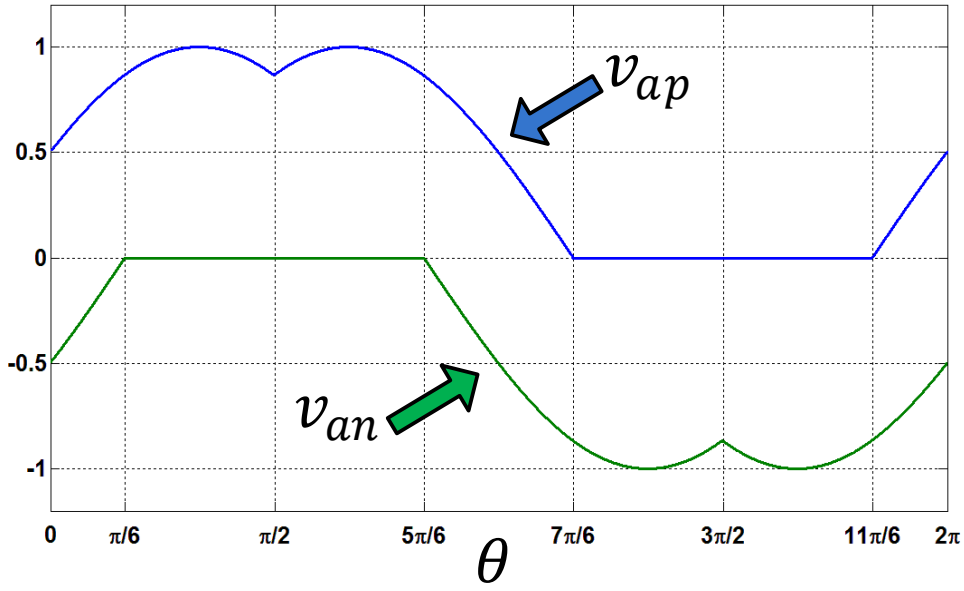


Fig. 2.13: Modulation signals for DSPWM.

The modulating signals v_{ap} and v_{an} for DSPMW are presented in **Fig. 2.13** and their analytical expressions are the following:

$$v_{ap} = \begin{cases} \frac{\sqrt{3}}{2} \cdot cos\left(\theta - \frac{\pi}{3}\right) - - \rightarrow 0 \leq \theta \leq \frac{\pi}{6} \\ \frac{\sqrt{3}}{2} m \cdot cos\left(\theta - \frac{\pi}{3}\right) - - \rightarrow \frac{\pi}{6} \leq \theta \leq \frac{\pi}{2} \\ \frac{\sqrt{3}}{2} m \cdot cos\left(\theta - \frac{2\pi}{3}\right) - - \rightarrow \frac{\pi}{2} \leq \theta \leq \frac{5\pi}{6} \\ \frac{\sqrt{3}}{2} m \cdot cos\left(\theta - \frac{2\pi}{3}\right) - - \rightarrow \frac{5\pi}{6} \leq \theta \leq \frac{7\pi}{6} \\ 0 \quad - - \rightarrow \frac{7\pi}{6} \leq \theta \leq \frac{11\pi}{6} \\ \frac{\sqrt{3}}{2} \cdot cos\left(\theta - \frac{\pi}{3}\right) - - \rightarrow \frac{11\pi}{6} \leq \theta \leq 2\pi \end{cases} \quad (16)$$

$$v_{an} = \begin{cases} \frac{\sqrt{3}}{2} m \cdot cos\left(\theta - \frac{2\pi}{3}\right) & --\rightarrow 0 \le \theta \le \frac{\pi}{6} \\ 0 & --\rightarrow \frac{\pi}{6} \le \theta \le \frac{5\pi}{6} \\ \frac{\sqrt{3}}{2} m \cdot cos\left(\theta - \frac{\pi}{3}\right) & --\rightarrow \frac{5\pi}{6} \le \theta \le \frac{7\pi}{6} \\ \frac{\sqrt{3}}{2} \cdot cos\left(\theta - \frac{\pi}{3}\right) & --\rightarrow \frac{7\pi}{6} \le \theta \le \frac{3\pi}{2} \\ \frac{\sqrt{3}}{2} \cdot cos\left(\theta - \frac{2\pi}{3}\right) & --\rightarrow \frac{3\pi}{2} \le \theta \le \frac{11\pi}{6} \\ \frac{\sqrt{3}}{2} \cdot cos\left(\theta - \frac{2\pi}{3}\right) & --\rightarrow \frac{11\pi}{6} \le \theta \le 2\pi \end{cases} \quad (17)$$

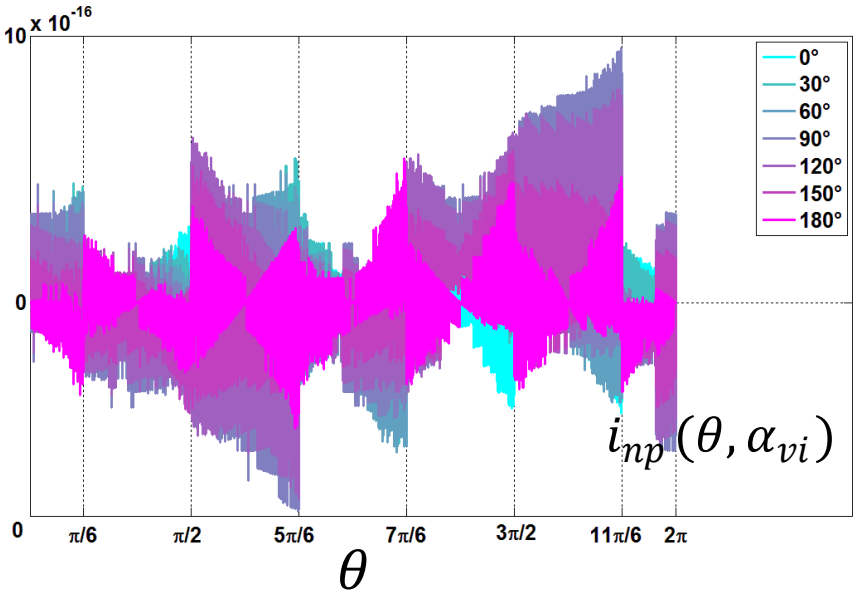


Fig. 2.14: NP average current waveform within a fundamental period for DSPWM at different values of α_{vi}.

The efficiency of such an approach in eliminating the low-frequency oscillations of the NP is clearly visible in **Fig. 2.14**. In fact, the amplitude of the NP current ripple is negligible on overall the load phase angle range. Thus, smaller dc link capacitors can be used, allowing significant space and cost savings, [46].

The implementation of the discussed modulation algorithm is straightforward and much easier with respect to classical space vector approaches. As previously mentioned, this technique has an important drawback, i.e. increasing significantly switching losses.

Hybrid PWM

Hybrid modulation techniques discussed hereafter try in fact to recover the part of the switching losses by relaxing the NP voltage oscillation constraint. In [20] the condition

introduced for fast-processing algorithm is applied only during certain switching periods of the fundamental wave, thus allowing a less efficient reduction of the NP current injection, but significantly reducing the number of commutations, i.e. leading to a reduction of the converter switching losses.

HPWM strategy, [30] [20], is based on the clamping of one modulation signal for some time during the non-common intervals between DSPWM and SPWM, where $0 \leq \theta \leq \frac{\pi}{6}$ or $\frac{5\pi}{6} \leq \theta \leq \frac{7\pi}{6}$ or $\frac{11\pi}{6} \leq \theta \leq 2\pi$ in **Fig. 2.13**. As the modulation signals are clamped to zero for an additional time, switching frequency of the power switches is reduced and switching losses also decrease. The exact combination is chosen by a sharing variable D, which can take values within the interval $[0; 1]$. When the parameter D takes the extreme values zero or one, the HPWM becomes DSPWM or SPWM, respectively.

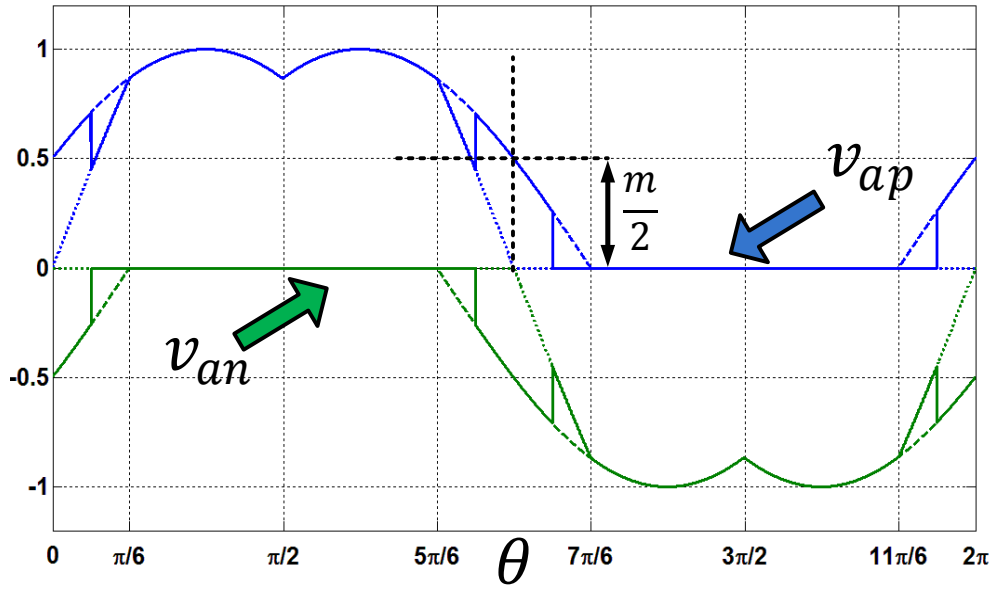


Fig. 2.15: Modulation signals for HPWM with D = 0, 5.

Fig. 2.15 shows the modulating signals for the hybrid modulation. It can be seen that, when the modulation signal from SPWM crosses zero, the absolute value of the DSPWM modulation signals are exactly half the modulation index (m = amplitude of the modulation signals). This condition is used to determine the extension of the common interval directly from the instantaneous values of the modulation signals obtained from DSPWM. The modulation signals are compared with the value of $x = D\frac{m}{2}$ to determine the additional intervals in which these signals need to be clamped to extend SPWM patterns further.

HPWM will be taken as a reference to evaluate the performance of the proposed interleaved modulation strategy.

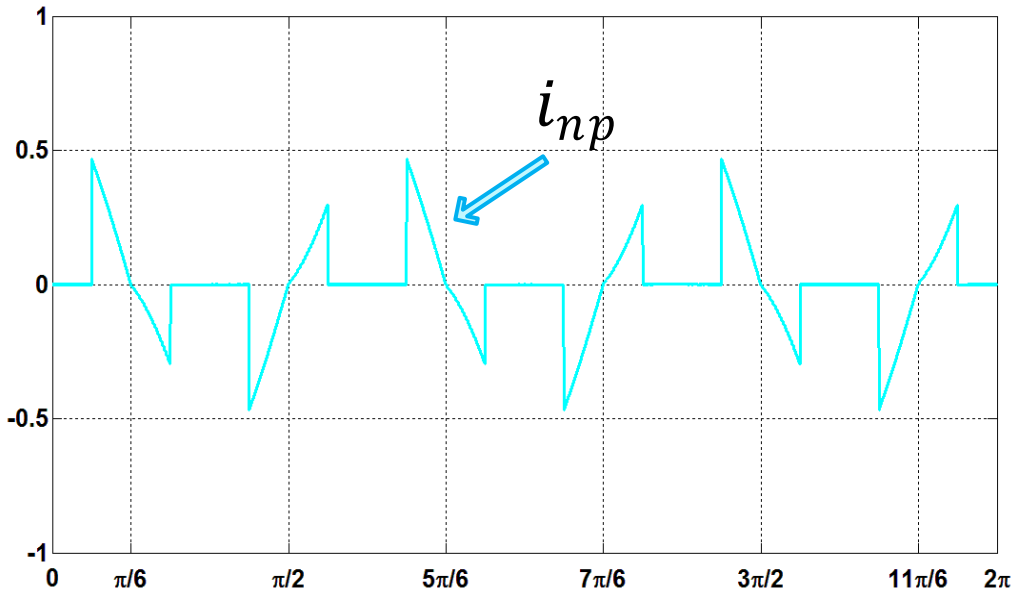


Fig. 2.16: NP current average value within a fundamental period for HPWM with D = 0,5 and.$\alpha_{vi} = 50°$.

The behavior of $\bar{\imath}_{np}(t)$ for HPWM within a modulating period T_m is shown in **Fig. 2.16**. In this figure, the value of α_{vi} has been fixed to 50 degrees.

In **Fig. 2.17**, the neutral point current at different values of the load phase angle is presented. Finally, a comparison between the three described modulation, i.e. sinusoidal, fast-processing and hybrid, is proposed in **Fig. 2.18** in terms of RMS value of the NP current.

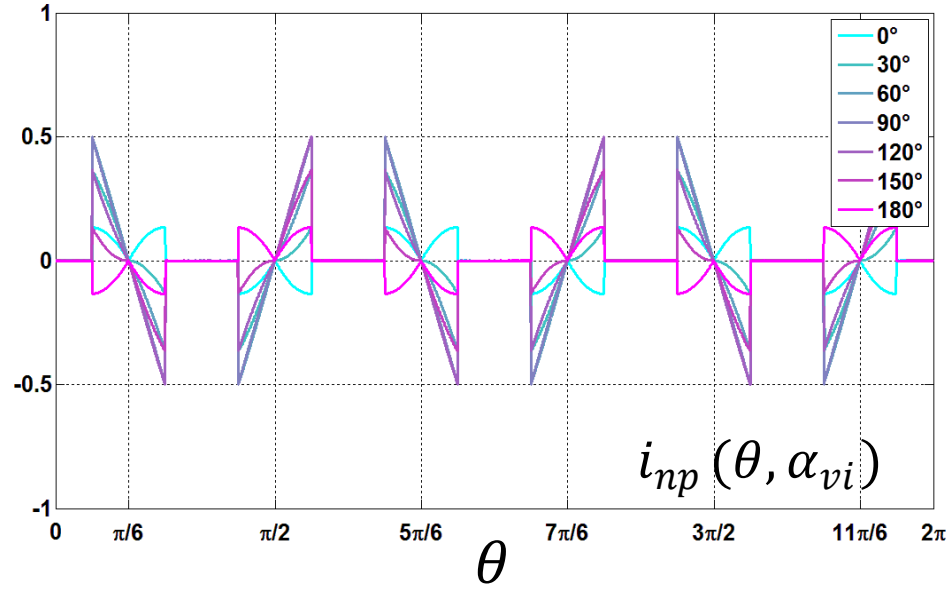


Fig. 2.17: NP average current waveform within a fundamental period for HPWM with D = 0,5 at different values of α_{vi}.

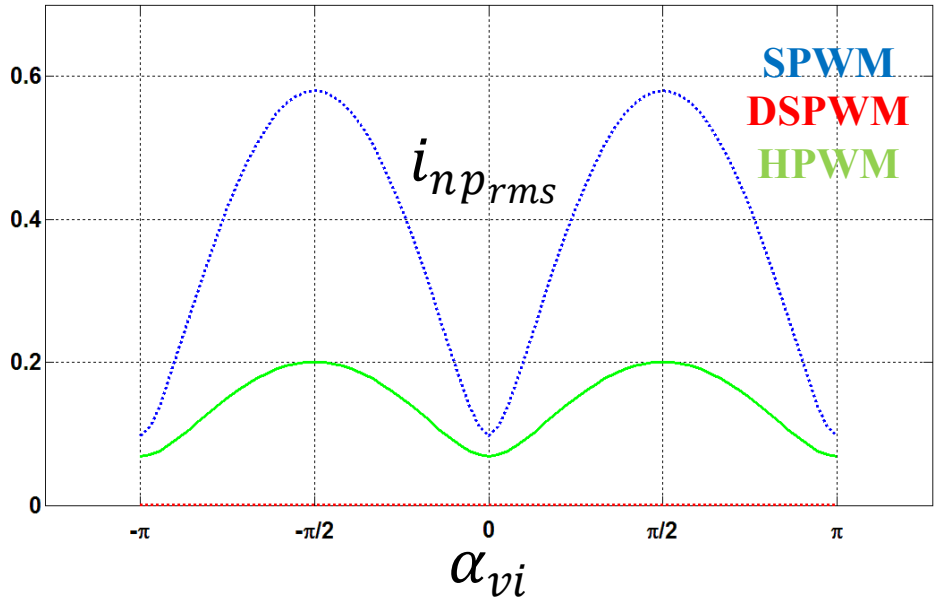


Fig. 2.18: NP current RMS value as a function of load phase angle α_{vi} for SPWM, DSPWM and HPWM with D = 0,5.

2.4.4 Optimal NP balancing regulator

Using the DSPWM and HPWM modulation techniques, the locally averaged NP current is kept near zero, and consequently, the low-frequency oscillations of the NP voltage on the dc-link capacitors are low ("AC" compensation). However, this does not imply "DC" balance between capacitor voltages. Indeed, if the initial voltages on the capacitors were different, this modulation strategy would tend to preserve imbalance because the locally averaged NP current is zero. This situation is even worse since dead times, different values and behaviors of the components, etc., can make the voltages drift slowly and without control. Moreover, in grid-connected applications the presence of grid faults and/or non-linear loads could quickly lead dc-link voltages to diverge. Thus, some compensation loop for voltage imbalances must be added.

Self-balancing phenomena

It's well known in literature [19]-[20] that, under particular work conditions, a "self-balancing" effect is present (**Fig. 2.19**). This intrinsic aspect tends to preserve "DC" balance between the two DC-link capacitors. Due to the slow dynamic and the low effectiveness at some work condition, it is desirable to use a control loop for the neutral-point voltage.

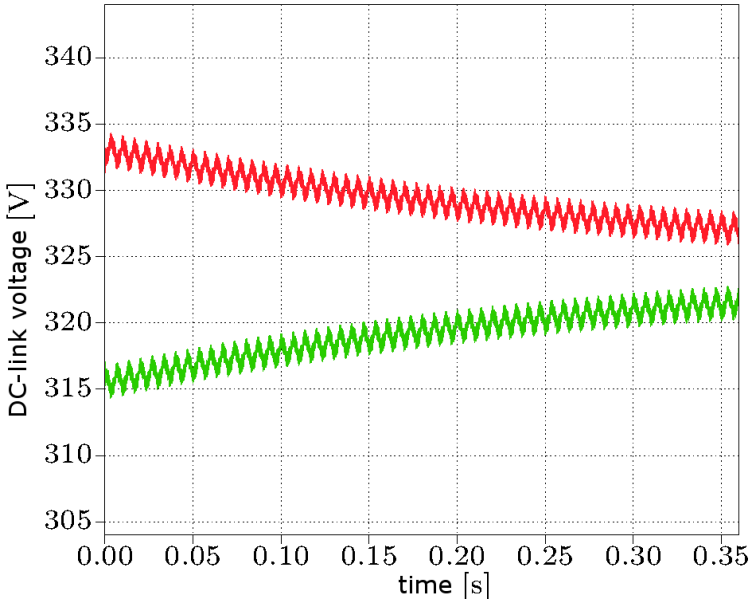


Fig. 2.19: Self-balancing effect in SPWM

In this section, three different control loops have been studied and compared in order to select the best solution to apply to the considered application: a "simple compensator" [14], an "exact compensator" [16] and a "dynamic compensator" [17].

Simple compensator

This type of controller synthesizes a v_{i_off} signal to be directly summed to the modulating signals in (2). By the known of the phase-current signs and the NP displacement, it is possible to calculate the right value that, added to the modulating signals, leads to compensation of the NP voltage. This off-set signal is given by the following expression:

$$\boldsymbol{v_{i\_off} = k_p|\Delta V_c|sign(\Delta V_c i_i)sign(v_{ip} - v_{in} - 1)} \qquad \textbf{(18)}$$

Simulations have been demonstrated that with this "simple compensator" it is not possible to stabilize the N-P in all power and PF conditions. The control loop dynamic and stability is strongly affected by the value of the parameter k_p.

Exact compensator

The second regulator, named "exact compensator" tries to exactly compensate the voltage imbalance every period of switching, representing an improvement of the previous one. The controller, first presented in [16], allows to estimate the proper offset to apply to the modulation signals in order to achieve good voltage-balancing performance. The algorithm takes into account the main system variables as the phase currents, the switching frequency, the bus-capacitor values and the NP voltage. The sign of the offset value is fixed by the term

$-\text{sign}(\Delta V_c i_i)$.“Exact” compensator has the best dynamic but it introduces more ripple, waveform quality deterioration and more algorithm complexity.

Dynamic compensator

This compensator is very easy to realize and has good performances in all conditions. As shown in **Fig. 2.20**, a PI regulator controls the voltage difference between the two capacitors ΔV_c by generating a proper value k to multiply to the modulating signals:

$$\begin{cases} v_{ip}^{*} = v_{ip} \cdot 2k \\ v_{in}^{*} = v_{ip} \cdot 2 \cdot (1-k) \end{cases} \quad \textbf{(19)}$$

Since the factor k decides the duty cycle of the switches in the converter, the output of the PI controller should be limited. In fact, the reference phase voltages for upper carrier should be between 0 and v_{dc} and the reference phase voltage for lower carrier should be between 0 and $-v_{dc}$ to ensure the PWM operation in the linear range. The maximum and minimum limits of the PI controller output are given by k_{max} and k_{min}. The controller limit expressions [17] is:

$$\begin{cases} k_{max} = min\left(\dfrac{m}{v_{max}^{pu} - v_{min}^{pu}}, 1\right) \\ k_{min} = max\left(1 - \dfrac{m}{v_{max}^{pu} - v_{min}^{pu}}, 0\right) \end{cases} \quad \textbf{(20)}$$

where k_{max} and k_{min} are function of the modulation index m and v_{max}^{pu} and v_{min}^{pu} are the instantaneous values per unit. The control loop has a specific dynamic given by the choice of the PI parameters. In steady-state conditions, k is equal to 0,5 and consequently $v_{ip}^{*} = v_{ip}$ and $v_{in}^{*} = v_{in}$.

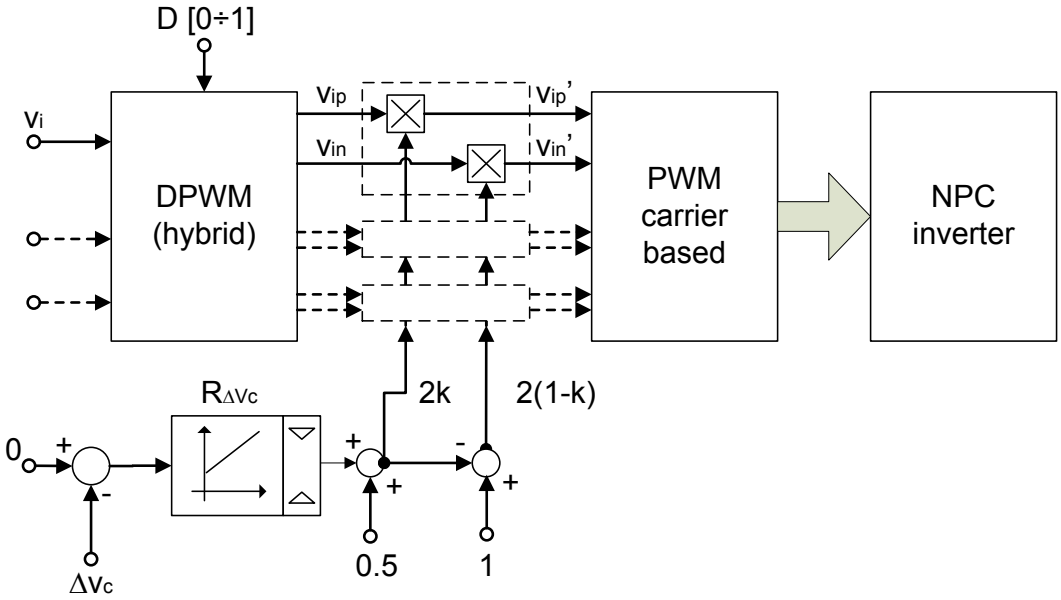


Fig. 2.20: Neutral-point control scheme for the HPWM.

2.4.5 Comparison between CBM and SVM

Extensive simulation have been performed in order to highlight the specific features of each method and provide a quantitative comparison test bench. Hereafter, the basic issues will be considered and compared among considered modulation strategies for the grid-connected 3-level NPC inverter [30].

Neutral-point "AC" ripple

A preliminary qualitative discussion of the considered modulation techniques performance highlights that the adoption of DSPWM and HPWM techniques provides a lower low-frequency ripple of the neutral point. This fact means that the waveform quality of the output voltage could be improved and smaller dc-link capacitors could be used, saving cost and space to realize the inverter module.

Neutral-point "DC" balance control

In **Fig. 2.22** the response of the bus capacitor control loop over imbalance conditions of the capacitor voltages is represented for the HPWM with $D = 0.4$ and for the SVM (**Fig. 2.23**). Initially, the voltage of the two DC-link capacitors are different (5% of unbalance); then, at $t = 0.06s$ a fixed load is introduced as a disturbance. Finally, at $t = 0.12s$ the three-phase symmetric load is changed with a non-symmetric one. As it can be seen, SVM has a quicker dynamic response but a higher value of ripple.

The dc balancing capabilities are on the other hand difficult to obtain with standard techniques. In the case of hybrid modulation two different unbalance controllers, namely "exact" and "dynamic" have been considered. The former provides very high dynamical balancing but raises the low-frequency ripple. The latter is less fast but it provides definitively a lower ripple. Finally the behavior of the different techniques has been compared in zero power factor conditions, showing an unstable behavior of the dynamic compensator.

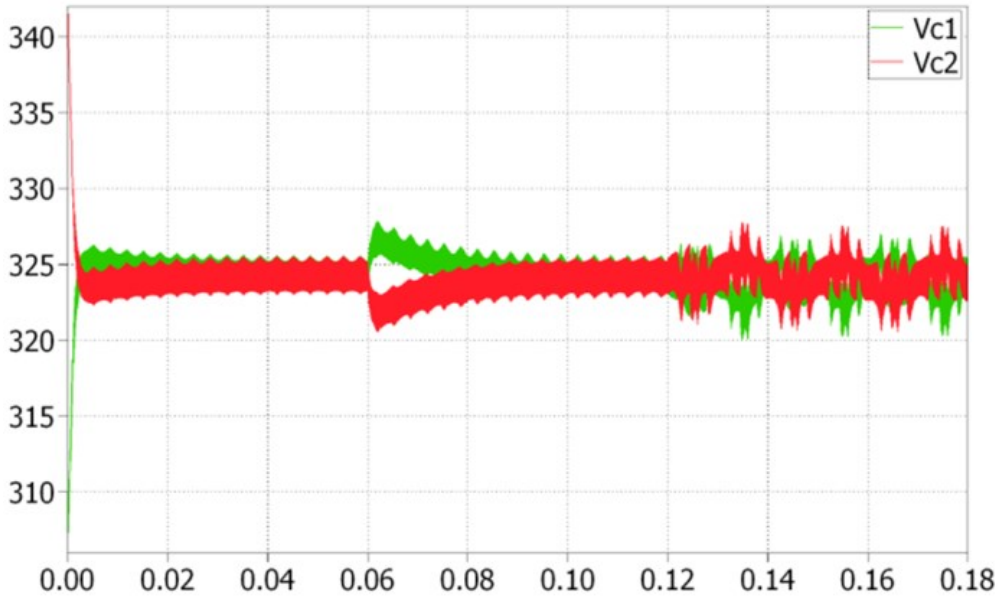


Fig. 2.21: Bus capacitor voltages for the H-PWM.

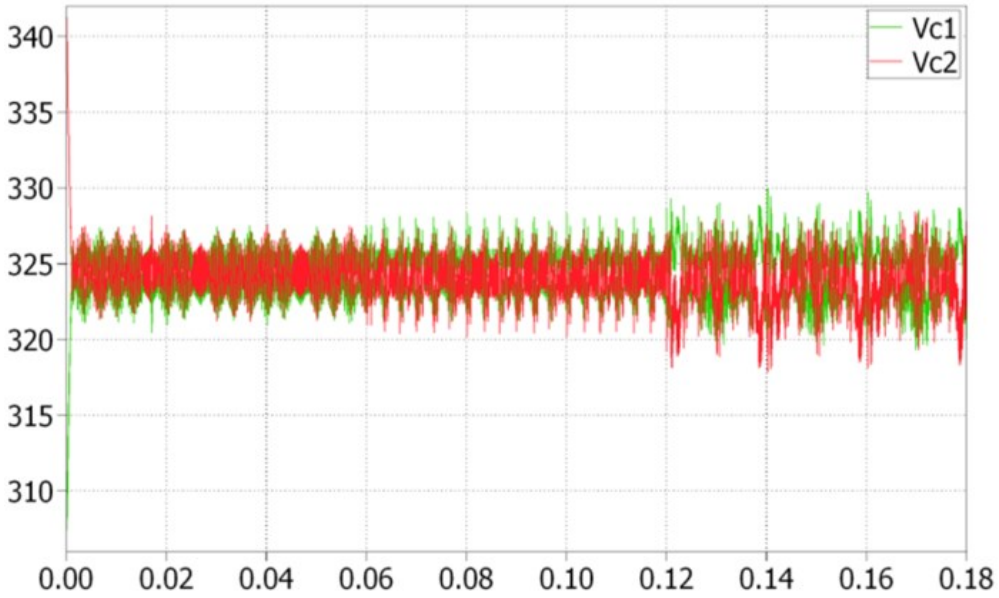


Fig. 2.22: Bus capacitor voltages for the NTV SV-PWM.

Number of commutations

Normally, total power losses can be divided into two main parts: switching losses and conduction losses. The critical parameter is clearly represented by switching losses since different modulation techniques introduce different number of switches. In this subsection, losses have been estimated by evaluating the number of switches inside a modulation period. A comparison of the considered modulation strategies in terms of number of commutations, is reported in **Table IV**. In particular, number of switches normalized s_n with respect to the SPWM commutations have been considered, in order to highlight the percentage increase or

decrease of a modulation strategy to the common used standard sinusoidal one. The 5-segment NTV SMS produces the best switching losses performance because every modulation cycle one phase is clamped. Furthermore, with HPWM commutation losses can be reduced with respect to DSPWM by acting with D parameter.

Tab. 2.3 Switching losses comparison

MODULATION TECHNIQUE	Normalized number of switches s_n
THI-PWM	1
DS-PWM	1,31
H-PWM (D=0.4)	1,18
5-Segment NTV	0,78
Symmetric NTV	1,05

Harmonic distortion

In grid-connected applications the output waveform (current and voltage) quality becomes very important in order to stay inside regulation limits. The Total-Harmonic-Distortion (THD) allows to evaluate how close the considered waveform is with respect to the fundamental component. This parameter is defined as:

$$\boldsymbol{THD = \frac{\sqrt{\sum_{n=2}^{+\infty} V_n^2}}{V_1}} \quad \textbf{(21)}$$

Another harmonic distortion meter, named Weighted-THD WTHD), can be used instead of THD. This parameter "weights" the harmonic amplitude with the harmonic order as follows:

$$\boldsymbol{WTHD = \frac{\sqrt{\sum_{n=2}^{+\infty} \left(\frac{V_n}{n}\right)^2}}{V_1}} \quad \textbf{(22)}$$

In **Tab. 2.4**, a comparison of the considered modulation strategies in term of line-to-line voltage and phase-current WTHD (up to 48-th harmonic) is presented. All techniques present limited harmonic distortion, in accordance with grid-injection regulations. The best harmonic content is provided by the SVM.

Tab. 2.4 Voltage and current WTHD comparison

MODULATION TECHNIQUE	WTHD VOLTAGE [%]	WTHD CURRENT[%]
THI-PWM	0,269	0,119
DS-PWM	0,310	0,232
H-PWM (D=0.4)	0,290	0,212
5-Segment NTV	0,182	0,163
Symmetric NTV	0,136	0,145

Modulation algorithm complexity

The carrier-based algorithms can be easily implemented with respect to the more complex algorithm required by space vector modulation. In DSP-based applications, if the modulation needs less cycle-time to be implemented, the remaining part of control period can be used for other tasks. Instead, speaking about neutral-point balance control loops, the so called "exact" compensator presents higher complexity, while the "dynamic" regulator is based on a simple PI. In future work, more details about algorithm complexity will be proposed comparing computing-time for all techniques.

NP balancer stability with LCL filter

When the NPC inverter is applied as an interface between a DC source (e.g. a PV system) and the AC-grid network, it is frequently necessary to put a filter between the converter and the grid in order to cut out the high frequency harmonics. Some of the considered techniques, especially the space-vector based ones, introduce instability in the neutral-point balancing mechanism (**Fig. 2.23**). Since the current sense, made before the filter, appears quite noisy and the redundant vector choice, used in SVM balancing algorithm, is based on the current sign, the control system could show instability. The LCL filter, considered in simulation, has the following parameters: inverter-side inductance $L_1 = 1{,}3\ mH$, grid-side inductance $L_2 = 50\ \mu H$, filter capacitance $C_1 = 12\ \mu F$.

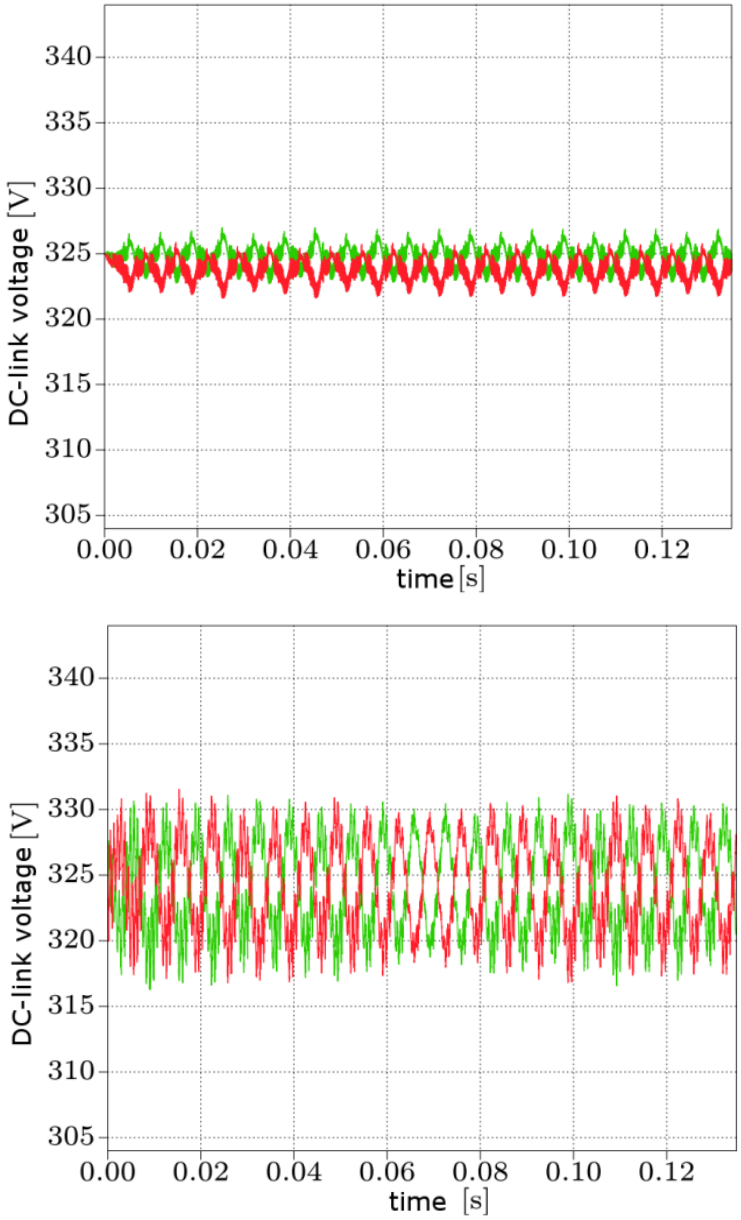


Fig. 2.23: Five-segment NTV SVM N-P ripple without (upper) and with (lower) LCL filter.

Grid-faults simulation

In **Fig. 2.24**, the behavior of the NPC inverter based on HPWM modulation technique assisted with "dynamic" NP balancer, under different possible grid-fault conditions, is shown. Simulations have been performed following CEI 0-21 Italian regulation [49]. For example, from $0{,}20\ s \leq t < 0{,}30$ a symmetric three-phase fault (nominal voltage reduction for all phases) is introduced; instead, from $0{,}40\ s \leq t < 0{,}50$ an asymmetric two-phase fault in MT (amplitude reduction for one phase and phase voltage relation variation) is simulated; finally from $0{,}60\ s \leq t < 0{,}80$ an asymmetric two-phase fault in BT (nominal voltage reduction for two phases) is represented.

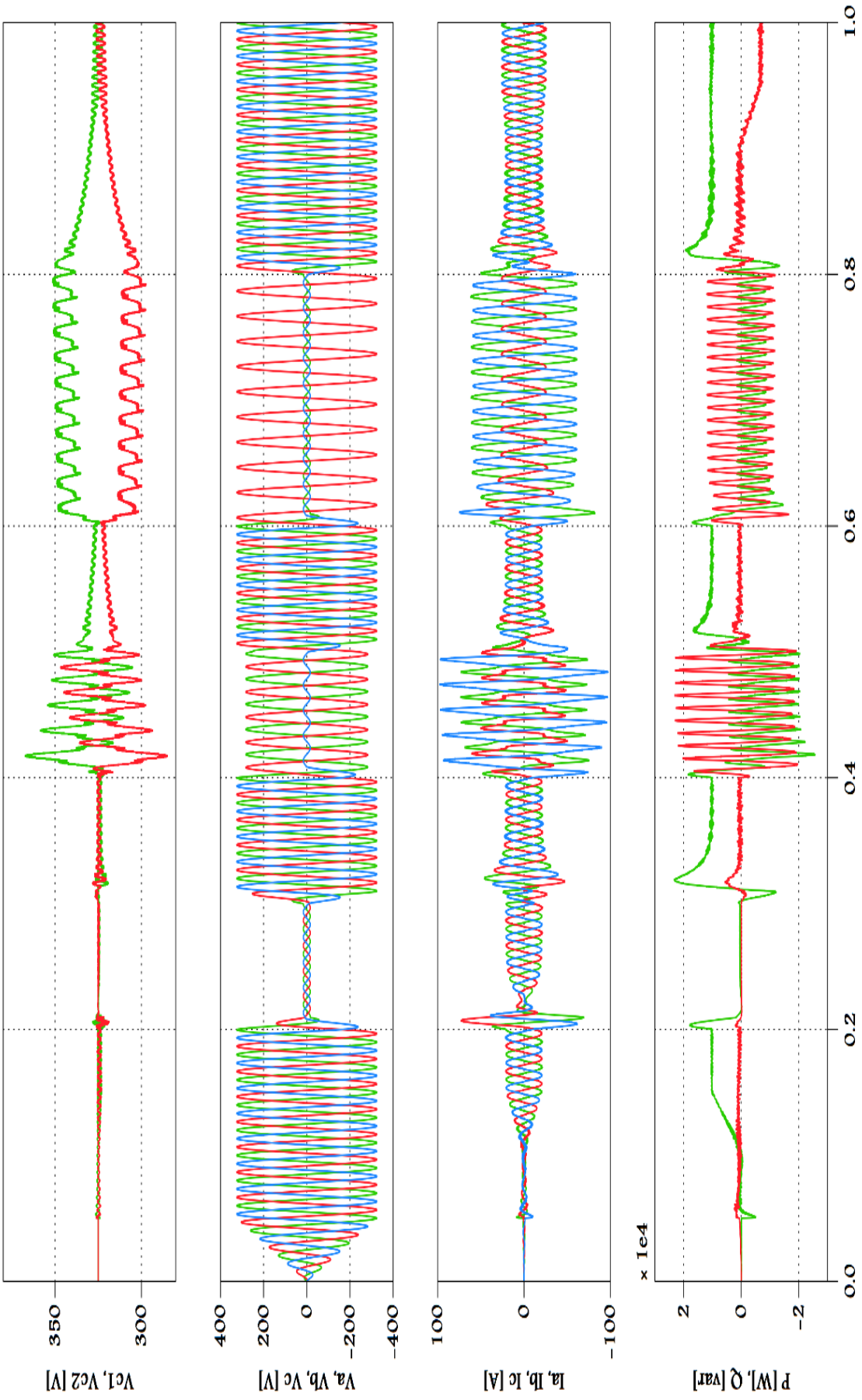


Fig. 2.24: HPWM technique with "dynamic" balancer under grid-faults.

2.5 Analytical approach for power device loss estimation

In this section, a general analytical approach for the calculation of conduction and switching losses will be proposed, emphasizing the role of the modulation strategy and taking also into account datasheet characteristics of the power devices and as a function of temperature [48]. Semiconductor losses are typically the sum of the individual IGBT's and free-wheeling diode's losses. In a 3-level NPC inverter, even clamping diode's losses have to be considered. The main types of losses introduced by power electronic devices are conduction losses and switching losses. Other types, as snubber losses, blocking losses or gate driving losses, usually can be neglected. Switching losses are directly associated with the switching frequency, therefore they usually play a big role in converter efficiency evaluation.

2.5.1 Conduction Losses

The conduction losses of the IGBTs are obtained from the linearization of the static characteristics of the power switches, extrapolated from device datasheet. The output characteristic of the IGBTs typically describes the relationship between voltage drop v_{F0} and collector current i_F, as shown in **Fig. 2.25**.

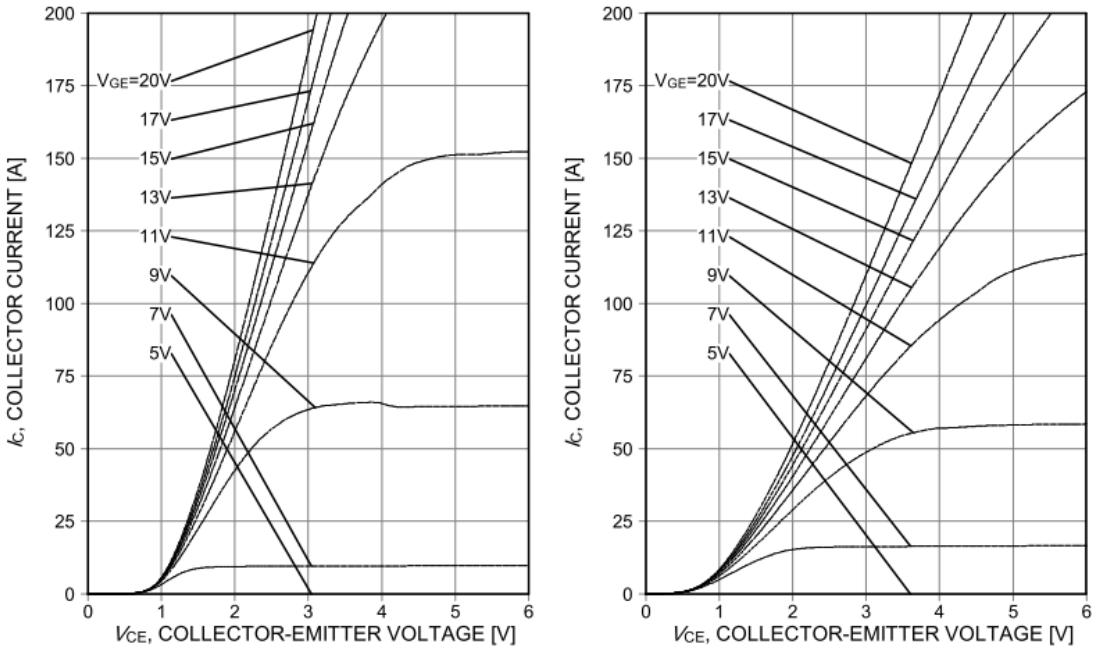


Fig. 2.25: Typical output characteristic from a device manufacturer datasheet.

This non-linear dependency in the on-state of the power switch is modeled by a linear model having an ideal voltage source and a series resistor, i.e.

$$\boldsymbol{P_{cond}(t) = V_{F0} \cdot i_F(t) + R_{on} \cdot {i_F}^2(t)} \quad \textbf{(23)}$$

where V_{F0} is the no-current collector-emitter voltage saturation voltage, R_{on} is the differential resistance of the output characteristics, i_F is the forward current flowing through the device.

Thus, the expression of the conduction losses can be approximated by a second-order polynomial fitting curve:

$$\boldsymbol{P_{cond} = c \cdot i_F + d \cdot {i_F}^2} \quad \textbf{(24)}$$

in which the coefficients c and d are calculated from the experimental curve.

To describe the temperature dependency of the curve, these coefficients can be made temperature-dependent. Normally, datasheets report two characteristics at different operating temperatures T, resulting in a first-order approximation:

$$\begin{cases} \boldsymbol{c(T) = c_0 + c_1 \cdot T \quad d(T) = d_0 + d_1 \cdot T} \\ \boldsymbol{P_{cond}(t,T) = (c_0 + c_1 \cdot T) \cdot i_F(t) + (d_0 + d_1 \cdot T) \cdot {i_F}^2(t)} \end{cases} \quad \textbf{(25)}$$

A similar approach can be utilized for free-wheeling and clamping diodes.

Now, due to conduction loss dependency on the modulating function, the average conduction losses during a modulating period T_m can be calculated as follows:

$$\boldsymbol{\langle P_{cond}(t)\rangle_{T_m} = \frac{1}{T_m}\int_0^{T_m} (V_{F0} + R_{on} i_F(t)) i_F(t)\, dt} \quad \textbf{(26)}$$

Splitting eq. (26) into two integrals, the conduction losses term can be rewritten as:

$$\begin{aligned} \boldsymbol{\langle P_{cond}(t,T)\rangle_{T_m}} &= \boldsymbol{V_{F0}\frac{1}{T_m}\int_0^{T_m} i_F(t)\, dt + R_{on}\frac{1}{T_m}\int_0^{T_m} {i_F}^2(t)\, dt} \\ &= \boldsymbol{V_{F0} I_F^{avg} + R_{on}(I_F^{rms})^2} \end{aligned} \quad \textbf{(27)}$$

in which I_F^{avg} is the average value of current within a modulating period, whereas I_F^{rms} is its root mean square value. These values are strongly affected by the modulation technique, the modulation index M and the power factor PF. Furthermore, they present different expressions for the IGBT, the freewheeling diodes and the clamping diodes.

Assuming that the load current is purely sinusoidal and resistive-inductive load is considered with a power factor angle φ, the load current can be expressed as:

$$\boldsymbol{i_L(t) = {I_F}^{max} sin(\omega t - \varphi)} \quad \textbf{(28)}$$

Current flowing through, for example, transistor T_1 is discontinuous and its average value during a switching period T_{sw} is:

$$\langle \boldsymbol{i_{T_1}(t)} \rangle_{T_{sw}} = \boldsymbol{d_{T_1}(t) i_L(t)} \tag{29}$$

where $i_L(t)$ is the mean current value and $d_{T_1}(t)$ is the duty-cycle function during a single switching period for the outer upper transistor T_1 of a single NPC leg.

Until now, the conduction loss derivation is independent of the adopted modulation strategy. If pure *sinusoidal modulation* is considered, the duty-cycle function in (29) is:

$$\boldsymbol{d_{T_1}(t)} = \begin{cases} \boldsymbol{M\, sin(\omega_m t)} & \boldsymbol{\varphi < \omega_m t < \pi} \\ \boldsymbol{0} & \boldsymbol{\pi < \omega_m t < 2\pi + \varphi} \end{cases} \tag{30}$$

Average and root mean square values of current during a modulating period in (27) for T_1 are:

$$\boldsymbol{I_{T_1}^{avg}} = \boldsymbol{\frac{1}{2\pi} \int_0^{2\pi} d_{T_1}(\alpha)\, i_L(\alpha) d\alpha = \frac{M \cdot {I_{T_1}}^{max}}{4\pi} [(\pi - \varphi) PF + sin\, \varphi]} \tag{31}$$

$$\boldsymbol{(I_{T_1}^{rms})^2} = \boldsymbol{\frac{1}{2\pi} \int_0^{2\pi} d_{T_1}(\alpha)\, i_L(\alpha)^2 d\alpha = \frac{M \cdot ({I_{T_1}}^{max})^2}{6\pi} (1 + \cos \varphi)^2} \tag{32}$$

Thus, the outer IGBT T_1 conduction loss expression is the following:

$$\begin{aligned} \langle \boldsymbol{P_{cond}(t)} \rangle_{T_m} = \boldsymbol{\frac{M \cdot {I_{T_1}}^{max}}{12\pi}} \{ & \boldsymbol{3V_{F0}[(\pi - \varphi) PF + sin\, \varphi]} \\ & \boldsymbol{+ 2R_{on} {I_{T_1}}^{max} (1 + cos\, \varphi)^2} \} \end{aligned} \tag{33}$$

Similarly, conduction loss values for the other transistors and diodes can be calculated, obtaining the expressions reported in **Tab. 2.5**.

Tab. 2.5 Integrals for pure SPWM

	$\mathbf{d(t)}$	$\mathbf{I_F^{avg}/I_F{}^{max}}$	$\mathbf{(I_F^{rms})^2 /(I_F{}^{max})^2}$
$\mathbf{T_1}$	$\begin{cases} \mathrm{M}\sin(\omega_\mathrm{m}\mathrm{t}) & \varphi < \omega_\mathrm{m}\mathrm{t} < \pi \\ 0 & \pi < \omega_\mathrm{m}\mathrm{t} < 2\pi + \varphi \end{cases}$	$\frac{\mathrm{M}}{2}[(\pi - \varphi)\cos(\varphi) + \sin(\varphi)\,]$	$\frac{\mathrm{M}}{3}[1 + \cos(\varphi)]^2$
$\mathbf{T_2}$	$\begin{cases} 1 & \varphi < \omega_\mathrm{m}\mathrm{t} < \pi \\ 1 - \lvert\mathrm{M}\sin(\omega_\mathrm{m}\mathrm{t})\rvert & \pi < \omega_\mathrm{m}\mathrm{t} < \pi + \varphi \\ 0 & \varphi + \pi < \omega_\mathrm{m}\mathrm{t} < 2\pi + \varphi \end{cases}$	$2 + \frac{\mathrm{M}}{2}[\varphi\cos(\varphi) - \sin(\varphi)]$	$\frac{\pi}{2} - \frac{\mathrm{M}}{3}[1 - \cos(\varphi)]^2$

D_5	$\begin{cases} 1-\lvert M\sin(\omega_m t)\rvert & \varphi < \omega_m t < \pi \\ 1-\lvert M\sin(\omega_m t-\pi)\rvert & \pi < \omega_m t < \pi+\varphi \\ 0 & \varphi+\pi < \omega_m t < 2\pi \end{cases}$	$2 + \frac{M}{2}[(2\pi-\varphi)\cos(\varphi) - 2\sin(\varphi)]$	$\frac{\pi}{2} - \frac{2M}{3}[1+\cos(\varphi)]^2$
$\boldsymbol{D_{1,2}}$	$\begin{cases} M\sin(\omega_m t) & 0 < \omega_m t < \varphi \\ 0 & \varphi < \omega_m t < 2\pi \end{cases}$	$\frac{M}{2}[-\varphi\cos(\varphi)+\sin(\varphi)]$	$\frac{M}{3}[1-\cos(\varphi)]^2$

Using SPWM with third harmonic injection, the duty-cycle functions change into:

$$d_{T_1}(t) = \begin{cases} M\left(\sin\omega_m t - \frac{3\sqrt{3}}{4\pi}\sum_{r=0}^{\infty}\frac{1}{(3r+1)(3r+2)}\sin[3(2r+1)\omega_m t]\right) & \varphi < \omega_m t < \pi \\ 0 & \pi < \omega_m t < 2\pi+\varphi \end{cases} \quad (34)$$

Evaluating the corresponding $I_{T_1}^{avg}$ and $(I_{T_1}^{rms})^2$, it can be demonstrated that the term introduced by third harmonic is negligible with respect the pure sinusoidal one.

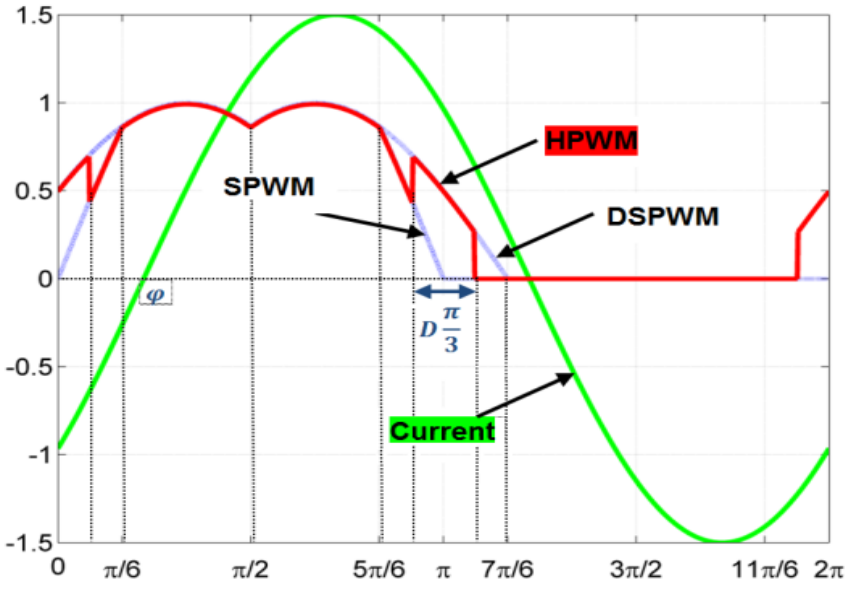


Fig. 2.26: Hybrid positive modulating signal (red) and current sinusoidal waveform (green).

Now, writing equations **(31)** and **(32)** for *hybrid modulation* (HPWM of Section 2.4.3) implies to evaluate the integral of the product between the modulating signal and the phase current. This product is non-zero for transistor T_1 only when both current (green curve in **Fig. 2.26**) and modulating signal (red curve) are positive.

$$I_{T_1}^{avg} = \frac{1}{2\pi}\int_{\varphi}^{\pi+D\frac{\pi}{6}} d_{T_1}(\alpha)\, i_L(\alpha)\, d\alpha \quad (35)$$

For each interval delimited by a dotted line in **Fig. 2.26**, the duty cycle can be expressed by a different analytical function and the integral have different integration bounds: e.g. the interval $\alpha \in \left[\frac{\pi}{6};\frac{\pi}{2}\right]$ can approximated with the function $\cos(\theta - \pi/6)$, and the interval $\alpha \in \left[\frac{5\pi}{6};\pi - \frac{D\pi}{6}\right]$with $\sqrt{3}\cos(\theta)$.Therefore, equation **(35)** can be split into the following terms:

$$\boldsymbol{I_{T_1}^{avg} = \frac{1}{2\pi}\int_{\varphi}^{\frac{\pi}{2}}(\cdot)d\alpha + \int_{\frac{\pi}{2}}^{\frac{5\pi}{6}}(\cdot)d\alpha + \int_{\frac{5\pi}{6}}^{\pi-D\frac{\pi}{6}}(\cdot)d\alpha + \int_{\pi-D\frac{\pi}{6}}^{\pi+D\frac{\pi}{6}}(\cdot)d\alpha} \qquad \textbf{(36)}$$

in which the last two terms clearly depends on the hybridization factor D. Also the power factor affects the number and type of terms that are present in integral function. Solution of equation **(36)** is quite complex and it has not been reported in this dissertation.

2.5.2 Switching Losses

Switching losses are generated during the turn-on and turn-off switching process of the power devices. Voltages and currents can assume relevant values simultaneously, thus reaching high instantaneous power levels. Switching losses are proportional to the switching frequency, becoming absolutely predominant with respect to conduction losses in high frequency applications. Hereafter, an analytical expression for the switching losses in NPC inverters will be calculated in the case of the considered modulation strategies.

The characteristic curves of the energy losses as a function of the current, blocking voltage, the junction temperature, gate resistor and the wiring stray inductance are reported on the data sheets of power devices, as shown in **Fig. 2.27**.

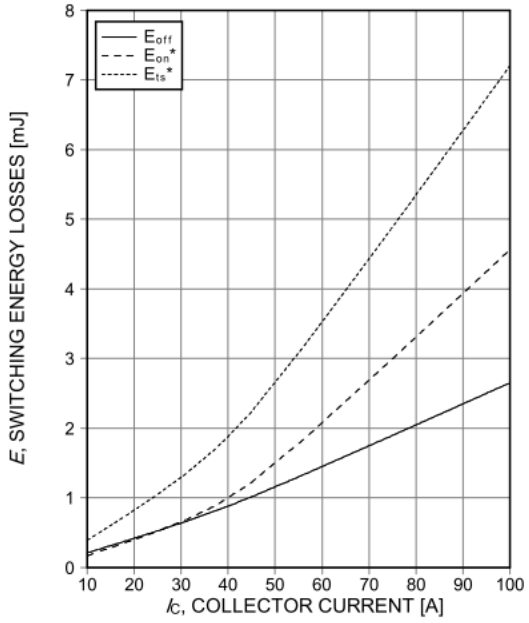


Figure 13. Typical switching energy losses as a function of collector current (ind. load, T_j=175°C, V_{CE}=400V, V_{GE}=15/0V, R_G=7Ω, test circuit in Fig. E)

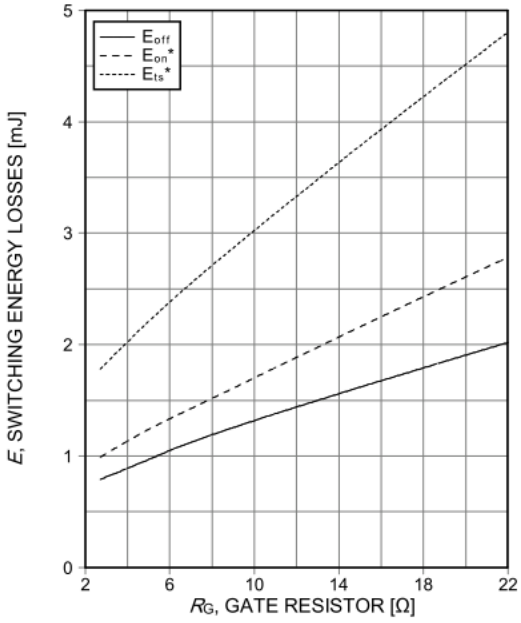


Figure 14. Typical switching energy losses as a function of gate resistor (ind. load, T_j=175°C, V_{CE}=400V, V_{GE}=15/0V, I_C=50A, test circuit in Fig. E)

Fig. 2.27: Typical switching energy characteristic from a device manufacturer datasheet.

These experimental curves can be easily approximated by sampling and interpolating with a second order equation.

The adopted expression used to calculate the mean value of the switching losses for transistor T_1 within a switching period T_{sw} is:

$$\langle \boldsymbol{P_{sw}(t)} \rangle_{T_{sw}} = \frac{\mathbf{1}}{\boldsymbol{T_{sw}}} \left[\boldsymbol{E^{on}}\left(\boldsymbol{I_F}^{ref}, \boldsymbol{V_{OFF}}^{ref} \right) + \boldsymbol{E^{off}}\left(\boldsymbol{I_F}^{ref}, \boldsymbol{V_{OFF}}^{ref} \right) \right] \frac{\boldsymbol{i_F(t)} \cdot \boldsymbol{v_{OFF}}}{\boldsymbol{I_F}^{ref} \cdot \boldsymbol{V_{OFF}}^{ref}} \tag{37}$$

where E^{on} and E^{off} are the energy dissipated during the turn on and turn off processes, respectively. These values are given for a certain forward current $I_F{}^{ref}$ and blocking voltage $V_{OFF}{}^{ref}$ ($i_F(t)$ is the current flowing through the device and v_{OFF} is its blocking voltage). Equation **(37)** assumes a proportional relationship between energy and both current and voltage, as normally done.

The average switching losses during a modulation period T_m are given by:

$$\langle \boldsymbol{P_{sw}} \rangle_{T_m} = \frac{\mathbf{1}}{\boldsymbol{n}} \sum_{\boldsymbol{j=1}}^{\boldsymbol{n}} \left\{ \frac{\mathbf{1}}{\boldsymbol{T_{sw}}} \left[\boldsymbol{E^{on}}\left(\boldsymbol{I_F}^{ref}, \boldsymbol{V_{OFF}}^{ref} \right) + \boldsymbol{E^{off}}\left(\boldsymbol{I_F}^{ref}, \boldsymbol{V_{OFF}}^{ref} \right) \right] \frac{\boldsymbol{i_F(jT_{sw})} \cdot \boldsymbol{v_{OFF}}}{\boldsymbol{I_F}^{ref} \cdot \boldsymbol{V_{OFF}}^{ref}} \right\} \tag{38}$$

in which n is the number of commutations within the period and conducted current is evaluated within each switching period, i.e. $i_F(jT_{sw})$, thus considering only average current value and neglecting the superimposed ripple.

$$\langle \boldsymbol{P_{sw}} \rangle_{T_m} = \boldsymbol{f_{sw}}\left(\boldsymbol{E^{on}} + \boldsymbol{E^{off}}\right) \frac{\boldsymbol{v_{OFF}}}{\boldsymbol{I_F}^{ref} \cdot \boldsymbol{V_{OFF}}^{ref}} \cdot \frac{\mathbf{1}}{\boldsymbol{n}} \sum_{\boldsymbol{j=1}}^{\boldsymbol{n}} \boldsymbol{i_F(jT_{sw})} \tag{39}$$

If the frequency ratio between switching and modulating frequencies is sufficiently high, the discrete summation can be approximated by a continuous time integral:

$$\frac{\mathbf{1}}{\boldsymbol{n}} \sum_{\boldsymbol{j=1}}^{\boldsymbol{n}} \boldsymbol{i_{F_j}} \approx \frac{\mathbf{1}}{\boldsymbol{2\pi}} \int_{\mathbf{0}}^{\boldsymbol{2\pi}} \boldsymbol{i_{T/D}(\omega_m t) d\omega_m t} \tag{40}$$

and the average value of the switching losses can be calculated in closed form.

$$\langle \boldsymbol{P_{sw}} \rangle_{T_m} = \boldsymbol{f_{sw}}\left(\boldsymbol{E^{on}} + \boldsymbol{E^{off}}\right) \frac{\boldsymbol{v_{OFF}}}{\boldsymbol{I_F}^{ref} \cdot \boldsymbol{V_{OFF}}^{ref}} \cdot \frac{\mathbf{1}}{\boldsymbol{2\pi}} \int_{\boldsymbol{\alpha_1}}^{\boldsymbol{\alpha_2}} \boldsymbol{i_L(\alpha) d\alpha} \tag{41}$$

where α_1 and α_2 depend on the considered device of the NPC half-leg ($\alpha_2 - \alpha_1$) is the interval in which the load current flows through the considered device).

In the case of *sinusoidal modulation*, the outcome of the integrals in **(41)** for the inverter half leg devices (T_1, T_2, D_1, D_2, D_5) has been reported in **Tab. 2.6**.

Tab. 2.6 Switching integrals for pure SPWM

Device	$\boldsymbol{\alpha_1, \alpha_2}$	$\int \ldots$
$\mathbf{T_1}$	φ,π	$1 + \cos(\varphi)$
$\mathbf{T_2}$	π,π + φ	$1 - \cos(\varphi)$
$\mathbf{D_5}$	φ,π + φ	2
$\mathbf{D_1 - D_2}$	0,φ	$1 - \cos(\varphi)$

In **Fig. 2.32**, the switching loss distribution over these devices is presented as a function of the load phase angle φ. One can notice that, if $\varphi = 0$, only T_1 and D_5 are switching and consequently they have non-zero switching losses. As the load phase angle increases, losses associated with T_1, D_2 and D_2 are becoming significant.

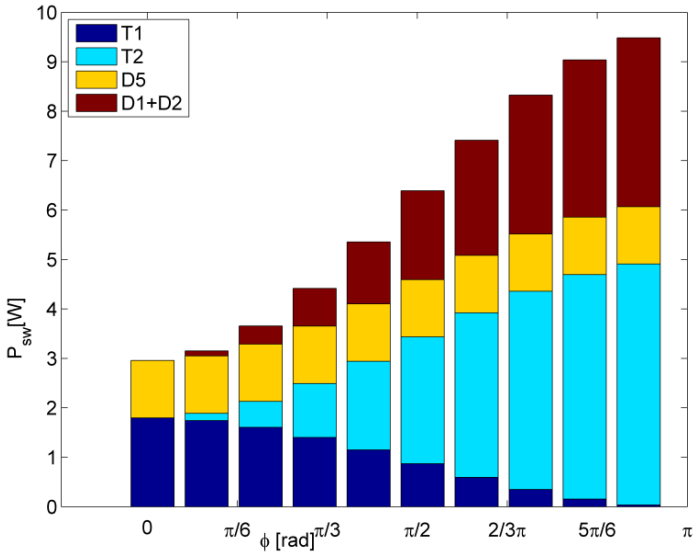


Fig. 2.28: Losses distribution for SPWM.

On the other hand, in the case of hybrid modulation, the current is not flowing in the top switch for the whole half-period of the modulating waveform, as the clamping interval $\left[\pi + D\frac{\pi}{6}\,;\frac{7\pi}{6}\right]$ has been introduced, as shown in **Fig. 2.26**. Depending on the value of φ, the continuous time integrals in **(41)** follow the expressions reported in **Tab. 2.7.**

In **Fig. 2.29**, the switching loss distribution over these devices is presented as a function of the load phase angle φ. In this case, if $\varphi = 0$, all devices are switching and consequently they have non-zero switching losses. As well as the sinusoidal case, when the load phase angle increases, losses are becoming larger. The 3D map of **Fig. 2.30** shows the normalized (with respect to SPWM case) switching losses as a function of both hybrid factor and phase angle. Two main aspects are well highlighted by **Fig. 2.30**, i.e. switching losses increase significantly with D and there is a peak in correspondence of phase angle $\varphi = \frac{\pi}{2}$, confirming analytical study of Section 2.4.3.

Tab. 2.7 Switching integrals for pure HPWM

Device	$\boldsymbol{\alpha_1, \alpha_2}$		$\int \ldots$
$\boldsymbol{T_1}$	$D\frac{\pi}{6} < \varphi < \pi - D\frac{\pi}{6}$	$\varphi, \pi + D\frac{\pi}{6}$	$1 + \cos(D\frac{\pi}{6} - \varphi)$
	$\varphi < D\frac{\pi}{6}$	$\varphi, \pi + \varphi$	2
$\boldsymbol{T_2}$	$D\frac{\pi}{6} < \varphi < \pi - D\frac{\pi}{6}$	$\pi - D\frac{\pi}{6}\,,\ \pi + \varphi$	$1 - \cos(D\frac{\pi}{6} + \varphi)$

	$\varphi < D\frac{\pi}{6}$	$\varphi, D\frac{\pi}{6}$ and $\pi - D\frac{\pi}{6}$, $\pi + \varphi$	$2 - \cos\left(D\frac{\pi}{6} + \varphi\right) - \cos(D\frac{\pi}{6} - \varphi)$
$\boldsymbol{D_5}$	$\varphi, \pi + \varphi$		2
$\boldsymbol{D_1/D_2}$	$-D\frac{\pi}{6}, \varphi$		$1 - \cos(D\frac{\pi}{6} + \varphi)$

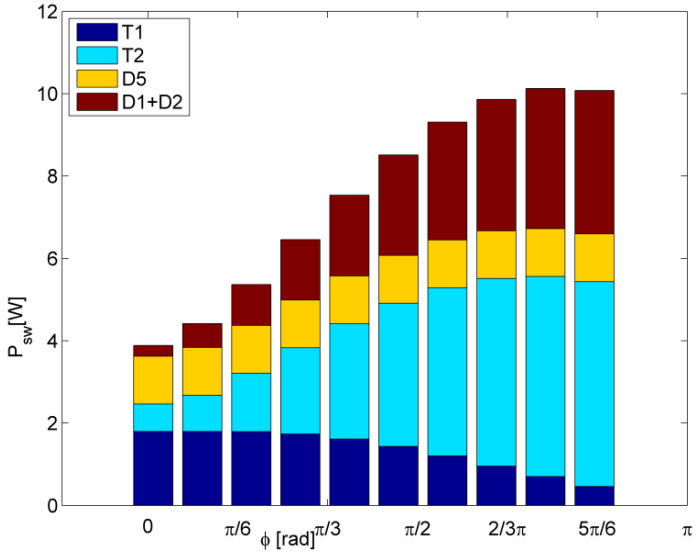


Fig. 2.29: Losses distribution for HPWM.

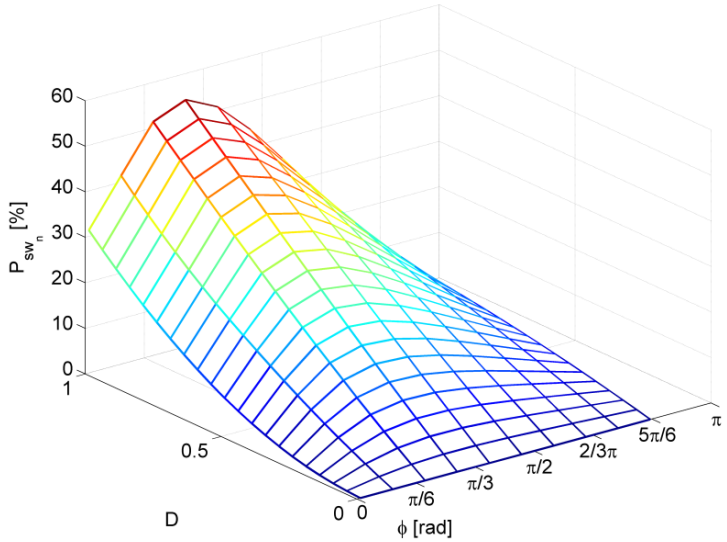


Fig. 2.30: Normalized switching losses as a function of hybrid factor and phase angle.

2.5.3 Simulations

A simulation model of the three-phase three-level neutral-point-clamped inverter has been implemented in a standalone PLECS tool. Thermal description of power switches are also

embedded in the model in order to characterize losses under different operating conditions. Complete list of model parameters can be found in **Tab. 7.2** of Appendix.

In **Fig. 2.31** main waveforms of the modulation are drawn, namely output phase current, modulating signals and output leg voltage in the case of a symmetric three-phase grid. HPWM with $D = 0.5$ is considered, as can be noticed from the shape of the modulating signals.

Power losses, both conduction and switching, are represented in **Fig. 2.32** as a function of the modulation index and the power factor of the load. Switching losses are roughly linear with respect to modulation index (as expected) and increase as the power factor decreases, due to the higher contribution of the diode losses. Conduction losses are slightly affected by modulation index, following a quadratic law, and increase with the power factor.

Fig. 2.33 shows the value of the weighted total-harmonic-distortion (WTHD) as a function of the modulation index and the power factor of the load. WTHD is particularly important due to EMI current harmonics regulations for grid connected devices. Peak values of WTHD are limited to less than 1.5%, decrease as a function of the modulation index and increase with power factor.

Finally in **Fig. 2.34** the neutral point peak-to-peak voltage oscillation is drawn in steady-state and symmetric load conditions.

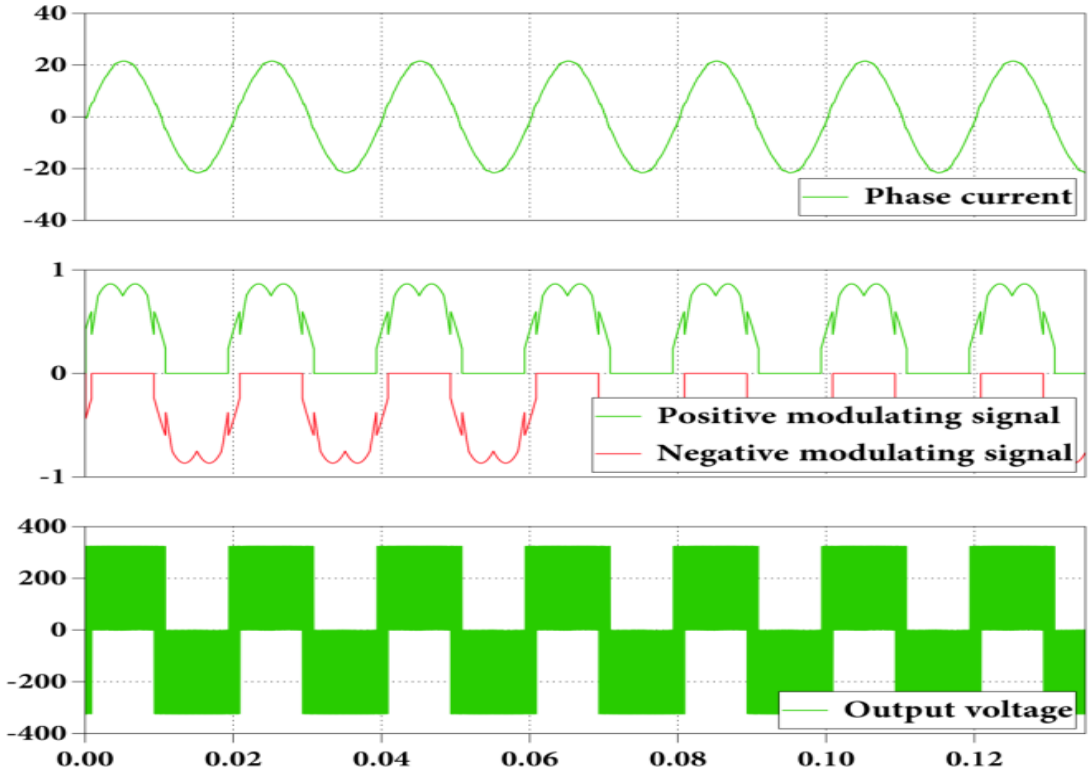


Fig. 2.31: Current, modulating signals and voltage for HPWM with $D = 0.5$

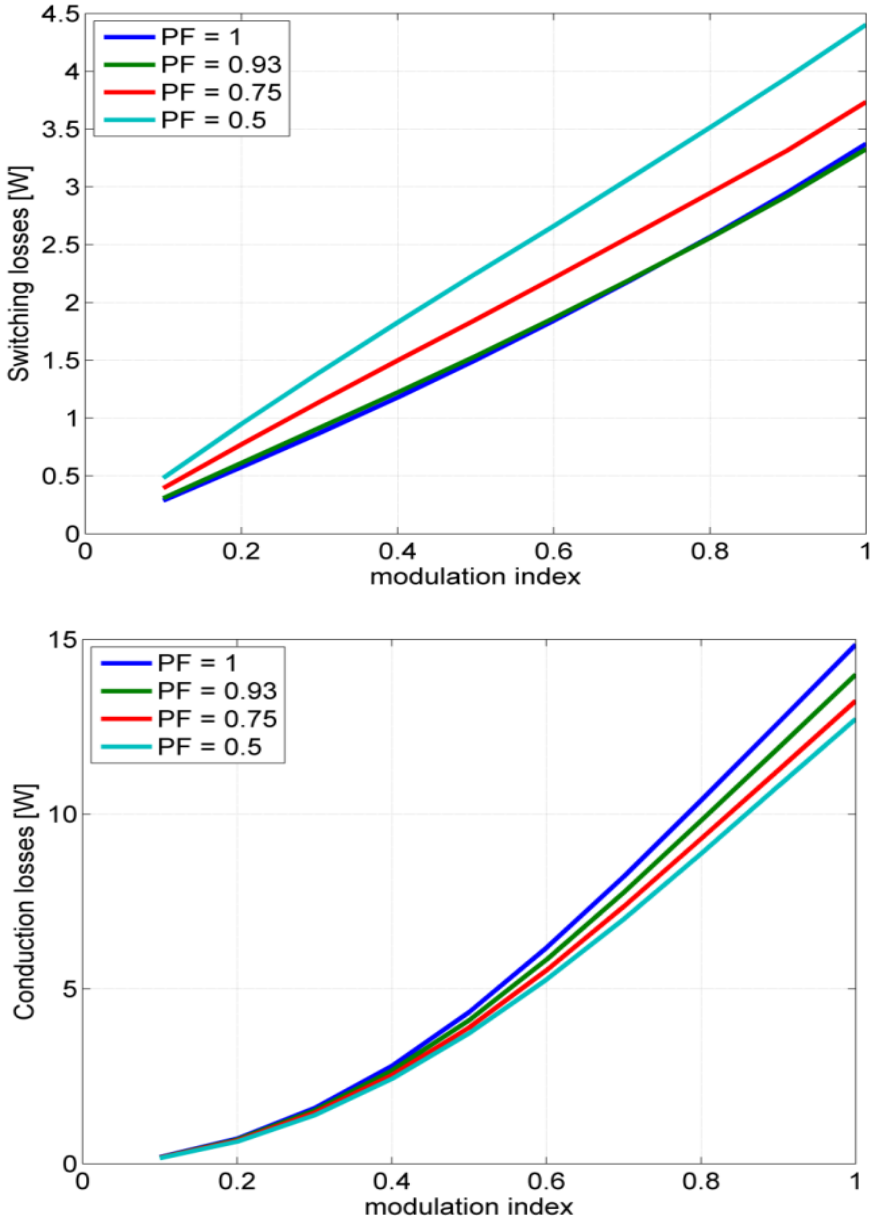


Fig. 2.32: Switching and conduction losses (HPWM,D = 0.5).

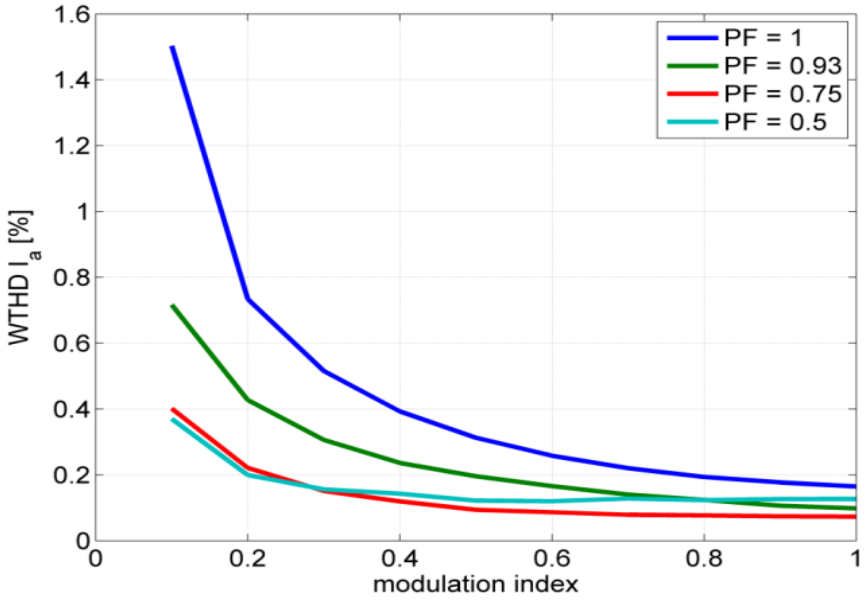


Fig. 2.33: Weighted total-harmonic-distortion of output current (HPWM, *D*=0.5).

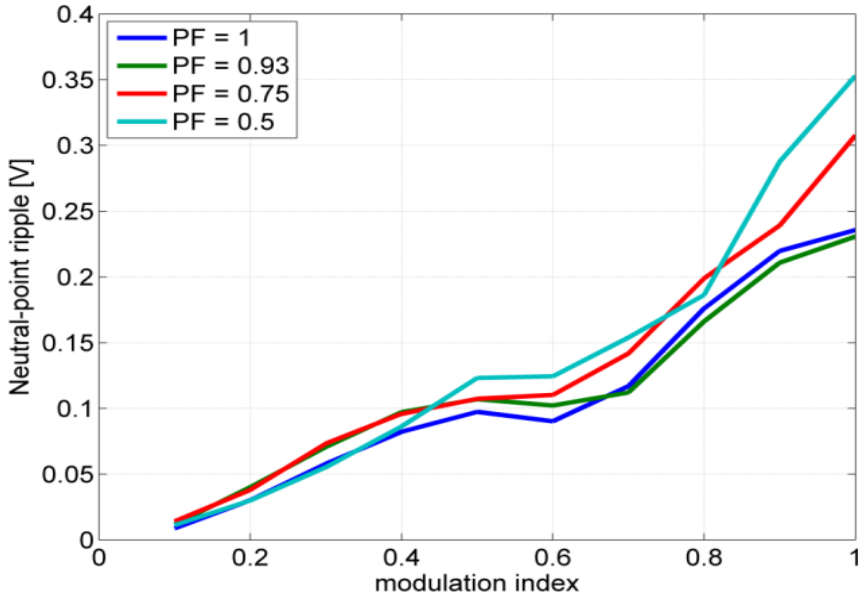


Fig. 2.34: Neutral-point peak-to-peak voltage ripple at steady-state (HPWM, *D*=0.5).

2.6 Proposed modulation techniques

2.6.1 Discontinuous-hybrid modulation (DHPWM)

Discontinuous modulation

The main idea of discontinuous PWM is to substantially reduce switching losses by clamping one phase every 60° of the fundamental wave during the maximum/minimum value of the phase current. This objective could be easily achieved by utilizing a proper type of zero sequence signal injection on standard sinusoidal modulating signals. In [24], a generalized discontinuous PWM modulation method with superior high modulation operating range performances is developed for three phase two level inverter. The Discontinuous algorithm is applied for a three phase three level neutral point clamped inverter in [29] and [37].

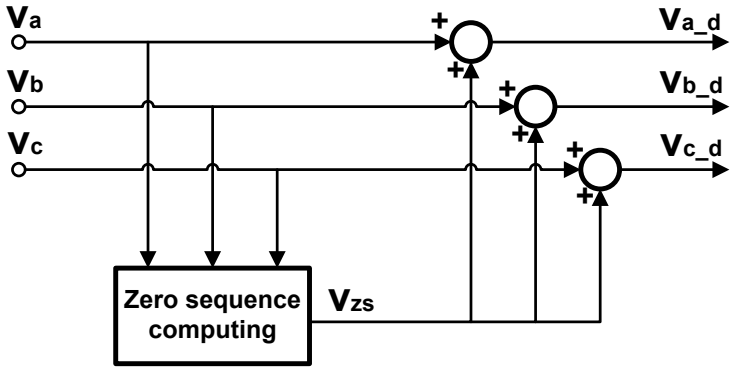


Fig. 2.35: Generation of discontinuous modulation signals.

As shown in **Fig. 2.35**, a zero sequence computing block calculates the signal to inject into every reference to obtain the desired discontinuous modulation signals. In **Fig. 2.36**, the discontinuous modulating signal for one of the three legs is shown. For a certain amount of the fundamental period, the PWM modulation of each phase is halted and the output voltage is clamped to the positive or negative DC-link. Since the clamping interval is one third of the fundamental period (i.e. 120°), this modulation reduces the average switching frequency by 33%. Consequently, it will provide a sensible reduction of switching losses.

Depending on the phase angle between the output voltage and current, the clamping zone midpoint can be shifted in order to align the non-commutating zones to the peaks of the current.

As a drawback the neutral-point ripple is higher as compared to the standard sinusoidal modulation and the control of the DC value of the NP voltage with the injection of a simple common mode value has limited effect.

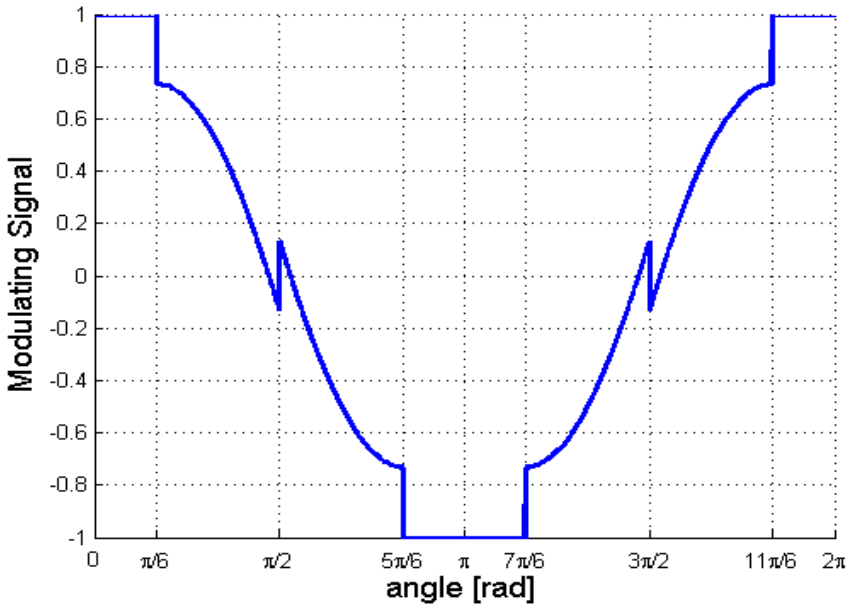


Fig. 2.36: Modulation signal for the DPWM with $\gamma = 0$.

DHPWM concept

Reduction of the switching losses is frequently achieved by the adoption of discontinuous modulation schemes, where the PWM modulation of each phase is halted and the output voltage is clamped to the positive or negative DC-link for a certain amount of the fundamental period. If the clamping intervals are properly chosen, the switching losses are reduced and better harmonic characteristics are obtained at a high modulation index as compared to CBPWM.

A new discontinuous hybrid modulation (DHPWM) technique is described here, obtained by combining discontinuous (DPWM) and hybrid (HPWM) pulse width modulations [38]. By sharing the advantages of both techniques a reduction of switching and conduction losses is obtained, control of the low frequency component of NP ripple is maintained and an additional degree of freedom for its active control is theoretically available.

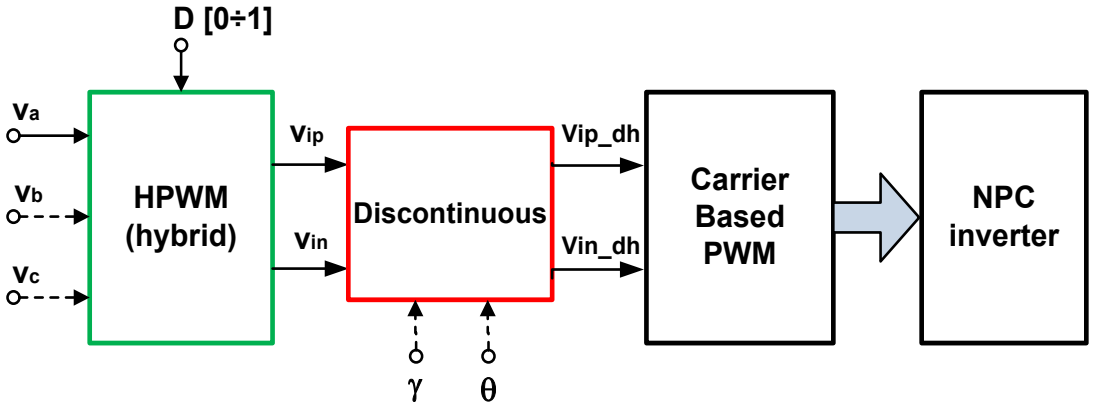


Fig. 2.37: General scheme of discontinuous-hybrid algorithm.

Fig. 2.37 shows the modulation scheme for DHPWM. The three sinusoidal phase voltage references (i.e. v_a, v_b, v_c), represent the input to the hybrid modulation block, together with the hybrid factor D. The outputs of this block are the positive and negative modulating signals v_{ip_h} and v_{in_h} ($i = a, b, c$), as calculated in (2). The two outputs are passed to the discontinuous block where two proper signals (i.e. v_{p_zs} and v_{n_zs}), are generated by the discontinuous algorithm, which determines when the clamping has to performed. These positive and negative zero-sequence values are added to the hybrid signals in order to perform a proper clamping of the output voltage. The output signals from the discontinuous algorithm are:

$$\begin{cases} v_{ip\_DH} = v_{ip\_h} + v_{p\_zs} \\ v_{ip\_DH} = v_{in\_h} + v_{n\_zs} \end{cases} \quad \textbf{(42)}$$

As shown in **Fig. 2.38**, the zero sequence signals v_{p_zs} and v_{n_zs} are a third harmonics of the fundamental frequency, not affecting the phase voltage of the load.

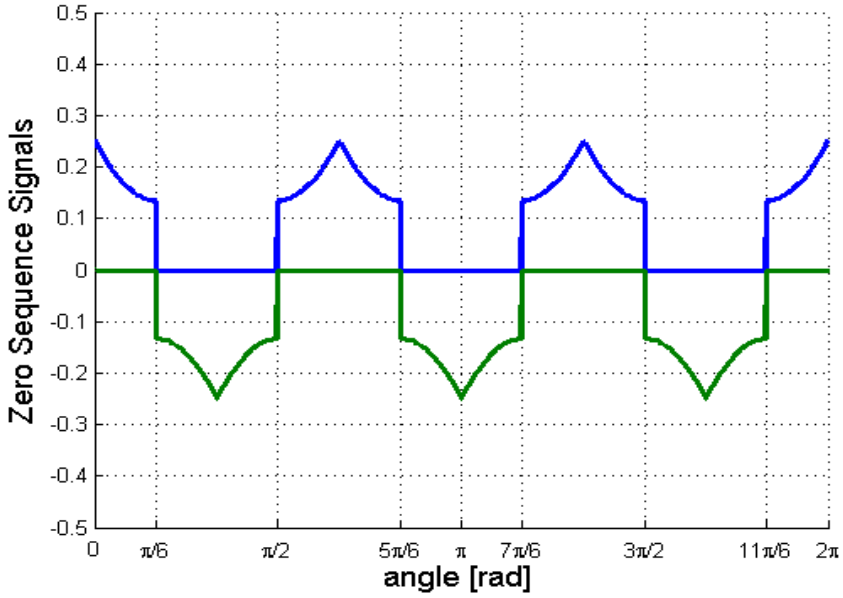


Fig. 2.38: Positive and negative zero sequence signals v_{p_zs} and v_{n_zs}.

The discontinuous block has two important input parameters: angles γ and θ. The first one is used to shift the clamping zone midpoint in order to align the non-commutating zones to the peaks of the current, thus reducing its impact on the switching losses. Its value should therefore be online adapted as a function of the load power factor.

The second parameter, i.e. θ, allows to change the width of the clamping zone and can be usefully employed to control the neutral point voltage, [37]. A combined control can be in fact performed by regulating the value of θ and by a proper additional common mode voltage, as it will be discussed in the next section.

Resulting modulating signals of this two techniques are shown in **Fig. 2.39**. One can notice that, even if the obtained signals are highly discontinuous, the phase voltage continue to be sinusoidal as only common mode voltage is added.

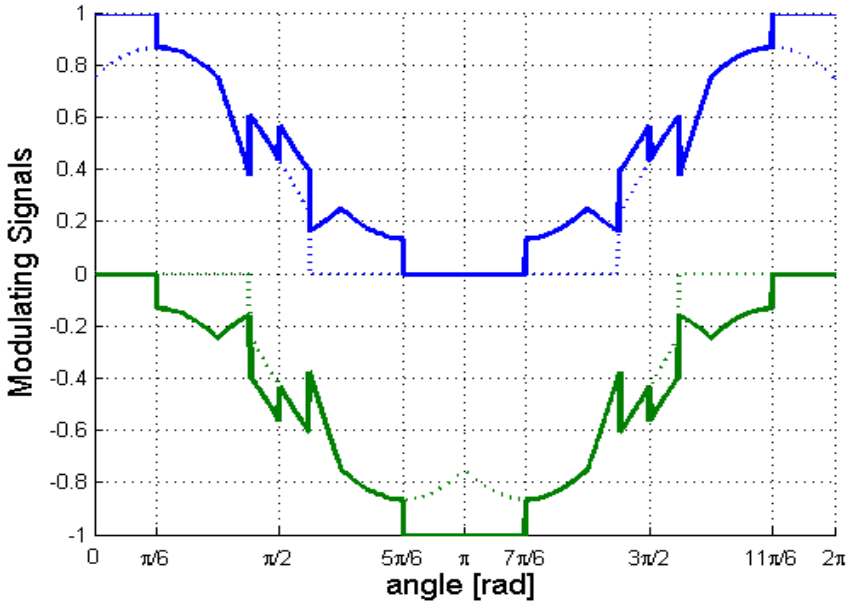


Fig. 2.39: Modulation signals for discontinuous hybrid modulation (solid line) and hybrid (dotted line) (both with $D = 0.5$).

Simulation results

A simulation model of an NPC 3-level three-phase converter driving a passive RL load has been implemented in the standalone PLECS tool, including conduction and switching loss models of the power devices. DHPWM as well as standard SPWM and HPWM techniques have been compared by taking into account overall losses, neutral point voltage ripple and injected current into DC-link capacitance. The same model has been tested with a permanent magnet synchronous motor to provide a preliminary investigation, as experimental results are obtained with such a load.

Simulation and load parameters are reported in **Tab. 7.3** of Appendix. With the considered passive load and the nominal feeding frequency, the phase delay between voltage and current is about $\pi/6$, thus allowing to fix the parameter γ entering into the discontinuous block. The modulating signals in this case are shown in **Fig. 2.40**.

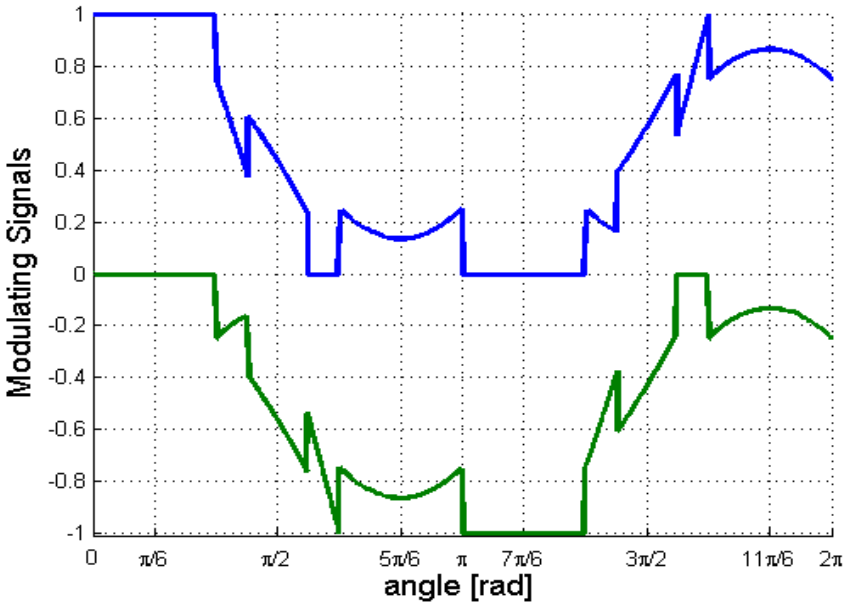


Fig. 2.40: Modulation signals for the DHPWM ($D = 0.5, \gamma = -\pi/6$).

A comparison of the low frequency ripple of the neutral-point voltage for discontinuous-hybrid technique (with D = 0.5) and standard SPWM is shown in **Fig. 2.41**. A sensible reduction of the oscillation amplitude is obtained by DHPWM.

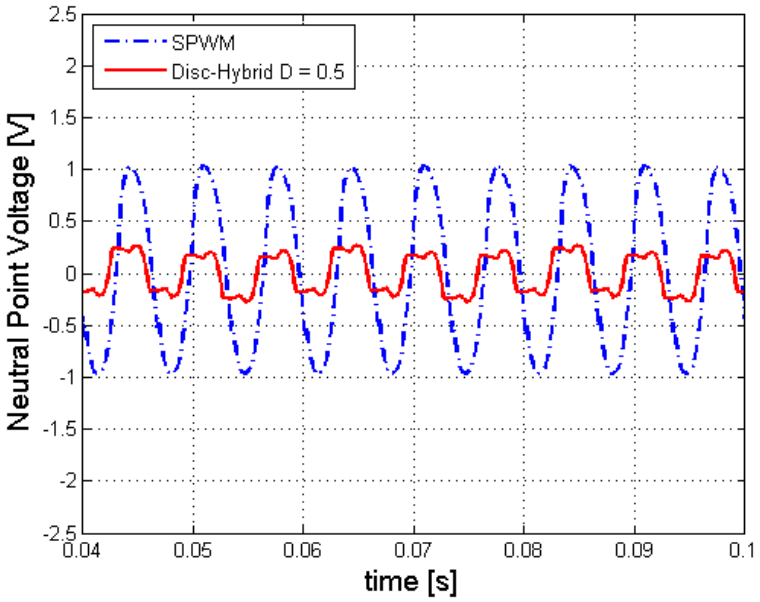


Fig. 2.41: Low frequency ripple of neutral point voltage for SPWM (dotted line) and DHPWM (D = 0.5, solid line).

The same qualitative result applies at different values of parameter D and minimum oscillation is obviously obtained for D = 1.0. In that condition, in fact, HPWM becomes DSPWM and the introduced discontinuity removes any application of zero voltage vectors, thus completely disconnecting the neutral point from the load.

Another important aspect of this technique is the reduction of the RMS value of the neutral point current, as it is highlighted in the results of **Fig. 2.42**. DHPWM technique injects a lower value of current into NP, thus leading to a strong reduction of the requirements for the dc-link capacitors. Furthermore a reduction of the ESR losses in the dc-link capacitors is also obtained.

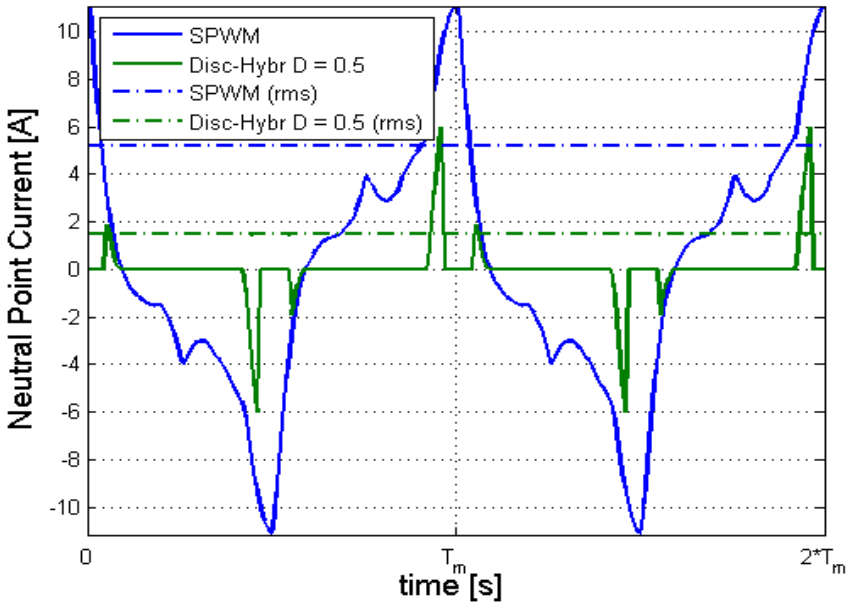


Fig. 2.42: Neutral point currents (solid line) and RMS values (dotted line) for standard SPWM and DHPWM ($D = 0.5$).

Moreover, the locally averaged neutral point current with DHPWM is reduced, thus providing a correspondent reduction of low-frequency variations of the NP voltage. This operating conditions is referred to as AC compensation.

This does not imply DC balance between capacitor voltages. In fact, this modulation strategy would tend to preserve any initial voltage unbalance of the DC-link capacitors. Some compensation loop is therefore needed. The compensator considered hereafter is very simple and provides the required performance in all the operating conditions.

The implementation block diagram is shown in **Fig. 2.43**. A PI regulator controls the voltage difference between the two capacitors (i.e. ΔV_c) by generating a proper gain k that is multiplied to the modulating signals.

Since the factor k decides the duty cycle of the switches in the converter, the output of the PI controller should be limited.

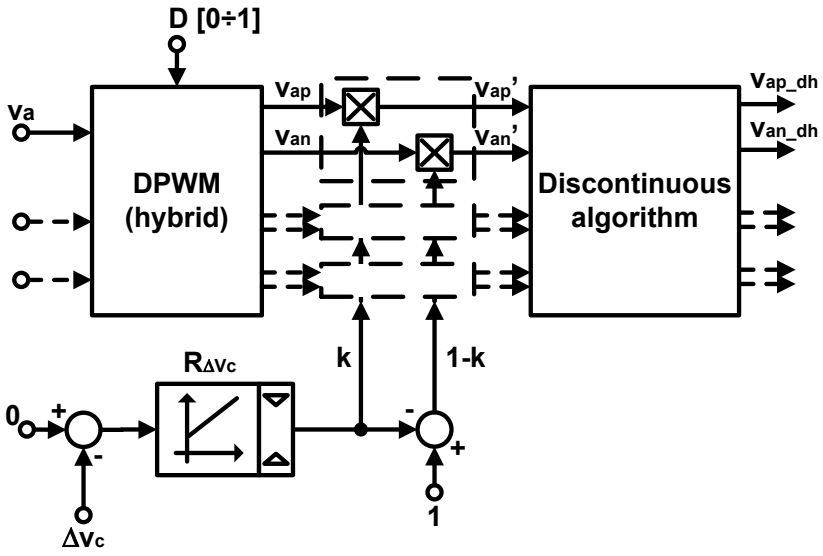


Fig. 2.43: Neutral point voltage control scheme adopting a PI compensator.

In fact, the reference phase voltages for upper carrier should be between 0 and v_{dc} and the reference phase voltage for lower carrier should be between 0 and $-v_{dc}$ to ensure the PWM operation in the linear range. The maximum and minimum limits of the PI controller output are a function of the modulation index m, as stated by **(20)**.

The response of the DC-link voltage unbalance regulation is shown in **Fig. 2.44** for the DHPWM with $D = 0.5$. Initially, the voltage of the two DC-link capacitors are different (10% of unbalance); then, the neutral-point is balanced in about 50 ms, confirming the effectiveness of the control loop.

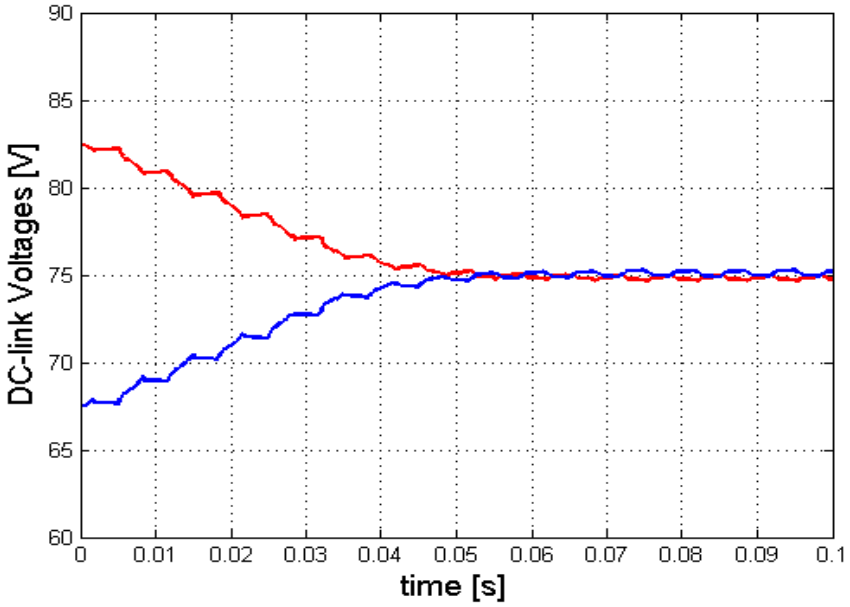


Fig. 2.44: Response of the DC-link voltage unbalance regulation loop (DHPWM, $D = 0.5$, 10% initial unbalance).

The control dynamics of the DC-link voltage can be further improved by an additional regulation loop controlling parameter θ (i.e. the width of the clamping zone) introduced in the previous section. This control loop will not be used and analyzed here as it will be discussed in the next sections.

Line voltage and current of one phase is shown in **Fig. 2.45** in the case of DHPWM (D = 0.5).Comparison of total harmonic distortion (THD) of the line voltage calculated up to the 48th harmonic shows that DHPWM provides a 3% higher value with respect to SPWM. Also the phase current ripple increases.

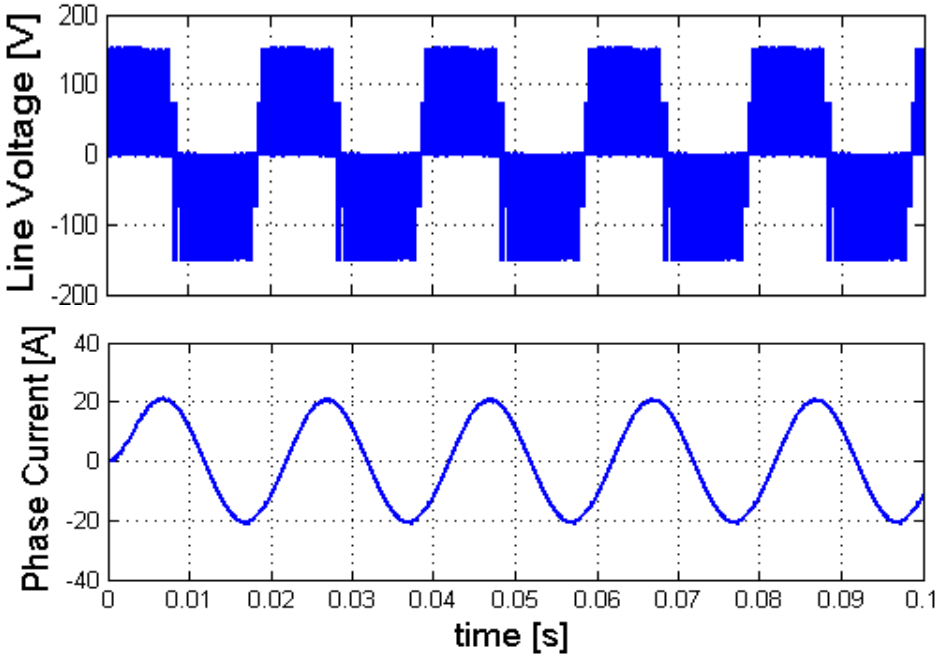


Fig. 2.45: Line voltage (top) and phase current (bottom) for the DHPWM (D = 0.5).

Finally DHPWM with three different values of parameter D (i.e. D = 1.0, D = 0.5, D = 0.0) and HPWM (D = 0.0 and D = 1.0) are compared in **Fig. 2.46** in terms of neutral-point voltage, neutral point current and load phase current.

One can notice that the neutral point current provided by DHPWM with D = 0.5 is even lower than the pure HPWM with D = 1.0 (i.e. DSPWM). Therefore a reduction of the ESR losses in the dc-link capacitors is expected. Also the voltage ripple is comparable but the converter losses are lower, as it will be discussed after.

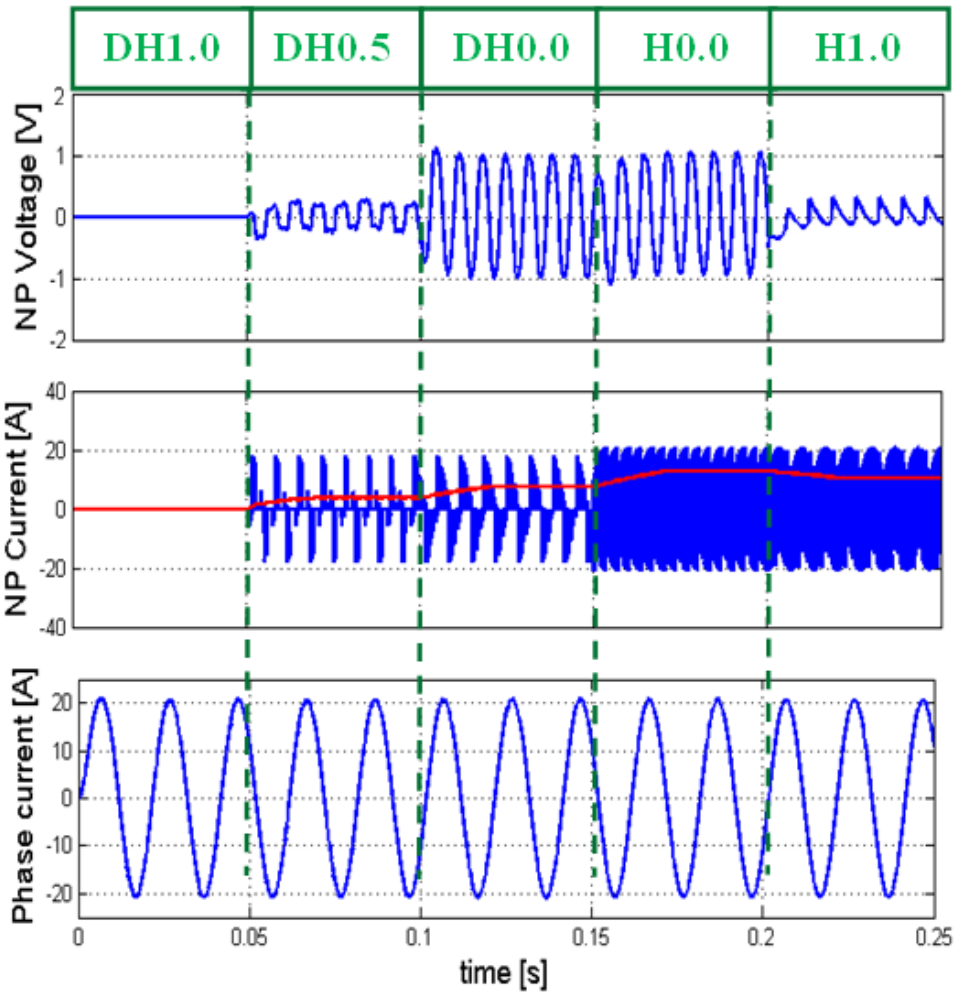


Fig. 2.46: Comparison between DHPWM and HPWM techniques in terms of NP voltage, NP current (RMS value in red line) and phase current.

Total power loss are typically divided into two main categories, namely switching and conduction losses. It can be demonstrated that switching losses represent the most important issue when comparing different modulation techniques.

A first comparison of the proposed modulation strategy with respect to other carrier-based modulations is done in terms of number of commutations averaged within a fundamental period (i.e. the average switching frequency). The results are shown in **Fig. 2.47a**, where normalization with respect to SPWM is adopted in order to highlight the difference in case of HWPM and DHPWM. The average switching frequency of HPWM is clearly linear with D, whilst it is constant in the case of DHPWM, but higher than HPWM. However switching is done at lower value of the load current if the correct value of the clamping zone midpoint is chosen as a function of the load power factor.

Reduction of the switching losses as compared to HPWM is therefore possible and is independent from parameter D, as shown in the results of **Fig. 2.47b**. Adoption of DHPWM

with D = 0.5 provides about 12%savings in the switching losses as compared to HPWM with the same value of D. Also conduction losses are reduced (i.e. about 6%), as they slightly depend on the type of adopted modulation, as shown in **Fig. 2.47**c.

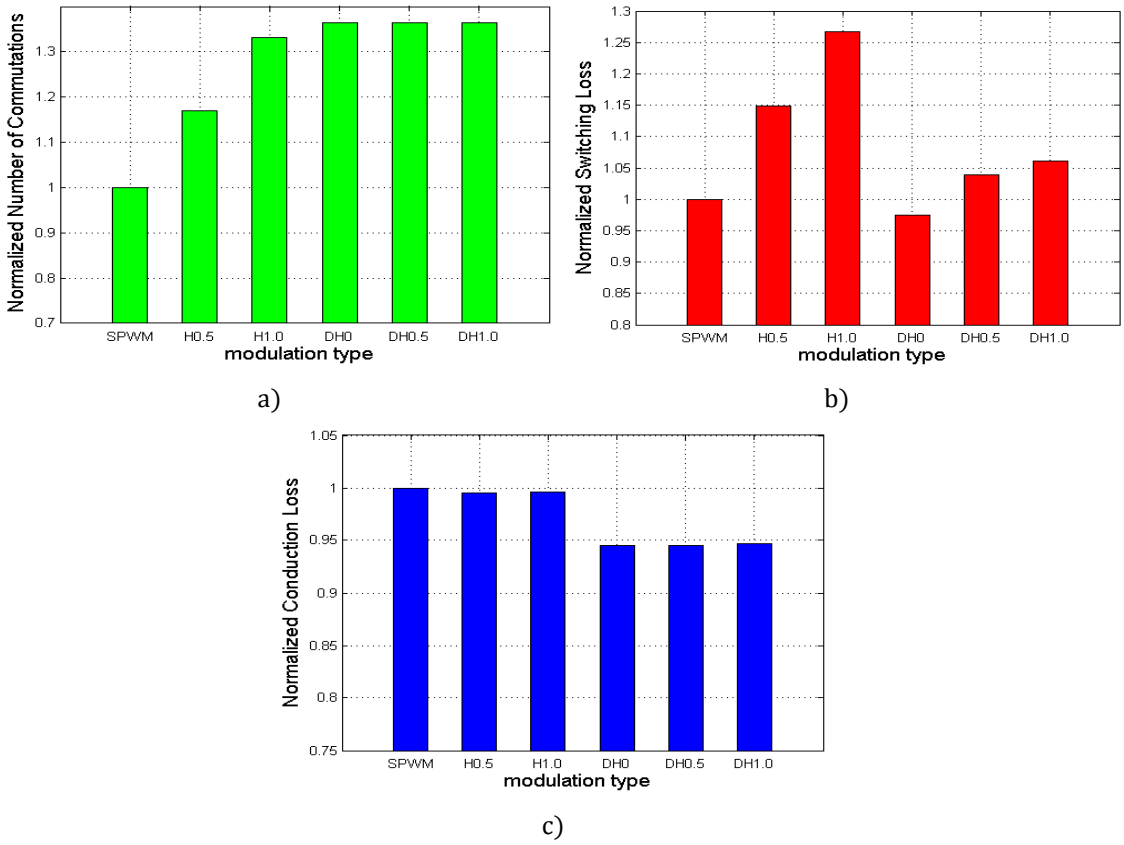


Fig. 2.47: Normalized a) number of commutations, b) switching and c) conduction losses during a fundamental period for SPWM, HWPM and DHPWM (with different values of parameter D).

Experimental results

A prototype test bench has been assembled in order to test the discussed modulation strategy and validate the theoretical and simulation analysis. The test-bench is composed of two external rotor permanent magnet synchronous machines with the same speed/torque/power rating and connected to the same shaft have been adopted. The first one acts as an integrated-starter alternator and is fed by a prototype three-phase three-level NPC inverter (described in detail in section 0). The second one is intended to emulate an internal combustion engine (or a constant load torque, in the proposed experiments), in order to simulate a hybrid traction system, and is driven by a standard drive. A digital power analyzer has been adopted for input and output power measurements on the NPC inverter.

Modulation strategies are implemented in the same control firmware and can be switched from one to the other by simply changing the set of main parameters discussed in the previous sections (i.e. D, θ, γ, and discontinuous modulation enable switch).

A first experiment refers to the generation of a three-phase voltage space vector in open loop, driving an induction motor an aiming at verifying the correct generation of the modulating signals. The results of this test are shown in **Fig. 2.48**, where positive and negative modulating signals v_{ap_dh} and v_{an_dh} (see also **Fig. 2.37**) are shown together with motor phase current A.

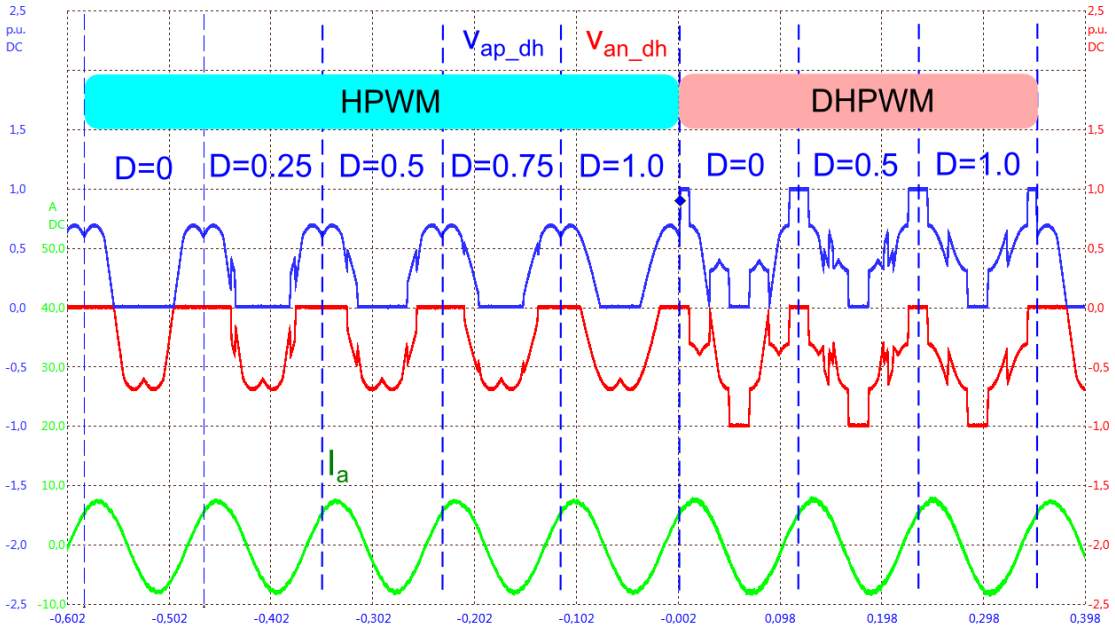


Fig. 2.48: Modulating signals and motor phase current (sequence of modulation strategies).

A sequence of modulation strategies is consecutively generated, one for each fundamental period of the voltage space vector, i.e. HPWM with increasing value of D from 0 up to 1.0 in 0.25 steps and DHPWM with increasing value of D from 0 up to 1.0 in 0.5 steps. One can notice that modulating signals have no overlapping regions only when HPWM with $D = 0$ is adopted, i.e. standard SPWM. Also clamping intervals in case of discontinuous PWM are clearly visible.

Fig. 2.49 is similar to **Fig. 2.48** but injected current into neutral point is measured (instead of motor phase current) together with the AC value of the negative DC-link, both low-pass filtered in order to remove any measurement disturbance. As it is clearly visible the considered modulation techniques exhibit different behavior, as previously discussed and also as shown in **Fig. 2.46**. Last period (i.e. DHPWM with $D = 1.0$) is the standard discontinuous two-level modulation, where no neutral point clamping is obviously present.

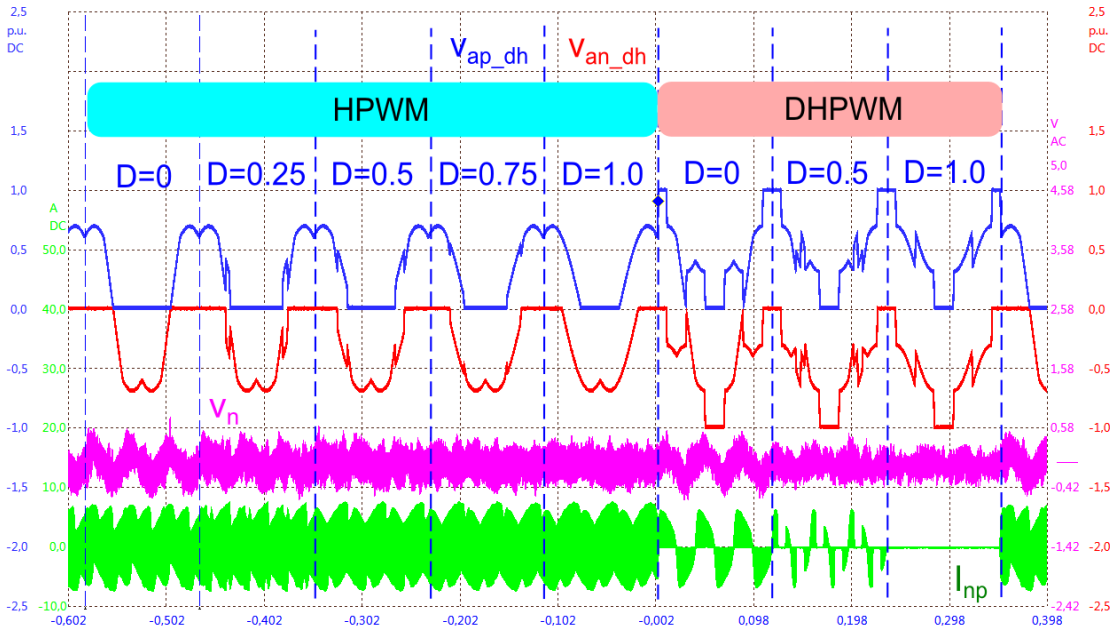


Fig. 2.49: Modulating signals, negative DC-link voltage and neutral point current(sequence of modulation strategies).

A set of efficiency measurements in different speed and torque operating conditions has been carried out on the experimental test bench shown in **Fig. 2.48**, in order to compare the discussed modulation strategies and to quantify the achievable gain with discontinuous hybrid modulation.

The motor driven by the NPC inverter is speed controlled whilst the brake machine is current (torque) controlled. Key results are shown in **Fig. 2.50**. Low speed and low torque operations allow an efficiency gain of more than 3%. This value is reduced as the speed or the load torque (or both) increase, but is however in the range of 1 to 2%. The explanation of the obtained results can only partially found in the decrease of the switching and conduction losses that, in the considered power conditions, is indeed quite small. Actually the most part of losses in those operating conditions is due to the injected current into the neutral point and the associated losses in the DC-link capacitors, that is mostly reduced with DHPWM, as already shown in **Fig. 2.49**. Further investigations and tests should be done in order to obtain a full characterization of the efficiency in the whole operating range and quantify the different components of losses.

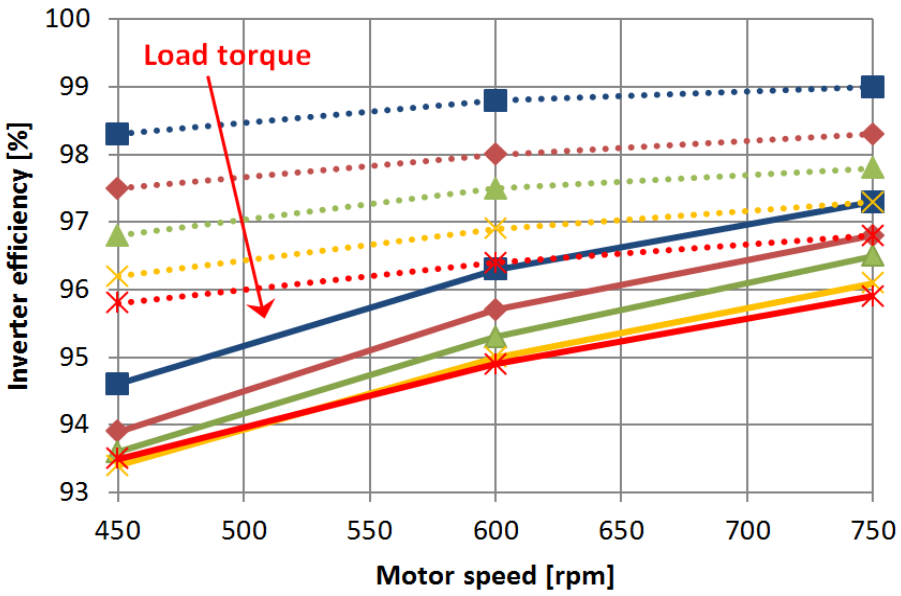


Fig. 2.50: Efficiency map for different operating speeds and load torque (HPWM with $D = 0.5$, solid lines; DHPWM with $D = 0.5$, dotted lines).

Last test is intended to show that a negligible increase in the total harmonic distortion of the motor phase current is introduced by discontinuous (hybrid) modulation. The same closed loop speed control is considered and the modulation strategy is changed every two periods of the phase voltage/current. The results are shown in **Fig. 2.51**. A debugging signal is shown to identify the zone where each modulation is adopted. Also the AC value of the negative DC-link is reported. A qualitative analysis of the results shows that the influence of the modulation strategy on the total harmonic distortion of the phase current is negligible. For the sake of completeness, a steady-state test has been performed for each modulation in the same operating conditions and the THD has been measured by a high performance power analyzer, confirming that the increase is limited to few fractions of percentage.

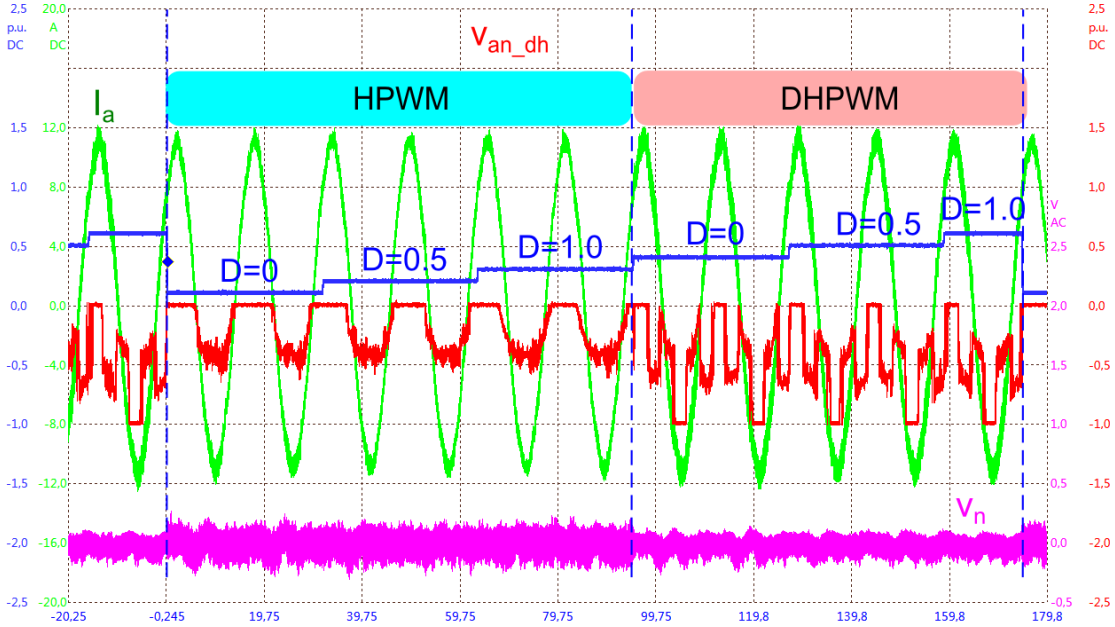


Fig. 2.51: . Motor phase current during closed-loop speed control and with a sequence of modulation.

Dual active NP voltage controller

A novel dual active NP controller, based on both common mode injection and clamping zone width modification, is introduced in this section in order to improve the dynamics of the neutral point voltage control. Simulation are presented to confirm the effectiveness of the proposal.

The locally averaged neutral point current with DHPWM is reduced, thus providing a correspondent reduction of low-frequency variations of the NP voltage. This operating conditions is referred to as AC compensation.

This does not imply DC balance between capacitor voltages. In fact, this modulation strategy would tend to preserve any initial voltage unbalance of the DC-link capacitors. Some compensation loop is therefore needed. The controller considered hereafter has two degrees of freedom in the NP control. In fact, NP regulation can be achieved by injecting a proper common mode voltage on modulating signals out of hybrid block and/or by adjusting the width of the positive and negative clamping zones. The two control loops can be used one at a time or simultaneously. When the two regulators operate together, the dynamic response of the control loop can be improved, as it will be demonstrated in the tests. Hereafter, a brief description of both control loops will be proposed.

In the *common mode injection* method, a PI regulator controls the voltage difference between the two capacitors (i.e. ΔV_c) by generating a proper gain k that is multiplied to the modulating signals, (19). In steady-state conditions, k is equal to 0.5, leading to $v'_{ip} = v_{ip}$ and $v'_{in} = v_{in}$.

Since the reference signals for the PWM are the function of the factor k, the average neutral-point current will also be a function of the factor k.

From [46], an expression for the neutral-point current is derived as:

$$\langle \boldsymbol{i_{np}} \rangle_{T_{sw}} = \frac{\mathbf{1} - \mathbf{2}\boldsymbol{k}}{\boldsymbol{V_{dc}}} \langle \boldsymbol{P} \rangle_{T_{sw}} \tag{43}$$

being P the inverter output power. If k = 0.5 the average neutral-point current will be zero. Since the NP voltage deviation depends on the NP current, a model for the NP voltage dynamics can be obtained depending on the factor k. The dc-link capacitor voltage variation is a continuous function of the inverter output power, the factor k, and the dc-link voltage, but it is a nonlinear function. A linear model describing the behavior of NP voltage dynamics for small AC perturbations about a DC working point can be calculated.

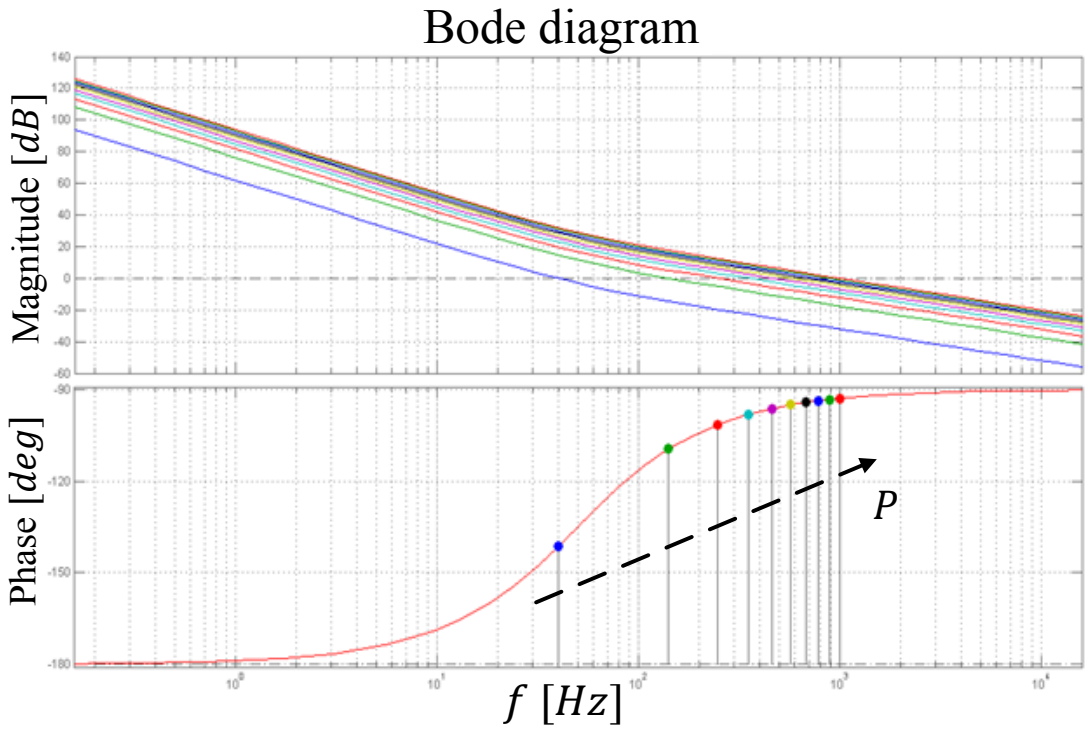


Fig. 2.52: Bode diagrams of NP control loop at different power levels.

The model can then be treated as a linear system, and linear control theories can be applied, e.g. a standard PI regulator can be adopted. The open-loop transfer function of the neutral-point voltage control system also depends on the inverter output power. An adaptation mechanism has therefore to be introduced to guarantee a proper response in the whole power range. The Bode diagrams of the open-loop transfer function are reported in **Fig. 2.52** to highlight the dependence on the inverter output power.

Another possibility to control the NP is by *adjusting the clamping section width*. The width of the positive and negative discontinuous sections can be adjusted in inverse proportion to each other according to the variable θ. If the positive clamped zone is enlarged, as shown in **Fig. 2.53a**, its switching state has a longer section maintained in the P state, which results in an increase in the P-type small vector [37].

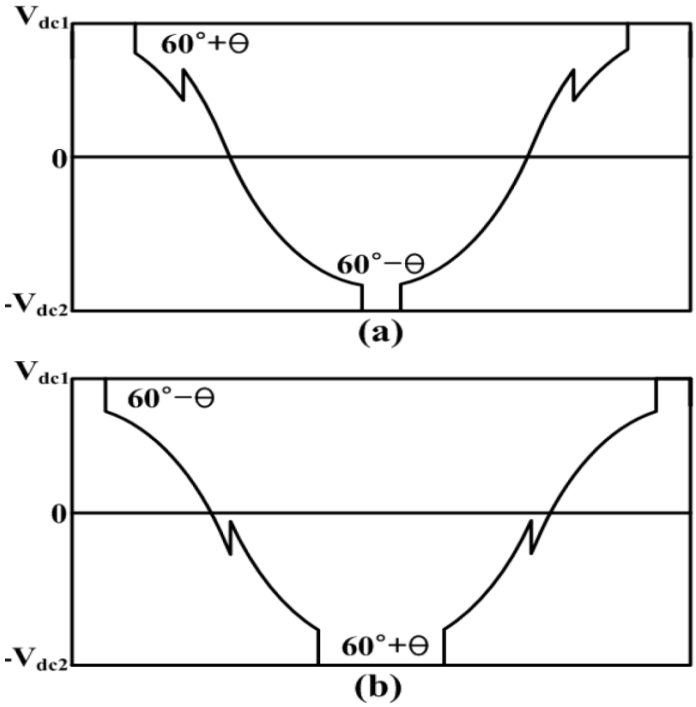


Fig. 2.53: Regulation of the clamping zone width by means of θ.

Moreover, the negative discontinuous section is shortened because it is in inverse proportion to the positive-clamped section, and the switching state of the clamped phase has a shorter section maintained in the N state, which leads to a decrease in the N-type small vector. Likewise, when the negative clamped section is lengthened, the N-type small vector decreases and the P-type small vector increases by a corresponding amount, **Fig. 2.53b**.

Fig. 2.54 indicates that θcan be adopted as the output of a simple PI controller monitoring the NP voltage unbalance.

The response of the DC-link voltage unbalance regulation is shown in Fig.4 (right) for the DHPWM with $D = 0.5$. Initially, the voltage of the two DC-link capacitors are different (10% of unbalance).Then, the NP is driven to a balanced condition by the regulation loops confirming the ability of the controllers. As highlighted in **Fig. 2.55** the control dynamics of the DC-link voltage is improved when using the additional regulation loop controlling parameter θ (solid line), with respect to the utilization of only the common mode regulator (dotted line).

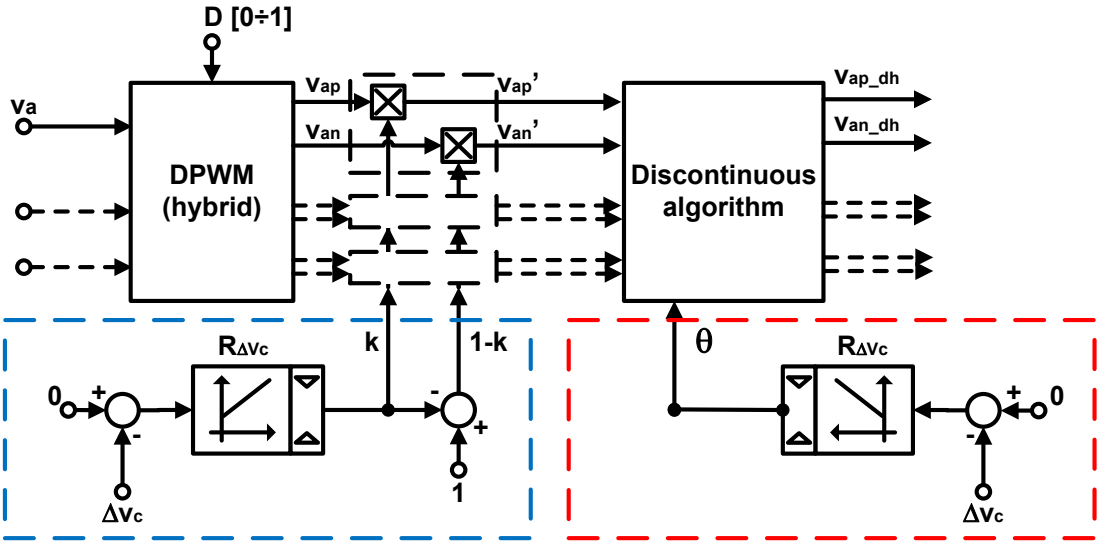


Fig. 2.54: Dual active NP control scheme

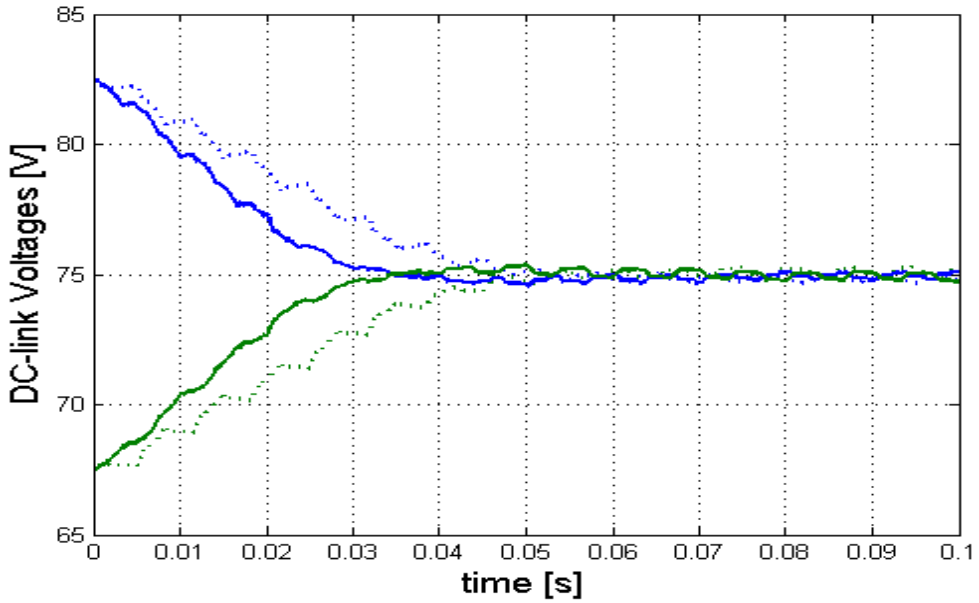


Fig. 2.55: Response of the DC-link voltage regulation loop (only common mode injection, dotted line, and with dual control, solid line).

2.6.2 Interleaved modulation

Hybrid modulation approaches belong to the double signal modulation class and are based on clamping modulation signals for some time during the non-common intervals. As the modulation signals are clamped to zero for an additional time, this leads to the switching frequency of the power switches being reduced, i.e. their switching losses also decrease. The exact combination is chosen by a sharing variable D, which can take values within the interval [0,1].

In **[41]**, a strategy that mitigates the drawbacks of the nearest three virtual vectors (NTV2, **[40]**) is described. The strategy can be classified as hybrid as the modulation period is shared between standard NTV and NTV2 Its formulation is based on a weighted total-harmonic-distortion (WTHD) minimization process, which should be performed offline for nonlinear or unbalanced loads. For the case of linear and balanced loads, the results of the minimization process can be approximated by analytical equations. An online estimator of the load power angle, as well as a detector of the linear and balanced nature of the load is considered in **[42]**, in order to perform the THD minimization.

In **[43]**, a hybrid space vector modulation is obtained by mixing symmetric nearest three vectors (NTV1) and nearest three virtual vectors. A trade-off between the two modulations is obtained, with the ratio of time spent in NTV1 or NTV2 modes adjusted on-line as a function of the modulation index, electrical angle, and power factor.

In [44], a simple way of creating hybrid strategies, as combination of space vector modulation, is presented in order to mitigate NP voltage oscillations.

In [50], a tracking method was proposed to achieve the maximum reduction of the voltage oscillation amplitudes by varying the combination of two strategies. This approach results very similar to the one proposed by the author but less general and without an experimental implementation of the algorithm.

In this section, a novel modulation technique based on the combination of the standard SPWM and DSPWM is proposed, obtaining a mitigation of both losses and low frequency NP voltage ripple. Comparison with hybrid PWM approach is reported, as far as losses and oscillation of NP voltage analysis.

Interleaving concept

The interleaved modulation approach, here referred as IntPWM, was proposed in [45] to mitigate the problem of low frequency NP voltage oscillations. IntPWM is based on a proper interleaving of both sinusoidal and double signal PWMs. The basic concept is to employ both modulation strategies during a period of the fundamental voltage and changed one to the other with a frequency six times the fundamental one ($f_{int} = 1/T_{int} = 6f_m$), as shown in **Fig. 2.56.**

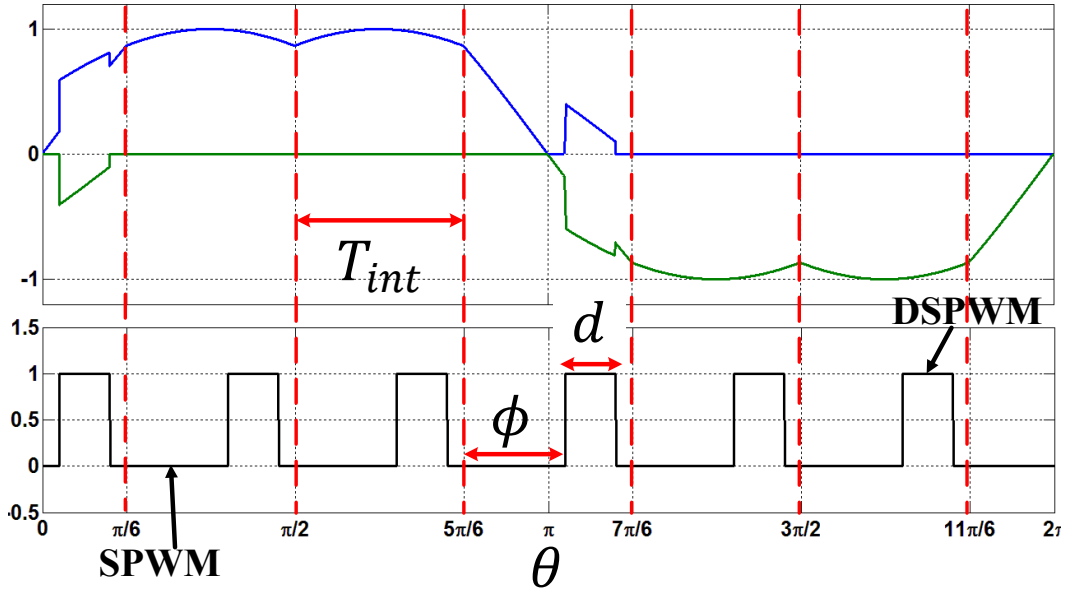


Fig. 2.56: Modulation signals for IntPWM with $d = 0,3$ and $d = 0,6$ and selection signal.

The key idea comes from the analysis of the shape of NP current for SPWM averaged within the switching period and already shown in Fig. 2.10. One can notice that the peaks repeat six times within the fundamental period. This means that, if in correspondence of that peaks the modulation is changed to DSPWM for some time, it is possible to reduce the overall amplitude of that current by a certain amount. The result is a trade-off between the two well-known carrier-based techniques, i.e. the beneficial effects of DSPWM in reducing the low frequency content of the NP voltage and the reduction of switching losses achievable with sinusoidal PWM.

The modulation selection command between the two modulation techniques can be therefore represented by a binary signal at frequency f_{int}, as already shown in **Fig. 2.56**. When the signal is 1, the DSPWM is adopted, otherwise SPWM is used. Additional parameters can be introduced to raise the degrees of freedom in the interleaving process:

the phase delay angle ϕ of the $0 \rightarrow 1$ transition of the selection signal with respect to a synchronization signal (dashed red lines in **Fig. 2.56**), here delayed $\frac{\pi}{6}$ with the positive-slope zero-crossing of the output voltage, but zero delayed in [Apec2014];

the duty-cycle d, assuming values in the interval $[0,1]$, which determines the utilization ratio of the two modulation techniques.

For the sake of simplicity the phase angle is also expressed as a ratio, therefore also assuming values in the interval $[0,1]$.

The choice of the interleaving parameters ϕ and d is quite complex and can be done on-line in order to minimize the low-frequency content of the NP voltage as well as losses and

harmonics content. Some hints will be discussed in the next section, where the simulation analysis of the proposed method will be reported.

Relationship with hybrid modulation

After an accurate analysis, it is possible to conclude that the proposed interleaved modulation is a generalization of the HPWM approach in [15]. Furthermore, the IntPWM modulating signals are identical to those of HPWM with a certain value D, when the following conditions are met:

$$\boldsymbol{d = D} \quad , \quad \boldsymbol{\phi_D = \frac{1 - D}{2}} \tag{44}$$

The interleaving modulation introduces one more degree of freedom compared to the hybrid modulation, when only the parameter D can be modified.

The relationship between IntPWM and HPWM is clearly highlighted in **Fig. 2.57**, where the duty-cycle d takes values $0{,}3 - 0{,}5 - 0{,}7$ and the phase delay is chosen to meet condition **(136)**.

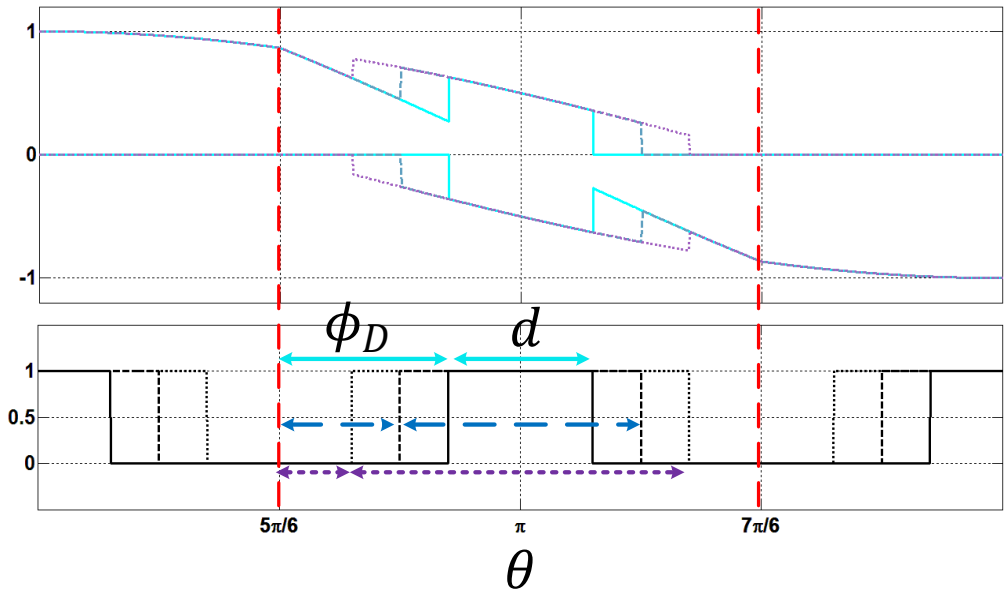


Fig. 2.57: HPWM as a particular case of IntPWM for $\mathbf{d = 0,3 - 0,5 - 0,7}$ and $\boldsymbol{\phi = \phi_D}$.

Adaptive interleaved modulation

The choice of the interleaving parameters ϕ and d can be done to exploit the additional degree of freedom, introduced by IntPWM, in order to minimize the low-frequency content of the NP voltage as well as losses and harmonics content.

If for example the value of the duty-cycle d is fixed at 0,5 (corresponding to the same value of D for HPWM), the behavior of the NP RMS current as a function of the other interleaved parameter, i.e. phase angle ϕ, at different loads α_{vi} is presented in Fig. 2.48. As it is clearly shown, for every load a minimum value of NP RMS current exists and is linkable with a ϕ_{min}. Furthermore, this minimum phase delay angle is equal to ϕ_D only when α_{vi} is equal to 0°, 90° and 180°. In all the other cases, employing the IntPWM with the ϕ_{min} leads to a reduction of NP injected current and consequently a lower low-frequency voltage ripple, compared to the HPWM with the same value of D.

Thus, in the interleaved modulation the value of ϕ can be adapted in function to the load to minimize the ripple on the neutral point, confirming the effectiveness of the proposal as shown in Fig. 2.59.

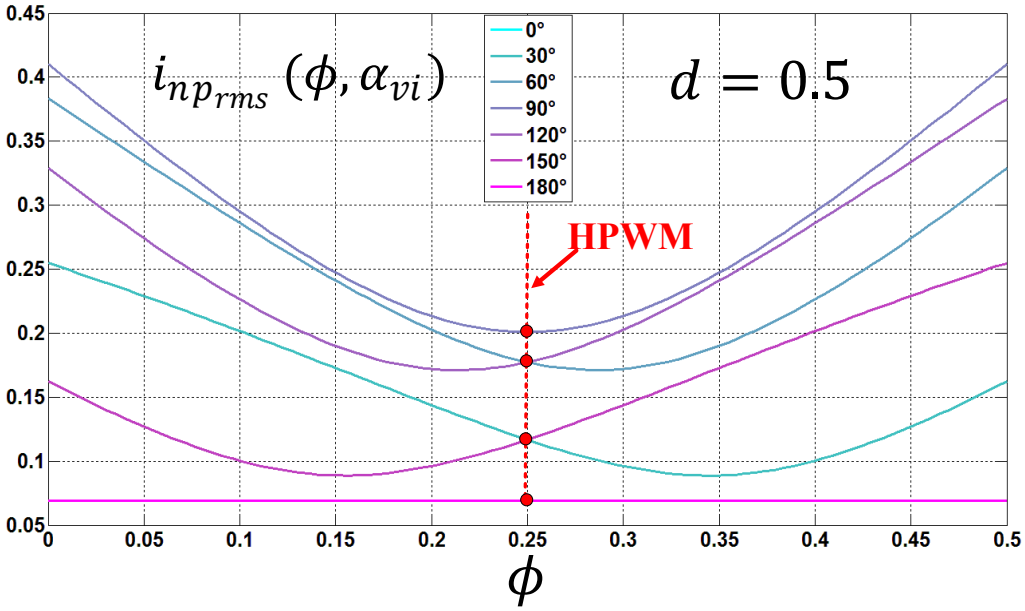


Fig. 2.58: RMS current for IntPWM as a function of ϕ with $d = 0,5$ at different values of α_{vi}.

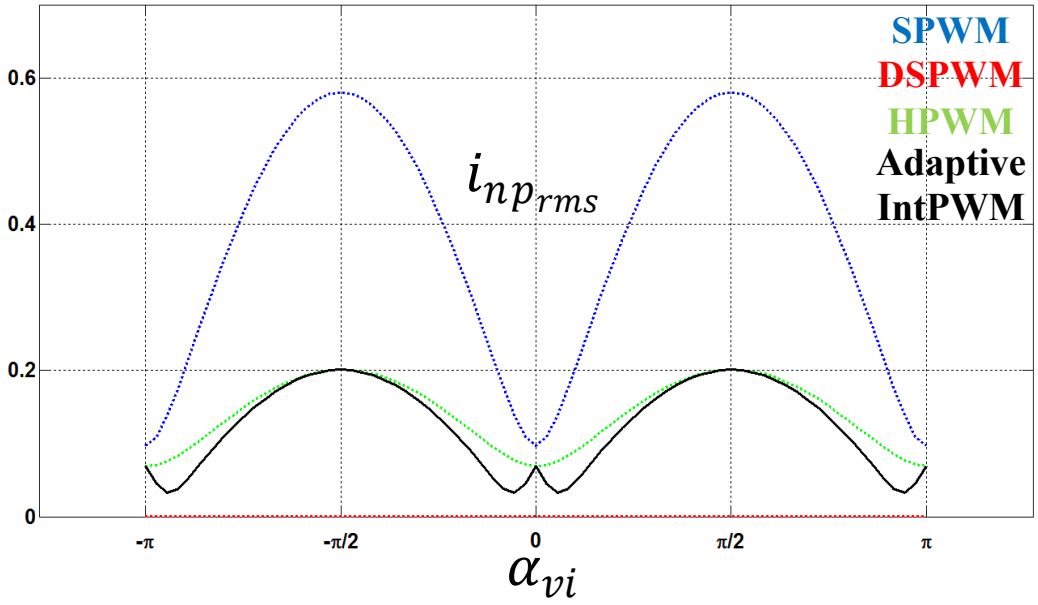


Fig. 2.59: NP current RMS value as a function of load phase angle α_{vi} for SPWM, DSPWM, HPWM and new Adaptive IntPWM.

Simulation results

A simulation model of an NPC 3-level three-phase converter driving a passive *RL* load has been implemented in the standalone PLECS tool, including conduction and switching loss models of the power devices. DSPWM as well as standard SPWM and new interleaved technique have been compared by taking into account neutral point voltage ripple , overall losses and harmonic content of the output voltage. Main parameters of the system are reported in Tab. 7.3. The same model has also been tested with a permanent magnet synchronous motor, as part of the experimental results are obtained with such a load. Extensive simulation and experimental investigations have been performed in order to highlight the specific features of each method and provide a quantitative comparison test bench.

First qualitative results are presented in **Fig. 2.60** aiming at illustrating the key idea of the interleaving modulation strategy. A sequence comprising DSPWM, SPWM and the interleaved technique with $\phi = 0.7$ and $d = 0.5$ is considered. Phase to phase output voltage, output current, modulating signals, NP voltage, averaged NP current (within a switching period) and the modulation selection signal are shown. A fundamental period, i.e. $20\ ms$ is assigned to each modulation technique.

One can notice that DSPWM provides roughly no variation of the NP voltage as the average value of the injected NP current is zero (see also Fig. 2.14). On the other hand SPWM provides a huge variation of the NP voltage due to the 3rd harmonic low-frequency oscillation of the NP current (see also Fig. 2.10).

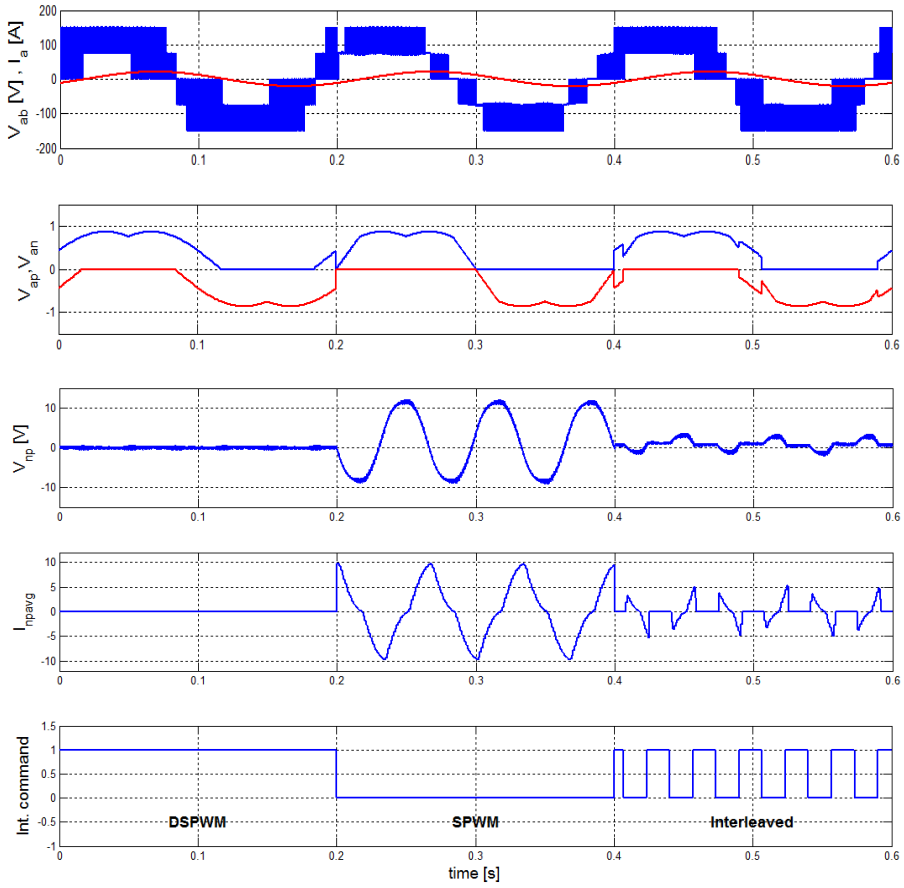


Fig. 2.60: DSPWM, SPWM and interleaved technique ($d = 0.5$,$\phi = 0.7$) sequence: (from top) phase-to-phase voltage and line current, modulating signals, NP voltage, NP current, modulation selection signal.

As previously mentioned, the effect of the interleaving parameters ϕ and d on the performance of the modulation strategy, i.e. NP voltage oscillation, harmonics distortion and losses, is hard to calculate in closed form. That is the reason why a simulation analysis has been performed in order to provide a complete map of those performance indexes as a function of the interleaving parameters.

NP Low-Frequency Oscillations

A series of simulations have been performed in order to identify the trend of the NP voltage peak-to-peak ripple as a function of the phase ϕ and with different values of the duty-cycle d when interleaved modulation is adopted. The resulting three-dimensional map is shown in **Fig. 2.61**. As it is clearly visible the ripple has its maximum values when the duty cycle of the interleaving is 0, i.e. SPWM is used for all the time. As soon as the interleaving duty cycle is reduced, the voltage ripple trend is not linear and becomes a function of the phase ϕ, i.e. a proper choice of this last parameter at constant duty cycle allows to minimize voltage ripple.

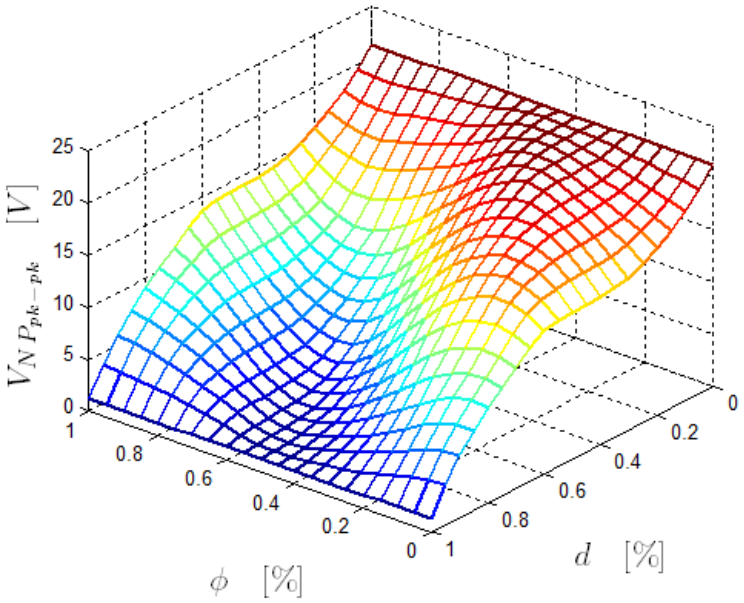


Fig. 2.61: NP voltage ripple map (interleaved modulation).

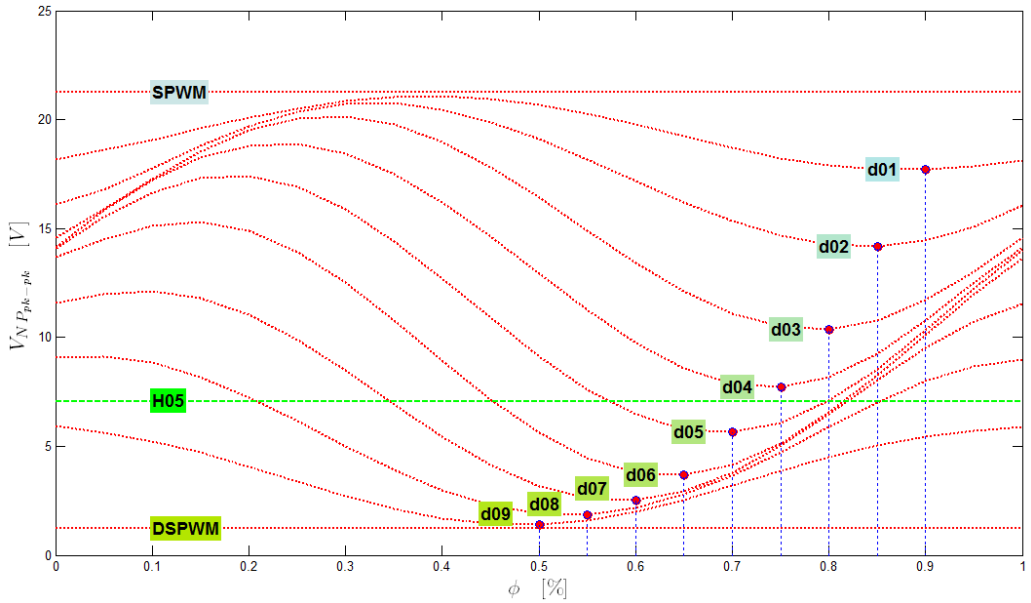


Fig. 2.62: NP voltage ripplecontour curves as a function of ϕ at different values of d for interleaved modulation (red lines) and hybrid modulation with $D = 0.5$ (green line).

The situation is further analyzed in **Fig. 2.62**, where the results of **Fig. 2.61** are drawn as two-dimensional contour curves, showing the NP voltage ripple for different values of duty cycle d and as a function of the interleaving phase ϕ. As it is clearly shown, for each value of the duty cycle, there exist a minimum for a certain value of the interleaving phase, that is identified by a red bullet. The absolute minimum value results obviously when $d = 1$, i.e. DSPWM (fast-processing) is adopted. For example, if $d = 0.5$, the minimum ripple is obtained for $\phi = 0.7$. A comparison with the HPWM could be useful to evaluate the performances of the proposed interleaved modulation. Green line in **Fig. 2.62** refers to the

voltage ripple value obtained for HPWM with hybridization factor $D = 0.5$. One can notice that its value is slightly higher than the minimum one achievable with interleaved modulation with $d = 0.5$.

Loss Analysis

The same approach has been adopted for the estimation of conduction and switching losses in the case of the proposed interleaved modulation.

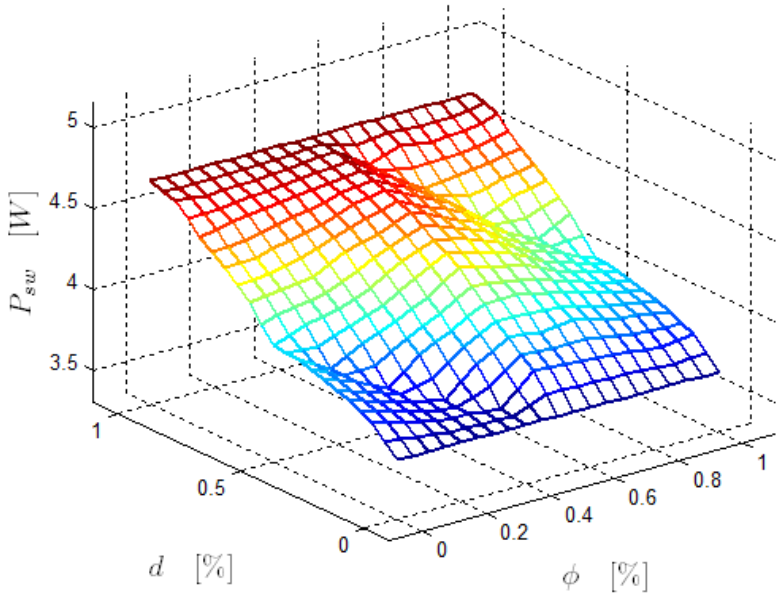


Fig. 2.63: Switching losses map (interleaved modulation).

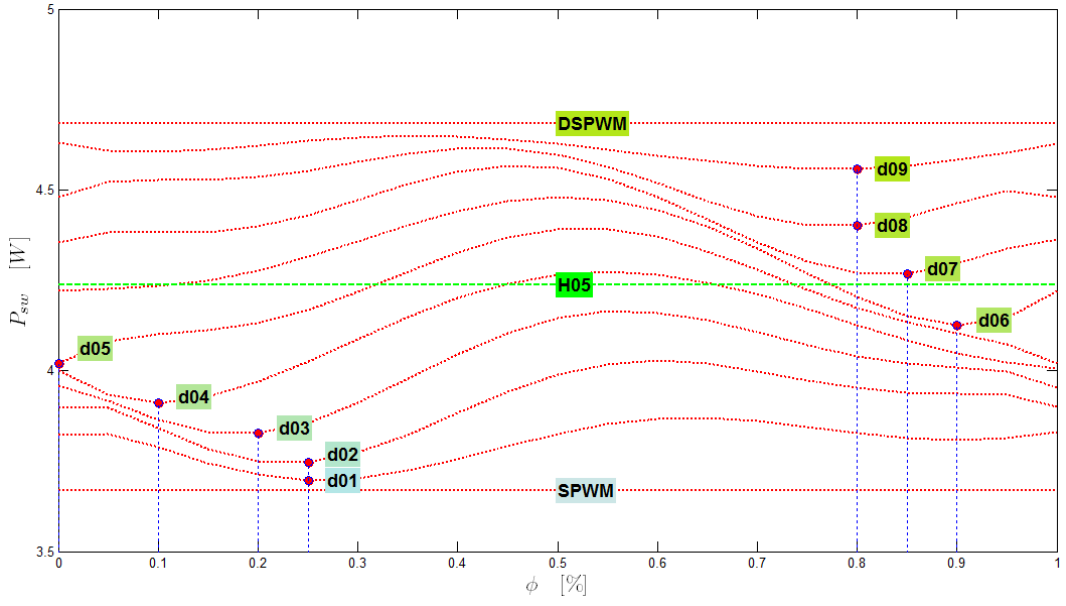


Fig. 2.64: Switching losses contour curves as a function of phase ϕ at different values of d for interleaved modulation(red lines) and for hybrid modulation with $D = 0.5$ (green line).

It will be demonstrated that switching losses represent the most important issue when comparing different modulation techniques.

The resulting three-dimensional map relating switching losses to the phase ϕ and the duty-cycle d is shown in **Fig. 2.63**. The maximum value of the switching losses is obtained when fast-processing algorithm is used, i.e. DSPWM with $d = 1$. Also in this case as soon as the interleaving duty cycle is reduced, switching losses trend is not linear and becomes a function of the phase ϕ, i.e. minimization approach can be adopted also in this case.

The situation is again further analyzed by drawing two-dimensional contour curves showing the switching losses for different values of duty cycle d and as a function of the interleaving phase ϕ, i.e. **Fig. 2.64**. It is still possible to find out a value of phase ϕ that minimizes switching losses for each value of the interleaving duty cycle.

Again the comparison with the HPWM could be useful to evaluate the performances of the proposed interleaved modulation. Green line in **Fig. 2.64** refers to the switching losses value obtained for HPWM with hybridization factor $D = 0.5$. One can notice that its value is slightly higher than the minimum one achievable with interleaved modulation with $d = 0.5$, i.e. a similar result is obtained as in the case of NP voltage ripple. This means that, in this particular situation, there exist an optimal choice of phase and duty cycle, both from NP voltage ripple and switching losses, confirming that the proposed modulation could provide the best tradeoff between ripple and losses with a proper choice of the interleaving parameters.

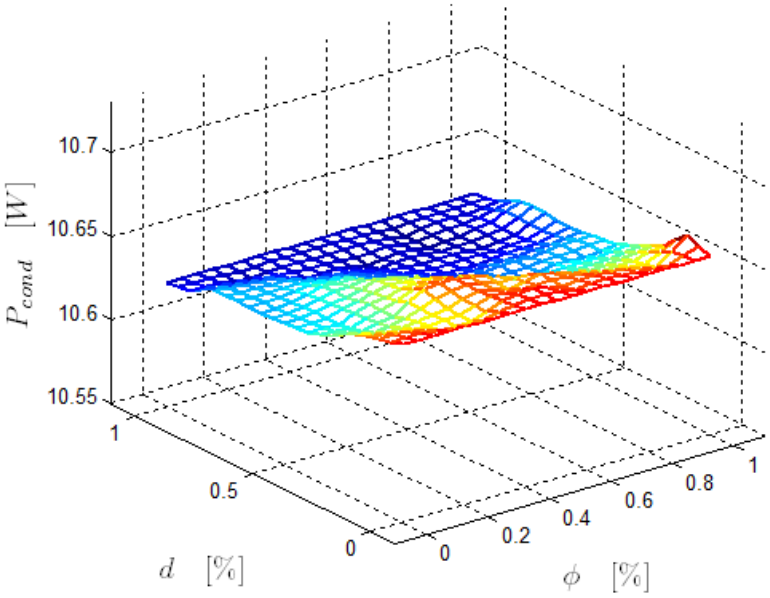


Fig. 2.65: Conduction losses map (interleaved modulation).

Finally the conduction losses are taken into account and the three-dimensional map reported in Fig. 2.65 is drawn in the same space of the interleaving parameters. The obtained surface

confirms that conduction losses are roughly constant as a function of interleaving parameters, as demonstrated by the almost flat surface in **Fig. 2.65**.

Output Voltage Harmonic Distortion

The trend of the total-harmonic-distortion of the line-to-line voltage as a function of the interleaving parameters is shown in **Fig. 2.66**. It is easy to understand that higher values of the THD are obtained by DSPWM modulation and, also in this case, there are some areas where the THD can be minimized by a proper choice of the phase ϕ and the duty-cycle d. The two-dimensional contour lines will not be taken into account in this case, but a similar behavior is expected.

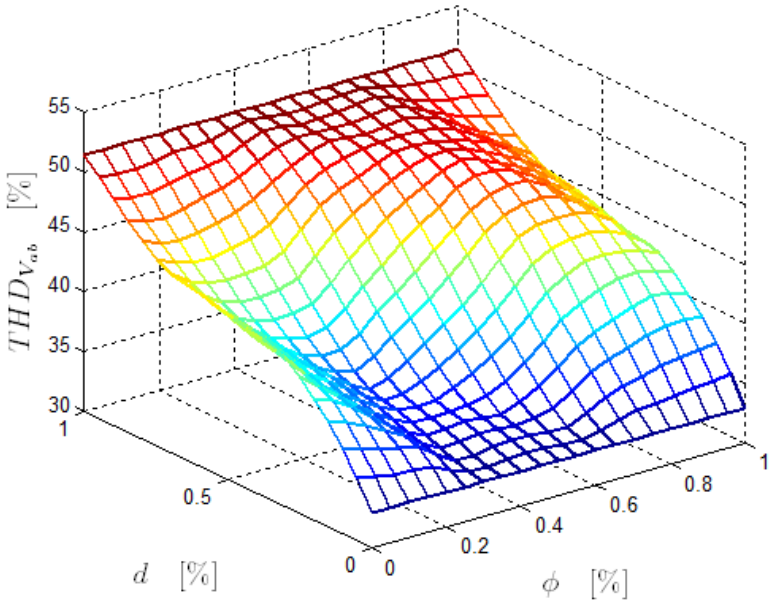


Fig. 2.66: Line to line voltage THD map (interleaved modulation).

Experimental results

The experimental test-bench used to verify the proposed modulation strategy is the same of the one discussed in section 2.6.1.

The proposed interleaved strategy requires the adaptation of the phase ϕ in order to minimize the injected current into the neutral point of the inverter. This in turn requires to synchronize the interleaving process with the output phase current in order to adopt DSPWM when its value is the maximum one. Also injection of the 6th harmonic variation of the adopted modulation strategy has to be performed, thus requiring the knowledge of he reference frequency. This information is normally not available to the PWM modulator as the reference voltage is provided by the current regulators in closed loop.

However, as the aim of our experimental tests is to provide a verification of the effectiveness of the proposed interleaving modulation, a simple induction motor drive operating in open

loop has been adopted here to simplify the implementation. Further investigations are being developed in order to improve the modulation algorithm and automatically adapt the phase ϕ for any operating condition.

Modulation strategies are implemented in the same control firmware and can be switched from one to the other by simply changing the set of main configuration parameters, i.e. hybridization factor D, the interleaving duty cycle d and phase angle ϕ.

The same sequence shown in the simulation test of **Fig. 2.60** has been implemented in the experimental firmware (with slightly different values if interleaving parameters).

In all the results presented hereafter the same interleaving duty cycle $d = 0{,}5$ has been considered. The optimal choice of phase angle $\phi = 0{,}25$ is used in the results reported in **Fig. 2.67**.

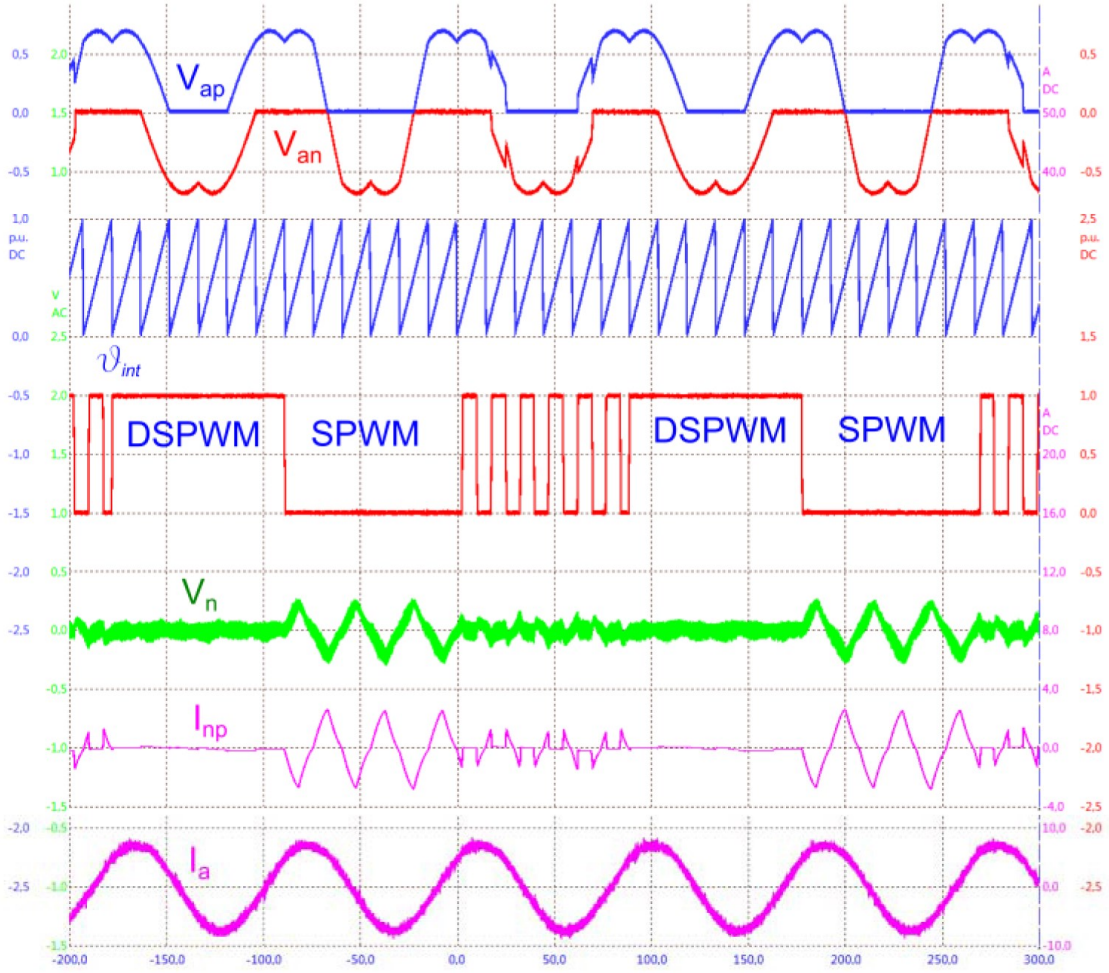


Fig. 2.67: Results of the interleaving process with duty cycle $d = 0,5$ and optimal $\phi = 0,25$.

The figure shows (from top): positive and negative modulating signals v_{ap} and v_{an}, 6th harmonic θ_{int} of the voltage reference space vector angle, selection signal between DSPWM and SPWM modulations, negative dc-link voltage (only the AC component), injected current

into the neutral point (1 kHz low-pass filtered) and motor phase current. One can notice that the results are completely matching those in **Fig. 2.60** and confirm the effectiveness of the proposed interleaved modulation. In fact, the adoption of the SPWM results in a very high 3th harmonic in the NP voltage and current. This value is strongly reduced with the interleaving and is completely zeroed by DSPWM. The resulting phase current is actually not noticeably affected by the adopted modulation strategy.

The same experiments have been repeated in the same conditions but with different values of the phase angle \phi and the results are presented in **Fig. 2.68**.

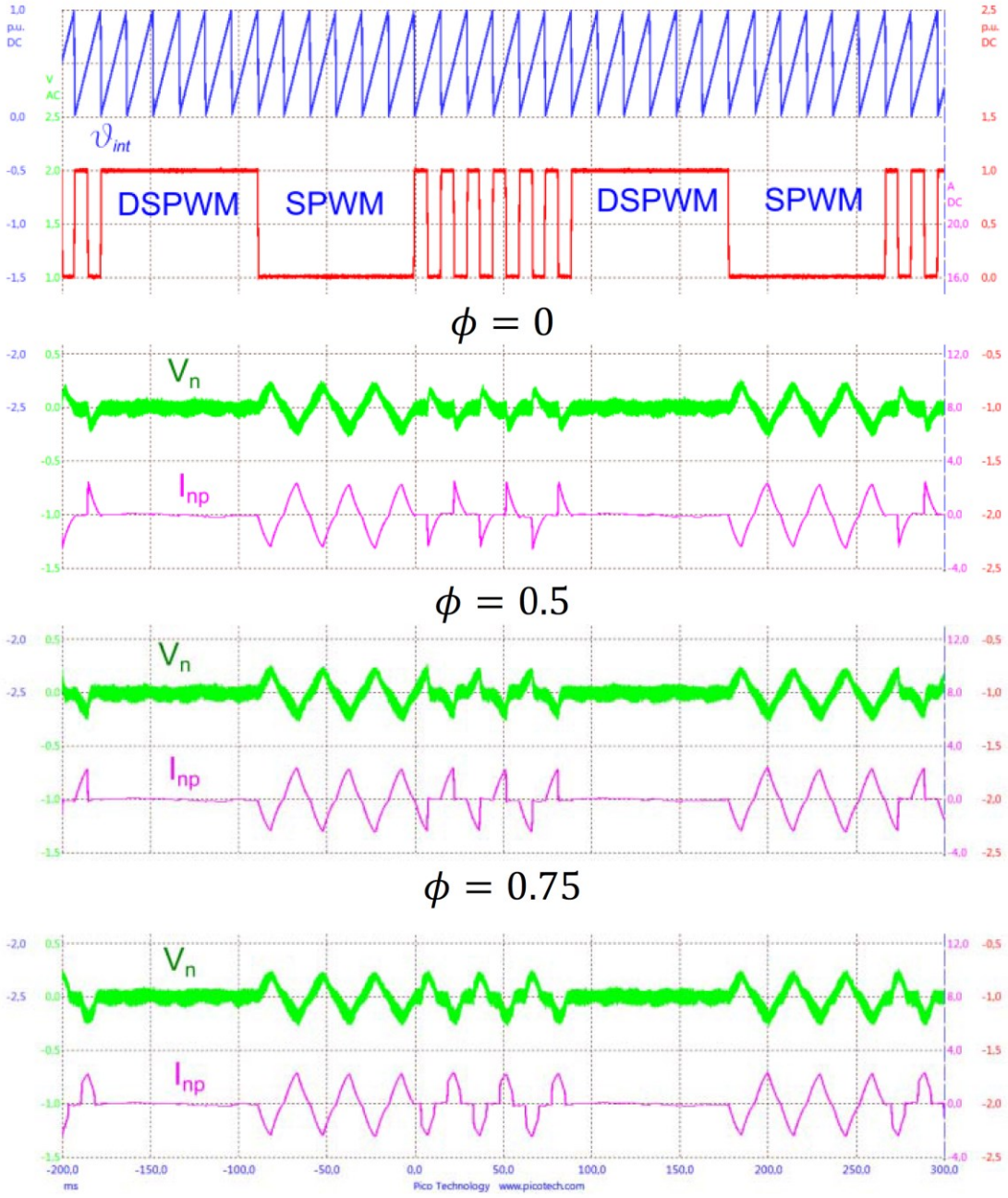


Fig. 2.68: Results of the interleaving process with duty cycle $d = 0,5$ and non-optimal $\phi = 0 - 0,5 - 0,75$.

Finally, the results with HPWM with $D = 0{,}5$ are shown in **Fig. 2.69**, demonstrating (slightly) worst performance with respect to the optimal case for the interleaving modulation.

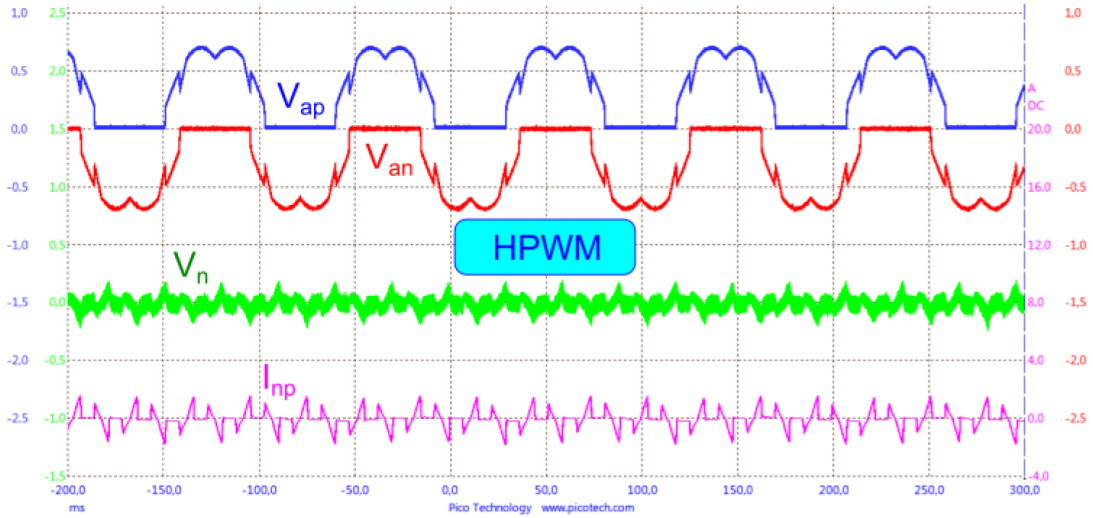


Fig. 2.69: Results of the hybrid modulation with $D = 0,5$.

2.7 Dead-time accurate model and compensation

2.7.1 Introduction

Inverter output voltage distortion with respect to the reference given to the modulation algorithm, since the presence of some non-ideal features. In particular, the necessary interlock time usually represents the most important cause of distortion. Accurate compensation of inverter distortion is important in applications like precision servo drives and in scalar control of induction motors, but is essential in sensorless control (especially at low-speed), where PWM reference is used as a measurement of the output voltage.

The availability of a model for the dependence of distortion voltage with current allows its estimation and, thus, compensation. Model parameters need to be identified (usually together with phase resistance), and self-commissioning is preferable. Many techniques have been proposed, based on linear models ([52]), off-line measurements and non-linear function fitting ([51]) or look-up tables ([53]),and adaptive algorithms ([54]).

The physical model behind the proposed compensation technique, which takes into account also the parasitic capacitance, has been proposed in [55]. In the present section a similar model has been derived from a more accurate one, allowing to evaluate the simplification hypotheses. For dead-time parameters and resistance identification a first option consists in the approximation of the distortion curve at high-current as a straight line. This simple technique, however, can result in significant errors (especially with current rating mismatch between inverter and motor or in the case of long motor cables), and a relatively large part of the data collected during self-commissioning had to be discarded. A second proposal overcomes these drawbacks by applying a more accurate approach, based on Multiple Linear Regression (MLR), which results in important improvements in the identification accuracy. The cost in terms of computation and memory is maintained low, so that the novel technique retains the important characteristic of being implementable on the drive controller.

Both techniques can be implemented on an actual drive, and the influence of compensation in different cases (e.g. PMSM sensorless control and induction motor V/f) will be analyzed in simulation and experimentally, comparing different techniques.

2.7.2 Accurate modelling of inverter distortion

The inverter output voltage characteristics is a function of the non-ideal behavior of the commutation phenomena, such as dead-time effect, commutation delays, voltage drops in power devices, equivalent parasitic resistance and inductance of the current paths, charging and discharging of the equivalent (parasitic or intrinsic) output capacitance of the leg. For

that reason the inverter instantaneous output voltage with respect to the DC bus reference level, i.e. V_{x0} in **Fig. 2.70**, will be considered in the following analysis. Averaging and extension to the phase voltage of the three-phase load will be considered as a consequence. The inductive behavior of the load allows to model the leg output current as a constant value during the switching period or, at least, during the dead-time intervals, as it will be explained shortly.

A first model will be considered which takes into account the recalled non-ideal conditions, but neglects the effects of the output capacitance. Later, those effects will be introduced and a complete model obtained. The simplified version of that model represents the base for the proposed compensation strategy, discussed in the next sections.

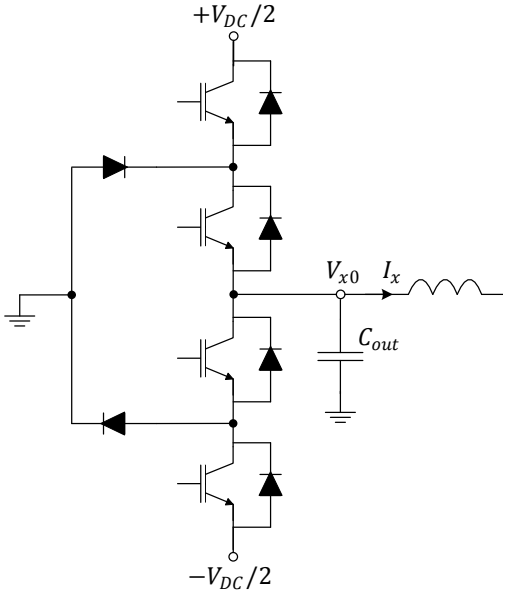


Fig. 2.70: NPC inverter leg representation.

Dead-time and voltage drops effects

The output voltage waveforms during dead time interval (T_{DT}) when considering voltage drops (V_{igbt} and V_d) and switching delays ($T_{delay,H\to L}$ and $T_{delay,L\to H}$) are sketched in **Fig. 2.71**. Two different cases has been introduced as a function of the sign of the output current, as its value affects the conduction state of the free-wheeling diodes and thus of the output voltage.

The voltage difference (increase or decrease) between ideal (dashed black lines) and actual switches (solid black lines) are highlighted by colored areas and identified by + and − signs, meaning that the corresponding contribution respectively increases or decreases the output voltage averaged over the switching period T_{SW}. This voltage will be referred to as "distortion voltage" in the following sections, i.e. the voltage contribution that produces the distortion of

the output voltage of the inverter. Symmetric commutation delays (if any) are considered with green areas, their average contribution being generally zero due to symmetry.

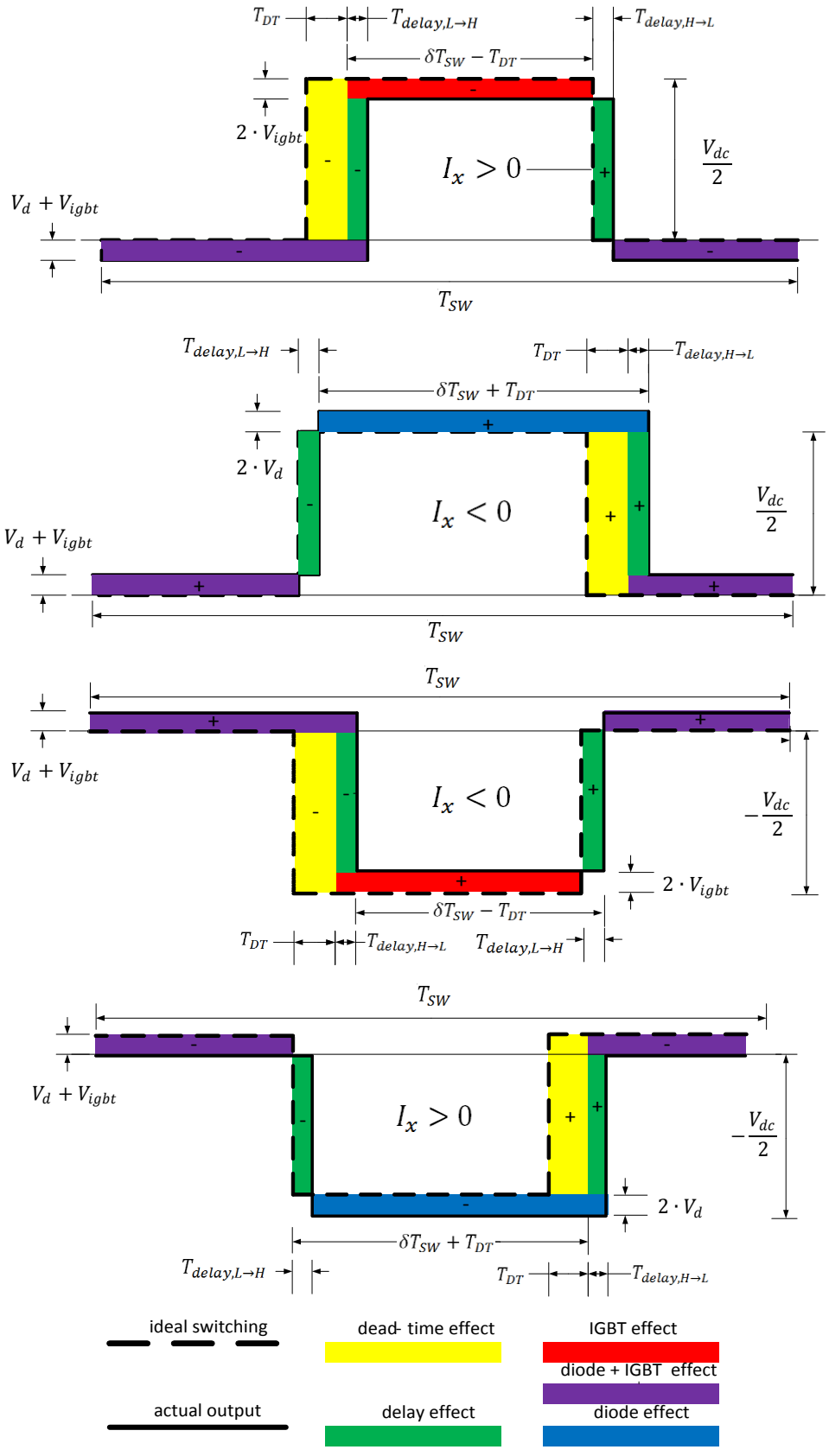


Fig. 2.71: Output voltage waveforms during dead time.

Asymmetric commutation delays can be considered as additional dead-time components and are therefore included in that value, represented with yellow areas. Finally IGBT and diode contributions are represented with red and blue areas.

The equivalent on-time of the output voltage can be therefore related to the commanded duty cycle δ_x and the dead-time, as shown in the same figure.

If the average value of the output voltage is considered within the switching period, the following equations are obtained as a function of the output current sign.

Transition $0 \rightarrow \frac{V_{dc}}{2} \rightarrow 0$:

$$\mathbf{I_x > 0}:\ \bar{V}_{x0} = \frac{1}{T_{SW}}\left\{\frac{V_{dc}}{2}\delta_x T_{SW} - \underbrace{\frac{V_{DC}}{2}T_{DT}} - \underbrace{(V_{igbt}+V_d)[(1-\delta_x)T_{SW}+T_{DT}]} - \underbrace{2V_{igbt}(\delta_x T_{SW}-T_{DT})}\right\} \tag{45}$$

$$\mathbf{I_x < 0}:\ \bar{V}_{x0} = \frac{1}{T_{SW}}\left\{\frac{V_{dc}}{2}\delta_x T_{SW} + \underbrace{\frac{V_{DC}}{2}T_{DT}} + \underbrace{(V_{igbt}+V_d)[(1-\delta_x)T_{SW}-T_{DT}]} + \underbrace{2V_d(\delta_x T_{SW}+T_{DT})}\right\} \tag{46}$$

Transition $0 \rightarrow -\frac{V_{dc}}{2} \rightarrow 0$:

$$\mathbf{I_x > 0}:\ \bar{V}_{x0} = \frac{1}{T_{SW}}\left\{\frac{V_{dc}}{2}\delta_x T_{SW} - \underbrace{\frac{V_{DC}}{2}T_{DT}} - \underbrace{(V_{igbt}+V_d)[(1-\delta_x)T_{SW}+T_{DT}]} - \underbrace{2V_{igbt}(\delta_x T_{SW}-T_{DT})}\right\} \tag{47}$$

$$\mathbf{I_x < 0}:\ \bar{V}_{x0} = \frac{1}{T_{SW}}\left\{\frac{V_{dc}}{2}\delta_x T_{SW} + \underbrace{\frac{V_{DC}}{2}T_{DT}} + \underbrace{(V_{igbt}+V_d)[(1-\delta_x)T_{SW}-T_{DT}]} + \underbrace{2V_d(\delta_x T_{SW}+T_{DT})}\right\} \tag{48}$$

Previous equations can be manipulated after the introduction of the following equation relating the IGBT and diode voltage drops:

$$\begin{cases} V_+ = V_{igbt} + V_d \\ V_- = V_{igbt} - V_d \end{cases} \tag{49}$$

and considering only phase voltage distortion as $\tilde{V}_{x0} = \bar{V}_{x0} - \frac{V_{dc}}{2}\delta_x$.

Transition $0 \rightarrow \frac{V_{dc}}{2} \rightarrow 0$:

$$\mathbf{I_x > 0}:\ \tilde{V}_{x0} = -\frac{V_{DC}}{2}\frac{T_{DT}}{T_{SW}} - V_+ - V_-\left(\delta_x - \frac{T_{DT}}{T_{SW}}\right) \tag{50}$$

$$\mathbf{I_x} < 0: \ \tilde{V}_{x0} = \frac{V_{DC}}{2}\frac{T_{DT}}{T_{SW}} + V_+ - V_-\left(\delta_x + \frac{T_{DT}}{T_{SW}}\right) \tag{51}$$

Transition $0 \rightarrow -\frac{V_{dc}}{2} \rightarrow 0$:

$$\boldsymbol{I_x > 0}: \ \boldsymbol{\tilde{V}_{x0} = -\frac{V_{DC}}{2}\frac{T_{DT}}{T_{SW}} - V_+ + V_-\left(\delta_x + \frac{T_{DT}}{T_{SW}}\right)} \tag{52}$$

$$I_x < 0: \ \tilde{V}_{x0} = +\frac{V_{DC}}{2}\frac{T_{DT}}{T_{SW}} + V_+ + V_-\left(\delta_x - \frac{T_{DT}}{T_{SW}}\right) \tag{53}$$

Unifying the four previous equations in a singular one, the following expression can be derived:

$$\tilde{V}_{x0} = \frac{1}{T_{SW}}\left\{-sign(I_x)\cdot\left[\frac{V_{DC}}{2}\cdot T_{DT} + V_+\cdot T_{SW}\right] - sign(\delta_x)\cdot V_- \cdot\left[\delta_x\cdot T_{SW} - sign(I_x\cdot\delta_x)\cdot T_{DT}\right]\right\} \tag{54}$$

Evaluation of equivalent parasitic capacitance

Hereafter, only transition from positive dc-link to neutral point with positive output current will be considered, in order to calculate the equivalent parasitic capacitance, representing both the transistor and diode parasitic capacitances and the external capacitance connected to inverter (i.e. the cable and load capacitances). Three operating situations can be distinguished as illustrated in **Fig. 2.72**. When the output node is connected to positive dc-link, parasitic capacitor of clamping diode D5 is charged to $+V_{dc}/2$ as well as parasitic capacitors of T3 and T4 (**Fig. 2.72a**). Other capacitances are out of charge. When a neutral point connection is triggered by the PWM control, T1 is immediately switched off, while its complementary switch T3 is still maintained off respecting dead-time condition. As shown in **Fig. 2.72b**, capacitance of D5 is discharged and T1 capacitor is charged to $+V_{dc}/2$. At the same time the lower part of inverter leg experiences a redistribution of charge through T3, T4 and D6 devices. By applying the conservation of energy, it is possible to evaluate voltage drops of T3, T4 and D6 parasitic capacitors as follows:

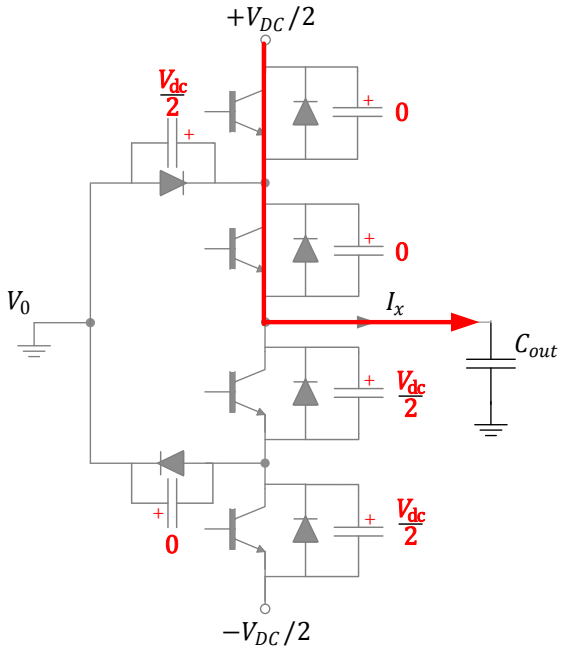
$$\begin{cases} E_p = 2\cdot\frac{1}{2}C\left(\frac{V_{dc}}{2}\right)^2 \\ E_0^{dt} = 2\cdot\frac{1}{2}C\cdot V_C^2 + \frac{1}{2}C\left(V_C - \frac{V_{dc}}{2}\right)^2 \rightarrow V_C = \frac{V_{dc}}{6} \\ E_p = E_0^{dt} \end{cases} \tag{55}$$

where E_p is the energy stored when the output is connected at positive dc-link, E_0^{dt} is the energy stored when the output is connected to neutral point during dead-time and V_C is the voltage drop of the middle point between T3 and T4 respect to the neutral point.

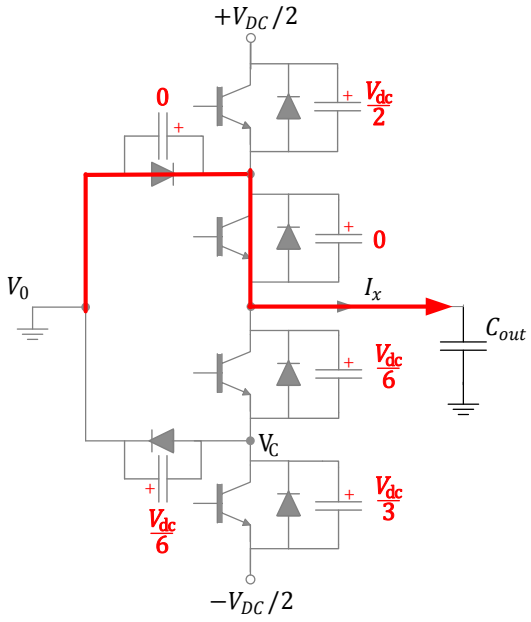
As the dead-time terminates, T3 is switched on and V_C is forced to be zero (**Fig. 2.72c**). Io order to evaluate the equivalent parasitic capacitance seen at the output node, the whole variation of charge flowing to the output has to be considered:

$$C_e = \frac{\Delta Q_{out}}{\Delta V_{out}} = \frac{\Delta Q_{D5} + \Delta Q_{T1} + \Delta Q_{T3}}{\Delta V_{out}} = \frac{8}{3} C_{out} \tag{56}$$

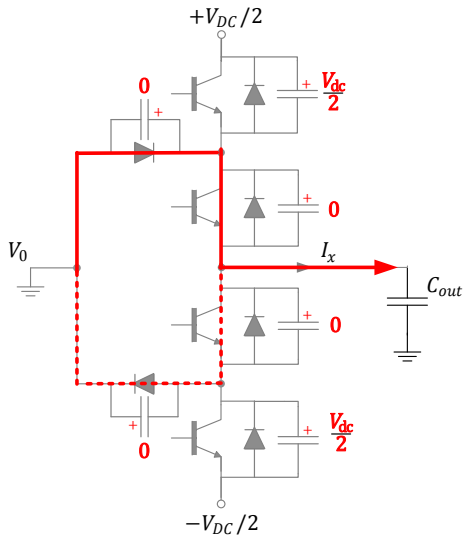
where it is assumed that all devices have the same collector-emitter capacitance C_{out}.



a) Output connected to positive dc-link



b) Output connected to neutral point during dead-time



c) Output connected to neutral point after dead-time

Fig. 2.72: Charging and discharging switch capacitance during positive dc-link to neutral point transition.

Adding the capacitance effect to the model

The adopted full model comprises parasitic capacitance charging effect. Eight different cases can be considered as a function of the sign, the absolute value of the output current and the type of voltage transition. Nevertheless, for the sake of simplicity only half cases has been reported here, as depicted in **Fig. 2.73**.

If the time required to charge/discharge the output capacitance is higher than the dead-time interval (i.e. when the output current is quite low), the commutation is slower and a discontinuity is experienced in the output voltage as soon as the higher IGBT switches on after the dead-time interval passed.

The limit condition between the ideal step transition and intermediate slower cases can be calculated by matching the charge and discharge time and dead-time, i.e.

$$\frac{V_{dc}}{2} = \frac{1}{C_e}\int_0^{T_{DT}} I_x\,dt = \frac{I_x T_{DT}}{C_e} \Rightarrow I_{thr} = \frac{C_e \frac{V_{dc}}{2}}{T_{DT}} \qquad (57)$$

where C_e is the overall output capacitance, T_{DT} is the dead- time and I_x is the generic leg output current.

If the IGBT and diode voltage drops are also taken into account, previous equation can be split into two different expressions as a function of I_x sign, i.e.

$$\begin{cases} I_x = \dfrac{C_e\left(\frac{V_{dc}}{2} + V_d - V_{igbt}\right)}{T_{DT}} & if\ I_x > 0 \\ I_x = \dfrac{C_e\left(-\frac{V_{dc}}{2} - V_d + V_{igbt}\right)}{T_{DT}} & if\ I_x < 0 \end{cases} \tag{58}$$

The difference between the areas in the first case, i.e. null capacitance, and that of **Fig. 2.73** are then considered, and two expressions are obtained as a function of the value of the output current:

$$if \quad |I_x| < \frac{C_e\left(\frac{V_{dc}}{2} + V_d - V_{igbt}\right)}{T_{DT}} \Rightarrow \overline{V}_{x0_{cap}} = \frac{1}{T_{SW}}\left[-\frac{I_x}{2C_e}T_{DT}^2\right] \tag{59}$$

$$if \quad |I_x| > \frac{2C_{out}(V_{DC} + V_{IGBT} - V_{diode})}{T_{DT}} \Rightarrow$$

$$\overline{V}_{x0_{cap}} = \frac{1}{T_{SW}}\left[-sign(I_x)\left(\frac{V_{dc}}{2} + V_d - V_{igbt}\right)T_{DT} + \frac{C_e\left(\frac{V_{dc}}{2} + V_d - V_{igbt}\right)^2}{2I_x}\right] \tag{60}$$

representing the contribution of the output capacitance to average output voltage distortion. Finally the two contributions, i.e. the last two equations and those calculated in (45)-(48) can be joined to obtain the overall average distortion voltage in the different current conditions, as reported in the following equations:

$$if \quad |I_x| < \frac{C_e\left(\frac{V_{dc}}{2} + V_d - V_{igbt}\right)}{T_{DT}} \Rightarrow$$

$$\widetilde{V}_{x0} = \frac{1}{T_{SW}}\left\{-sign(I_x)\cdot\left[\frac{|I_x|}{2C_e}\cdot T_{DT}^2 + V_+\cdot T_{SW}\right] - sign(\delta_x)\cdot V_- \cdot [\delta_x\cdot T_{SW} - sign(I_x\cdot\delta_x)\cdot T_{DT}]\right\} \tag{61}$$

$$if \quad |I_x| > \frac{2C_{out}(V_{DC} + V_{IGBT} - V_{diode})}{T_{DT}} \Rightarrow$$

$$\tilde{V}_{x0} = \frac{1}{T_{SW}}\left\{-sign(I_x)\cdot\left[\left(\frac{V_{dc}}{2} - V_-\right)T_{DT} - \frac{C_e\cdot\left(\frac{V_{dc}}{2} - V_-\right)^2}{2|I_x|} + V_+\cdot T_{SW}\right] - sign(\delta_x)\cdot V_-\cdot[\delta_x\cdot T_{SW} - sign(I_x\cdot\delta_x)\cdot T_{DT}]\right\} \tag{62}$$

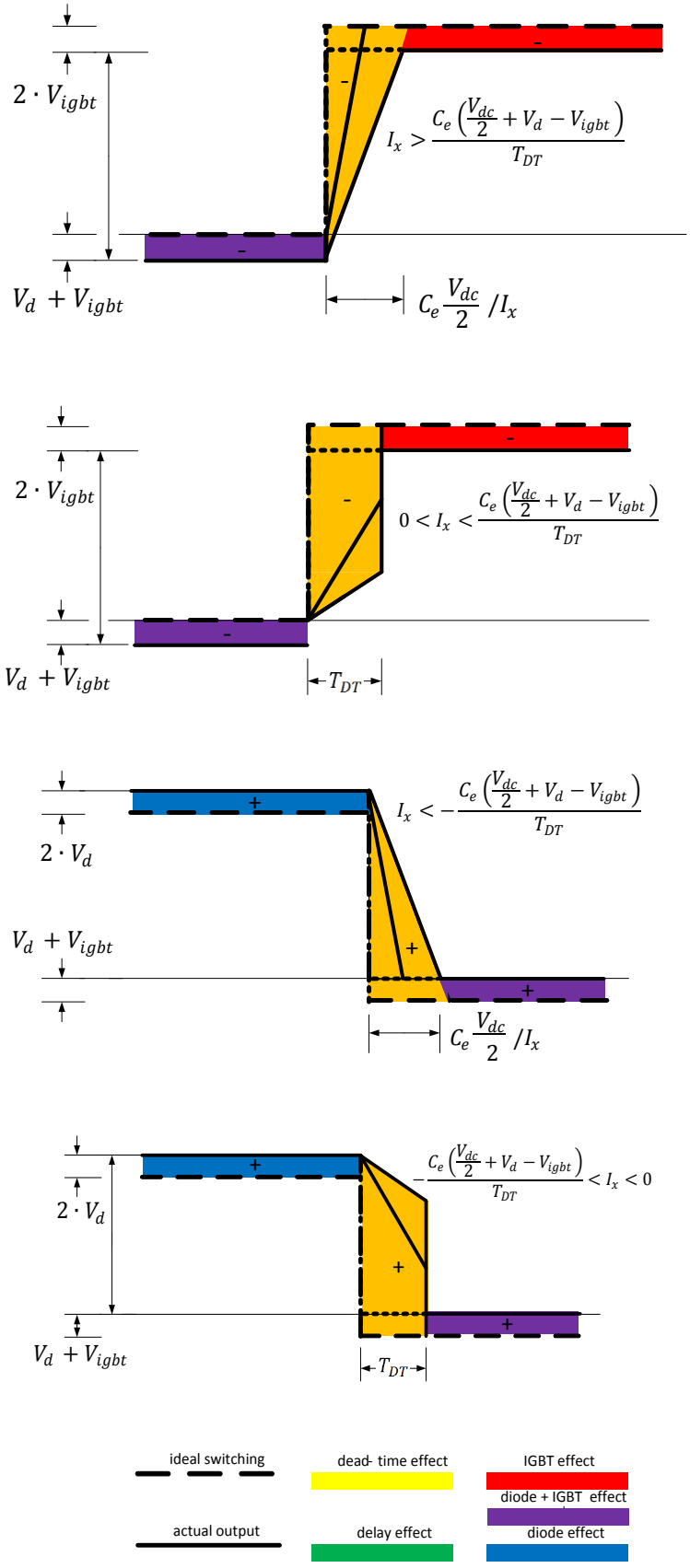


Fig. 2.73: Output voltage waveforms during dead time if considering output capacitance C_e.

2.7.3 Model simplification and simulation results

The model introduced above can be greatly simplified if $\delta_x \approx 0$; $T_{DT} \ll \delta_x T_{SW}$, $V_{IGBT} \ll V_{DC}$ and $V_{diode} \ll V_{DC}$ (small diode voltage drop). Distortion voltage component can be therefore expressed as a function of T_{DT}, C_e and A simple example of compensation of the phase voltage will be considered hereafter by considering the injection of a controlled current space vector along the phase a of the motor. This case can be considered as a meaningful one as standard experimental tests for parameters identification are normally referred to it. Due to the particular choice of the current space vector the following trivial condition holds $I_b = I_c = \frac{I_a}{2}$ that allows to calculate all the voltage distortion components as a function of the same current I_a. **Fig. 2.74** shows the results of a dynamical simulation of the complete inverter and digital current control system for a balanced 3P RL load in order to compare the actual phase voltage distortion characteristic, the accurate model and the simplified one. Phase voltage and current are obtained by averaging over the T_{SW}, and the distortion signal V_{anDT} of **Fig. 2.74** is the difference of the reference voltage coming from vector current control and the actual voltage value.

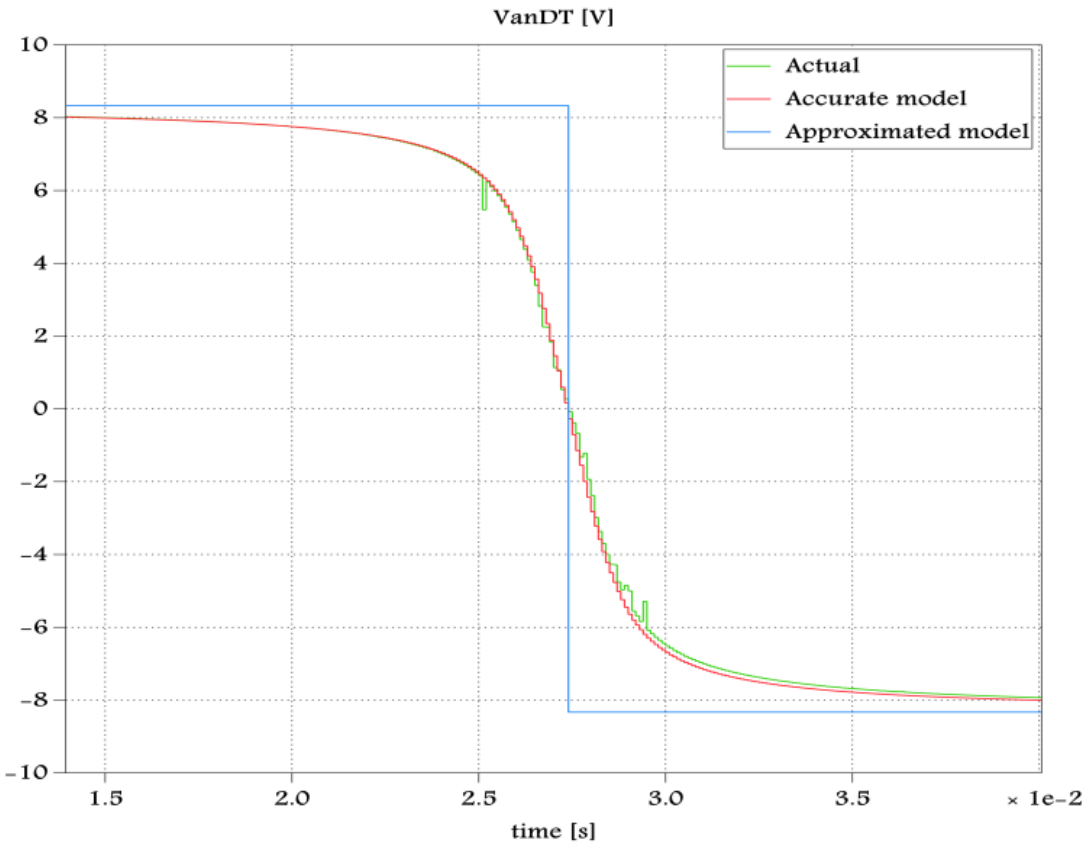


Fig. 2.74: Simulation: distortion voltage as a function of current.

3 NON-ISOLATED DC/DC CONVERTERS

3.1 Introduction

In the next Sections of this Chapter some non-isolated DC/DC converters will be investigated and studied. Firstly, a simple bi-directional topology will be presented. Then, a neutral point clamped configuration of the three-level buck converter will be studied and a new multiphase version of it will be discussed in detail.

3.2 Bi-directional DC/DC converter

3.2.1 Introduction

The bidirectional DC/DC converter along with energy storage has become a promising option for many power related systems, including hybrid electric vehicles, fuel-cell vehicles, renewable energy system, etc. The use of a bidirectional interface sometimes allows a cost reduction and improves the overall efficiency and performance of the system.

In the hybrid electric vehicle applications, an auxiliary energy storage battery absorbs the regenerated energy fed back by the electric machine. In addition, bidirectional dc-dc converter is also required to draw power from the auxiliary battery to boost the high-voltage bus during vehicle starting, accelerate and hill climbing. With its ability to reverse the direction of the current flow, and thereby power, the bidirectional dc-dc converters are being increasingly used to achieve power transfer between two dc power sources in either direction. In renewable energy applications, the multiple-input bidirectional dc-dc converter can be used to combine different types of energy sources [2-8]. Figure 1.2 shows a fuel cell based system for domestic applications [2]. The multi-input bidirectional dc-dc converter is the core that interconnects power sources and storage elements and manages the power flow [5]. This bidirectional dc-dc converter features galvanic isolation between the load and the fuel cell, bidirectional power flow, capability to match different voltage levels [9], fast response to the transient load demand, etc.

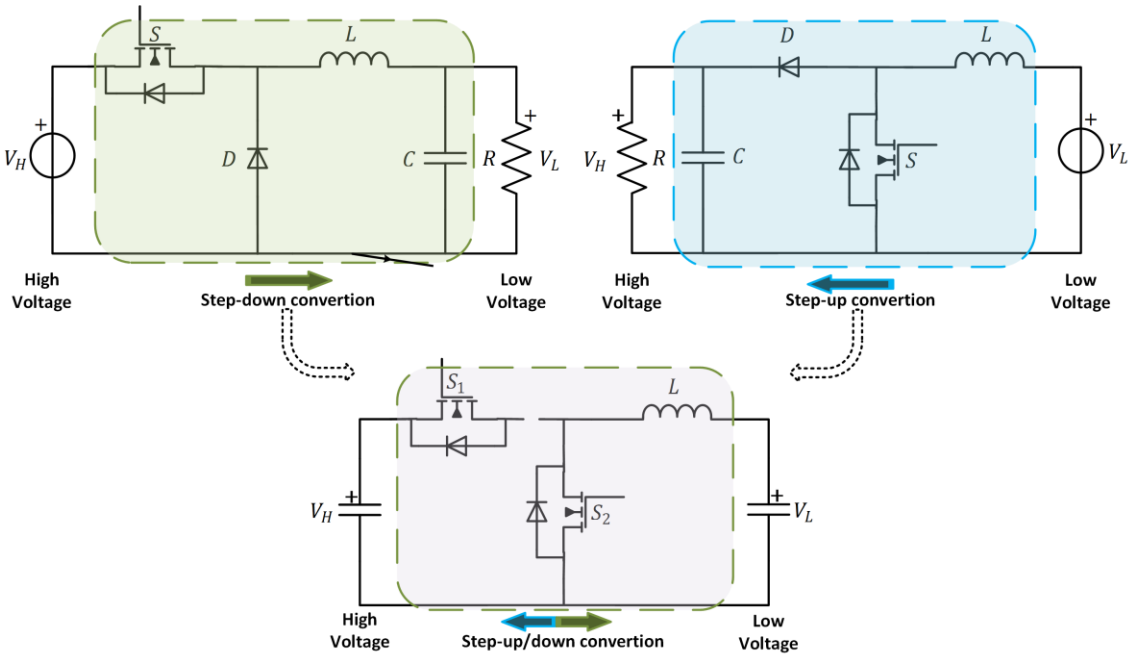


Fig. 3.1: Evolution of bi-directional half-bridge DC/DC converter from standard buck and boost topologies.

3.2.2 Topology

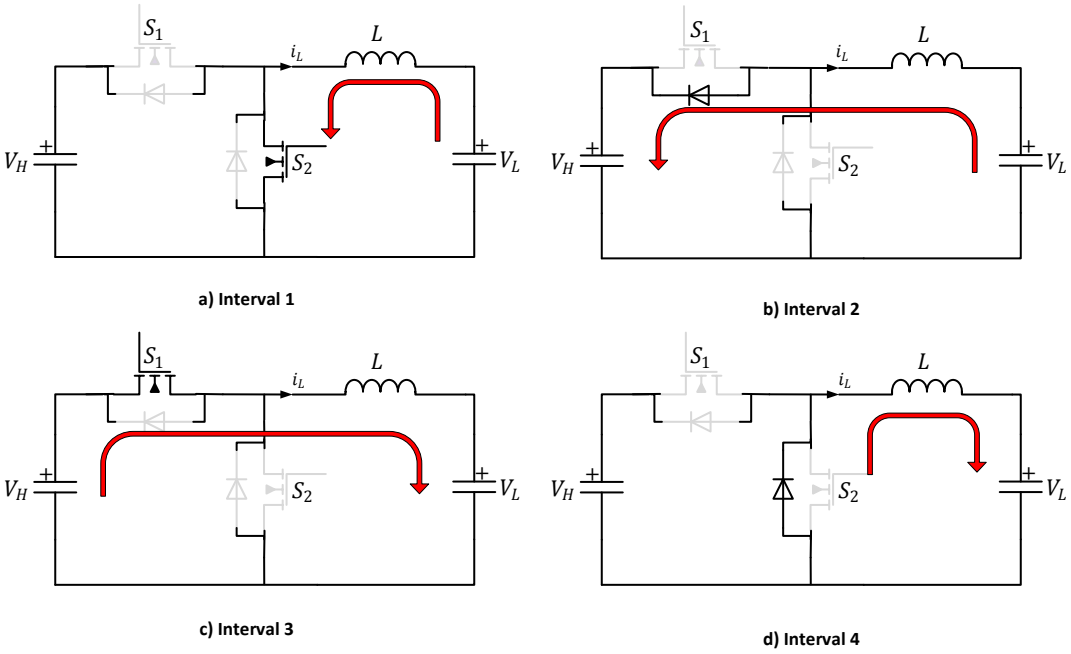
The standard non-isolated bidirectional DC/DC topology is based on the synchronous buck (or boost) half-bridge converter, in which the diode has been replaced by another switch. Thanks to this feature compare to the standard unidirectional topology, the bidirectional DC/DC converter can work both as a step-down voltage converter and a step-up converter depending on the direction of the power flow, as clearly shown in **Fig. 3.1**.

3.2.3 Operating modes

The bidirectional DC/DC converter is operated in continuous conduction mode (CCM). It means that inductor current is always positive and different from zero.

The MOSFETs S_1 and S_2 are switched in a complementary way (using a small dead-time between them), such that the converter operates in steady state with four sub-intervals namely interval 1 $(t_0 - t_1)$, interval 2 $(t_1 - t_2)$, interval 3 $(t_2 - t_3)$, and interval 4 $(t_3 - t_4)$. According to the circuit characteristics, a high voltage dc-link is taken as V_H and low voltage side (typically battery side) is taken as V_L.

The circuit operating modes for the different intervals are described as follows.



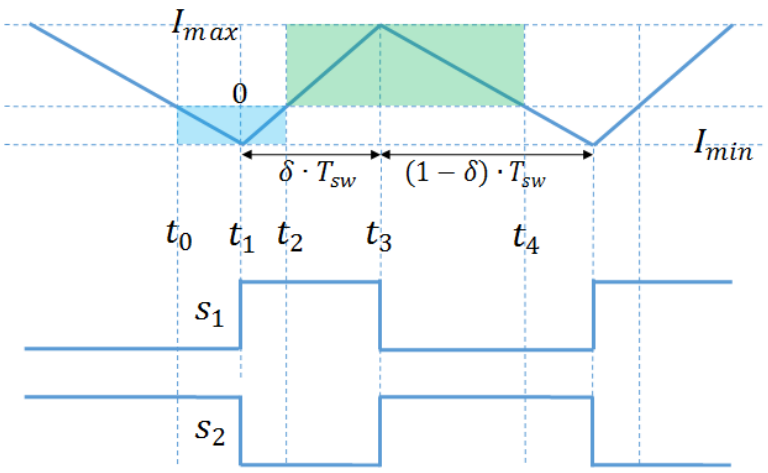


Fig. 3.2: Bi-directional converter operation sub-intervals (a, b, c, d) and complementary gate signals and inductor current.

Interval 1 ($t_0 - t_1$)

At time t_0 the low side switch S_2 is turned on and the high side switch S_1 is turned off with diode D1 and D2 reverse biased. During this time interval the converter operates in boost mode and the inductor is charged and current through the inductor increases.

Interval 2 ($t_1 - t_2$)

During this interval both switches S_1 and S_2 are turned off. The diode D_1 of upper switch starts conducting.

Interval 3 ($t_2 - t_3$)

At time t_3 the upper switch S_1 is turned on and the lower switch S_2 is turned OFF with diode D_1 and D_2 reverse biased. During this time interval the converter operates in buck mode.

Interval 4 ($t_3 - t_4$)

During this interval both switches S_1 and S_2 are turned off. The diode D_2 of lower switch S_2 starts conducting. During this time interval the converter operates in buck mode.

In a standard buck converter, the freewheeling diode turns on, on its own, shortly after the switch turn off, as a result of the rising voltage across the diode. This voltage drop across the diode results in a power loss which is equal to:

$$\boldsymbol{P_D = V_D(1 - D)I_o} \tag{63}$$

By replacing the diode with a second switch the power loss is equal to:

$$\boldsymbol{P_{S_2} = (1 - D)R_{DS_{on}}I_o^2} \tag{64}$$

Considering that using a well selected MOSFET as switch the RDSON is about few decimals of Ohm, it is possible to consider $V_D > I_o R_{DS_{on}}$ and thus the efficiency will increase and the heat loss can be reduced using a switch instead of a diode.

3.2.4 Unified state-space averaging model

A unified power stage model for the bidirectional half-bridge DC/DC converter, comprehensive of both the buck and the boost operating modes equations, has been developed [56]. In **Fig. 3.3** the converter configuration during the intervals 2 and 3 of **Fig. 3.2** (S_1 turned on and S_2 turned off) is illustrated.

Three energy storage elements are present, leading to the following Kirchhoff equations:

$$\begin{cases} \boldsymbol{L\dfrac{di_L}{dt} + i_L(R_{DS_{on}} + R_{DCR}) = v_1 + v_2} \\ \boldsymbol{C_H\dfrac{dv_1}{dt} = -i_L + \dfrac{v_1 - V_H}{R_H}} \\ \boldsymbol{C_L\dfrac{dv_2}{dt} = i_L + \dfrac{v_2 - V_L}{R_L}} \end{cases} \tag{65}$$

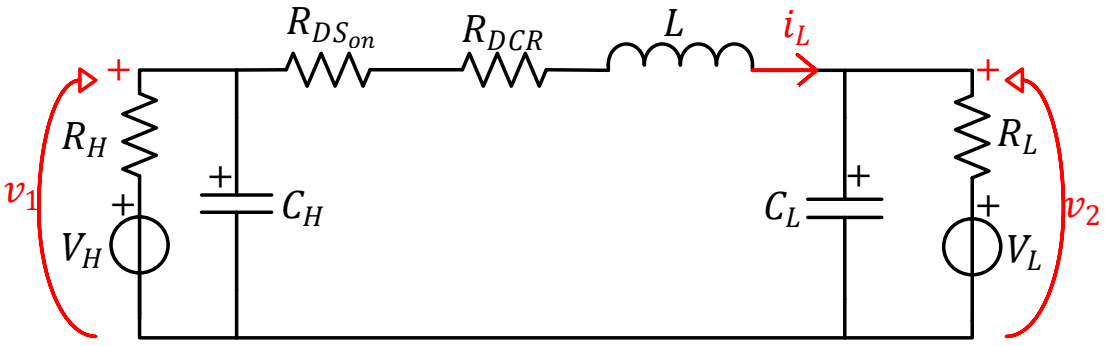


Fig. 3.3: Bidirectional DC/DC converter circuit model during turn ON of S_1.

In Fig. the converter configuration during the intervals 1 and 4 of **Fig. 3.2** (S_1 turned off and S_2 turned on) is illustrated. The Kirchhoff equations for the circuit this time are:

$$\begin{cases} L\dfrac{di_L}{dt} + i_L\left(R_{DS_{on}} + R_{DCR}\right) = -v_2 \\ C_H\dfrac{dv_1}{dt} = -\dfrac{v_1 - V_H}{R_H} \\ C_L\dfrac{dv_2}{dt} = i_L - \dfrac{v_2 - V_L}{R_L} \end{cases} \tag{66}$$

Considering a complete switching period, the following state-space averaging can be derived:

$$\begin{cases} L\dfrac{d\bar{i}_L}{dt} = D(\bar{v}_1 - \bar{v}_2) - \bar{i}_L\left(R_{DS_{on}} + R_{DCR}\right) + D'(-v_2) \\ C_H\dfrac{d\bar{v}_1}{dt} = -D\left(\bar{i}_L + \dfrac{\bar{v}_1 - V_H}{R_H}\right) - D'\left(\dfrac{\bar{v}_1 - V_H}{R_H}\right) \\ C_L\dfrac{d\bar{v}_2}{dt} = \bar{i}_L - \dfrac{\bar{v}_2 - V_L}{R_L} \end{cases} \tag{67}$$

Finally, considering $D = \bar{d}$ and $D' = 1 - \bar{d}$, a general averaging model is derived in the following group of equations:

$$\begin{cases} L\dfrac{d\bar{i}_L}{dt} = \bar{d}\cdot\bar{v}_1 - \bar{v}_2 - \bar{i}_L\left(R_{DS_{on}} + R_{DCR}\right) \\ C_H\dfrac{d\bar{v}_1}{dt} = -\bar{d}\cdot\bar{i}_L - \dfrac{\bar{v}_1 - V_H}{R_H} \\ C_L\dfrac{d\bar{v}_2}{dt} = \bar{i}_L - \dfrac{\bar{v}_2 - V_L}{R_L} \end{cases} \tag{68}$$

Considering $R_p = R_{DS_{on}} + R_{DCR}$, the previous system can be written in terms of a state-space averaged DC matrix that describes the converter in equilibrium:

$$\boldsymbol{Ax + Bu = 0} \tag{69}$$

where $x = (I_L, V_1, V_2)$ represents the state variable vector and $u = (V_H, V_L)$ the input voltage vector.

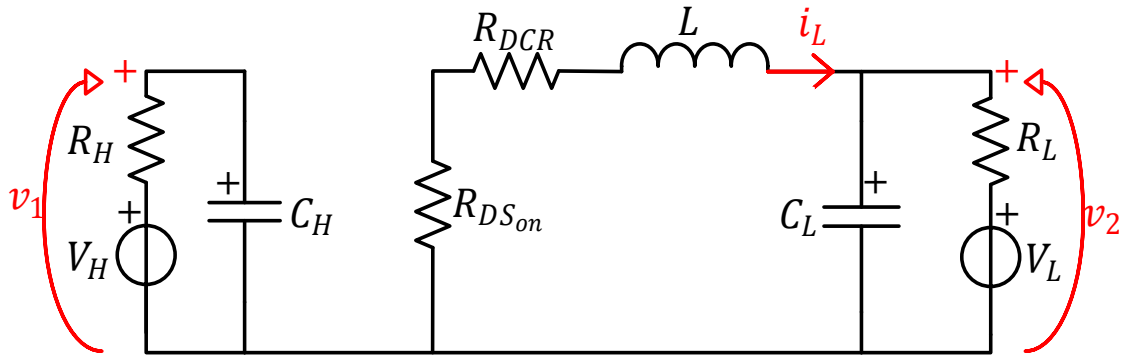


Fig. 3.4: Bidirectional DC/DC converter circuit model during turn OFF of S_1.

Solving this matrix equation permits to obtain the following solution for I_L, V_1, V_2 in the large signal domain:

$$\begin{cases} I_L = \dfrac{DV_H - V_L}{R_H D^2 + R_L + R_p} \\ V_1 = V_H(R_L + R_p) + DR_H V_L \\ V_2 = \dfrac{D(V_H R_L + DR_H V_L) + R_p V_L}{R_H D^2 + R_L + R_p} \end{cases} \quad (70)$$

The state-space AC equations that describe the converter in equilibrium can be written as:

$$\begin{cases} L\dfrac{d\hat{\imath}_L}{dt} = (\hat{d} + D)\cdot(\hat{v}_1 + V_1) - (\hat{v}_2 + V_2) - (\hat{\imath}_L + I_L)(R_{DS_{on}} + R_{DCR}) \\ C_H\dfrac{d\hat{v}_1}{dt} = -(\hat{d} + D)\cdot(\hat{\imath}_L + I_L) - \dfrac{\hat{v}_1 + V_1 - V_H}{R_H} \\ C_L\dfrac{d\hat{v}_2}{dt} = \hat{\imath}_L + I_L - \dfrac{\hat{v}_2 + V_2 - V_L}{R_L} \end{cases} \quad (71)$$

Transforming in Laplace domain and neglecting the higher order items, the control to high-side-voltage transfer function, the control to low-side-voltage transfer function and the control-to-current transfer function can be obtained:

$$\begin{cases} \dfrac{\hat{v}_1}{\hat{d}} = -\dfrac{\frac{D}{C_H}\frac{\hat{\imath}_{L1}}{\hat{d}} + \frac{I_L}{C_H}}{s + \frac{1}{R_H C_H}} \\ \dfrac{\hat{v}_2}{\hat{d}} = -\dfrac{\frac{1}{C_L}}{s + \frac{1}{R_L C_L}}\dfrac{\hat{\imath}_{L1}}{\hat{d}} \\ \dfrac{\hat{\imath}_{L1}}{\hat{d}} = \dfrac{\left(s + \frac{1}{R_L C_L}\right)\left[\left(s + \frac{1}{R_H C_H}\right)\frac{V_1}{L} - \frac{DI_L}{C_H L}\right]}{\left(s + \frac{R_p}{L}\right)\left(s + \frac{1}{R_H C_H}\right)\left(s + \frac{1}{R_L C_L}\right) + \frac{D^2}{C_H L}\left(s + \frac{1}{R_L C_L}\right) + \frac{1}{R_L C_L}\left(s + \frac{1}{R_L C_L}\right)} \end{cases} \quad (72)$$

The current transfer function $\frac{\hat{\imath}_{L1}}{\hat{d}}$ clearly describes the three order characteristic of the system given by the three energy storage components C_H, C_L and L. Since the buck charging and

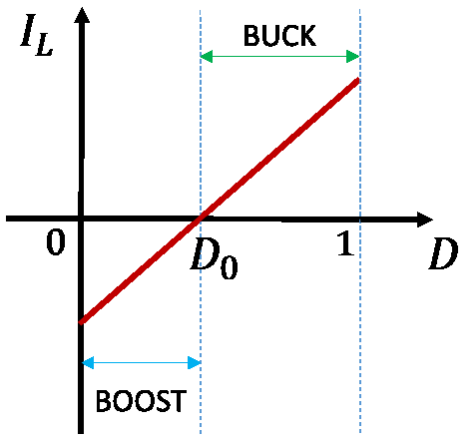


Fig. 3.5: Duty-cycle versus inductor averaged current.

boost discharging modes share the same power plant transfer function, they can share a unified controller. The inductor average current I_L reference flow direction is the same as low voltage side power flow and only depends on the relationship between control duty cycle D and zero current duty cycle $D_o = \frac{V_L}{V_H}$., as shown in **Fig. 3.5**

In fact, when $D > D_o \rightarrow \mathrm{I_L} > 0$ the converter works in buck operation mode; otherwise, when $D < D_o \rightarrow \mathrm{I_L} < 0$ the converter works in boost operation mode. This means that the current flow direction (and so the converter operation mode) is determined by controlling the duty cycle.

3.3 Three-level buck converter

Three-level buck converter could allow a reduction of the size of the magnetic parts or a reduction of the switching frequency by maintaining a reasonable size of the magnetic parts. This makes very attractive for low current point of load converters, [76]. Moreover voltage stress across power switches are halved in three-level topology, provided that the input capacitors voltages remain balanced. This makes three-level converter very suitable in high voltage/high power applications [77] and, for certain voltage levels, could allow replacement of IGBTs with MOSFETs power devices.

Different topologies and applications have been investigated in literature. A single-switch three-level converter was proposed in [78] for dimmable LED lighting. A simple ZVS auxiliary circuit that achieves ZVS even at no load, in order to maximize the efficiency of the converter for all load conditions was presented in [79].

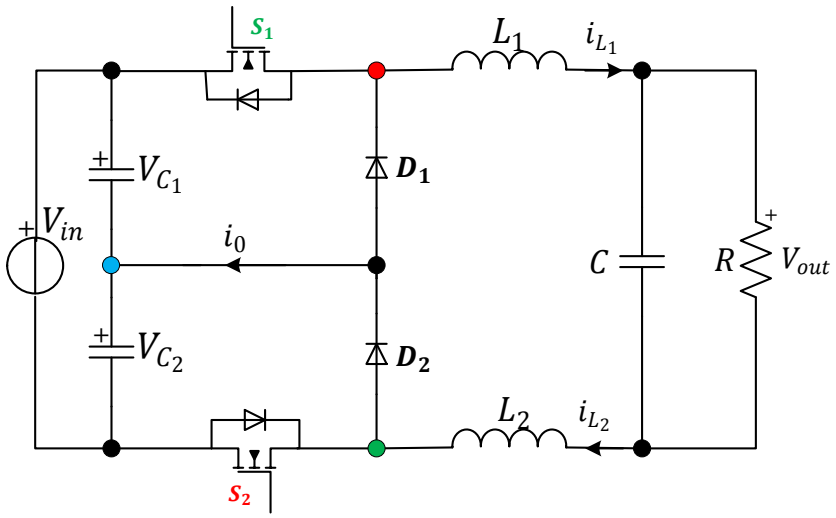


Fig. 3.6: Three-level buck converter.

3.3.1 Operating principle

The circuit diagram of the three-level buck converter is shown in **Fig. 3.5**. The input voltage source is split with a capacitive voltage divider, whose middle point represents the neutral point of the converter. The output inductor is also split and symmetrically placed. The chopped voltage entering the output filter has three levels, i.e. 0 when both switches S_1 and S_2 are OFF, $V_{in}/2$ when one of the switches is ON (in the case the voltages across the input capacitors are equal), and V_{in} when both switches are ON. S_1 and S_2 are driven with the same duty-cycle and with a phase shift of 180°.

Hereafter the operating modes and the output inductor ripple current of the three-level buck converter are analyzed.

Operating modes

The output current i_{L1} is supposed positive as the converter is operating in buck mode and is providing power to the load.

1) S_1 is ON and S_2 is OFF

The red point of **Fig. 3.5** is connected to V_{in} and the green point is connected to the common point of the input capacitors (blue point). D_1 is in inverse operation since its voltage is equal to$V_{C_2} - V_{in} \approx -V_{in}/2$and D_2 is forced to conduct due to i_{L_2}. Thus, the total inductance ($L_1 + L_2 = L_o$) is charged with a voltage equal to$V_{in} - V_{C2} - V_{out} \approx \frac{V_{in}}{2} - V_{out}$. In this situation, C_1discharges and C_2charges of the following voltage value:

$$\boldsymbol{\Delta V_{C1} = -\frac{1}{2}\frac{i_{L_2} \cdot \delta_1}{C \cdot f_{sw}} = -\Delta V_{C2}} \qquad \textbf{(73)}$$

Where δ_1 is the duty cycle of S_1 and $\Delta V_{Cx}$is the variation of capacitor C_x voltage after the switching interval$t_{on,1} = \frac{\delta_1}{f_{sw}}$.

2) S_2 is ON and S_1 is OFF

The red point is connected to the blue point (D_1 if forward biased) and the green point to the reference terminal of the input voltage source.D_2 is in inverse operation since its voltage is equal to $V_{C_1} - V_{in} \approx -V_{in}/2$ and $D_1$is forced to conduct due to i_{L_1}. Thus, L_o is charged with a voltage equal to $V_{in} - V_{C1} - V_{out} \approx \frac{V_{in}}{2} - V_{out}$. In this situation, C_1 charges and C_2discharges of the following voltage value:

$$\boldsymbol{\Delta V_{C1} = \frac{1}{2}\frac{i_{L_1} \cdot \delta_2}{C \cdot f_{sw}} = -\Delta V_{C2}} \qquad \textbf{(74)}$$

3) S_1 and S_2 are ON

This condition is met when duties are above 0.5. L_o is charged with a voltage equal to $V_{in} - V_{out}$ and the blue point is not affected by the output current. Thus, the voltages across the input capacitors remains unchanged.

4) S_1 and S_2 are OFF

Both D_1 and D_2 are conducting and the inductance discharges with a voltage equal to $-V_{out}$. As well as the previous case, no current is injected into the blue point.

Inductor ripples current analysis

If the input capacitor voltages are assumed to be equal to half the input voltage and $\delta_1 = \delta_2 = \delta$, the current ripple has the following expression:

$$\Delta I_{L_0} = \begin{cases} \dfrac{V_{in} \cdot (0.5 - \delta) \cdot \delta}{L_0 \cdot f_{sw}}, & \delta \leq 0.5 \\ \dfrac{V_{in} \cdot (1 - \delta) \cdot (0.5 - \delta)}{L_0 \cdot f_{sw}}, & \delta \geq 0.5 \end{cases} \quad (75)$$

In **Fig. 3.7** a comparison of current ripple as a function of duty cycle is reported in the case of standard two-level one-switch buck converter, a three-phase interleaved buck converter and the three-level version.

The current ripple for this last topology approaches to zero when the duty-cycle is 0, 0.5 or 1. The maximum current ripple occurs when the duty cycle is 0.25 and 0.75, being four times lower than the conventional two-level one-switch converter. Also in comparison with three-phase interleaved converter, the achievable ripple reduction is significant. This enhanced

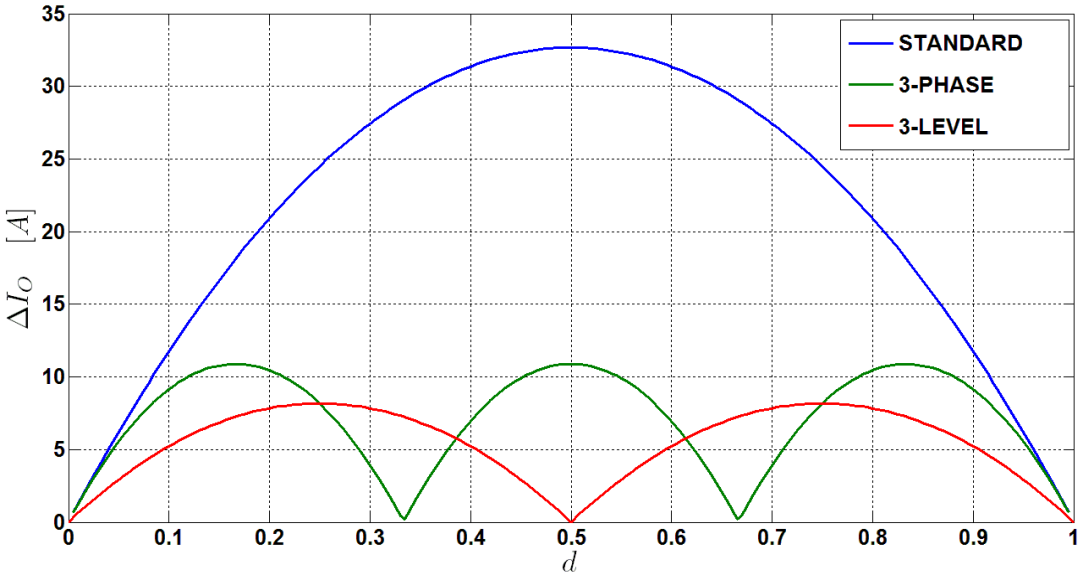


Fig. 3.7: Current ripple comparison.

ripple performance is similar to the one that can be achieved with coupled-inductor interleaved buck converters, [47].

Therefore three-level buck converter could allow a reduction of the size of the magnetic parts or a reduction of the switching frequency by maintaining a reasonable size of the magnetic parts.

3.3.2 Neutral-point voltage regulation

The three-level converter benefits are fully achieved only if the input capacitor voltages are properly balanced to half of the input voltage. As shown in **Fig. 3.8** the current i_o injected into the neutral point can be written as:

$$\boldsymbol{i_o(t) = i_{C_2}(t) - i_{C_1}(t) = C_2 \frac{dv_{C_2}(t)}{dt} - C_2 \frac{dv_{C_1}(t)}{dt} = C \frac{d}{dt}\left[v_{C_2}(t) - v_{C_1}(t)\right]} \quad \textbf{(76)}$$

Thus, the voltage difference between the two capacitors within a switching period is:

$$\boldsymbol{\left[v_{C_2} - v_{C_1}\right] = \frac{1}{C}\int i_o \cdot dt = \frac{1}{C}\left[\int i_{L_2} \cdot dt\Big|_{S_1 ON} + \int i_{L_1} \cdot dt\Big|_{S_2 ON}\right]} \quad \textbf{(77)}$$

In theory, if the duty cycles δ_1 and δ_2 remain the same and operating condition is steady-state (this means$i_{L_2} = i_{L_1}$), the two integrals have opposite values, so the capacitor voltages are supposed to remain balanced. Obviously, the instantaneous voltage ripple depends on the value of the two capacitors. During a transient, the current values of i_{L_1} and i_{L_2} are dynamically changing within a switching period, resulting in an unbalance situation for v_{C_1} and v_{C_2}. Therefore the voltage unbalance $\Delta v_C = v_{C1} - v_{C2}$ has to be dynamically compensated to avoid dangerous operations of power devices.

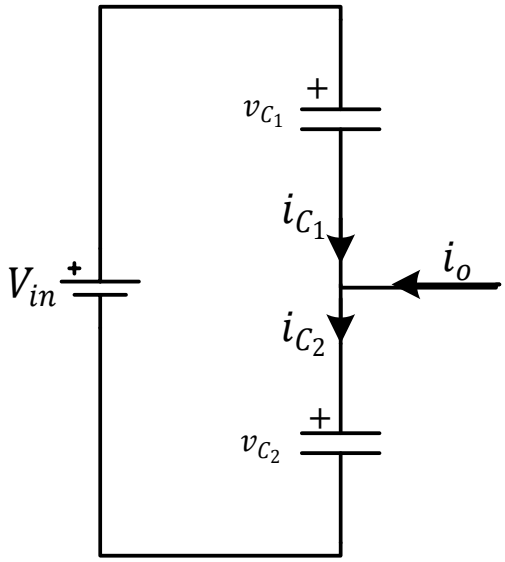


Fig. 3.8: Current in the input capacitors.

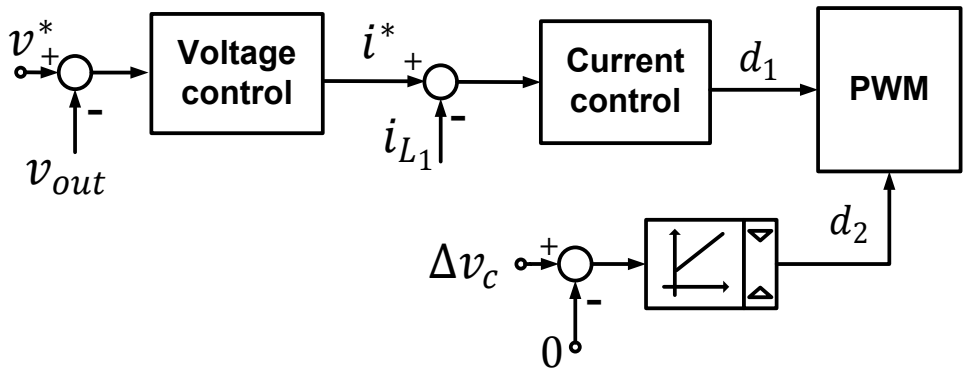


Fig. 3.9: Capacitor voltage unbalance compensation scheme.

The method proposed here is resumed in the block diagram of **Fig. 3.9**. The duty cycle d_1 is controlled in order to regulate the current flowing in inductorL_1, whilst the duty cycle d_2 is controlling the voltage unbalance between the two input capacitors. The effectiveness of the proposed scheme is demonstrated by simulation analysis, as reported hereafter.

In the results of **Fig. 3.10** the output current (actual in green, reference in red) and the voltage difference across the input capacitors (actual in green and average value within T_{sw} in blue line), are reported during a current transient without any balancing control. As one can notice the voltages across the two input capacitor experience a transient condition leading to permanent unbalance after the transient has expired. The amount of the unbalance voltage is limited due to the adopted value of input capacitance, the value of the output current reference and the current loop dynamics.

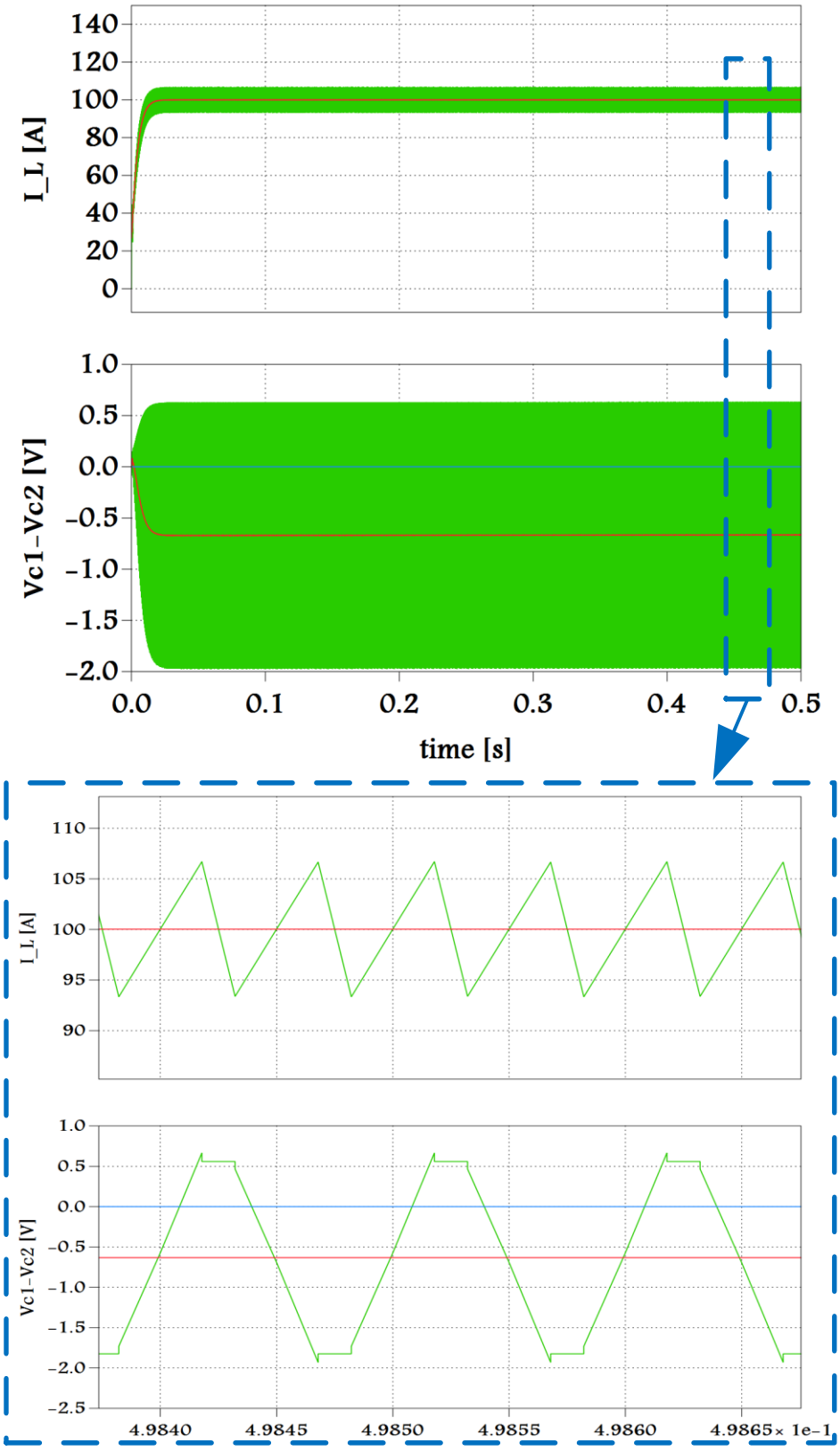


Fig. 3.10: Output current and capacitor voltage difference during a transient condition (start-up) and at steady-state without any unbalance control.

The same test is considered in the results of **Fig. 3.11**. In this case voltage unbalance control loop is active and the dc value of $v_{C_1} - v_{C_2}$ is driven to zero after the initial transient condition, proving the effectiveness of the proposed unbalance control method.

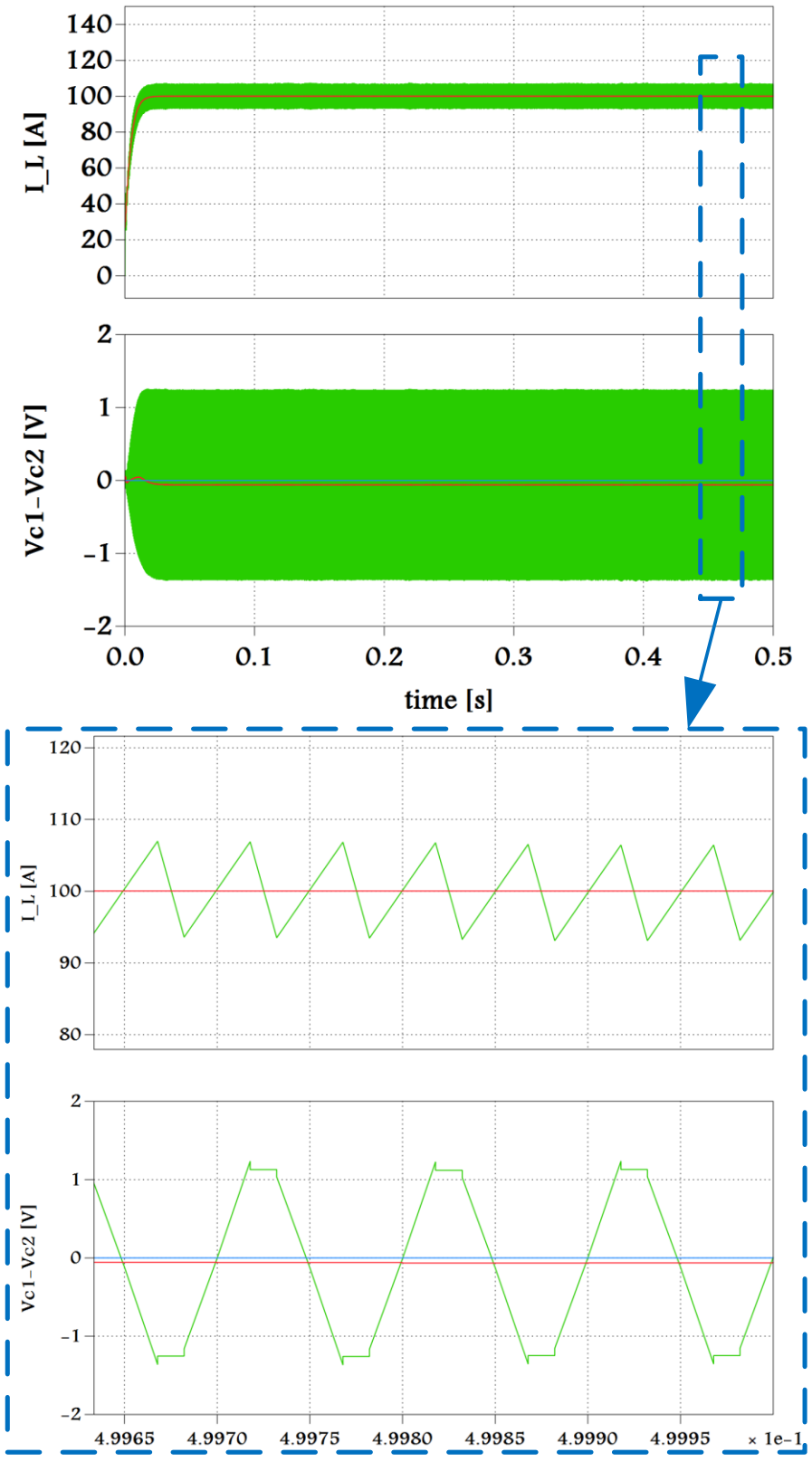


Fig. 3.11: Output current and capacitor voltage difference during a transient condition (start-up) and at steady-state with active unbalance control.

3.4 Interleaved zero current transition 3L buck converter

Various zero current transition (ZTC) techniques that have been proposed to mitigate switching problems dealing with IGBTs could be also applied to the three-level non-isolated converters. Some references proposed the use of a resonant circuit for zero current transition, but especially for the TL topologies this circuit adds significant complexity.

In [80], a simple ZCT scheme was proposed, providing the advantages of both soft switching and interleaving. The switch turn-on and diode reverse recovery losses are reduced by using an interleaved converter configuration with small commutation inductors. The topology of this ZCT three level buck converter is reported in **Fig. 3.12**.

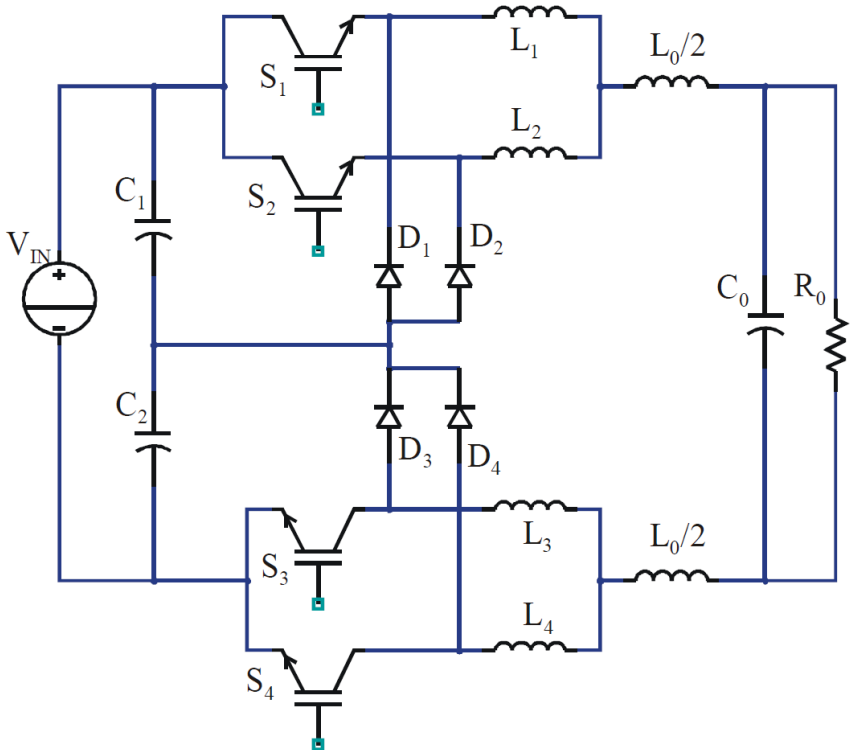


Fig. 3.12: Interleaved ZCT 3L buck topology [80].

Compared with the hard-switched PWM converter, the following improvements can be achieved using this ZCT topology.

- The switch voltage and current stresses are not increased, and there are no significant restrictions on the range of operating duty ratios.
- Each switch operates at two times lower switching frequency and conducts half of the time.
- Both switches in the interleaved ZCT configuration participate in the power processing function of the converter and share the power equally.

- The small auxiliary inductors L_1, L_2, L_3, L_4 enable the ZCT turn-on and reduced switching losses, whereas the larger inductor L_0 results in CCM operation with good average current sharing and low current ripple.

Fig. 3.13 shows the main waveforms of the converter, i.e. switches commands S_1, S_2, S_3, S_4, inductor currents, one switch current and one diode current.

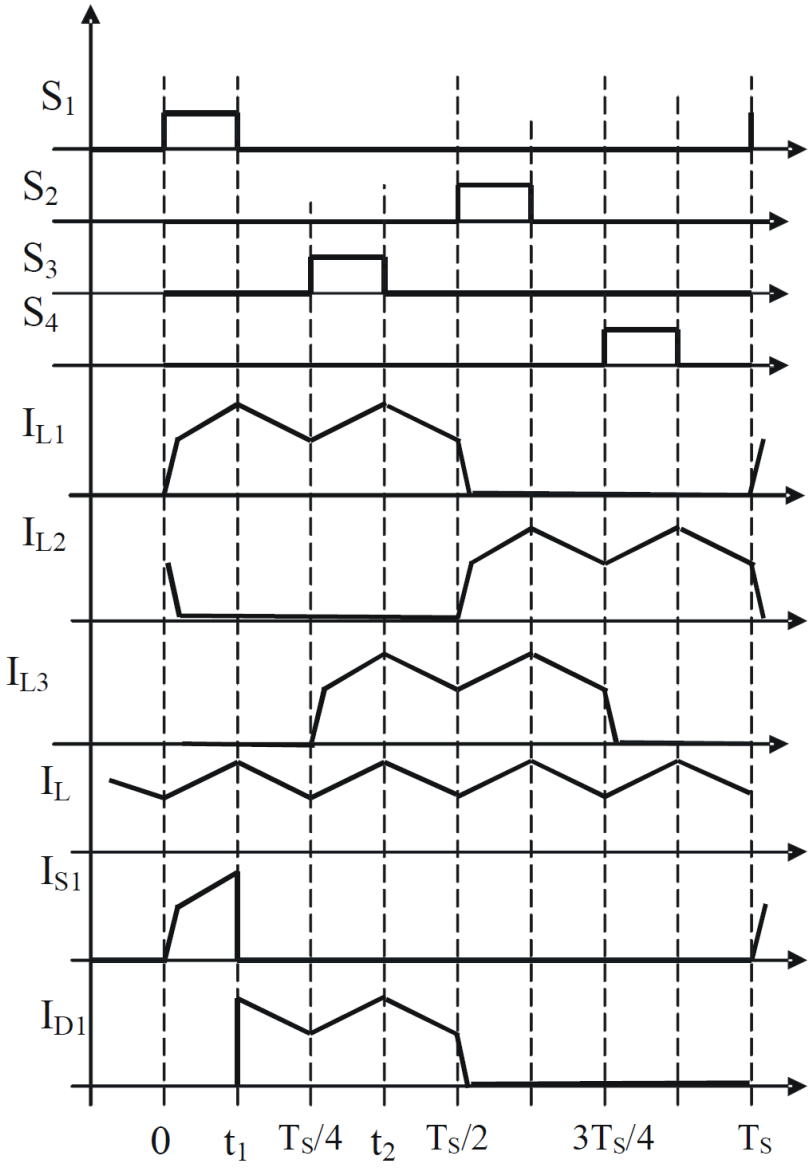


Fig. 3.13: Interleaved ZCT 3L buck main waveforms [80].

3.4.1 Implementation in PLECS

A simulation model of the ZCT three-level buck converter has been implemented in the standalone PLECS, in order to verify the effectiveness of the proposal and to highlight the specific features of this topology.

The implementation circuit within PLECS has been reported in **Fig. 3.14**.

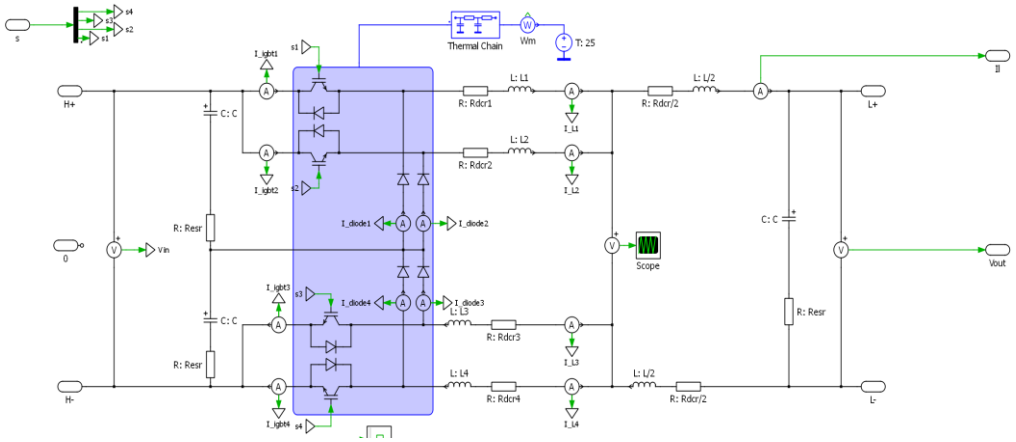


Fig. 3.14: Interleaved ZCT 3L buck PELCS implementation.

The same theoretical waveforms of **Fig. 3.13** has been achieved with the simulation scheme and are shown in **Fig. 3.15**.

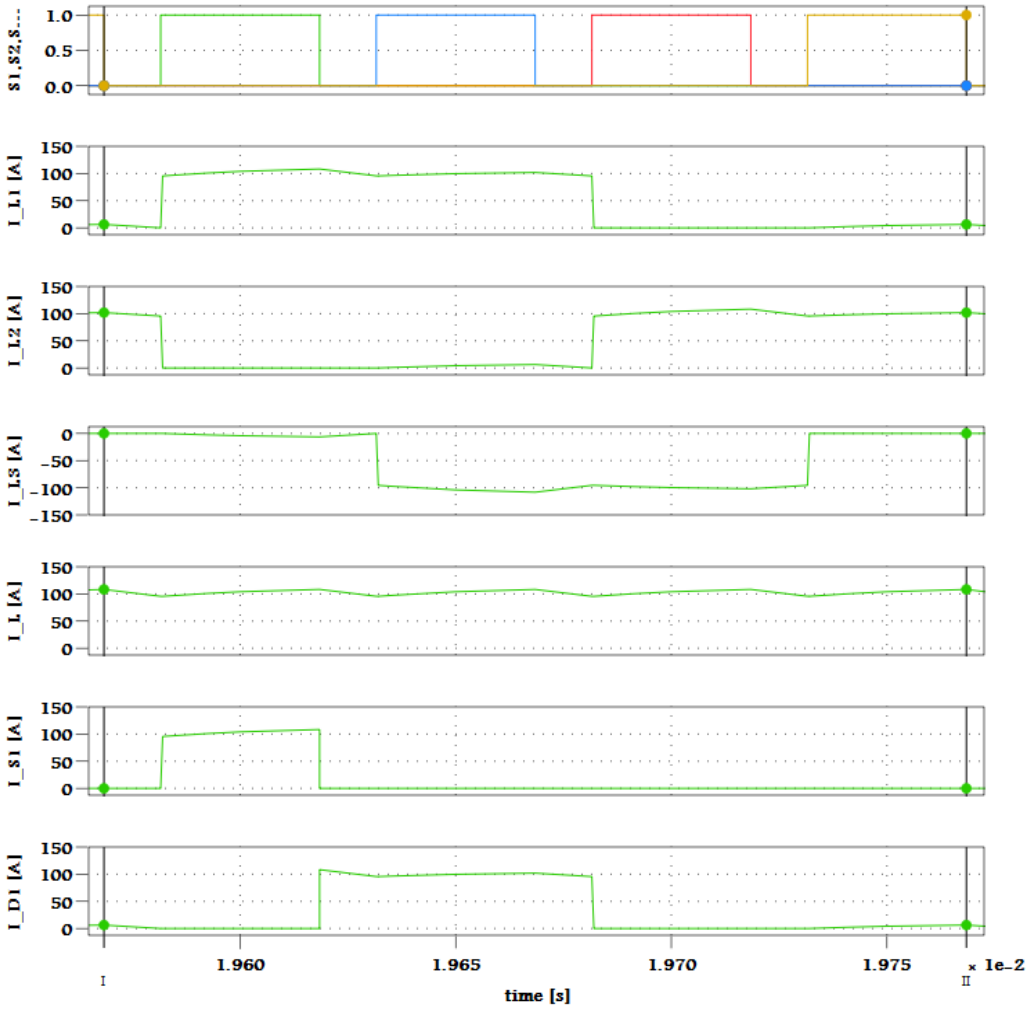


Fig. 3.15: Interleaved ZCT 3L buck PELCS simulation.

3.5 Proposed multiphase 3L buck converter

In this section, the new multiphase interleaved three-level buck converter is introduced [109]. The main objective is to exploit the advantages of this configuration, i.e. split the output current between two inductors, increase both the energy density and the equivalent switching frequency seen at the output, but preserving the three-level topology.

As it is shown in **Fig. 3.16** this converter is composed mainly by four switches, four diodes and four inductors. S_1 and S_2 refer to the same phase PH_1 and they are driven in the same way of a conventional three-level buck converter, i.e. identical duty-cycles phase shifted by 180 degrees. On the other side, S_3 and S_4 form the otherthree-level buck phasePH_2.These switching commands are still phase shift by 180° one to each other, but they are shifted by 90° and 270°with respect to S_1 and S_2.

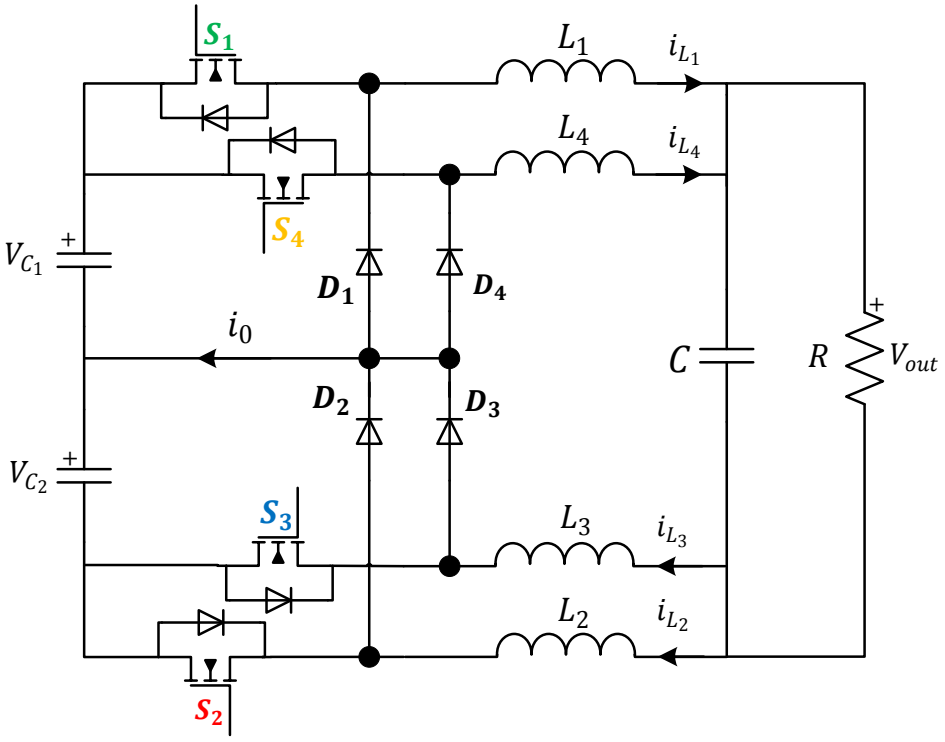


Fig. 3.16: Proposed multiphase interleaved 3L buck topology.

In **Fig. 3.17**, the output current, the current of each inductor and the switching commands are reported. One can notice that the equivalent switching frequency seen by the output is doubled compared to the standard three-level topology and four times with respect to a single-phase two-level buck converter.

The current ripple behavior of two phase interleaved three-level buck is thus comparable with a four phase interleaved standard buck converter. Also the same figure shows how a converter phase experiences only a half of the total average output current.

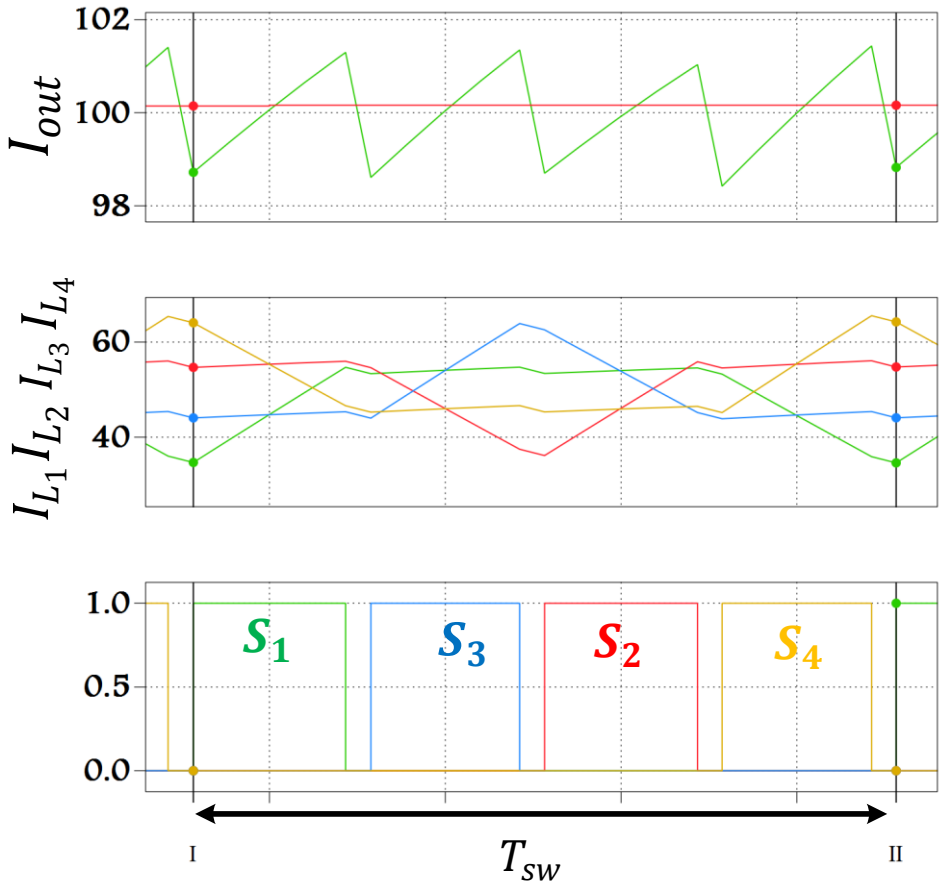


Fig. 3.17: Output current, phase currents and command signals for the proposed multiphase interleaved three-level buck topology.

3.5.1 Switching modes

In this section the operating modes and switching intervals of the proposed topology are presented and discussed. The actual case of $d < 0.25$ is considered as a practical case and extension to other operating conditions is straightforward.

A full switching period is depicted in

Fig. 3.18, where current waveforms and sub-intervals $I_1 - I_8$ are shown within a switching period T_{sw}. Each inductor current (i_{L_1}, i_{L_2}, i_{L_3}, i_{L_4}), phase current ($i_{ph_1} = i_{L_1} + i_{L_2}$, $i_{ph_2} = i_{L_3} + i_{L_4}$) and output current ($i_{out} = i_{L_1} + i_{L_4} = i_{L_3} + i_{L_2}$) are represented. One can notice that phase currents i_{ph_1} and i_{ph_2} experience ripple components at twice the frequency of a single inductor configuration. Moreover, the ripple on the output current i_{out} is at four times the switching frequency, providing the same result of a four-phase interleaved standard buck converter.

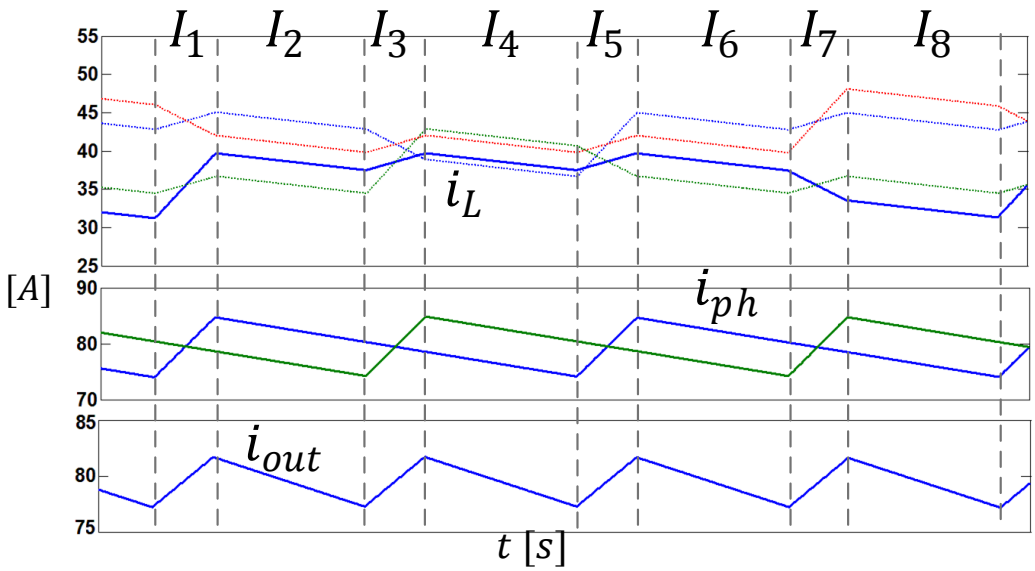


Fig. 3.18: Switching states of the proposed multiphase interleaved three-level buck converter: current waveforms and intervals during a switching period.

Within this general switching pattern five switching modes can be identified and related to the sub-intervals, as it will be discussed hereafter.

Mode 1 (charging inductor L_1)

In this switching mode switch S_1 is turned on, while S_2, S_3 and S_4 are all turned off. The equivalent circuit is shown in **Fig. 3.19**. Inductor L_1 charges at a rate determined by the following voltage:

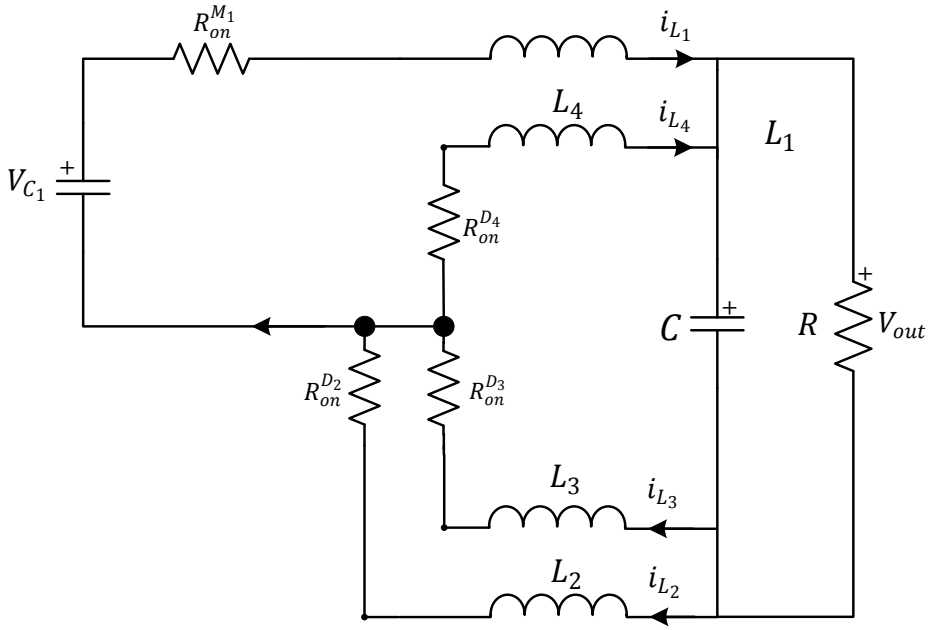


Fig. 3.19: Operating mode 1 equivalent circuit (interval 1).

$$\boldsymbol{v_{L_1} = \left(\frac{V_{dc}}{2} - V_o\right) - v_{L_2} - \left(V_{M_1} + V_d\right)} \quad \textbf{(78)}$$

where v_{L_1} and v_{L_2} are the voltages across L_1 and L_2, V_{M_1} and V_d are the voltage drops across the switch and the diode, respectively. The corresponding interval is I_1. The current i_0 flowing through the neutral point is equal to i_{L_1}.

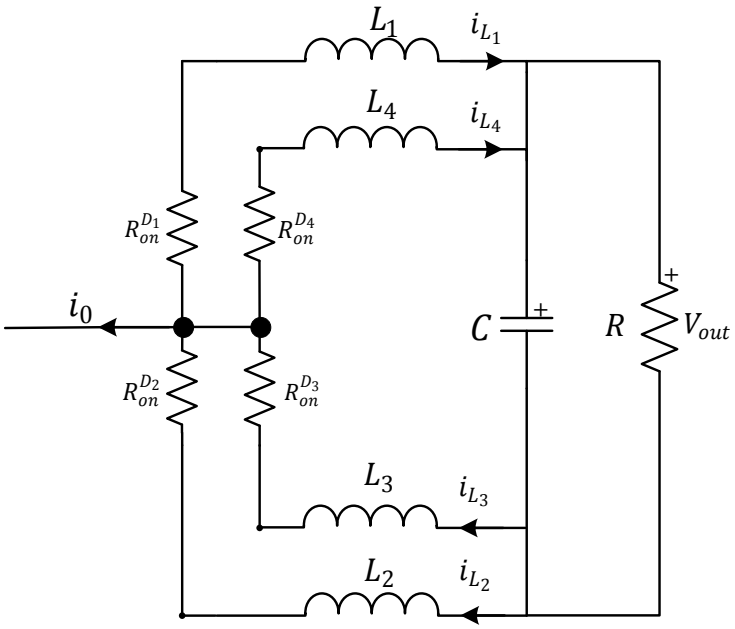


Fig. 3.20: Operating mode 2 equivalent circuit (intervals 2, 4, 6, 8).

Mode 2 (circulating inductor currents)

In mode 2 all switches are turned off (see **Fig. 3.20**) and the corresponding intervals are I_2, I_4, I_6, I_8. All inductors currents decrease with the same slope determined by the following voltage equation:

$$\boldsymbol{v_{L_1} + V_o + v_{L_2} + 2V_d = 0} \quad \textbf{(79)}$$

Mode 3 (charging inductor L_3)

In mode 3 only switch S_3 is turned on, while S_1, S_2 and S_4 are all turned off. The equivalent circuit is shown in **Fig. 3.21**. The inductor L_1 charges at a rate determined by the following voltage:

$$\boldsymbol{v_{L_1} = -v_{L_2} - V_o - 2V_d} \quad \textbf{(80)}$$

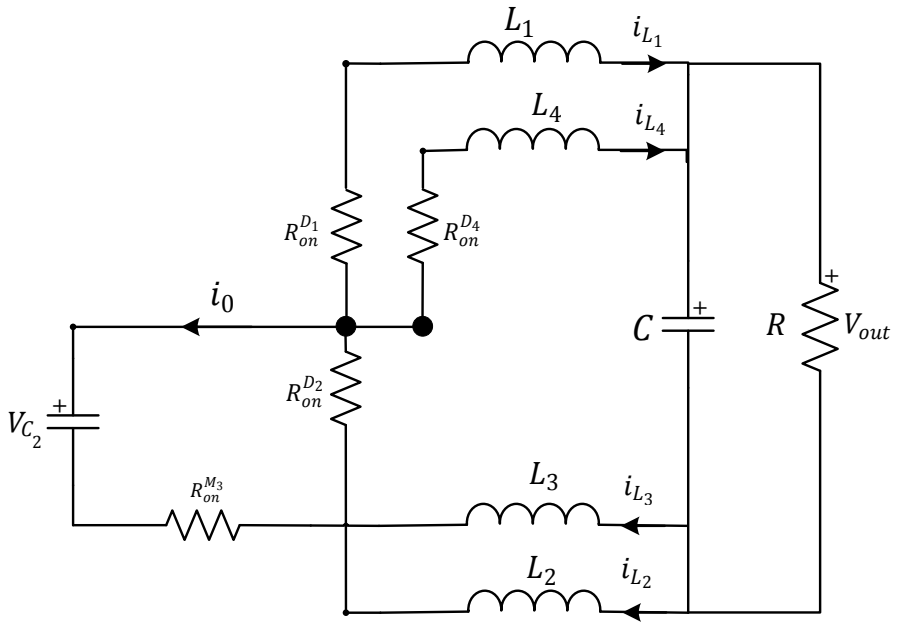


Fig. 3.21: Operating mode 3 equivalent circuit (interval 3).

The corresponding interval is I_3. The current i_0 flowing through the neutral point is equal to $-i_{L_3}$.

Mode 4 (charging inductor L_2)

In mode 4 only switch S_2 is turned on, while S_1, S_3 and S_4 are all turned off. The equivalent circuit is shown in **Fig. 3.22**. The inductor L_2 charges at a rate determined by the same voltage

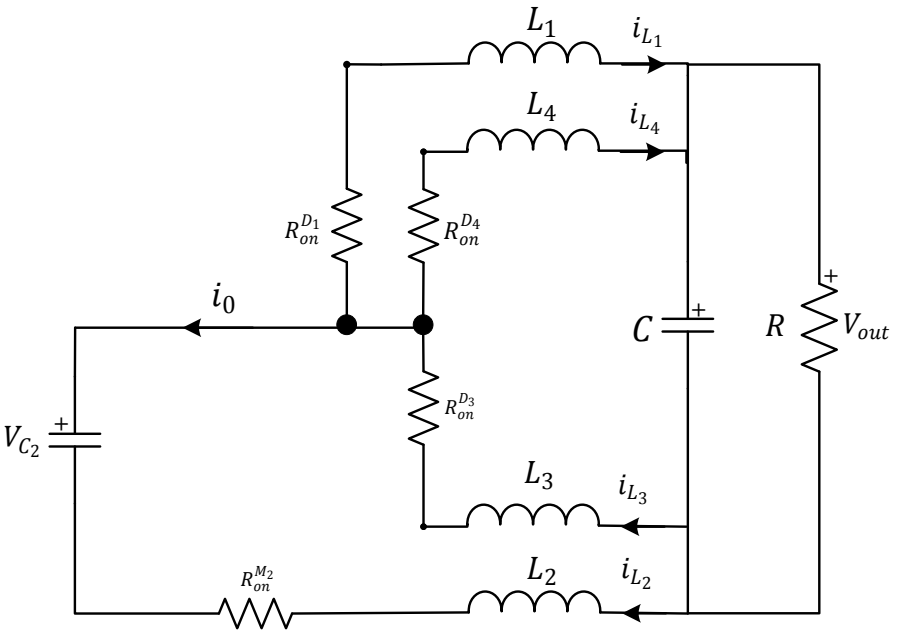


Fig. 3.22: Operating mode 4 equivalent circuit (interval 5).

of (78). The corresponding interval is I_5. The current i_0 flowing through the neutral point is equal to $-i_{L_2}$.

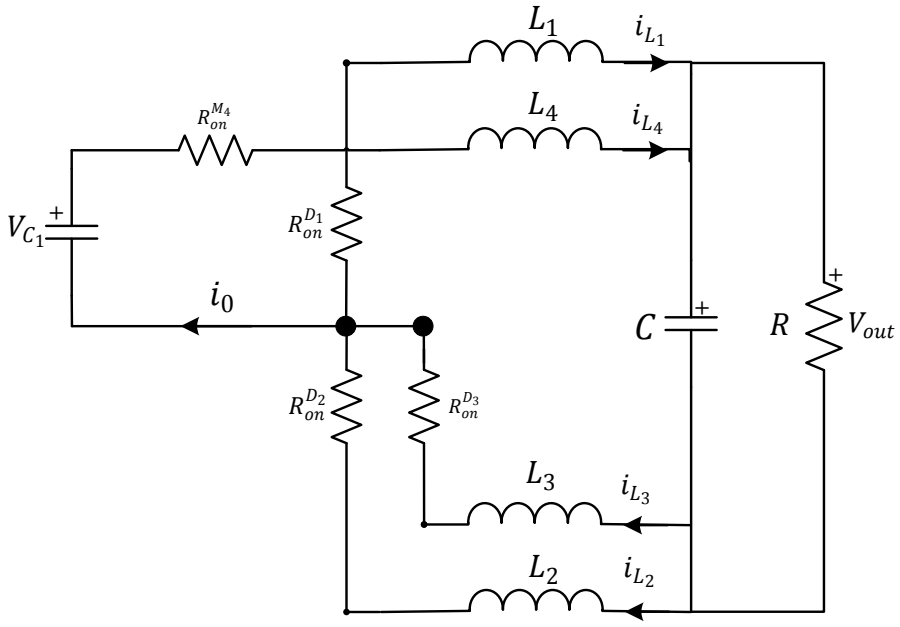


Fig. 3.23: Operating mode 5 equivalent circuit (interval 7).

Mode 5 (charging inductor L_4)

Finally, in mode 5 only switch S_4 is turned on. The equivalent circuit is shown in **Fig. 3.23**. The inductor L_4 charges at a rate determined by the same voltage of (80). The corresponding interval is I_7. The current i_0 flowing through the neutral point is equal to i_{L_4}.

3.5.2 Simulation analysis

A simulation model of the proposed multiphase interleaved NPC three-level buck converter has been implemented in the standalone PLECS tool, including conduction and switching loss models of the power devices. Main parameters of the system are reported in Appendix. Extensive simulation have been performed in order to verify the effectiveness of the proposal and to highlight the specific features of this converter, mainly phase and output current ripple reduction, nested current/voltage control scheme and current sampling issues. Finally some preliminary efficiency figures will be reported.

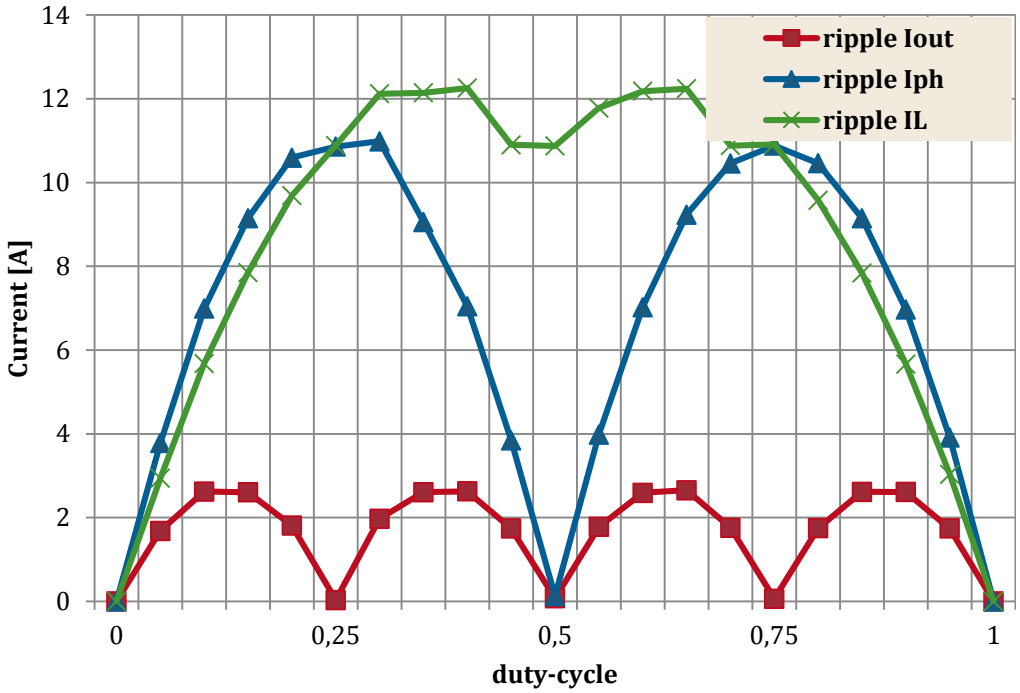


Fig. 3.24: Current ripples as a function of duty-cycle.

Phase and output current ripple reduction

The use of multiple switching devices fulfilling the same function offers a possibility to split the converter into smaller units processing a fraction of the output power. When the units operate in the so-called interleaving operation; a phase shift between their switching signals improves the operation of input and output filters.

As already shown in **Fig. 3.17**, the behavior of each inductor, phase and the output current is a function of the operating condition. A certain number of simulation case have been considered in order to prove the strong reduction of the ripple current in the output current with respect to a single phase design and as a function of the converter duty cycle. The obtained results are shown in **Fig. 3.24**. One can notice that the peak value of the output current ripple is about one fourth of the one of a single phase and it is obtained for certain values of duty cycle (i.e. $12.5\%, 37.5\%, 62.5\%, 87.5\%$).

Voltage/current control and current sampling issues

The block diagram of the average voltage/current control loops adopted to test the performance of the proposed converter is shown in **Fig. 3.25**.

Each current controller allows the regulation of one half of each phase current. The reasons behind this choice will be explained hereafter. The reference input i^* is common to both current loops, thus achieving current sharing between the two phases. Sampling of the average value of each inductor current is a strong issue for this converter, as current is not purely triangular. Therefore it is not possible to obtain the average current value by adopting a sampling instant being simply linked to the switching sequence, as it normally happens in standard converters operating in CCM. This is the reason why phase currents are considered instead. Since they are triangular with a ripple at twice the switching frequency, the average value can be simply obtained by sampling synchronously with switching period. Unfortunately this choice does not allow current sharing between each inductor, being however an issue of relatively significance.

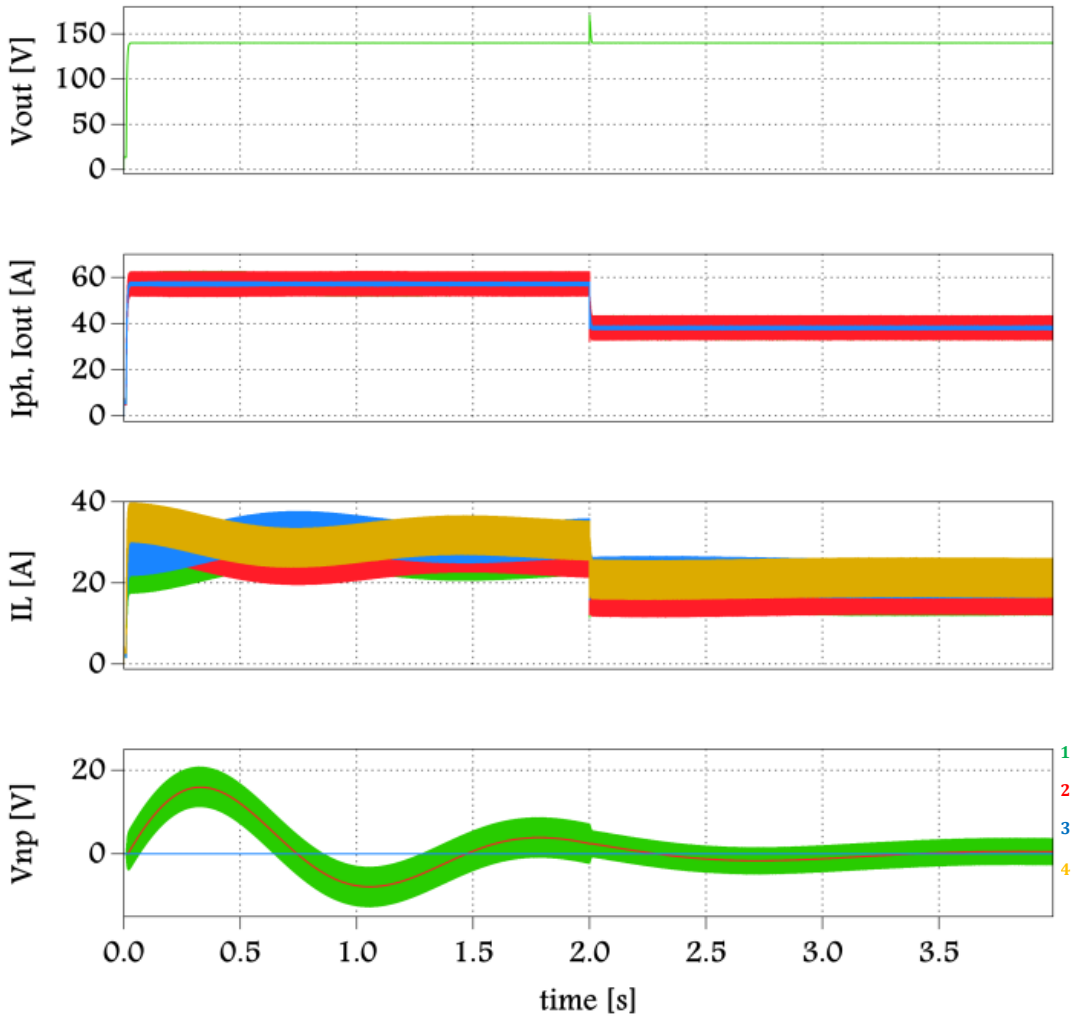


Fig. 3.25: Two-phase three-level interleaved buck average voltage/current control scheme.
Fig. 3.26: Voltage reference step from 0V to 140 V and load reduction at t = 2.

Steady-state and transient operating conditions are considered in the test results of **Fig. 3.26** and **Fig. 3.27**. A voltage reference step from zero to 140 V (d = 0.2) has been simulated under constant and varying load conditions. Output voltage, phase, output currents and inductor currents and neutral-point voltage have been reported in both cases. One can notice that the initial transient step reference voltage is properly controlled with a relatively fast dynamics. Also the ripple amplitude reduction (phase-to-inductor and output-to-phase)is clearly visible. Also the transient behavior to a load step (reduction and increase) is shown. One can notice that a damped oscillation of the neutral point voltage is reported during transient output voltage/current operating conditions. The oscillation are naturally damped in this case, as no closed loop voltage balancing scheme has been adopted. In fact the extension

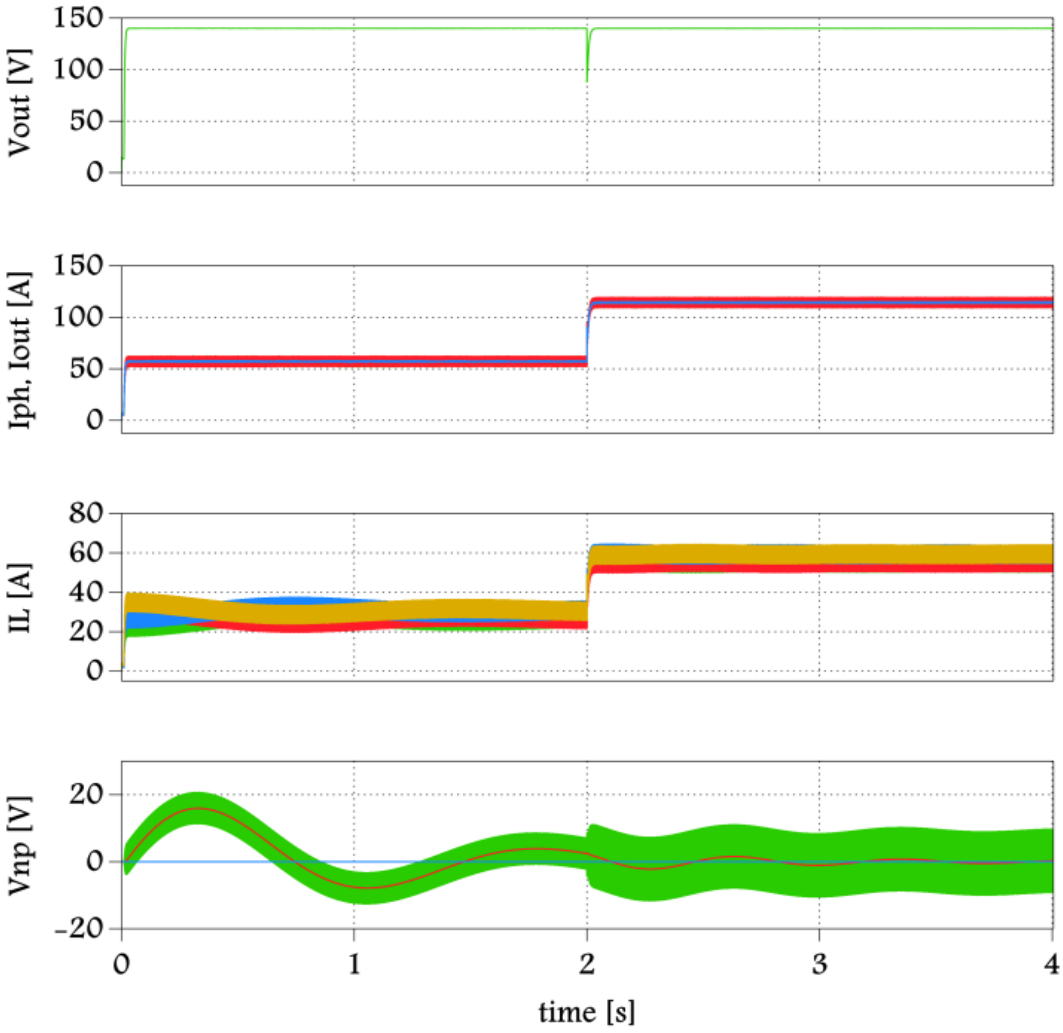


Fig. 3.27: Voltage reference step from 0V to 140 V and load increase at t = 2s.

Fig. 3.28three-level converter to multiphase topologies is not trivial and further investigations are needed, being therefore the topic of a future paper by the author of this dissertation.

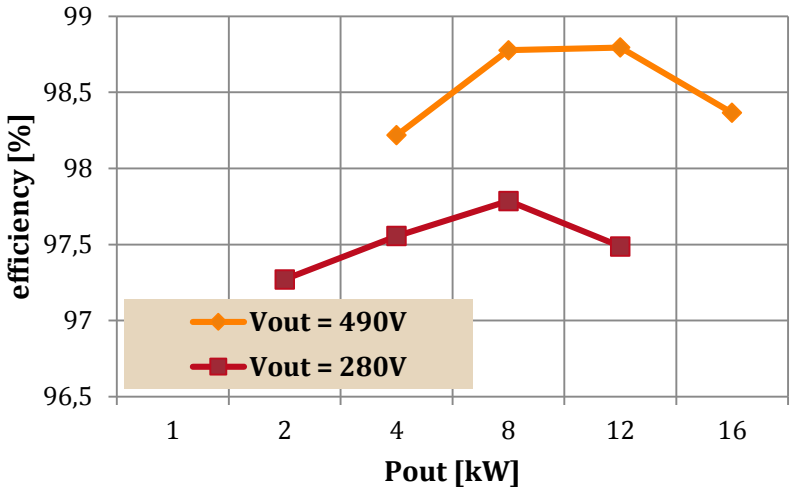


Fig. 3.28: Efficiency figures of the proposed three-level interleaved buck converter.

Efficiency maps

A set of efficiency measurements in different output power and voltage ratio operating conditions has been carried out on the simulation test bench, aiming at providing a rough idea of the performance of the proposed topology. Each switch loss has been modeled with the thermal library in PLECS, referring to the datasheet of the actual power devices. Commercial silicon carbide power MOSFETs (SCT2120AF) and diodes (SCS230AE2) have been considered. Inductor losses have been modeled using modeling tools available from magnetic manufacturers, [81]. Some results are reported in **Fig. 3.28**, where the efficiency of the proposed converter is mapped as a function of the output power and for two different values of the output voltage. Further analysis and comparisons with classical two-level interleaved topologies is quite interesting and will be the scope of future paper by the author of this dissertation.

4 BI-DIRECTIONAL CONVERTER FOR HYBRID TRACTION

4.1 Introduction

The transition from internal combustion engine (ICE) vehicles to pure electric vehicles (EVs), or hybrid electric vehicles (HEVs) is very attractive and desirable, but there are still open issues and possible optimizations to be investigated.

Hybrid electric vehicles is one of the solutions to address those issues, because the fuel economy can been improved by optimizing internal combustion engine efficiency, regenerating brake energy and shutting down ICE during the idle time. Researchers all over the world are facing several technical development areas concerning HEV components, systems and control strategies, [57]-[61]

Efficiency, lifetime, stability and volume issues has pushed the analysis of a number of bidirectional conversion solutions, both for the energy transfer to/from the storage element, [6]–[9], and to/from the electric machine side, [66], [67]. The motor drive system is constantly under frequent start/stop and high acceleration/deceleration rates. The motor drive should exhibit a high ratio of torque/inertia and power/weight, high maximum torque capability, high speed, low level of audible noise, low maintenance, small size, low weight, reasonable cost, high efficiency over low and high speed ranges and energy recovery on braking, [67].

Induction or synchronous three-phase electric machines are commonly adopted, driven by two level inverters. Recently, multilevel power converters has emerged as a technical way to improve motor drives performance, [21] [22] [66]. As already stated in Chapter 2, a clear advantage of multilevel inverters is the improved voltage waveform and lower dv/dt and common-mode voltage, leading to lower stresses on motor windings and bearings. The reduced voltage levels on power switches allow to choose among lower on-resistance devices, aiming at higher efficiency figures.

Among the three main multilevel topologies, the diode clamped inverter (NPC) topology has been found to be a suitable solution, [30]. The active version of that converter, namely the active NPC inverter, is gaining lot of attention in the last years due to the possibility of solving

one problem of the standard configuration, i.e. the unequal losses distribution among the power switches, by introducing more degrees of freedom, [21]. Associated with multilevel inverter based drives is the problem of dc bus voltage balancing, normally solved by a proper modulation strategy employing redundant configurations of power switches (see Chapter 2). Energy transfer to/from the storage element (battery, super-capacitors, and so on) is dealt by proper bi-directional dc/dc converters, [62]–[65]. Interleaving topologies and control techniques are normally employed due to a number of beneficial issues, such as the reduction of the device stress by separating power into multiple phases, reduction of the filter size by increasing the effective frequency and reduction/cancellation of current ripple effect. This last feature could also leads to other beneficial technology changes, such as the replacement of aluminum electrolytic capacitors with film or ceramic capacitors, therefore providing improvement of the equivalent series resistance, power density and reliability in a rugged thermal environment.

In this section a practical and novel solution for a hybrid traction system is described. It is based on a surface permanent magnet (SPM) synchronous motor drive supplied by a three level active neutral point clamped (ANPC) inverter and a bidirectional half-bridge interleaved converter on the battery side. Design issues, optimization (especially from the efficiency point-of-view) and advantages of the considered system architecture are analyzed through simulations with Matlab/Simulink and PLECS tools. Experimental results are based on a prototype test bench, composed by two external rotor permanent magnet synchronous machines with the same speed/torque/power rating and connected to the same shaft, intended to emulate a hybrid traction system. The drive system is controlled by multiple digital signal controllers based on a TMS320F28035 DSP.

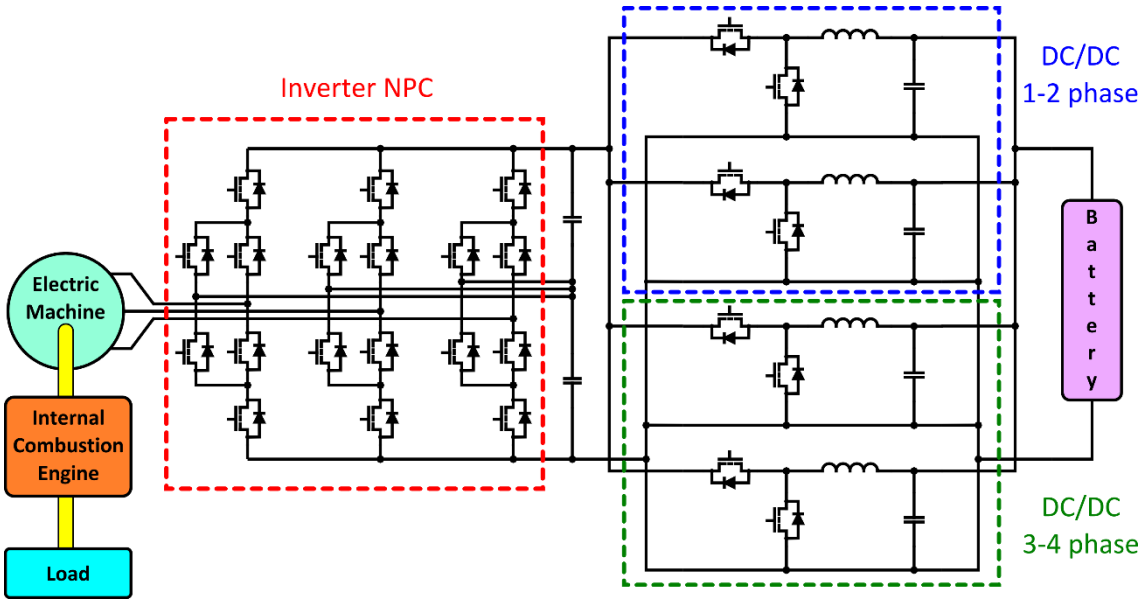


Fig. 4.1: Proposed system overview.

4.2 System overview

The proposed system architecture is a two-stage power converter controlled by digital signal controllers, as shown in **Fig. 4.1**. The electric machine is fed by a three-phase three-level active neutral point clamped inverter. The middle dc bus feeds a four-phases interleaved half-bridge converter connected to the battery pack, having two operating modes: buck and boost. In the boost mode, power is transferred from the battery to the motor drive, e.g. during startup or to provide a torque boost to the ICE. In the buck mode excess mechanical energy available at the mechanical shaft is recuperated back into the battery pack. Electric machine is driven accordingly. Indeed the proposed system can be used also as stand-alone battery charger and pure electric vehicles. The power rating of the electric machine is about 4 kW, due to the requirements of the considered application. The battery voltage level is a standard value (28 V), leading to a rated current of about 150 A. The intermediate dc bus voltage has been fixed to 150 V. Electric machine design has been optimized for the available dc bus voltage.

4.2.1 Four-phase interleaved half-bridge converter

As already shown in **Fig. 4.1** a bidirectional half-bridge interleaved converter is designed. The battery side has high current and in order reduce the Joule device losses this stage is composed by 4 phases. This is a good compromise solution between the increase of complexity/cost of the converter and its efficiency. The advantage of interleaved converter is that, for a given ripple current specification, the required inductance or the switching frequency can be lowered. Main parameters of the designed converter are shown in **Tab. 7.6**.

4.2.2 Three-phase active NPC inverter

The active NPC inverter is a variant of the standard NPC topology (described in Chapter 2), where additional active switches in anti-parallel to the clamping diodes are introduced, as depicted in **Fig. 4.1**. The additional switches make new switch states and new commutations possible compared to the standard NPC inverter. In particular they allow a specific utilization of the upper and lower path of the neutral point, thus affecting the distribution of conduction and switching losses, [12]. Therefore a mitigation of the loss distribution problem present in the standard NPC topology can be achieved and a higher power density obtained. The parameters of the ANPC converter are given in **Tab. 7.7**.

4.2.3 Electric machine

The machine used in this work is a SPM synchronous motor with 18-pole and 27-slot machine able to deliver 10 Nm of nominal torque and more than twice that as peak torque. For space saving, an outer rotor is adopted. It allows a more compact machine with a higher torque density to be obtained. In addition, a tooth-wound, in the inner stator structure, is chosen in order to reduce the copper weight and, consequently, cost and Joule losses. The whole set of the electric machine parameters are given in Tab. 7.8 and a sketch of its structure is shown in **Fig. 4.2**.

The EM constant torque loci are reported in **Fig. 4.3**, such maps have been obtained by a finite element analysis (FEM). The MTPA trajectory line is only in q-axis up to twice the nominal current, so this demonstrated the typical isotropic behavior of the SPM machine.

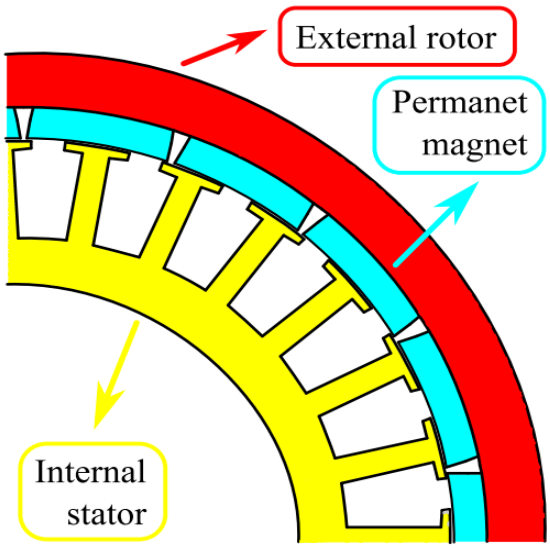


Fig. 4.2: EM lamination sketch.

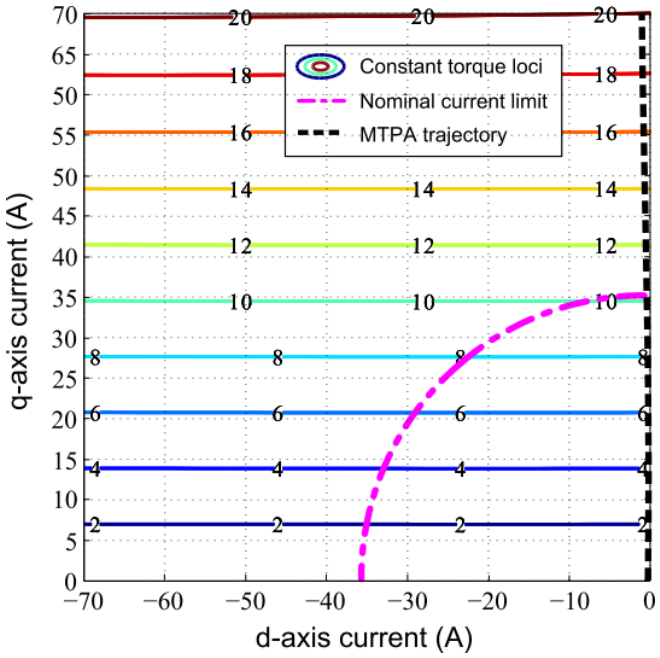


Fig. 4.3: Constant torque loci of the EM (current values are the peak ones).

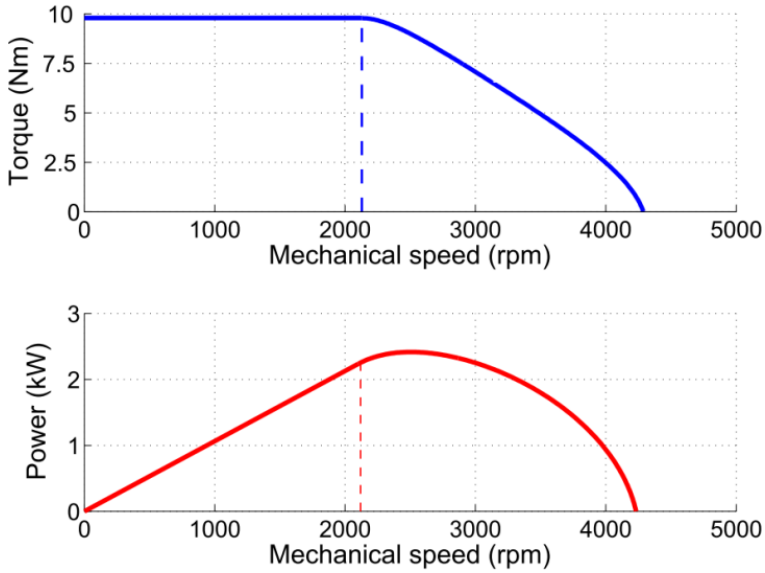


Fig. 4.4: Nominal torque and power characteristics of the EM prototype.

This electric machine is able to deliver 10 Nm of nominal torque and more than twice that as peak torque during starting-up phase of the engine. As shown in **Fig. 4.4** the maximum value of the required torque is 10 Nm at 2200 rpm and the maximum peak power is 2.5 kW at 2500 rpm.

Machine performances have been estimated with FEM analysis. The fundamental equations used for losses calculation are reported below. In particular the copper losses are:

$$P_j = 3R \cdot I^2 \qquad (81)$$

in which R is the winding phase resistance and I is the rms phase current. The iron losses are estimated by:

$$\boldsymbol{P_{iron} = P_{s,steel} \cdot \left(k_{hyst} \cdot \frac{f}{50} + k_{ecc} \cdot \frac{f^2}{50^2} \right) \left(\frac{\hat{B}}{I} \right)^2} \quad \textbf{(82)}$$

where $P_{s,steel}$ is the specific loss of the lamination steel (given at $\hat{B} = 1\,T$ and $f = 50\,Hz$) and k_{hyst}, k_{ecc} are two coefficients that indicate the contribution of hysteresis and eddy currents losses respectively. Finally the mechanical losses are calculated as:

$$\boldsymbol{P_m = kP_{out} \cdot \sqrt{n}} \quad \textbf{(83)}$$

where k is a coefficient in the interval $[0.6;\ 0.8]$, P_{out} is the mechanical power (in kW) and n is the rotor speed expressed in rpm.

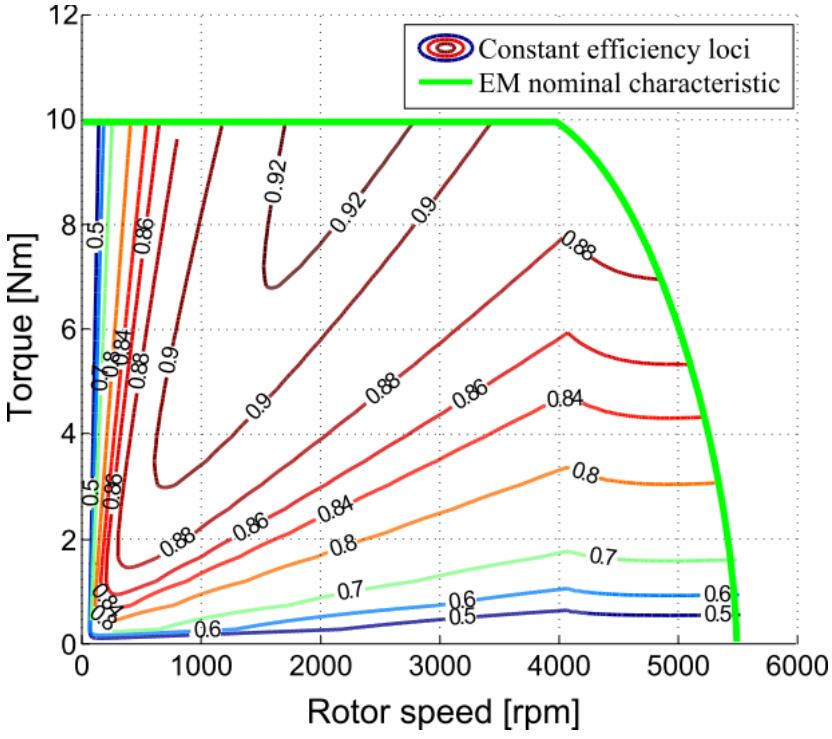


Fig. 4.5: EM efficiency map.

Therefore, from the equations **(81)-(83)** the efficiency maps, reported in **Fig. 4.5**, has been computed into the EM working regions.

The real EM working points are also drawn in order to underline the actual efficiency achieved.

4.2.4 Design choices

With ANPC converter the voltage rating of power switches is halved with respect to the two-level topology and so better performance may be expected. A search of optimal number of device in parallel has been done in order to increase the efficiency of converter. Joule losses have been reduced with the adoption of more devices in parallel but the cost of the overall converter is consequently increased. The switching losses and conduction losses in fact become a dominant factor in the total power loss for power electronics converters. A simple yet reasonably accurate method of estimating power switching losses is based on device datasheet information. The main parameters of the power switches used in this work are reported in **Tab. 7.9**. Commonly used formulae, [16], for estimating the switching losses, P_{sw}, and conduction losses P_{on} are:

$$\boldsymbol{P_{sw} = \frac{1}{2} I_d V_d (t_r + t_f) f_{sw}} \quad \textbf{(84)}$$

$$\boldsymbol{P_{sw} = R_{on} I_d} \quad \textbf{(85)}$$

where I_d and V_d is the current and the voltage of device respectively, f_{sw} is switching frequency, $t_r = t''_{rise} I_d$ the turn-on switching time and $t_f = t''_{fall} I_d$ turn-off switching time. Equations **(84)** and **(115)** have been used to calculate the total losses of ANPC inverter and DC/DC converter.

In addition to switching losses, also conduction losses in the inductors have to be taken into account. Calculation can be simply done with **(115)** and parameter in **Tab. 7.9**.

The power consumption of converter control electronics can also be included and are estimated in the worst case as 40 W when driving 3 power devices in parallel. This choice will be shown hereafter to be the optimal one. In **Fig. 4.6**-**Fig. 4.7** the loss analysis results are shown as a function of different number of power device in parallel and at two different dc bus voltage values: low, $V_{dc} = 50\ V$, and high, $V_{dc} = 150\ V$.

Both with low and high dc bus voltage, it is possible to notice that a good solution from the efficiency point-of-view is to have 3 switches in parallel.

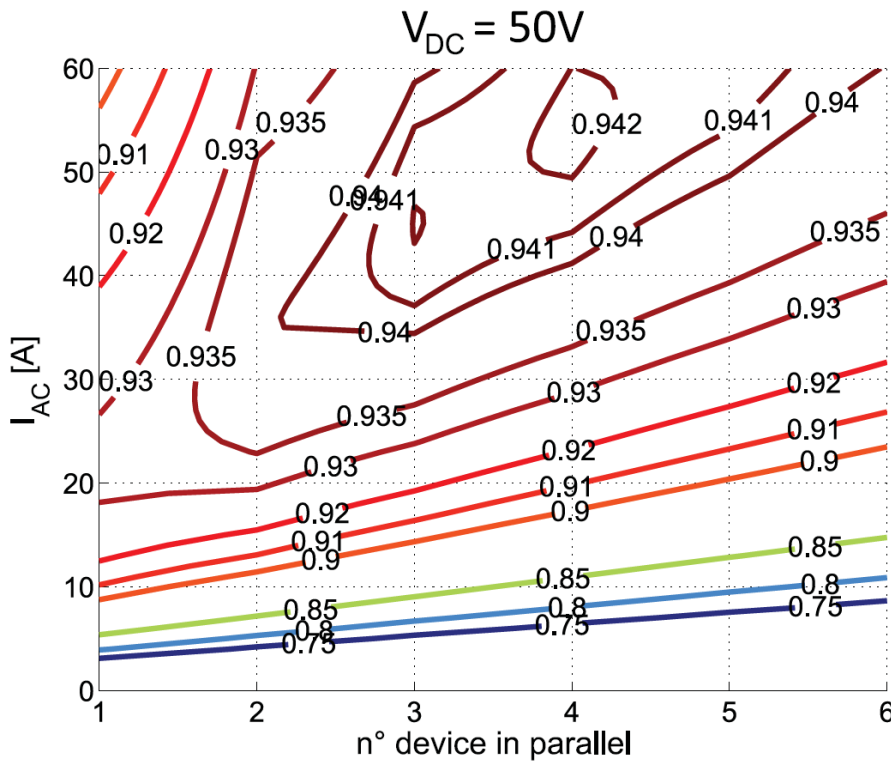


Fig. 4.6: Constant efficiency maps of total converter (DC/DC an NPC) as a function of the parallel device number with $V_{dc} = 50\ V$.

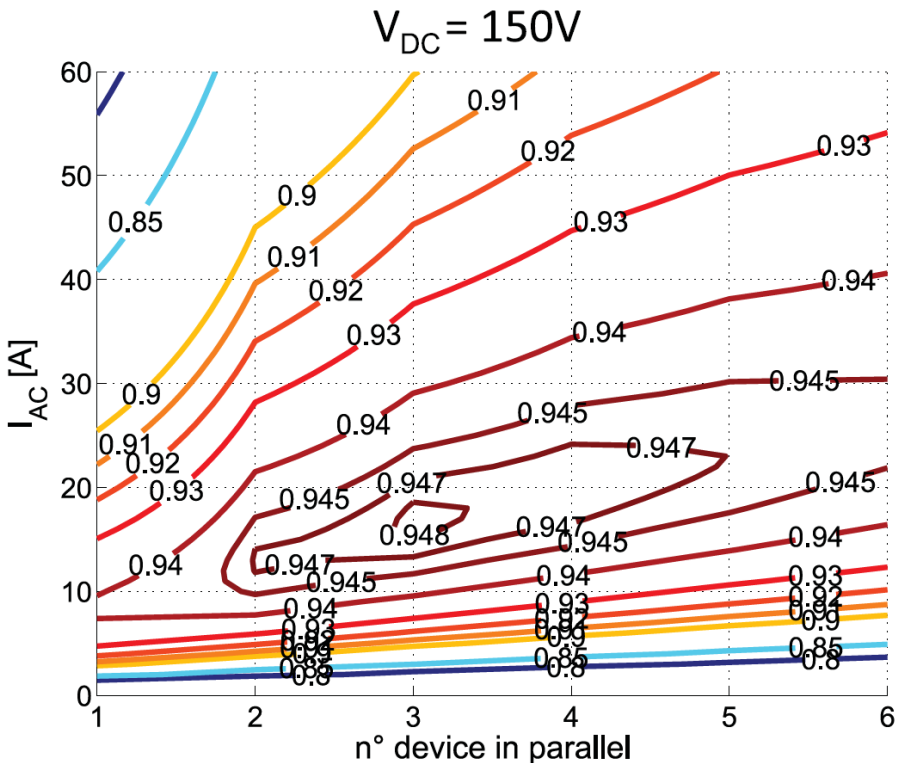


Fig. 4.7: Constant efficiency maps of the overall converter (DC/DC an NPC) as a function of the parallel device number with $V_{dc} = 150$.

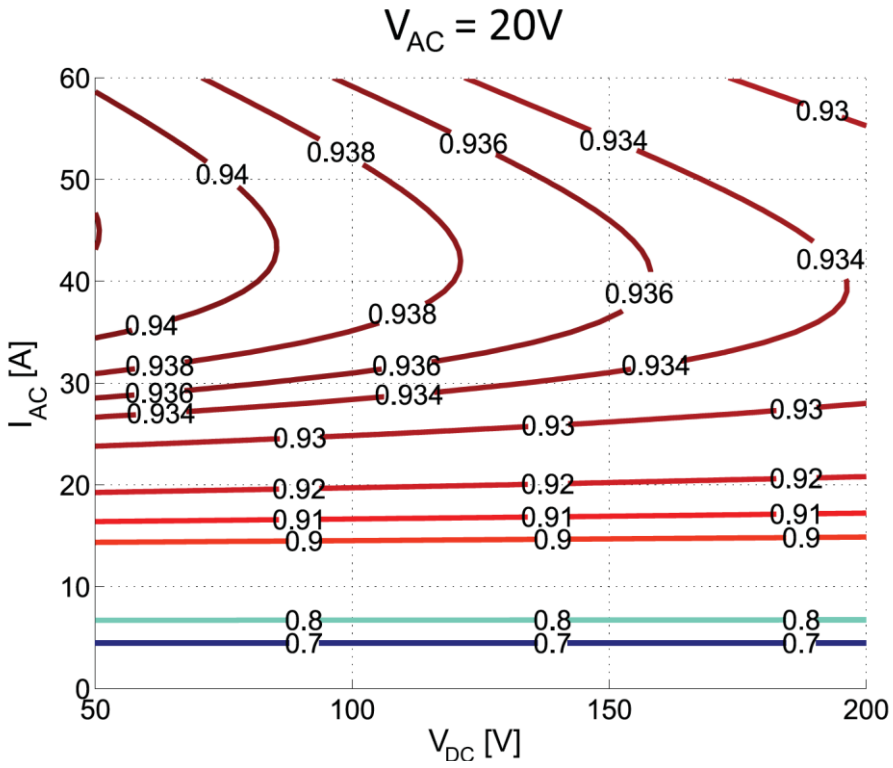


Fig. 4.8: Constant efficiency maps of the overall converter (DC/DC an NPC) as a function of the dc link voltage with $V_{ac} = 20\ V_{rms}$.

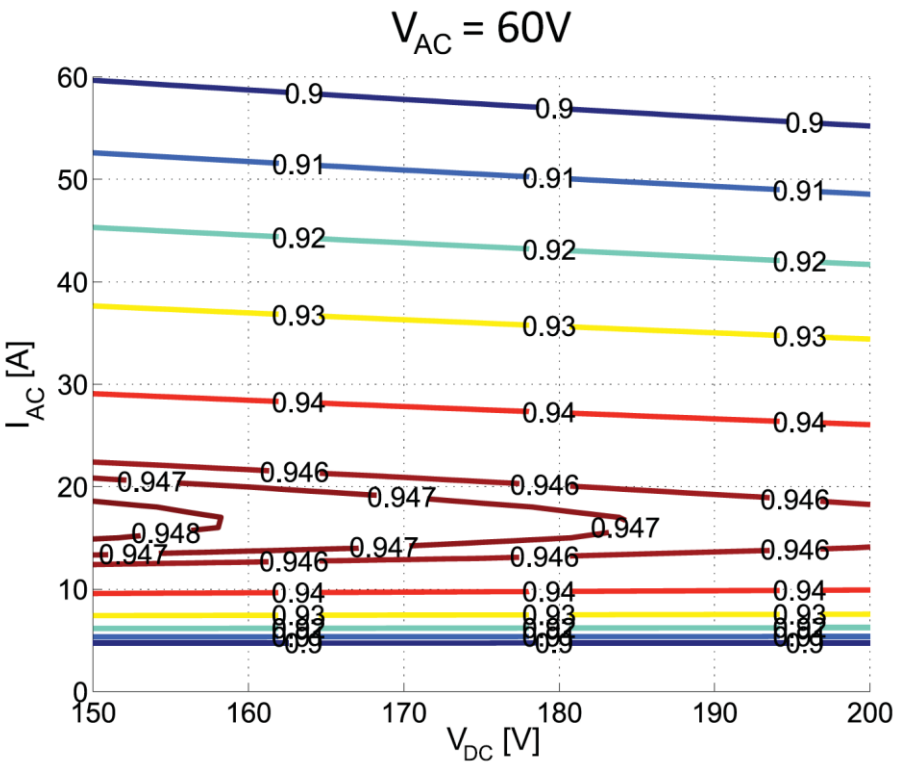


Fig. 4.9: Constant efficiency maps of the overall converter (DC/DC an NPC) as a function of the dc link voltage with $V_{ac} = 60\ V_{rms}$.

An additional efficiency analysis is carried out by considering that condition and different values of the dc bus voltage and ac inverter output voltage, i.e. low value, $V_{ac} = 20\ V_{rms}$, and high value, $V_{ac} = 60\ V_{rms}$.

The results are reported in **Fig. 4.8**-**Fig. 4.9**. With different values of the output ac voltage, i.e. at different rotor speeds, the highest efficiency is achieved with the lowest allowable value of the dc bus voltage, also considering the current level (i.e. torque) span over the rated machine conditions.

4.3 Control method

The proposed control system is equipped by three independent but interacting digital signal controllers (DSPs), one for the implementation of the electric machine and ANPC control algorithms (DSP master), and two for each two-phase interleaved DC/DC converter control (DSP slaves).

Each phase of the DC/DC converter has its current and voltage battery control (generating phase) or dc bus voltage control (motoring phase). The NPC converter has torque motor control (motoring phase) or dc bus voltage control (generating phase). The overall block diagram of the control scheme is shown in **Fig. 4.10**. The operating mode (motoring or generating) is controlled by a logical state ("G/M" in the diagram), provided by the vehicle management and control unit.

Motor Operation Mode (BOOST)

The machine is operated in motoring mode at the thermal engine starting or when torque boost is required. The DC/DC converters are operated in boost mode and dc bus voltage is controlled to the rated value, while the electric machine is speed or torque controlled.

4.3.1.1 Generator Operation Mode (BUCK)

In generating mode the (braking) torque of the electric machine is controlled in order to maintain a constant dc bus voltage, whilst the dc/dc converters are controlled in buck mode to regulate battery current. Reference battery current calculation and control of battery voltage are performed inside the"Battery Management" unit.

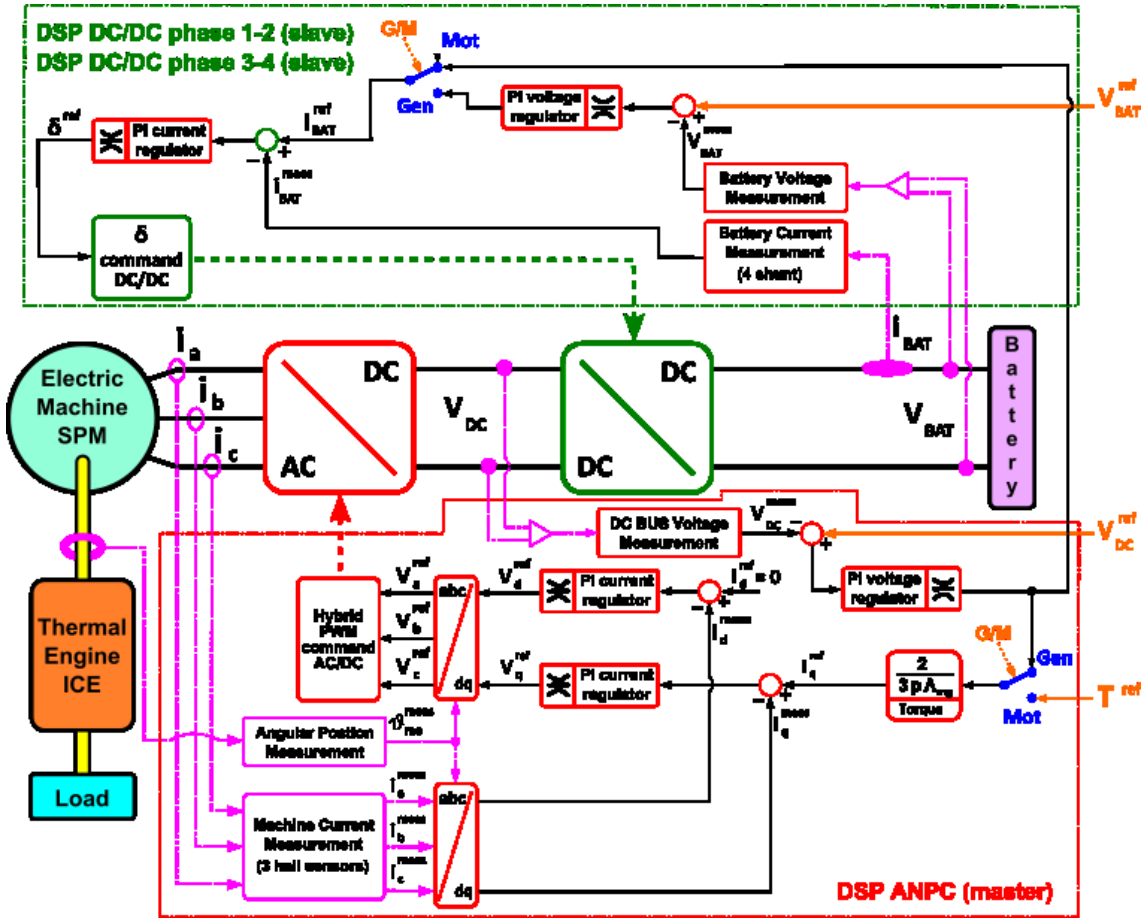


Fig. 4.10: Overall converter control scheme.

4.4 Simulation results

The simulation results reported hereafter are mainly intended to show the behavior of the hybrid system under the different operating modes. Matlab/Simulink and Plecs tools have been adopted and actual implementation constraints, such as switching level simulation of both the converters and discrete time control, have been considered in order to obtain reliable results and allow system tuning and optimization of control performance. A simple but effective torque/speed model of the thermal engine has been developed, that however does not include the torque ripple effects.

4.4.1 Dc-link pre-charge at ICE start-up

Fig. 4.11 shows the startup of the thermal engine and pre-charge of the dc bus. The thermal engine starts at $50\,rpm$ and follows its torque-speed characteristic up to $800\,rpm$. The electric machine works in generator mode, without any control as the NPC inverter control is off, and it acts therefore as a pure rectifier up to $50\,V$. The difference between electromechanical and load torque is due to friction.

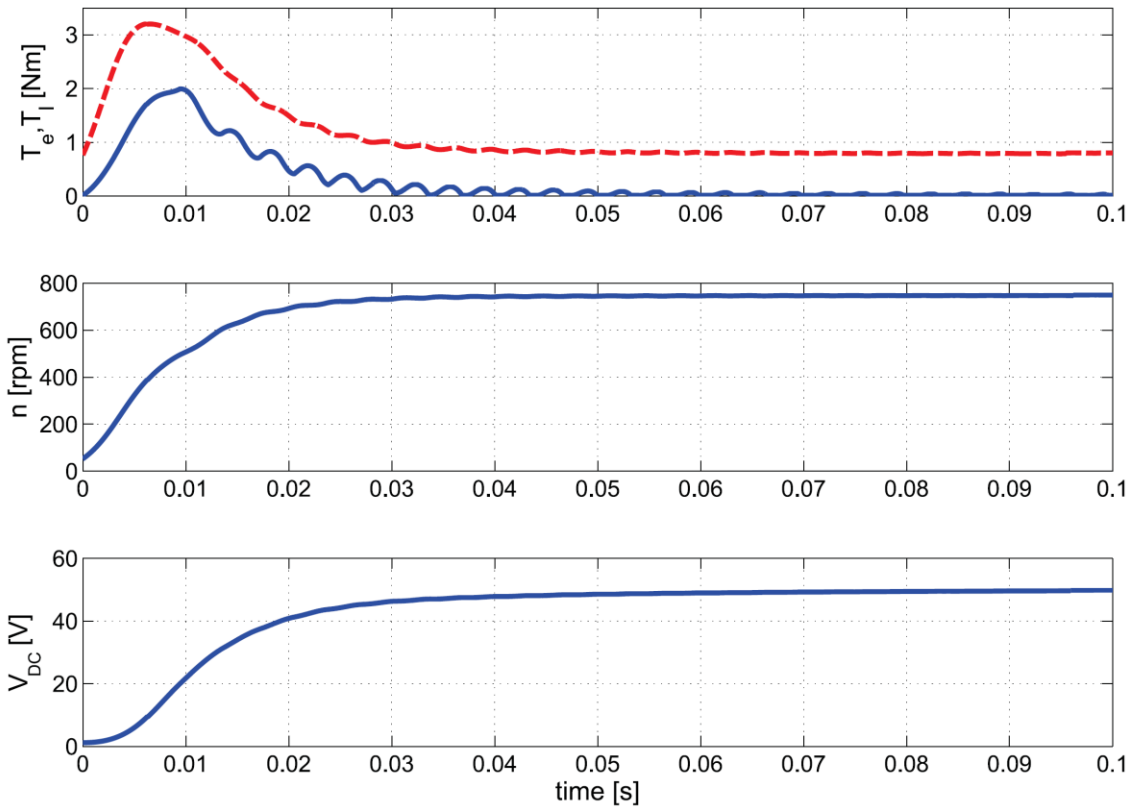


Fig. 4.11: Thermal engine start-up and pre-charge of the dc-link (electromechanical and load torque, rotor speed and dc-link voltage).

4.4.2 Dc-link charge through SPM braking

After a certain voltage level (i.e. about 30 V) the control is switched on and boosting of the dc bus voltage up to the nominal value of 150 V can be achieved by a proper control of the electric machine (braking) torque, as shown in **Fig. 4.12**. Then a power demand from the load side is simulated (battery or resistive) and the dc/dc interleaved converter works in buck mode. Motor speed follows the torque/speed characteristics of the thermal engine.

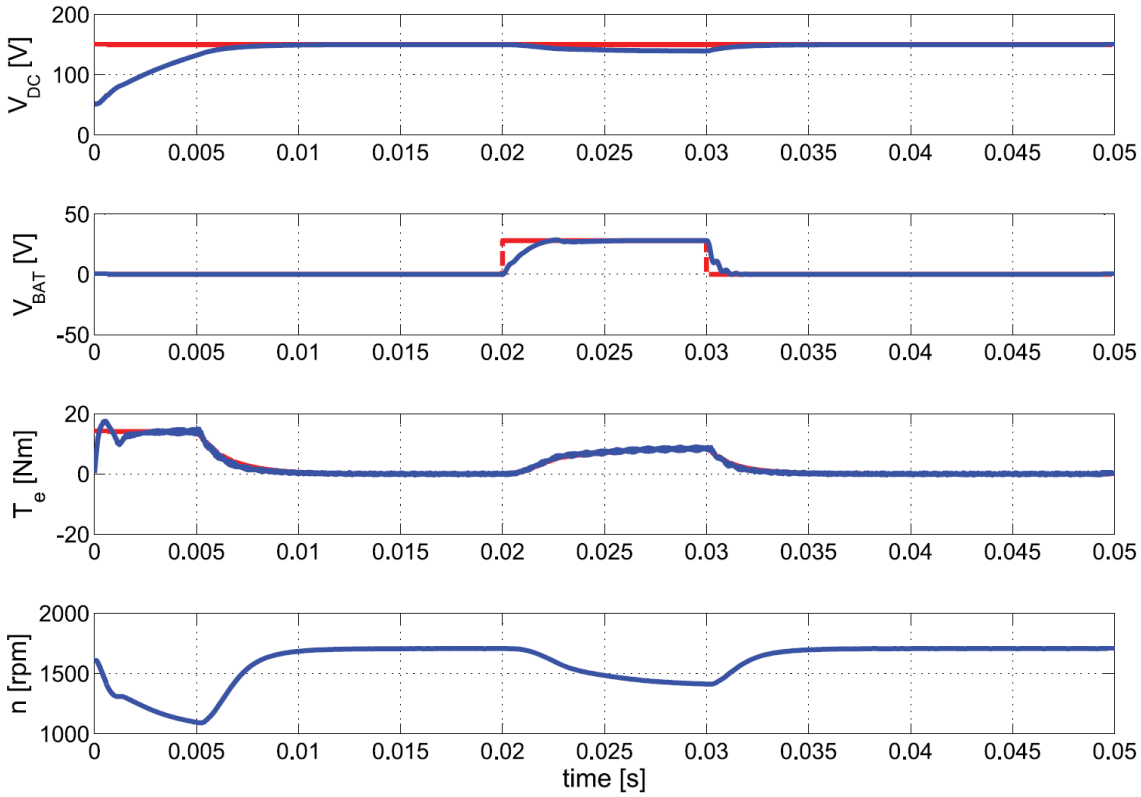


Fig. 4.12: Boosting of the dc-link and load power demand (reference and actual dc-link voltage, electromechanical torque, rotor speed).

4.4.3 Battery Charging (i.e. Control of Battery Voltage)

In **Fig. 4.13** the startup of the dc/dc converter is shown and charging of the battery considered. In the first phase, the battery voltage has a value of 25 V , simulating a low state-of- charge condition, and charges the capacitor of the output filter of the dc/dc converter, which is considered to be initially discharged. This provides a (negative) and relatively high value of the battery current. In the second phase, the battery is charged to a value of 28 V . Finally, a power demand from the load side, i.e. in parallel with the battery, is simulated. In order to reduce the simulation time, a lower value of the capacitor of the battery equivalent circuit has been considered. This is not a limiting condition as it provides a harder (higher bandwidth) requirement to the battery current control loop.

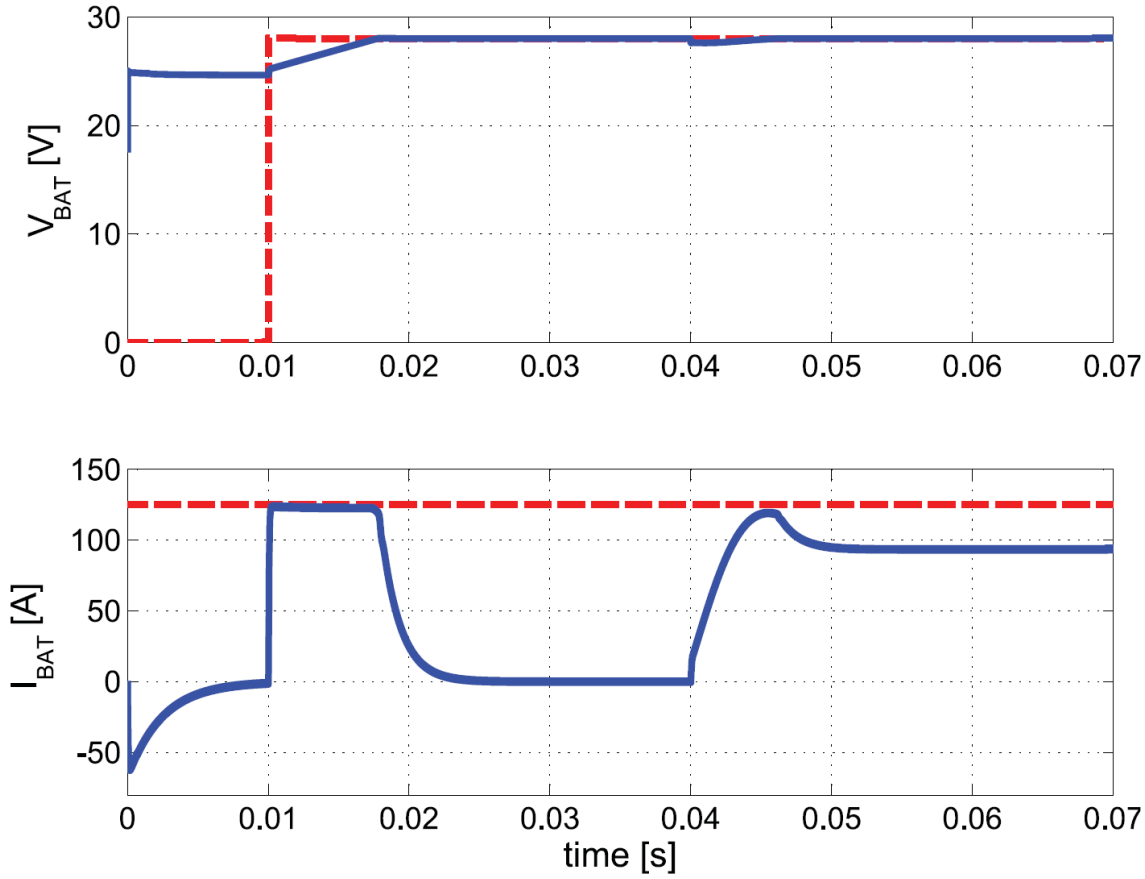


Fig. 4.13: Battery charge during buck mode (reference and actual battery voltage, limit and actual battery current).

4.4.4 Charge of dc Bus from Battery

Charging of the dc bus from battery is considered in the simulation results of **Fig. 4.14**. The battery voltage is supposed at the rated value of 28 *V* and dc/dc converter is operated in the boost mode. A resistive load is also considered in parallel to the bus capacitor, emulating the load of the electric machine during the motoring phase.

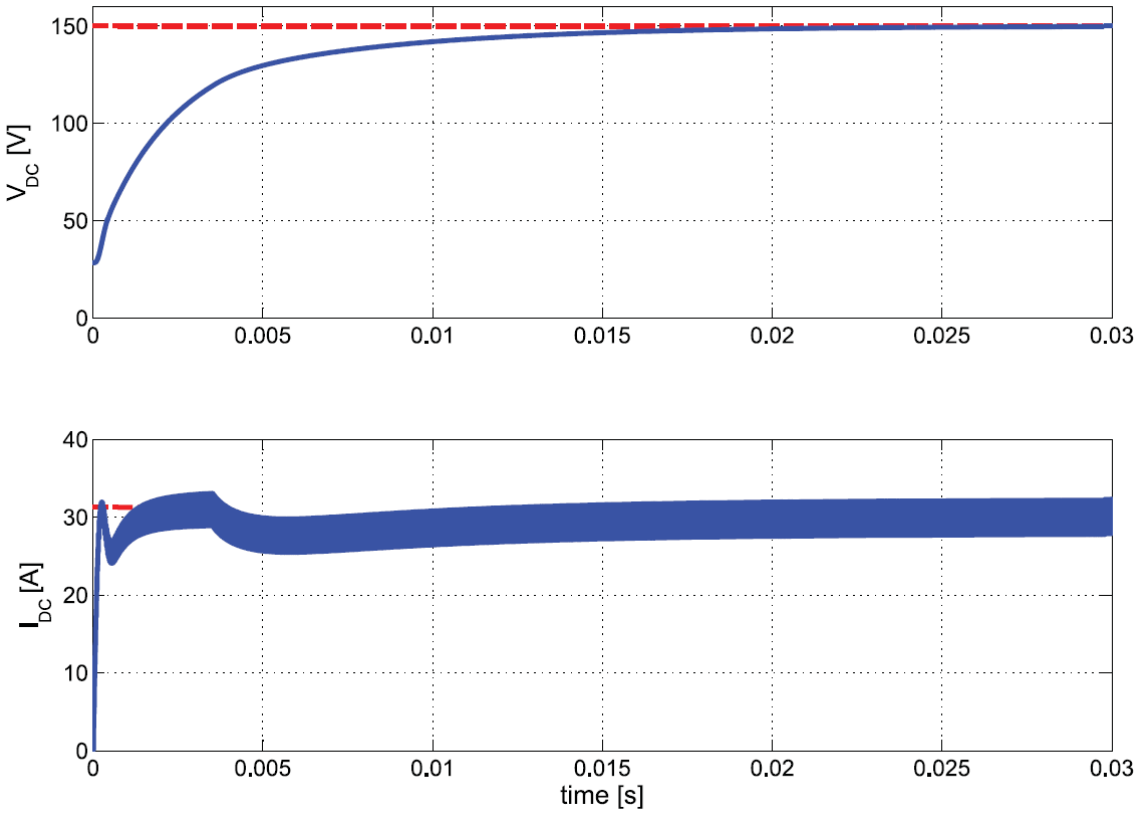


Fig. 4.14: Dc-link charge during boost mode (reference and actual dc-link voltage, limit and actual dc-link current).

4.4.5 Generator Mode of SPM Machine

The generator mode of the SPM motor is considered in the results of **Fig. 4.15**. The thermal engine is started while the electric machine torque is kept controlled to zero. After 10 *ms* the machine reference torque is raised. The typical phase-to-phase output voltage of the NPC inverter and motor phase current are shown.

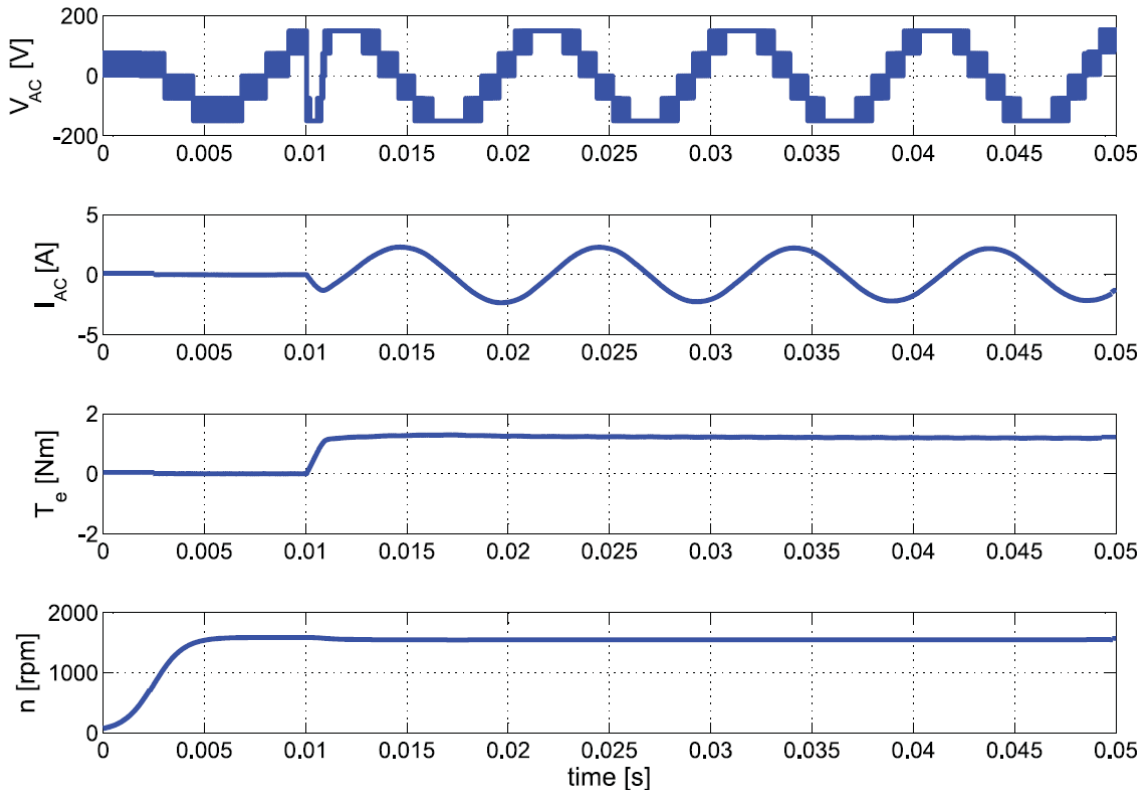


Fig. 4.15: Generator mode SPM machine (phase-to-phase voltage, phase current, electromagnetic torque, rotor speed).

4.4.6 Full Start-up of Diesel Engine from Battery Source

In Fig. 13, simulation results for a full startup performed on battery power are shown. Ignition of the ICE is achieved by means of the electric machine working in motoring mode, confirming the suitability of the system to be employed as an ISA (Integrated Starter Alternator). The dc bus is first charged, and then maintained to the reference value by the boosting dc/dc converter. The motor is speed controlled to a minimum value (according to the diesel engine minimum working speed), but a large torque feed-forward is added to the usual reference torque. In the simulation, some approximations have been made, such as the use of an arbitrary load torque (which has been experimentally acquired during an actual engine startup). The first trace on the graphs is the rotor speed, which is strictly related to the load and generated torque (second axis). The last traces show how, even with a low-capacity battery and high starting torque (thus high dc bus currents) the dc bus voltage is correctly regulated by the boost.

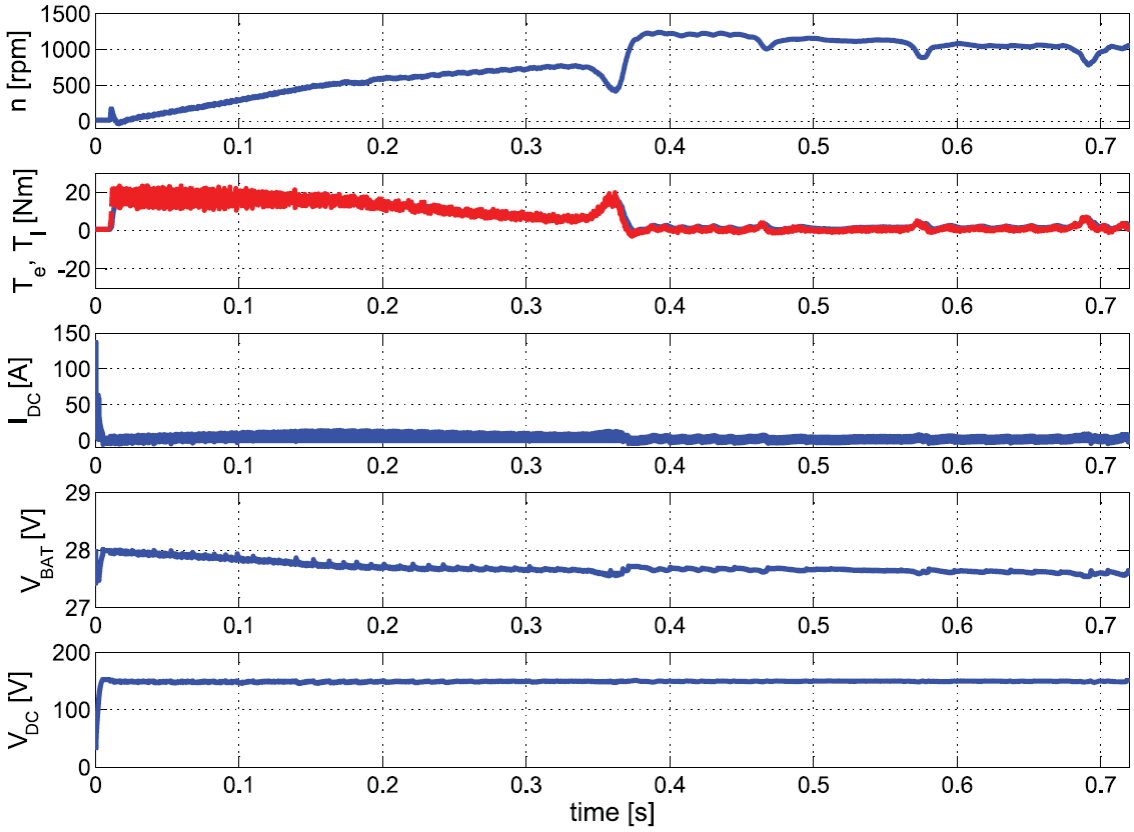


Fig. 4.16: Full start-up of diesel engine (rotor speed, electromagnetic and load torque, dc-link current, battery voltage, dc-link voltage).

4.5 Drive prototype

The electronics of the proposed drive system has been split into five electronic boards (:

- power section;
- auxiliary systems (e.g. low-power supply, gate drivers, capacitors, current sensors, etc.);
- ANPC controller (DSP master);
- two identical DCDC controllers (DSP slaves).

The power section has been realized on an insulated metal substrate (IMS) for robustness and better heating dissipation, as shown in **Fig. 4.17**. It includes all the power devices for ANPC inverter, DC/DC converters and battery inversion protection devices. Every switch of the power converters is physically realized by paralleling three devices, in order to increase the efficiency of converter, handle the high-current ratings of the low-voltage subsystem (i.e. the battery side of the converter) and allow a certain degree of overload on the electric machine side, as already discussed in section 4.2.4.

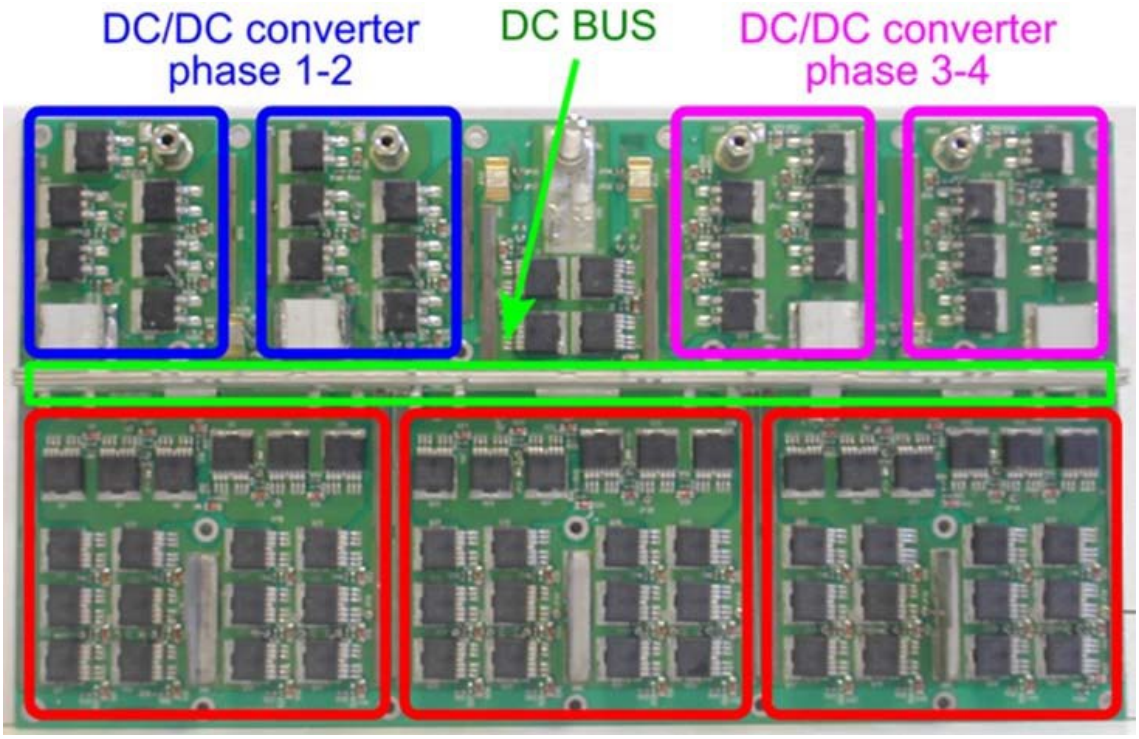


Fig. 4.17: Power board prototype.

The bidirectional half-bridge interleaved converter is composed by 4 phases, in order to split the high-current paths and allow a reduction of the total magnetic energy handled by the inductive components for a given output current ripple specification and at a given value of the switching frequency of each power device, [62]-[65].

This represents a good compromise between complexity and cost increase of the converter from one side, and efficiency from the other. Main parameters of the DC/DC converter are resumed in **Tab. 7.6**. The ANPC inverter is a derivation of the standard NPC topology, where additional active switches in anti-parallel to the clamping diodes have been introduced. The additional switches make more possible states compared to the standard NPC inverter. Particularly, they allow a specific utilization of the upper and lower path of the neutral point, thus affecting the distribution of conduction and switching losses, [21]. Therefore a mitigation of the loss distribution problem present in the standard NPC topology could be achieved. Main parameters of the ANPC converter are resumed in **Tab. 7.7.** At the moment the active feature of the converter is not used and neutral point clamping devices are always commanded in the off state, allowing only diode conduction for standard NPC operations. Further investigations will be done in the near future to exploit the benefits of active clamping feature.

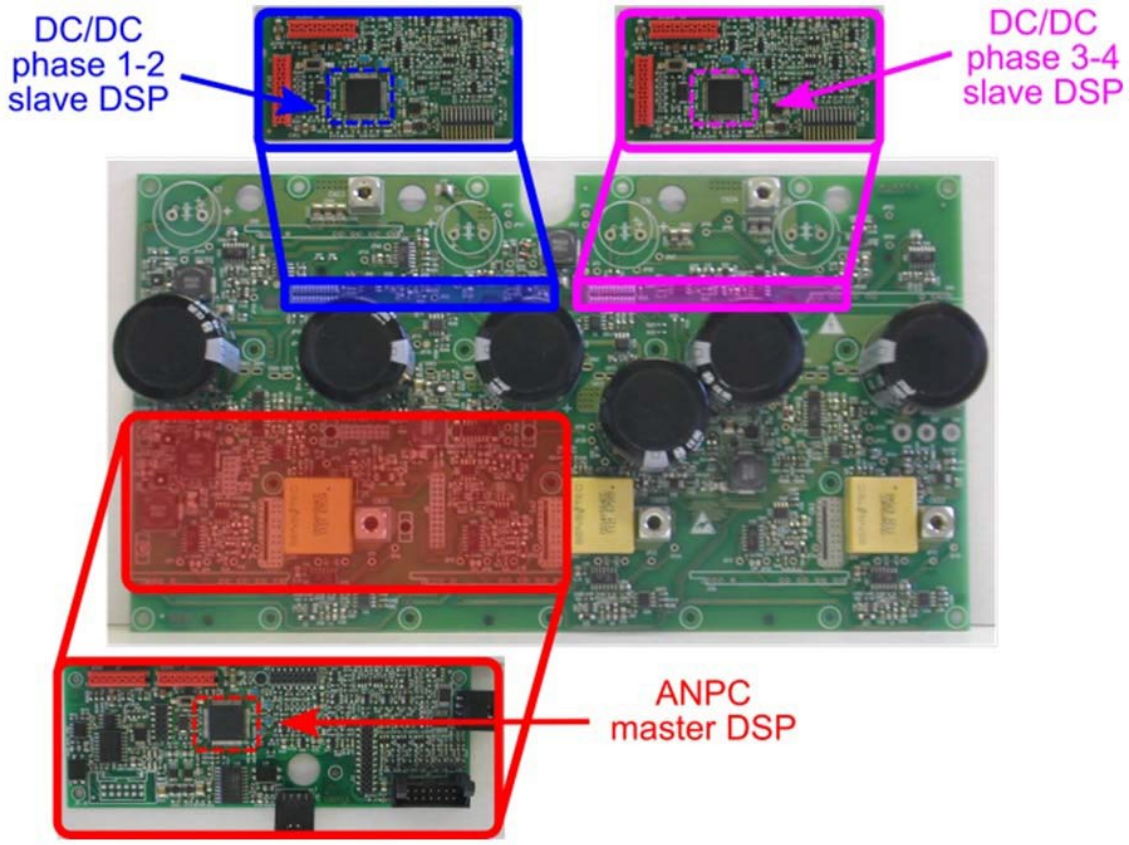


Fig. 4.18: Control sections and auxiliary board.

The control section of the proposed system is equipped by three independent but interacting digital signal controllers, i.e. TMS320F28035, one for the execution of the electric machine control algorithm and two for two-phase DC/DC control, as shown in **Fig. 4.18**. Communication among the three controllers is realized by means of I2C bus. Auxiliary systems, such as low- power supplies, dc-link and output capacitors, current sensors, and the digital controllers are hosted on a separate board, providing also interconnection with the power board (see again **Fig. 4.18**).

4.6 Experimental results

The experimental test-bench used to verify the proposal of this section is composed by two external rotor permanent magnet synchronous machines with the same speed/torque/power rating and connected to the same shaft. The first one acts as an integrated starter alternator and is fed by the three-phase three-level ANPC inverter. On the other side, the DCDC converter can be connected either to a power supply or to a battery pack. The second SPM is intended to emulate an internal combustion engine (or a constant load torque, in the proposed experiments), in order to simulate hybrid traction system, and is driven by standard drive (Gefran). A high-accuracy digital power analyzer has been adopted for input and output

power measurements on the NPC inverter. A photograph of the experimental setup is shown in **Fig. 4.19**.

Fig. 4.19: Experimental setup.

All the controllers are synchronized to the PWM generation, i.e. at 10 KHz for electric machine and 50 kHz for the interleaved DCDC converter. A hardware signal is used to provide the required phase shift of the carriers for the two slave controllers, in order to provide a real 4 phase interleaving.

The results shown in **Fig. 4.20**, **Fig. 4.21** and **Fig. 4.22** are referred to the DC/DC converter. Operation in buck and boost modes are considered in the two power flow directions. A proper resistive load is considered in the experiments. In **Fig. 4.20** transient and steady state buck mode is shown for 28 V and 25 A output voltage and current respectively. The input voltage of the dc-link is kept constant at 150 V by an auxiliary power supply. In this experiment only two phases (and one control board) are adopted. In the results of **Fig. 4.21** the same converter is operated in boost mode, having 28 V input voltage on the battery side and providing 120 V on the dc-link. Finally, in the results of **Fig. 4.22** a steady-state condition is reported showing the output phase current (including the effect of 2 phases) and the contribution of only one phase. The ripple reduction and equivalent frequency of the output current due to interleaving is clearly visible.

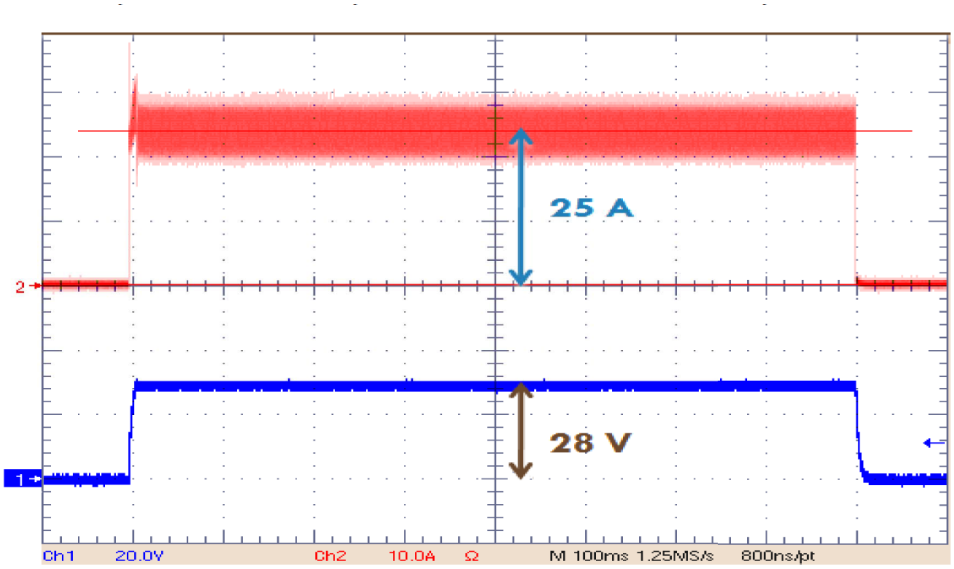


Fig. 4.20: Buck mode operation of the DC/DC converter in the case of a resistive load: current (top) and voltage (bottom).

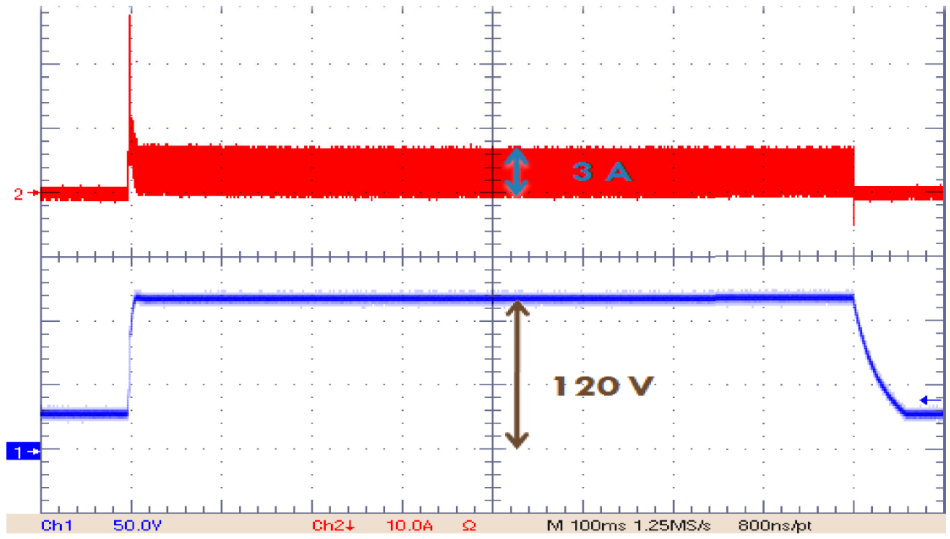


Fig. 4.21: Boost mode operation of the DC/DC converter in the case of a resistive load: current (top) and voltage (bottom).

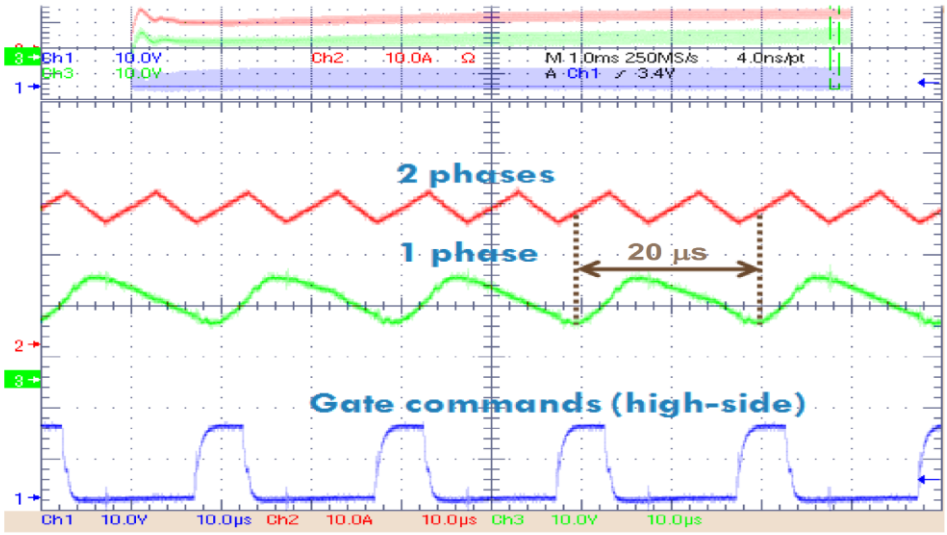


Fig. 4.22: Detail of the output current for 2-phases.

Operation of the electric machine side converter is considered in the results of **Fig. 4.23**, **Fig. 4.24** and **Fig. 4.25**. The machine works in motoring conditions and the load torque is provided by the auxiliary machine/drive already discussed.

In **Fig. 4.23** a transient speed response to a linear reference from $0{,}1\ pu$ to $0{,}25\ pu$ at no load is considered. Motor speed, actual q-axis current, motor phase a current and the ac component of the dc-link voltage are shown. The shape of the shown variables is typical, but the dynamics of the response is relatively slow due to the high inertia of the motors. One can notice that the regenerative behavior of the drive after target speed is reached, causing overvoltage of about $4\ V$ on the dc-link. Also steady-state and i_q and phase currents show that a certain friction is present.

In **Fig. 4.24** the speed response to a step load torque insertion and removal is shown at constant speed of $0{,}25\ pu$. The same variables as in the previous figure are considered. In this case system inertia causes a quite high overvoltage (about $12\ V$) during torque removal. Speed undershoot and overshoot are visible during transient operation too.

A steady-state speed condition of $0{,}25\ pu$ is considered in the results of **Fig. 4.25**, where hybrid modulating signals, motor phase a current and neutral point current i_{np} are shown. One can notice that the adoption of hybrid PWM allows a very low amplitude neutral point current with respect to a standard sinusoidal modulation.

Finally some efficiency measurements have been done on the NPC inverter in steady-state conditions as a function of speed and load torque. The results are shown in **Fig. 4.26**. The considered operating range is relatively limited with respect to the machine rated conditions

due to limitations of the experimental setup. However, the curves show that in the higher power operating range the efficiency trends are in excess of 97%.

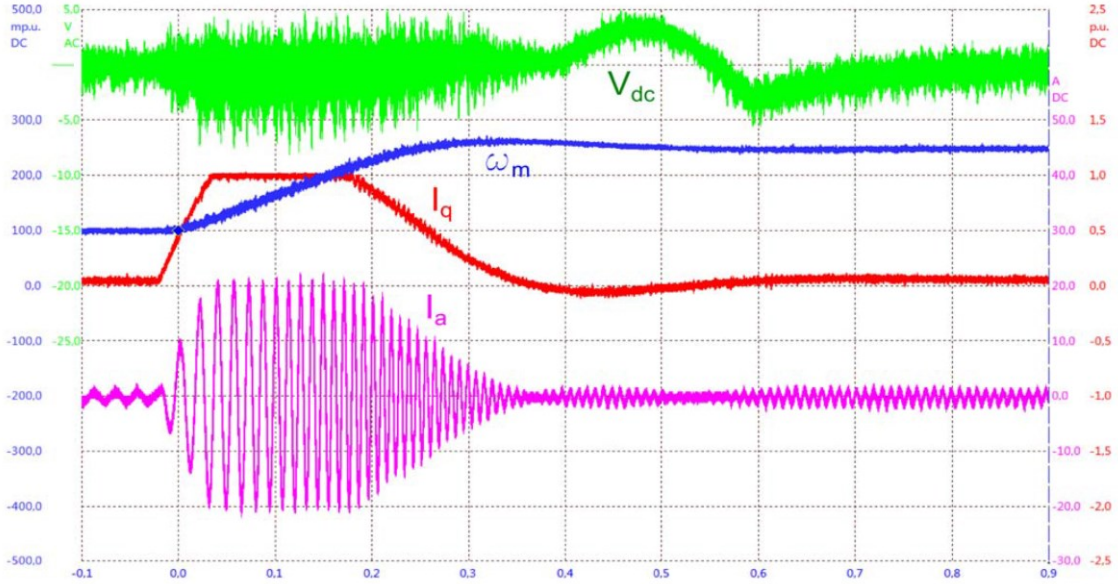


Fig. 4.23: Speed transient condition at no load: motor speed ω_m, i_q current, i_a phase current, dc-link voltage V_{dc} (ac component).

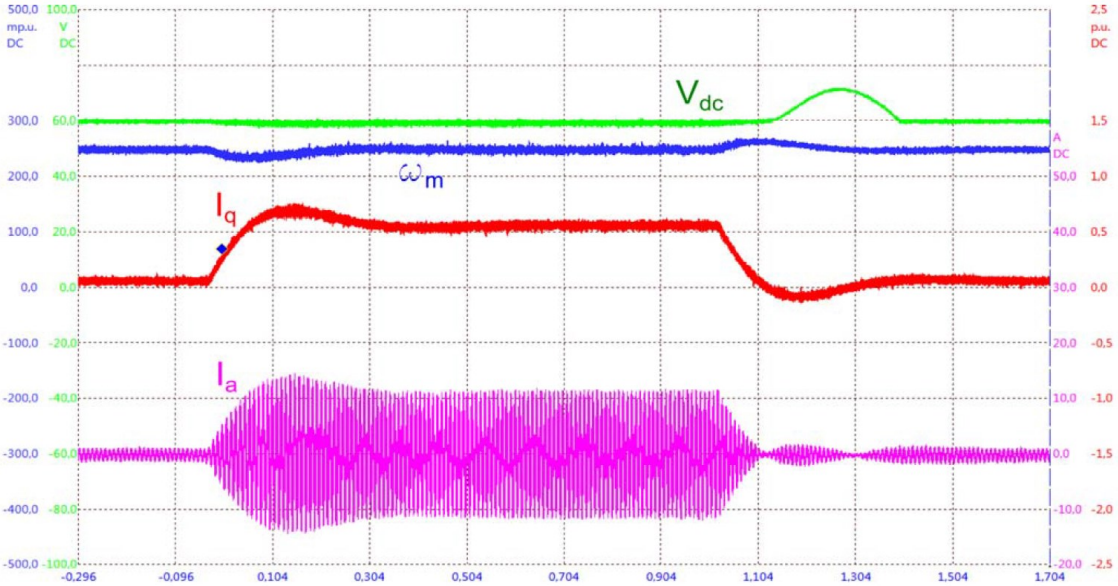


Fig. 4.24: Speed response to load torque insertion an removal: motor speed ω_m, i_q current, i_a phase current, dc-link voltage V_{dc} (ac component).

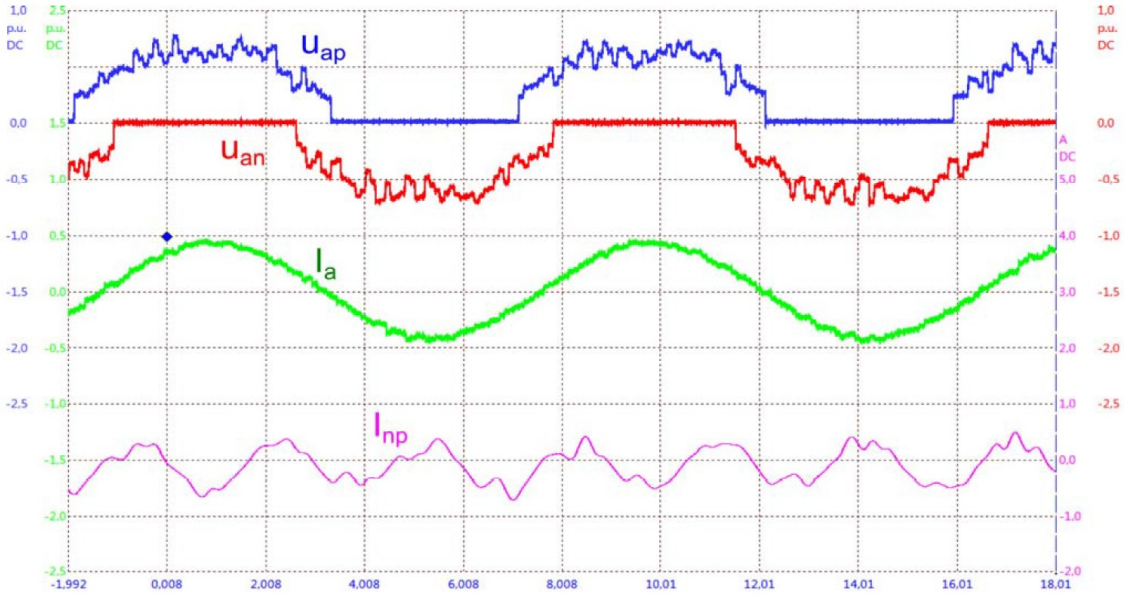


Fig. 4.25: Steady-state speed/ torque condition: modulating signals (a phase, HPWM, $D = 0,5$), phase current, NP current (1 kHz low-pass filtered).

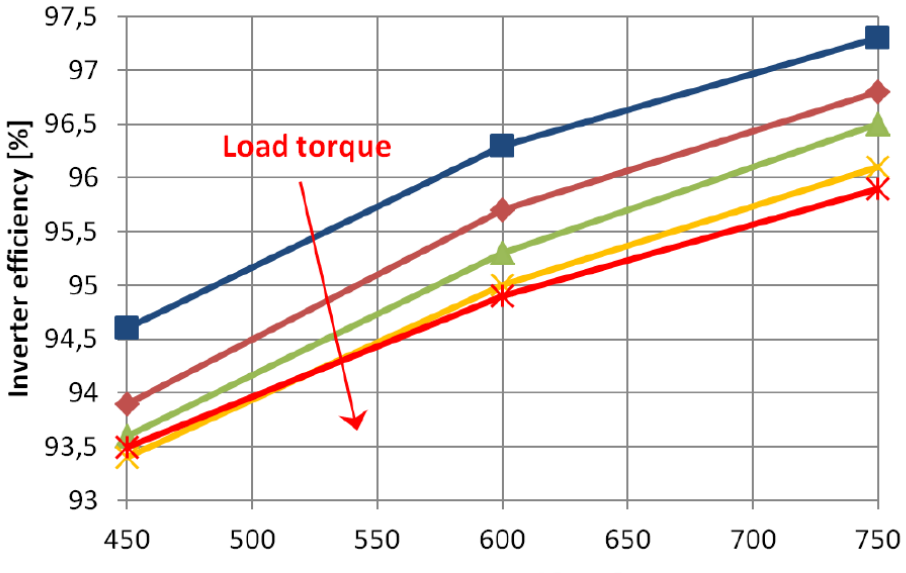


Fig. 4.26: Efficiency of NPC inverter as a function of motor speed and load.

4.7 Internal combustion engine model

In this section an effective ICE model will be described. The model of the ICE, described in detail in the next subsection and shown in **Fig. 4.27**, allows to simulate more accurately the start-up of the engine from the proposed drive system and furthermore to study the problem of the engine torque oscillation directly in simulation (section **4.8**).

The nonlinear geometry of the ICE's piston and crank mechanism has been modeled by Simulink® software using the engine fundamental kinematic equations, [69]. In **Fig. 4.27** a schematic representation of a single-cylinder four-stroke Diesel engine geometry and its basic parts are shown. The notations list used in this analysis has been reported in **Tab. 7.10.**

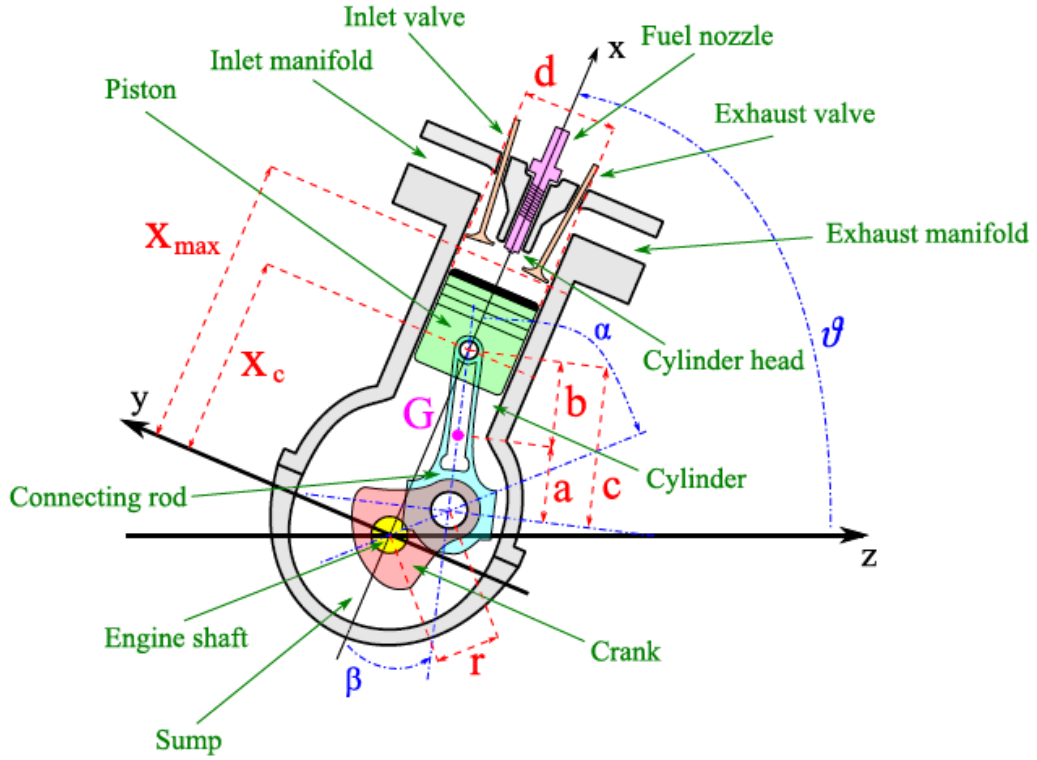


Fig. 4.27: ICE schematic model.

4.7.1 Trigonometric analysis

The kinematic analysis consists in determining the piston evolution, x_c, as function of crank angle, α. The coordinate x_c is given by the simple relation:

$$\boldsymbol{x_c(\alpha,\beta) = r\,cos(\alpha) + c\,cos(\beta)} \qquad \textbf{(86)}$$

and with assumption that $r\cos(\alpha) = c\cos(\beta)$ it is possible to simplify equation (86) in:

$$\boldsymbol{x_c(\alpha) = r\,cos(\alpha) + c\sqrt{1 - \frac{r^2}{c^2}sin(\alpha)^2}} \qquad \textbf{(87)}$$

notation $x_c(\alpha)$ highlights that this variable depends on the angle α. The speed of the connecting rod has been obtained from differentiating $x_c(\alpha)$ as a function of time:

$$\dot{x}_c(\alpha) = \left(-r\,sin(\alpha) - \frac{r^2\,sin(\alpha)\,cos(\alpha)}{\sqrt{c^2 - r^2\,cos(\alpha)}}\right)\dot{\alpha} \tag{88}$$

differentiating further $\dot{x}_c(\alpha)$ the acceleration of the piston is obtained:

$$\ddot{x}_c(\alpha) = -\left[\frac{r^2(2c^2\,cos(\alpha)^2 + r^2\,sin(\alpha)^4 - c^2)}{(c^2 - r^2\,sin(\alpha)^2)} + r\,cos(\alpha)\right]\dot{\alpha}^2 + \frac{x_c}{\alpha}\ddot{\alpha} \tag{89}$$

for different values of α, the mass center of the connecting rod changes along the x-axis, indicated with $x_G(\alpha)$, and along the y-axis, indicated with $y_G(\alpha)$. This point forms an angle with respect to the x-axis called σ, that is equal to the opposite of the angle β.

$$\sigma(\alpha) = -sin^{-1}\left(\frac{r}{c}sin(\alpha)\right) \tag{90}$$

The first and second derivatives of $\sigma(\alpha)$ are described in the following equations:

$$\dot{\sigma}(\alpha) = -\frac{\frac{r}{c}cos(\alpha)}{\sqrt{1 - \frac{r}{c}sin(\alpha)^2}}\dot{\alpha} \tag{91}$$

$$\ddot{\sigma}(\alpha) = \left[\frac{\frac{r}{c}sin(\alpha)\sqrt{1 - \frac{r}{c}sin(\alpha)^2}}{1 - \left(\frac{r}{c}sin(\alpha)\right)^2} - \frac{\frac{r^2\,sin(\alpha)\,cos(\alpha)^2}{c\sqrt{c^2 - r^2\,sin(\alpha)^2}}}{1 - \left(\frac{r}{c}sin(\alpha)\right)^2}\right]\dot{\alpha}^2 + \frac{\dot{\sigma}}{\dot{\alpha}}\ddot{\alpha} \tag{92}$$

The x-coordinate dynamics of point G is:

$$x_G(\alpha) = r\,cos(\alpha) + a\,cos(\alpha) = cos(\alpha) + a\sqrt{1 - \left(\frac{r}{c}sin(\alpha)\right)^2} \tag{93}$$

$$\dot{x}_G(\alpha) = -\left[a\frac{r^2}{c^2}\frac{cos(\alpha)\,sin(\alpha)}{\sqrt{1 - \left(\frac{r}{c}sin(\alpha)\right)^2}} + r\,sin(\alpha)\right]\dot{\alpha} \tag{94}$$

$$\ddot{x}_G(\alpha) = -\left[ar^2\,\frac{2c^2\,cos(\alpha)^2 + r^2\,sin(\alpha)^4 - c^2}{\sqrt{1 - \left(\frac{r}{c}sin(\alpha)\right)^2}} + r\,cos(\alpha)\right]\dot{\alpha}^2 + \frac{\dot{x}_G}{\dot{\alpha}}\ddot{\alpha} \tag{95}$$

Similarly, the y-coordinate dynamics of point G is:

$$y_G = b\frac{r}{c}sin(\alpha) \tag{96}$$

$$\dot{y}_G = b\frac{r}{c}cos(\alpha)\,\dot{\alpha} \tag{97}$$

$$\ddot{y}_G = b\frac{r}{c}[-sin(\alpha)\,\dot{\alpha}^2 + cos(\alpha)\,\ddot{\alpha}] \tag{98}$$

4.7.2 Dynamic analysis

The acting force on the piston due to the cylinder internal pressure, F_p, is defined as:

$$F_p = (P_i - P_{atm})\pi\left(\frac{d}{2}\right)^2 \tag{99}$$

where P_i is the internal cylinder pressure and P_{atm} is the atmospheric pressure. The gravitational force due to the piston weight, F_{m_p}, is:

$$F_{m_p} = m_p g\, cos\left(\theta - \frac{\pi}{2}\right) \tag{100}$$

where m_p is the piston mass and g is the gravitational acceleration. The system kinetic energy is given by the sum of two components due to the translations and the rotations of the various rigid bodies of the engine. The analyzed engine can be considered as a system with a single degree of freedom and so it may be reduced like a system constituted by a single rotating component. The parameters that describe the new reduced system are called reduced torque M^*, and reduced inertia I^*. The system power, P, can be expressed by the following relation:

$$P = M^*\dot{\alpha} \tag{101}$$

that is equal to the sum of the power generated by the forces applied to the system itself:

$$P = M_{ext}\dot{\alpha} - F_p\dot{x}_c - F_{m_p}\dot{x}_c - P_{cr_{ort}}\dot{y}_G - P_{cr_{paral}}\dot{x}_G \tag{102}$$

where M_{ext} is the external torque applied to the crank, $P_{cr_{ort}} = m_{cr}g\cos(\theta)$ and $P_{cr_{paral}} = m_{cr}g\sin(\theta)$ are respectively the y-axis and x-axis components of the connecting rod weight force (with mass m_{cr}). From equations (101) and (102) it is possible to obtain the equation of the torque M:

$$M^* = \frac{P}{\dot{\alpha}} = M_{ext} - F_p\frac{\dot{x}_c}{\dot{\alpha}} - F_{m_p}\frac{\dot{x}_c}{\dot{\alpha}} - P_{cr_{ort}}\frac{\dot{y}_G}{\dot{\alpha}} - P_{cr_{ort}}\frac{\dot{x}_G}{\dot{\alpha}} \tag{103}$$

Indicating with $\tau = \frac{\dot{x}}{\dot{\alpha}}$ the ratio between the two speeds it is possible to compute the mechanism torque:

$$M_{mec} = F_p \tau_{x_c} + F_{m_p} \tau_{x_c} + P_{cr_{ort}} \tau_{y_G} + P_{cr_{ort}} \tau_{x_G} \quad (104)$$

The total kinetic energy is given by the following relation:

$$E_c = \frac{1}{2} I^* \dot{\alpha}^2 = \frac{1}{2} m_p \dot{x}_c^2 + \frac{1}{2} I_m \dot{\alpha}^2 + \frac{1}{2} m_{cr} \dot{x}_G^2 + \frac{1}{2} m_{cr} \dot{y}_G^2 + \frac{1}{2} I_{cr} \dot{\sigma}^2 \quad (105)$$

where I_{cr} is the connecting rod inertia (which rotation axis passes through its mass center) and I_m is the inertia given by the sum of the crank, the flywheel and the crankshaft. In equation **(105)** the connecting rod kinetic energy has been computed with the second theorem of Konig. From equation **(105)** and using the definition of τ, the relation between the reduced inertia and the angle α is obtained:

$$I^* = \frac{2E_c}{\dot{\alpha}^2} = m_p \tau_{x_c}^2 + I_m + m_{cr} \tau_{x_G}^2 + I_{cr} \tau_\sigma^2 \quad (106)$$

The power system, P has been calculated by following equation:

$$P = \frac{dE_c}{dt} = \frac{d\left(\frac{1}{2} I^* \dot{\alpha}^2\right)}{dt} + B\dot{\alpha}^2 = M^* \dot{\alpha} \quad (107)$$

where B is friction coefficient of the engine and it is assumed constant in this analysis, so M^* becomes:

$$M^* = \frac{P}{\dot{\alpha}} = \frac{1}{2} \frac{dI^*}{dt} \dot{\alpha}^2 + I^* \ddot{\alpha} + B\dot{\alpha} \quad (108)$$

where:

$$\frac{1}{2} \frac{dI^*}{dt} = m_{cr} \frac{d\tau_{x_G}}{d\alpha} \tau_{x_G} + m_{cr} \frac{d\tau_{y_G}}{d\alpha} \tau_{y_G} + I_{cr} \frac{d\tau_\sigma}{d\alpha} \tau_\sigma + m_p \frac{d\tau_{x_c}}{d\alpha} \tau_{x_c} \quad (109)$$

Equating equations (5.19) and (5.23) the following fundamental equation has been obtained:

$$M_{ext} - M_{mecc} = \frac{1}{2} \frac{dI^*}{dt} \dot{\alpha}^2 + I^* \ddot{\alpha} + B\dot{\alpha} \quad (110)$$

4.7.3 Model implementation in simulation

Using the mathematical relationships described above, an analytical model of the single cylinder diesel engine has been modeled inside PLECS standalone software, as shown in **Fig. 4.28**.

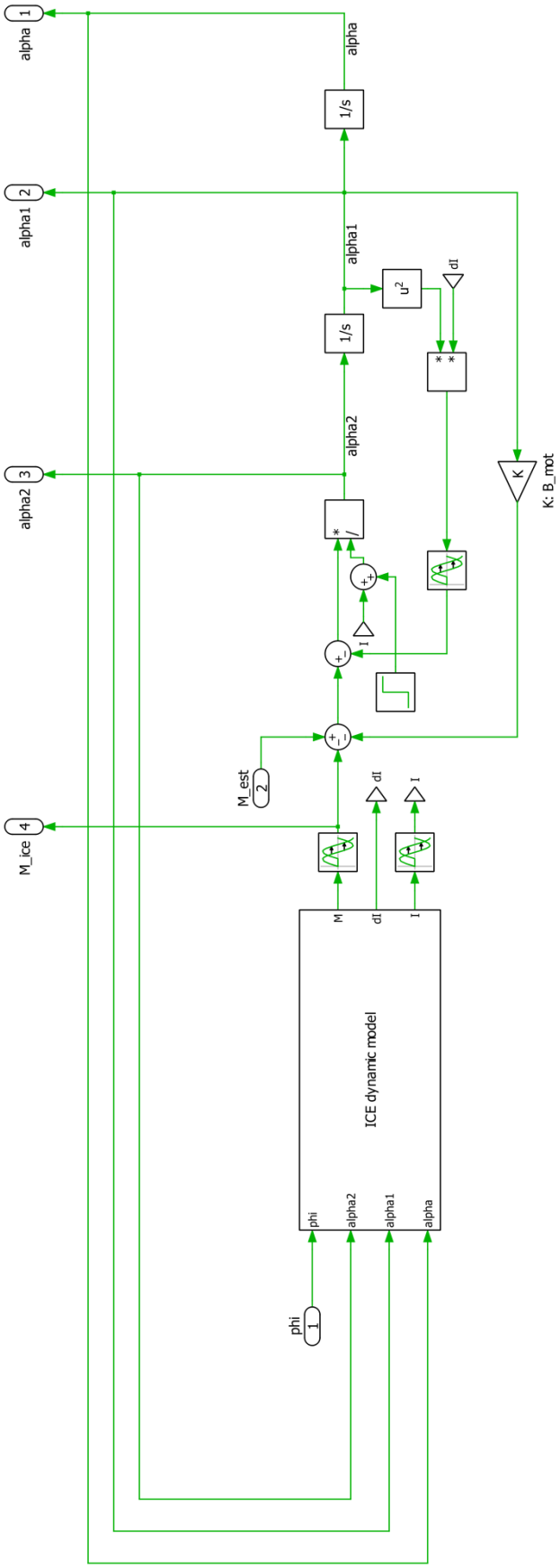


Fig. 4.28: PLECS schematic implementing the ICE model.

Extensive simulations for the considered system (ICE + proposed drive) has been considered. Hereafter, a selected operating condition will be shown, i.e. a full startup of the internal combustion engine is reported in **Fig. 4.29**. The model takes into account a complete electro-mechanical dynamical model of the drive system, including sampled-time control, PWM modulation delay and the complete non-ideal model of the inverter and of the internal combustion engine, as previously discussed. A high torque exceeding the rated value is considered in the results of Fig. 4.29, since it is necessary for a safe start of the engine. Reference and actual motor speed, electromagnetic and engine torque, line-to-line voltage and electric machine phase current are shown.

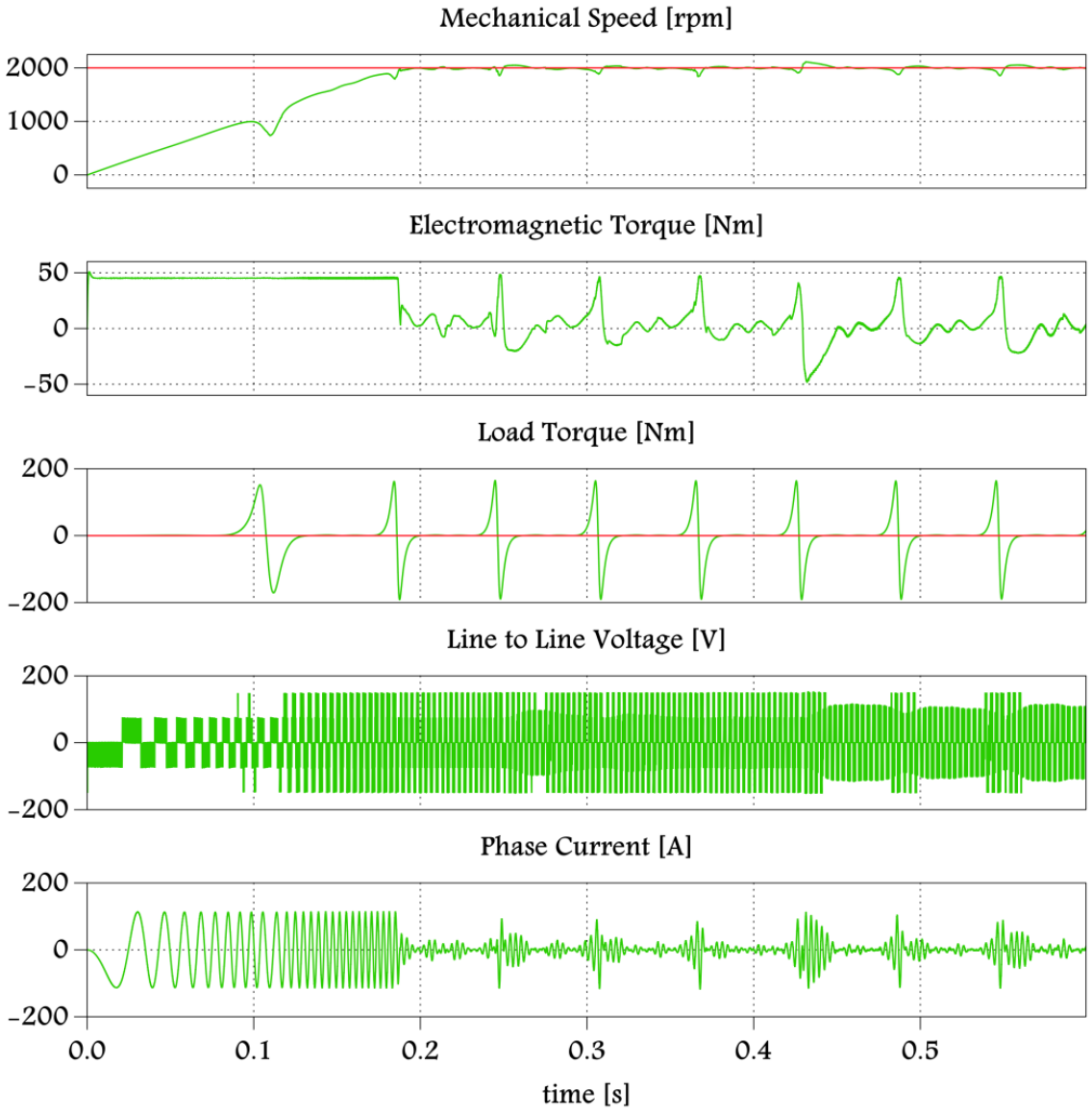


Fig. 4.29: Staring of the internal combustion engine.

One can notice that load torque experiences the typical behavior of a single cylinder combustion engine, providing very high torque peaks during cranking and expansion phases.

This in turn reflects in sudden variations of shaft speed. Line-to-line voltages shows the three-level modulation of the inverter. At steady-state the required torque is obviously much lower and within the rated conditions for the electric machine.

4.8 Torque damping techniques

In the previous section, an effective ICE model of the Diesel engine has been described. This model of the ICE allows to study the problem of the engine torque oscillation directly in simulation; so the experimental tests can be carry out only using the best techniques that reduced the oscillation phenomena.

The nonlinear geometry of the ICEs piston and crank mechanism has been modeled by PLECS standalone software using the engine fundamental kinematic equations, **(86)-(110)**. The engine start-up simulation, reported in **Fig. 4.29,** highlights that typically problem of single cylinder ICE namely it produces a pulsating torque which is reflected in speed oscillations in the engine shaft as is reported in **Fig. 4.30** and **Fig. 4.31** respectively. The **Fig. 4.30** underlines as the average torque value is very small, about 10-15 times lower, compared to peak one. The **Fig. 4.31** shows that during the compression of piston the speed value becomes 65 % of the average one instead during the end of expansion phase the speed value becomes 110 % of the average.

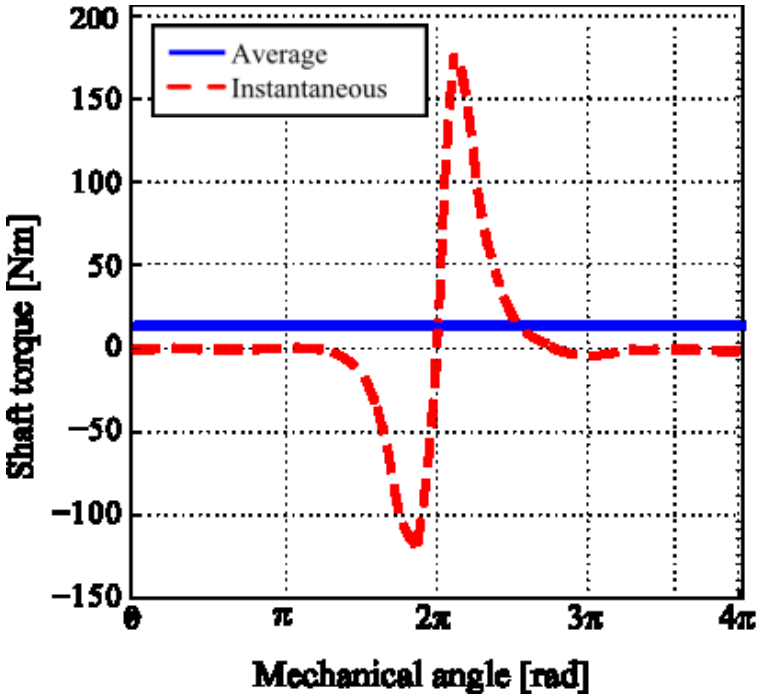


Fig. 4.30: ICE oscillating torque.

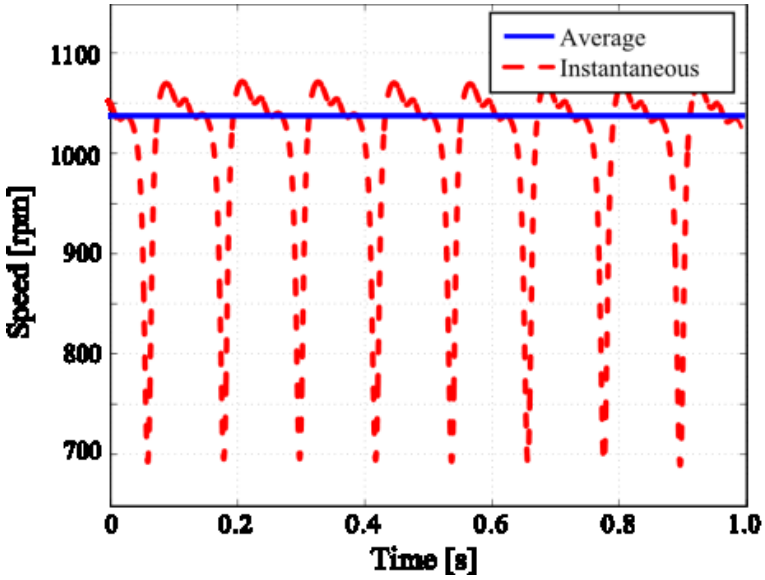


Fig. 4.31: ICE oscillating speed.

In order to find the optimal active damping for n-CHP application, three different techniques have been investigate by means of simulation and experimental test. It has been chosen the most effective solution for this work; however other solutions are available in the literature, [8]–[10].

4.8.1 Conventional techniques

PI regulator

The EM is controlled by constant speed operation and the control scheme is that reported in **Fig. 4.10**. Please note that **Fig. 4.31** highlights the speed oscillation due to engine pulsating torque. This measurements have been carried out with classical PI regulator as speed controller; it scheme is shown in **Fig. 4.32**. It consists to employee a standard PI regulator with anti-wind up to the integral part. The K_p and K_i parameters are chosen in order to fix the bandwidth at 120 Hz and to guarantee the system stability.

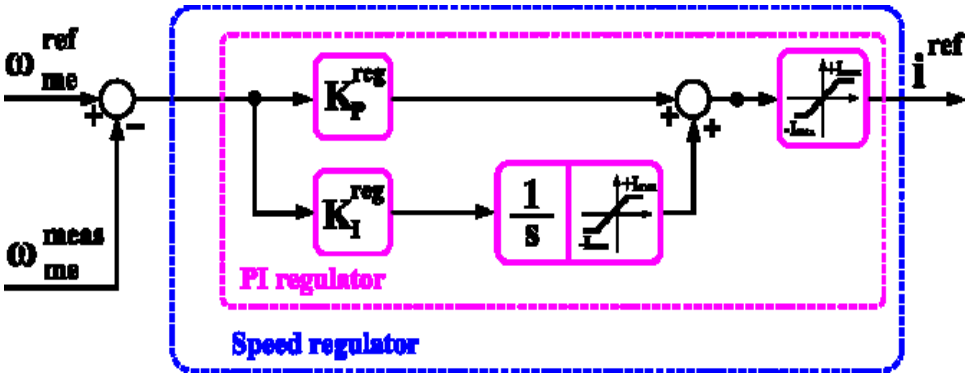


Fig. 4.32: Conventional PI regulator, Reference case.

The output of the regulator has been limited at the double of the nominal current.

The obtained results with this controller are indicated as Reference case and the performance of this control is used as term of comparison for the two different active damping techniques. Hereafter the most effective solution has been reported and it has been compared with the new technique here proposed; however other solutions are available in the literature, [69]-[72].

Torque estimator

As is reported in [72] the most effective damping technique foresees the use of an observer to carry out a torque feed-forward, [73], [74]. It estimates the ICE torque from the rotor position measurements, estimate EM torque (proportional to the current), and load model of of electric machine. In this damping technique no additional measures is necessary because rotor position information is available from the EM control and other information are contained by the knowledge of the EM parameters. The control technique block scheme is reported in **Fig. 4.33**

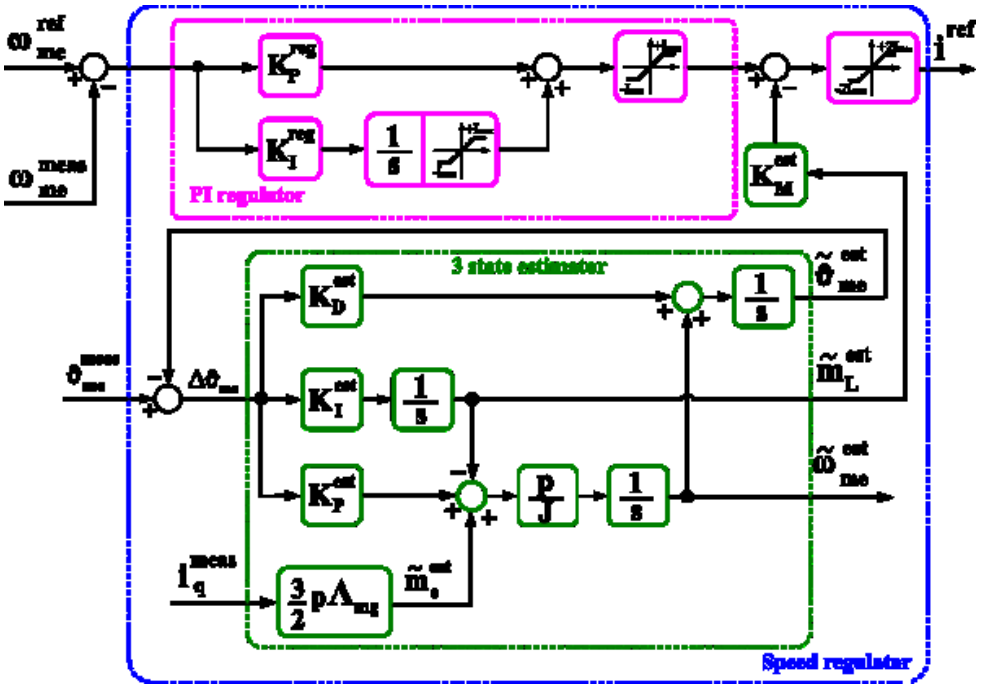


Fig. 4.33: PI regulator with estimate torque feed-forward.

4.8.2 Proposed resonant control approach

The third control method takes origin from harmonic analysis of the torque load pulsation.

A brief introduction of the resonant control operation principle and some insights of the digital implementation, based on [75], are presented in the following subsection. The main

characteristic of a resonant controller is the infinite gain at a specific frequency, i.e. resonant frequency. The transfer function of a resonant regulator, realized by two complex and conjugate poles at the resonance ω_0 and a zero in the origin, is explained by the following expression:

$$\boldsymbol{H(s) = K_I \frac{s}{s^2 + {\omega_0}^2}} \quad \textbf{(111)}$$

The controller is then obtained by introducing a proportional component, i.e.:

$$\boldsymbol{G_C(s) = K_P + K_I \frac{s}{s^2 + {\omega_0}^2} = K_P \frac{s^2 + \frac{K_I}{K_P} s + \omega_0^2}{s^2 + {\omega_0}^2}} \quad \textbf{(112)}$$

Bode diagrams of (112) provide zero phase and a constant gain K_P for all frequencies, except at resonance where the two un-damped poles provide infinite gain. The value of K_I regulates the bandwidth of the resonance term.

Aiming at introducing a finite gain at the resonance frequency and having a complete independence between the proportional gain K_P and width of the resonant terms, the following expression has been considered instead:

$$\boldsymbol{H(s) = K_I \frac{s^2 + 2\xi_z \omega_0 s + {\omega_0}^2}{s^2 + 2\xi_p \omega_0 s + {\omega_0}^2}} \quad \textbf{(113)}$$

where $\xi_z = \frac{\sqrt{2}}{2}$ and ξ_p is chosen in order the fix the gain (equal to the ratio ξ_z/ξ_p) and the width at the resonant frequency. Gain K_I defines the overall gain of the resonant term. The independence of the properties and parameters of the resonant terms are very useful as also 2^{nd} and 3^{rd} harmonic compensators are introduced to cope with harmonic content of the speed. The following expression of the current control is therefore obtained:

$$\mathbf{G_C(s) = K_I \sum_{i=1}^{3} \frac{s^2 + 2\xi_z(i \cdot \omega_0)s + (i \cdot \omega_0)^2}{s^2 + 2\xi_p(i \cdot \omega_0)s + (i \cdot \omega_0)^2}} \quad \textbf{(114)}$$

where the gain K_I, for simplicity, is chosen equal for all harmonics.

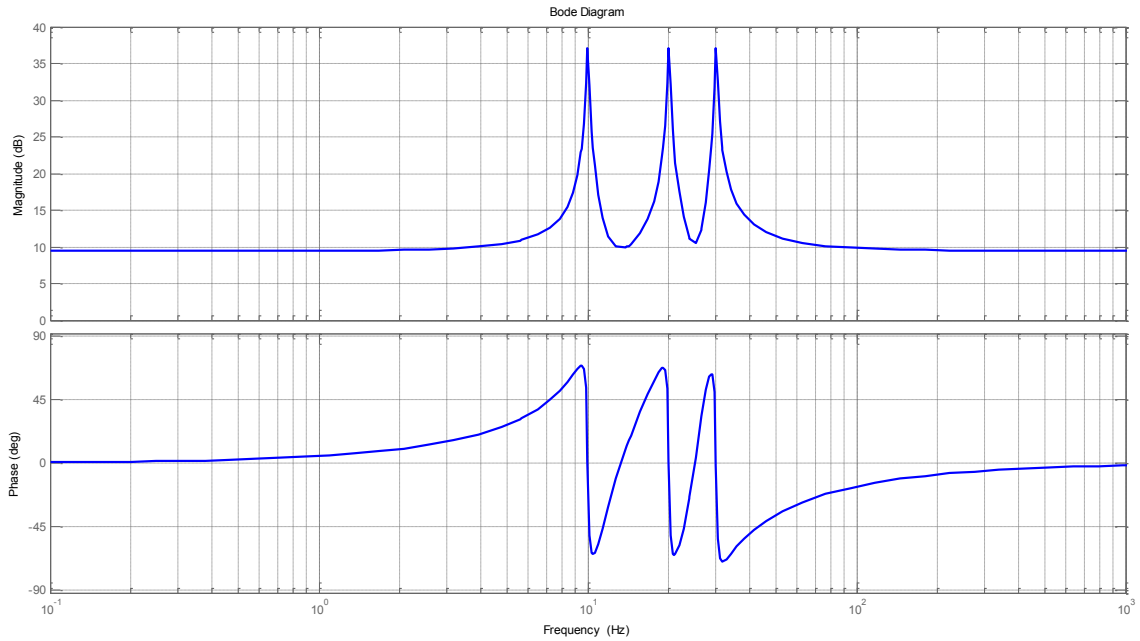


Fig. 4.34: Bode diagrams of the multiple resonant controller

Fig. 4.34 shows the magnitude Bode diagram of a multiple resonant controller (114) having 3 modes in the frequencies $\omega_0^{\mathrm{I}} = 2\pi \cdot 10\ \mathrm{rad/s}$, $\omega_0^{\mathrm{II}} = 2\pi \cdot 20\ \mathrm{rad/s}$ and $\omega_0^{\mathrm{III}} = 2\pi \cdot 30\ \mathrm{rad/s}$ and $\mathrm{K_I} = 50$.

The digital implementation of each resonant controller (114) has been performed by means of Tustin approximation, with a sampling period equal to the control period of the inverter ($\mathrm{T_s} = 100\ \mu\mathrm{s}$). The discrete transfer function and its coefficients have the following expressions:

$$G_C(z) = K_i \frac{b_0 z^2 + b_1 z + b_2}{a_0 z^2 + a_1 z + a_2} \begin{cases} b_0 = (4 + 4\xi_z \omega_0 T_s + \omega_0^2 T_s^2) \\ b_1 = -(8 - 2\omega_0^2 T_s^2) \\ b_2 = (4 - 4\xi_z \omega_0 T_s + \omega_0^2 T_s^2) \\ - - - - - - - - - - - - - - - - \\ a_0 = (4 + 4\xi_p \omega_0 T_s + \omega_0^2 T_s^2) \\ a_1 = b_1 \\ a_2 = (4 - 4\xi_z \omega_0 T_s + \omega_0^2 T_s^2) \end{cases} \quad \textbf{(115)}$$

The control technique block scheme is reported in **Fig. 4.35**.

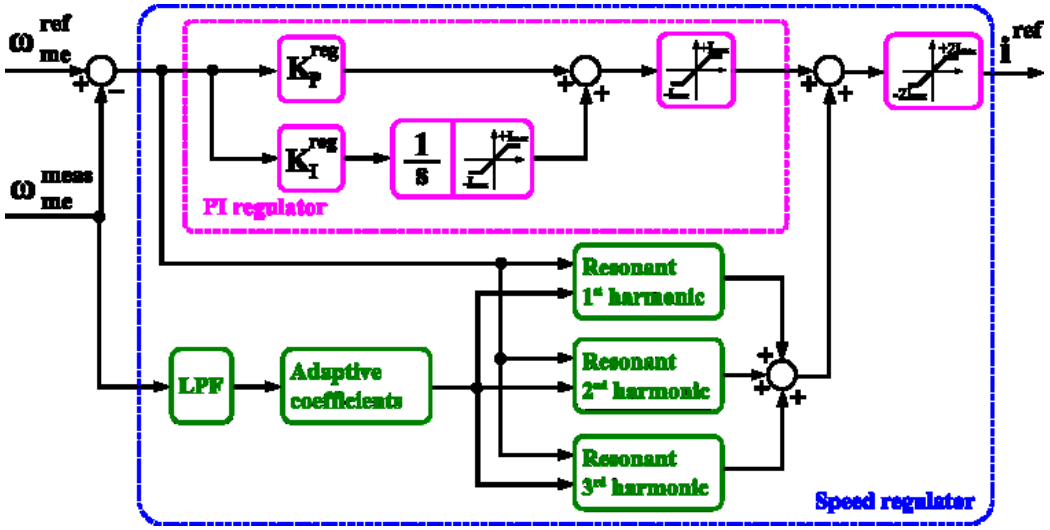


Fig. 4.35: Multi-resonant regulator control scheme.

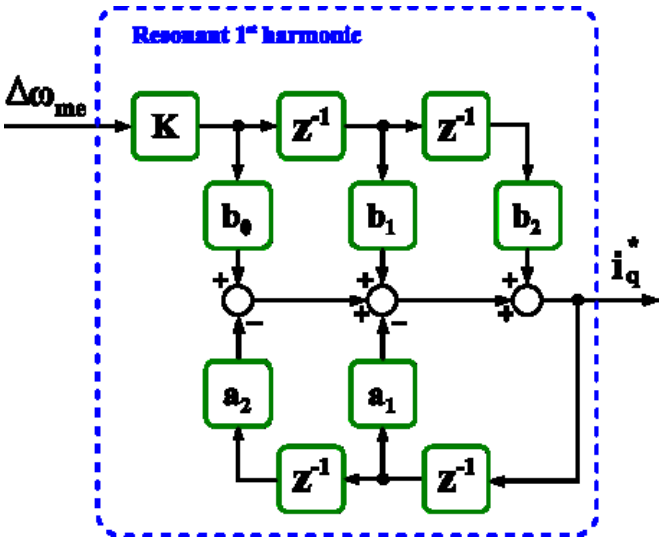


Fig. 4.36: Multi-resonant regulator digital implementation.

4.8.3 Simulation results

A complete simulation model of the motor and the drive was built aiming at validating the effectiveness of the proposed speed control method. The simulation scheme takes into account a complete electro-mechanical dynamical model of the drive system and of the internal combustion engine, including piston and crank mechanism. The model of the engine is implemented and simulated within PLECS standalone toolbox.

The performance improvements of all active damping techniques compared to a Reference case are highlighted in **Fig. 4.37**, **Fig. 4.38, Fig. 4.39** and **Fig. 4.40**. In all cases the EM is not sized to fully compensate the engine torque ripple otherwise it would become too large, however in the real system any additional EM losses would be retrieved from the cooling system of the ICE. To better compare these techniques a frequency analysis of the speed has

been carried out. **Fig. 4.41** reports the Fourier analysis: the fundamental frequency of the signal is 10 Hz and it highlights that all techniques reduce the speed harmonicespecially the components at 5^{th} order.

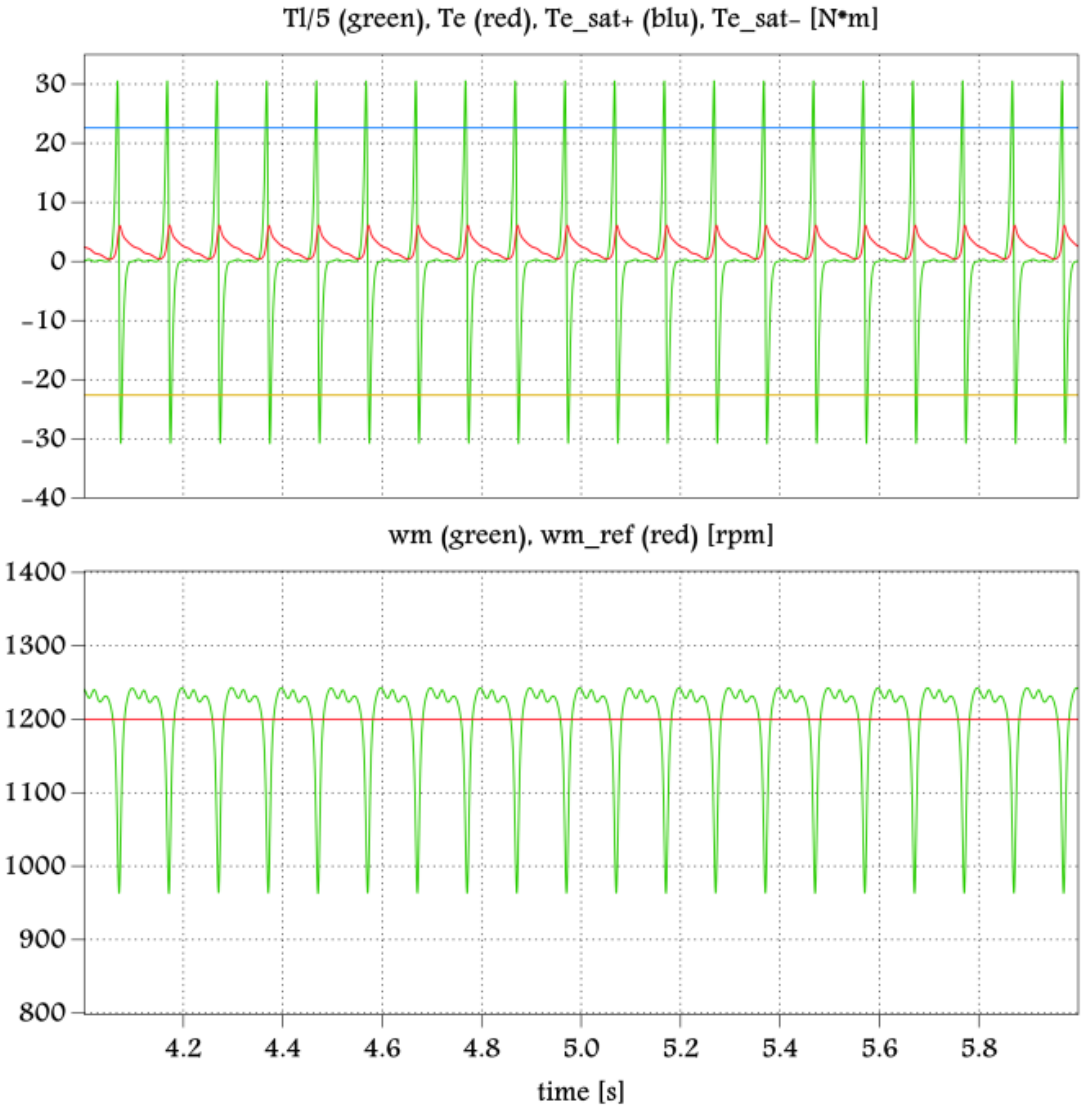


Fig. 4.37: Torque and speed in steady-state conditions at 1200 rpm with PI controller.

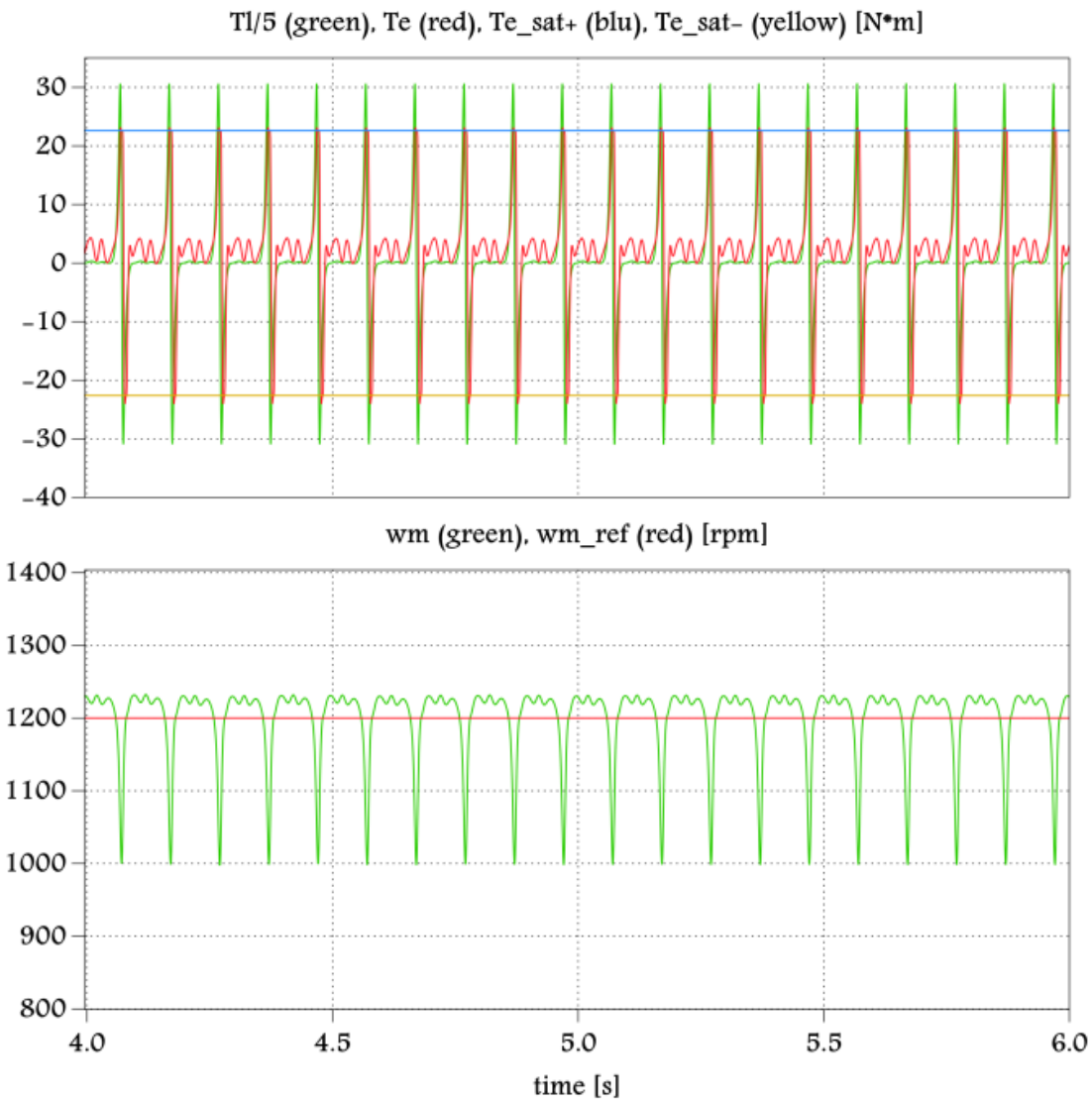


Fig. 4.38: Torque and speed in steady-state conditions at 1200 rpm with torque estimator.

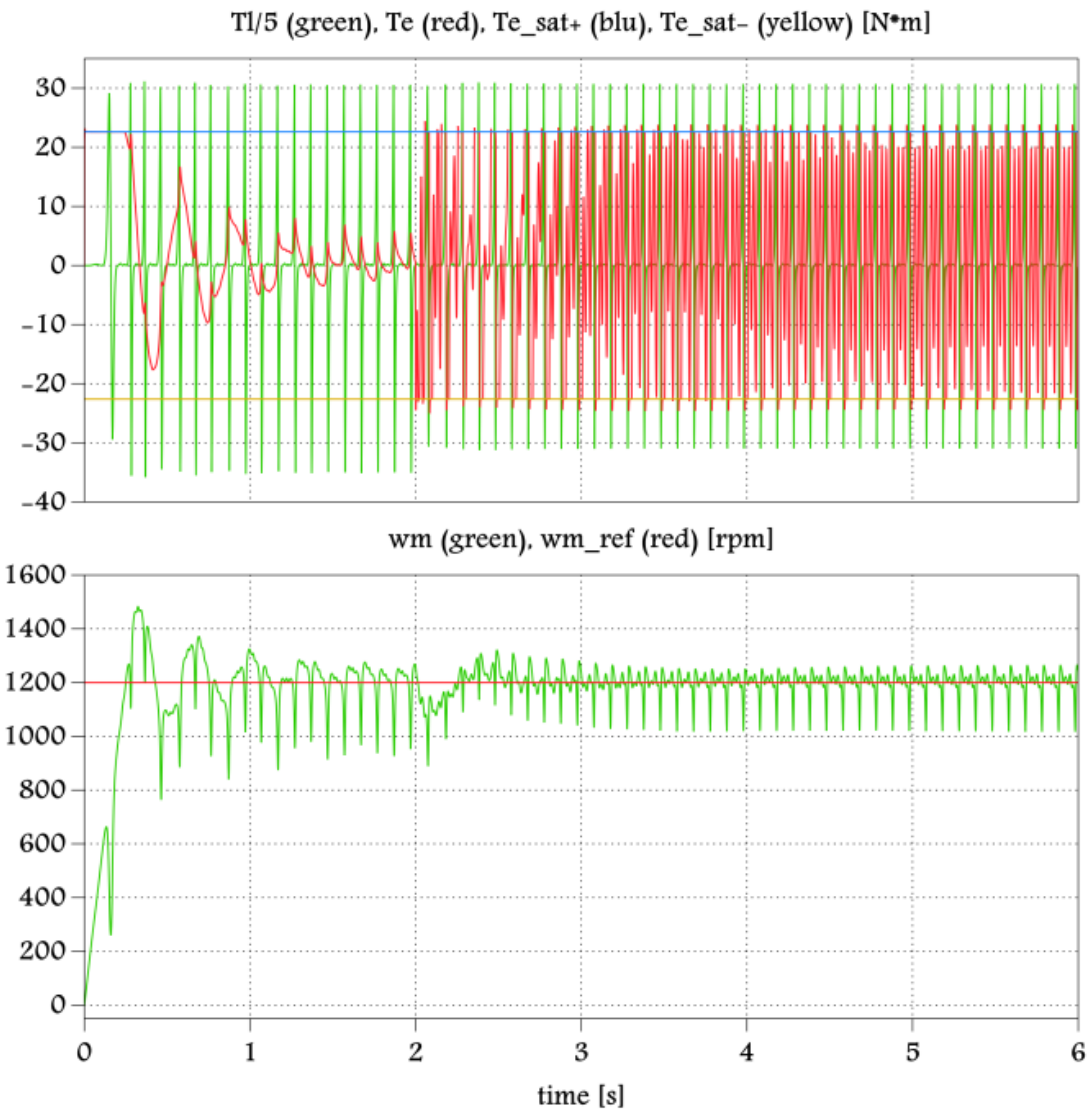


Fig. 4.39: Speed controller with multi resonant regulators: engine startup and reference pursuit.

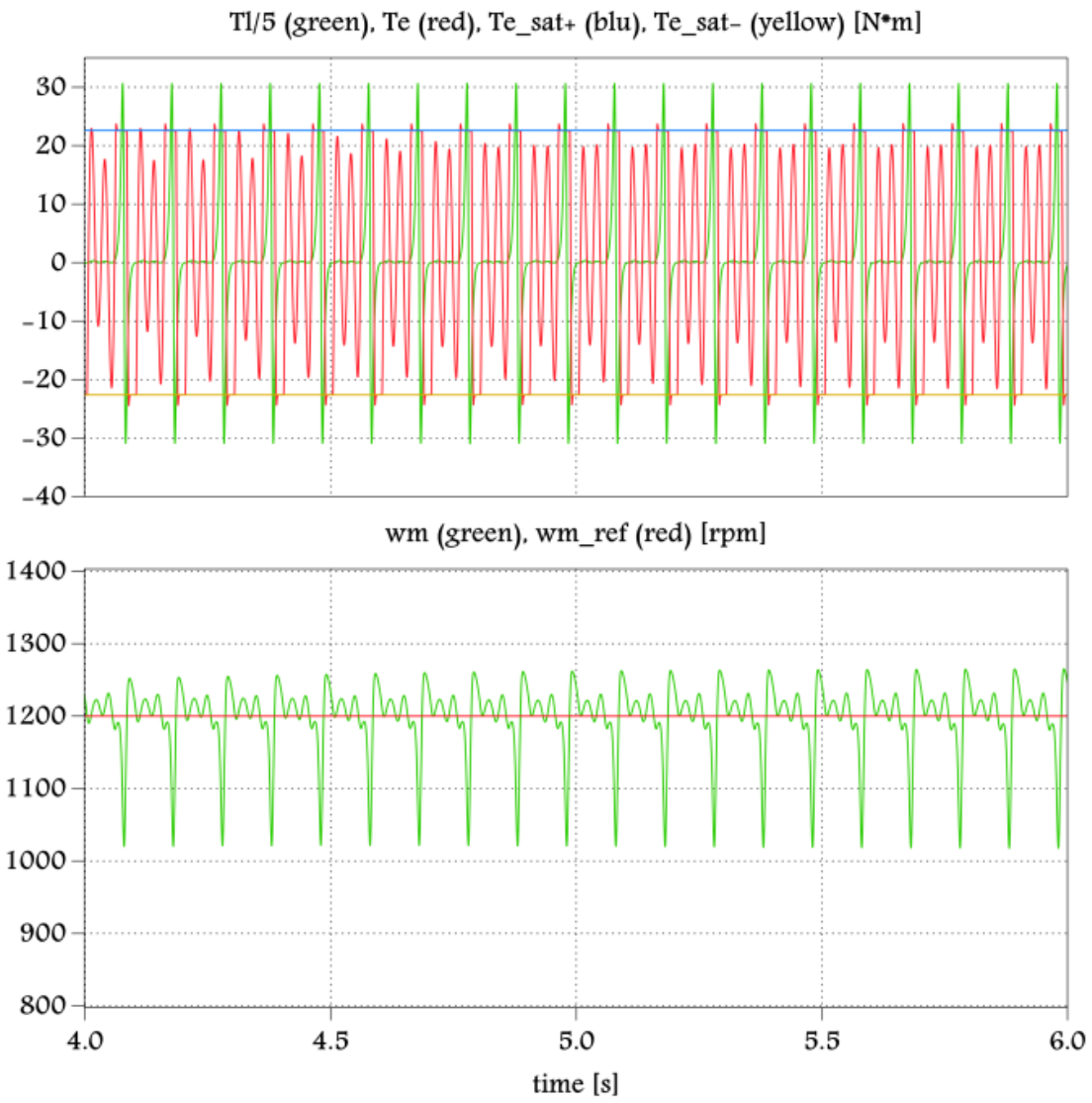


Fig. 4.40: Speed controller with multi resonant regulators: Steady-state detail at 1200 rpm .

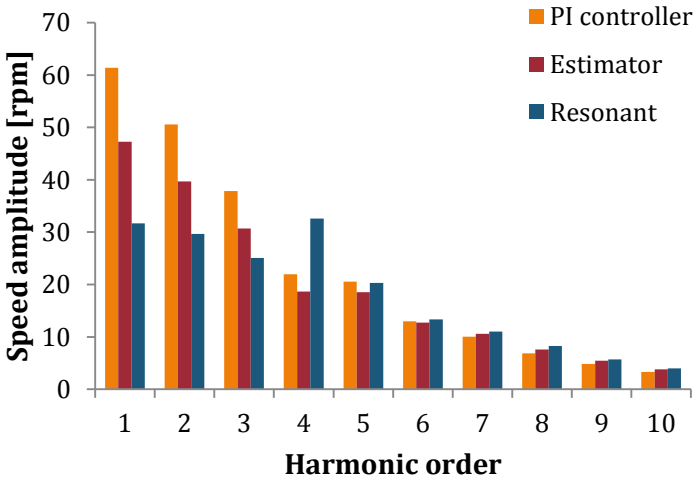


Fig. 4.41: Speed harmonic components up to $10 \cdot \omega_0$.

5 DESIGN AND CONTROL OF A WIRELESS CHARGER FOR ELECTRIC VEHICLES

5.1 Introduction

The technology of wireless charging, also referred to as wireless power transfer (WPT) or inductive power transfer (IPT), has been successfully applied at the low power level, such as applications for biomedical implants devices [82]-[85] and smart phones [86]. Along with the fast growing interest in electric vehicles (EVs) and plug-in hybrid electric vehicles (PHEVs), wireless charging, as a new way of charging batteries, has drawn the attention of researchers, car manufacturers, and customers recently [87]-[88]. Compared to conductive power transfer (usually plug-in), WPT is more convenient, weather proof, and electric shock protected. Some companies, such as WiTricity, Evatran, Qualcomm, etc., have developed products which can transfer power at 3.3 kW with an acceptable efficiency. However, there is still more research work needs to be done to further optimize efficiency, reduce cost, increase misalignment tolerance, and reduce size of the WPT chargers.

Wireless power transfer was first discovered by Nikola Tesla [89]. The basic principle of WPT is that the power transfers though electromagnetic field which is generated by the high frequency current in the transmitter coil. The receiver resonant circuit should have the same resonant frequency as that of the transmitter resonant circuit. A better explanation of this principle had been given by MIT and verified by using self-resonant coils in a strongly coupled magnetic resonance regime [90]. There are many research areas in WPT, such as compensation network and circuit analyses [91]-[106], coil design techniques for large gap and misalignment tolerance [91]-[93], link optimization for high efficiency [94]-[95], control methods, foreign object detection and safety issues. Among them, compensation topology is very important because it helps to adjust resonant frequency, minimize the VA rating of power supply, improve coupling and power transfer capability, and achieve high efficiency [96]. As for the EV/PHEV application, the coupling coefficient varies with the changing of the vehicle ground clearance and misalignments. This will result in the variations of the

circuit parameters and resonant frequencies for some compensation topologies. So it is of significant importance to design an appropriate compensation topology for EV/PHEV wireless chargers.

Based on the way the capacitors connected to the transmitting and receiving coils, four basic compensation topologies labeled as SS, SP, PS, and PP are widely adopted, where the first S or P represents the capacitor in series or parallel with the transmitting coil and the second S or P stands for capacitor in series or parallel with the receiving coil. A systematic analysis of these topologies can be found in [97]-[99]. The selection of the compensation topology is dependent on the application. In [26], it proposed an optimized method to select compensation topology from an economic perspective. The results showed that SS and SP topology were more suitable for high power transmission and SS compensation topology requires less copper. In [99], it indicated that SS compensation topology seemed to be the best topology because the system can work at a frequency independent of coupling coefficient and load. However PP compensation topology was adopted in their work because parallel compensated transmitter could provide a large current and parallel compensated receiver had the current source characteristic which was more suitable for battery charging. It is widely accepted that WPT system can get maximum efficiency when it works at the resonant frequency. For SS topology, there may be one or two resonant frequencies depending on the coupling coefficient [101]. This is similar to bifurcation phenomena [99], which is inevitable for the four basic compensation topologies and brings difficulties to controller design.

Some other novel compensation topologies have been put forward in the literature. A series-parallel-series (SPS) compensation topology was proposed in [100]. This particular topology, which was composed of one capacitor in series and another in parallel with the transmitting coil, and one capacitor in series with the receiving coil, had characteristics of both SS and PS topologies. In [102], a LCL parallel resonant circuit was proposed, it made the track (transmitter) to have constant current characteristic. This is essential for a WPT system with multiple pickups (receivers). Following this topology, the same group also proposed another compensation topology called CLCL network. Due to the symmetrical topology and phase modulated control method, the IPT system could achieve bidirectional power transfer.

5.2 Proposed system design

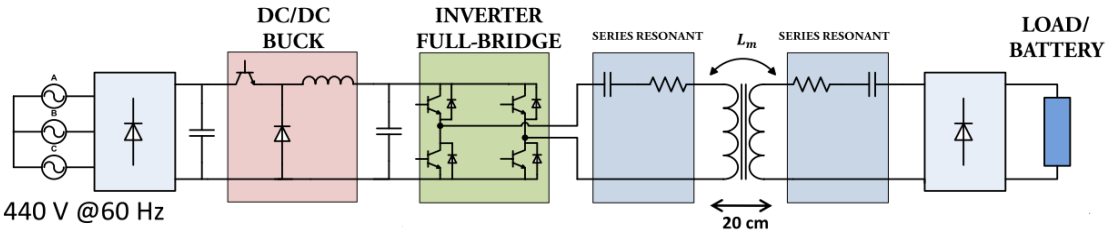


Fig. 5.1: Overall system scheme.

The block diagram of the wireless charging system proposed here [108] is shown in **Fig. 5.1**. On the primary (transmitter) side, the circuit is composed by a three phase rectifier, a step-down converter, a full-bridge resonant converter with series compensation topology. The rectifier stage converts 3-phase AC to DC and the DC/DC converter is employed here to control the input voltage of the full-bridge resonant inverter. In this way, it is possible to control the power flow to the load adjusting the buck output voltage, as explained in the next sections. The primary part produces an essentially constant current in the track or coil inductance using a suitable resonant high frequency inverter with primary compensation to minimize the VA rating of the supply. The secondary coil can move with respect to the track. A compensation is also often required to enhance the power transfer capability. The power supply and controller normally control both the frequency and the primary current to achieve maximum power transfer capability to the load (fixed- and variable-frequency control can be used). Fixed frequency controllers are much simpler, but increase the required VA rating of the power supply. Variable-frequency controllers ideally operate at the zero phase angle point of the load impedance seen by the power supply in order to minimize the VA rating of the supply.

SAE J2954™ Team for WPT of Light Duty, Electric and PEVs has determined three power classes, i.e. WPT 1 (up to 3,7 kW), 2 (7,7 kW) and 3 (22 kW). The system presented in this section is meant to belong to the third power class.

5.3 Power control methods

5.3.1 Review

There are several reports on WPT control methods, i.e. transmission frequency control [103], dual side control [104], voltage ratio control method with a proper DC/DC converter positioned in the primary or in the secondary side [105] and phase-shift control strategy [106].

5.3.2 Proposed approach

The control of the wireless power transfer is proved here by a step-down DC/DC converter positioned at the primary side just before the resonant full-bridge.

Buck converter design

The conventional buck converter is the simpler way of realize a step down converter. Afterwards, the buck converter design, under company specifications and some design hypothesis, will be considered.

Design fixed requirements

Input voltage from rectifier:	$\boldsymbol{V_{in} = 700\ V}$
Output voltage range:	$\boldsymbol{V_o = (250 - 500)\ V}$
Switching frequency:	$\boldsymbol{f_{sw} = 20\ kHz}$
Maximum power:	$\boldsymbol{P_{max} = 25\ k\mathrm{W}}$

Design hypothesis and derived parameters

Output voltage ripple:	$\boldsymbol{\Delta V_o < 5\ \%}$
Maximum output current	$\boldsymbol{I_{max} = {P_{max}}/{V_{out}^{min}} = 100\ A}$
Inductor current ripple (pk-pk):	$\boldsymbol{\Delta I_L < 30\ \%}$
Load range:	$\boldsymbol{R_{load} = (2,5 - \infty)\ \Omega}$
Duty-cycle range:	$\boldsymbol{\delta = 0,35 - 0,71}$

Output filter design

The minimum output capacitance value is determined by the following expression:

$$\boldsymbol{C = \frac{V_o \cdot (1 - \delta)}{8L \cdot \Delta V_o \cdot f_{sw}^2} = \frac{I_L^{min}}{4 f_{sw} \cdot \Delta V_o}} \qquad \textbf{(116)}$$

In Continuous Conduction Mode (CCM) the relationship between the input and output voltage is linear with the duty-cycle of the main switch:

$$\boldsymbol{\frac{V_o}{V_{in}} = \delta} \qquad \textbf{(117)}$$

Instead, when working in Discontinuous Conduction Mode (DCM) this voltage ratio is non-linear and becomes load-dependent:

$$\boldsymbol{\frac{V_o}{V_{in}} = \frac{2}{1 + \sqrt{1 + \frac{8L \cdot f_{sw}}{R \cdot \delta^2}} +}} \qquad \textbf{(118)}$$

valid for $\boldsymbol{R > R_{cr}}$. DCM occurs when the converter works at light loads, but sometimes the converter can be purposely designed to operate in DCM al all loads, in order to exploit the fact that the main switching device switches on at zero current (ZVS condition).

Minimum inductance current that guarantees CCM operation, normally referred as the critical current, can be derived as:

$$\boldsymbol{I_L^{min} = \frac{V_o \cdot (1-\delta)}{2L \cdot f_{sw}} = \frac{\Delta I_L}{2}} \quad \textbf{(119)}$$

Thus, minimum inductance value to satisfy the above relationship is:

$$\boldsymbol{L^{min} \geq \frac{V_o \cdot (1-\delta)}{2I_L^{min} \cdot f_{sw}}} \quad \textbf{(120)}$$

If the converter operates at constant power, the maximum power condition is achieved at the minimum output voltage, i.e. $V_o = 250\ V$.

If $\Delta V_o = 2{,}5\ V$; $I_{max} = 100\ A$ and $\Delta I_L = 30\ A$, the critical current, the inductance and capacitance values are; $I_L^{min} = 15\ A$, $C = 15\ \mu F$ and $L^{min} = 268\ \mu H$.

In **Fig. 5.2** the minimum (blue line), the RMS (green line) and the peak (red line) values of inductor current are represented as a function of the inductance value in two current load conditions, i.e. $I_o = 15\ V$ (solid lines) and $I_o = 100\ A$ (dotted lines). It can be seen that in the first case the critical value of the inductance (the intersection of the minimum current with the x-axis) is equal to $L = 268\ \mu H$, confirming previous analytical derivation when the

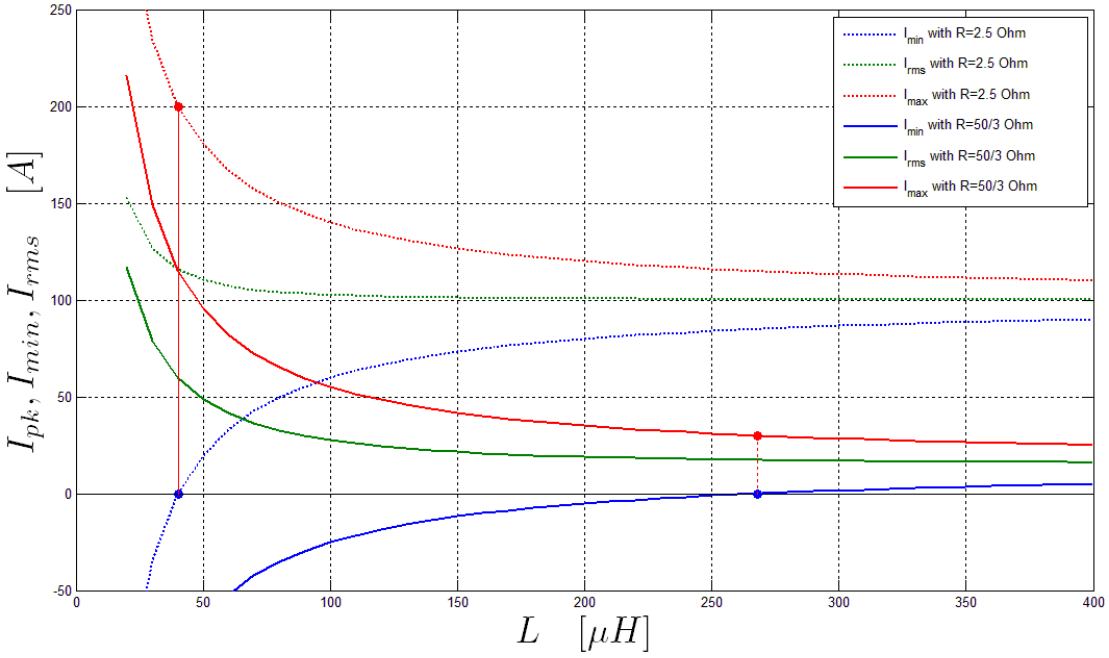


Fig. 5.2: Inductor current as function of inductance value at two different loads ($\boldsymbol{R = 2{,}5\ \Omega}$). and $\boldsymbol{R = \frac{50}{3}\ \Omega}$).

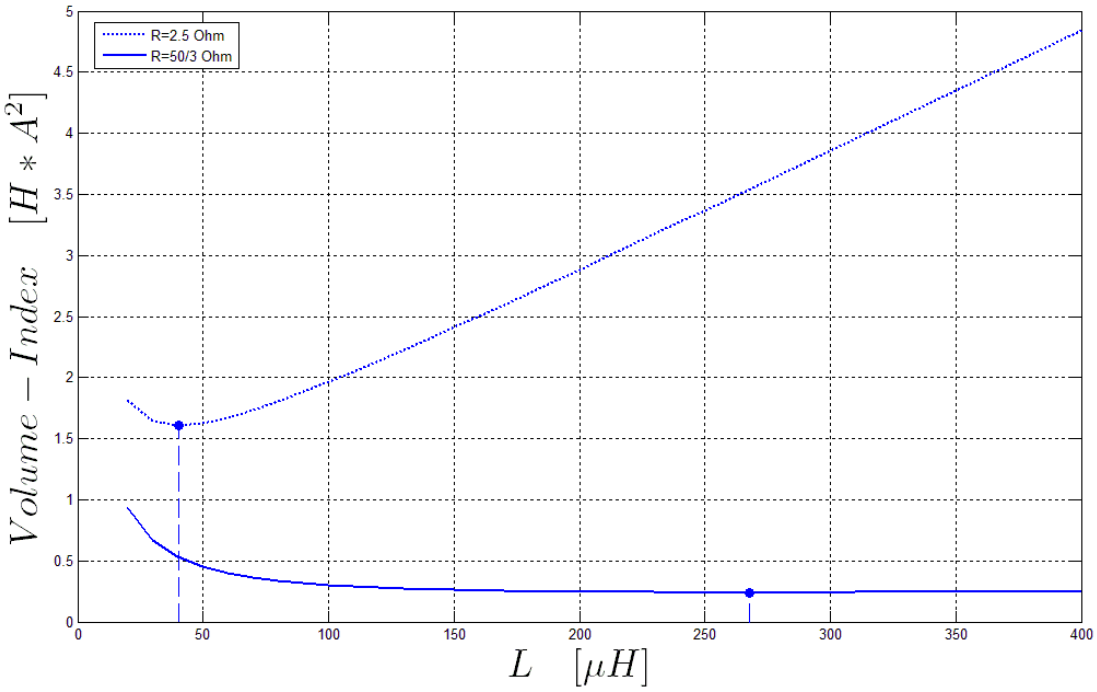


Fig. 5.3: Volume-index as function of inductance value at two different loads ($R = 2,5\ \Omega$ and $R = \frac{50}{3}\ \Omega$).

minimum current was fixed as half of the peak-to-peak ripple. Instead, if the minimum current guaranteeing continuous conduction mode is increased to the maximum current value, the critical inductance will be about $L = 40\ \mu H$. With this last inductance value the converter will operate in transition mode, that is the boundary operating condition between CCM and DCM, at the maximum current. As the load current decreases, the converter will work in discontinuous mode, reaching CVS but increasing the RMS value of the inductor current.

In **Fig. 5.3** the volume index (inductance per square current) is represented as function of the inductance for two current load conditions, i.e. $I_o = 15\ V$ (solid lines) and $I_o = 100\ A$ (dotted lines).The highlighted points are the values of the volume index at the critical inductances.

Multiphase converter approach

Multiphase interleaved soft-switching synchronous buck has been selected as a suitable topology to realize the step-down DC/DC converter. An example of a two phase converter is shown in **Fig. 5.4**, where every buck switching leg has been realized by two IGBTs. A gate signal complimentary control scheme is used here in order to turn on the originally non-active switch and to divert the current into the anti-paralleled diode of the active switch. In this way, the main switch can be turned on under zero-voltage condition. The soft-switching operation can be considered a zero-voltage resonant transition (ZVRT) [107].

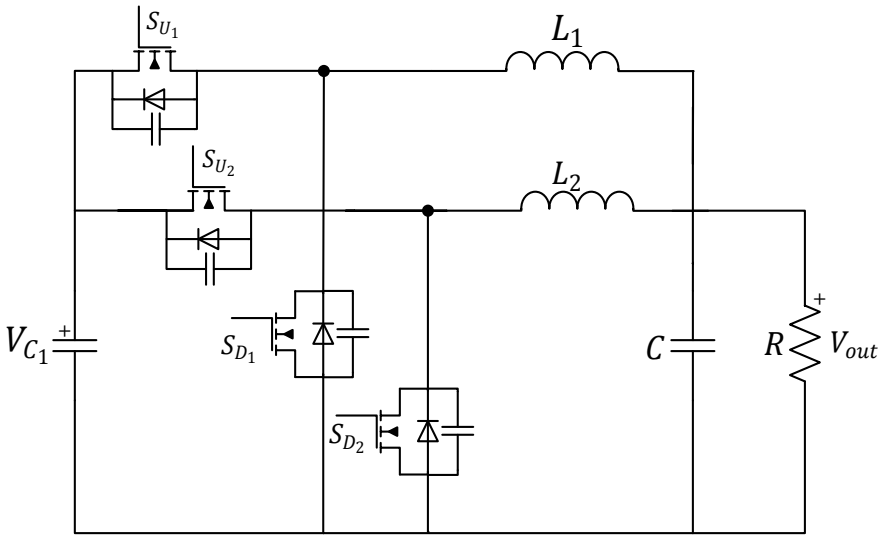


Fig. 5.4: Multiphase synchronous buck converter with $N = 2$.

Output current ripple reduction

The use of multiple switching devices fulfilling the same function offers a possibility to split the converter into smaller units processing a fraction of the output power. The units operate with so-called interleaving; a phase shift between their switching signals improves the operation of input and output filters. The inductor current ripple ΔI_o varies depending on the number N of phases as:

$$\boldsymbol{\Delta I_o = \frac{V_{in} \cdot T_{sw}}{L} \cdot N \cdot \left(\delta - \frac{M}{N}\right) \cdot \left(\frac{M+1}{N} - \delta\right)} \quad \textbf{(121)}$$

where $M = \mathrm{floor}(N \cdot \delta)$ is the maximum integer that does not exceed the $N \cdot \delta$.

The current ripple cancellation coefficient K_I can be defined as the ratio of the magnitudes of output current ripple ΔI_o and inductor current ripple ΔI_{ph}, i.e.:

$$\boldsymbol{K_I = \frac{\Delta I_o}{\Delta I_{ph}} = \frac{N \cdot \left(\delta - \frac{M}{N}\right) \cdot \left(\frac{M+1}{N} - \delta\right)}{\delta \cdot (1 - \delta)}} \quad \textbf{(122)}$$

In (122), coefficient K_I is represented as a function of the duty-cycle for different number of phases.

One can notice that the current ripple cancellation is less effective when a very small or very high δ is considered. Furthermore, cancellation performance increases as the number of phases is higher and there are some values of δ (for example $\delta = 0$) where theoretically ripple can be deleted.

The voltage ripple seen by the output capacitor is then:

$$V_o = \frac{1}{C}\frac{1}{2}\frac{\Delta I_o T_{sw}}{2N} = \frac{V_o \cdot (1-\delta) \cdot T_{sw}^2}{8CL} \cdot \frac{N \cdot \left(\delta - \frac{M}{N}\right) \cdot \left(\frac{M+1}{N} - \delta\right)}{\delta \cdot (1-\delta)} \qquad (123)$$

As a consequence, the minimum output capacitance value is also affected by this ripple cancellation coefficient as follows:

$$C = \frac{\Delta I_o/2}{4 f_{sw} \cdot \Delta V_o} = \frac{\Delta I_{ph}}{8 f_{sw_{eq}} \cdot \Delta V_o} \cdot K_I \qquad (124)$$

where $f_{sw_{eq}} = f_{sw} \cdot N$ is the equivalent switching frequency seen at the output and ΔV_o is the desired voltage ripple.

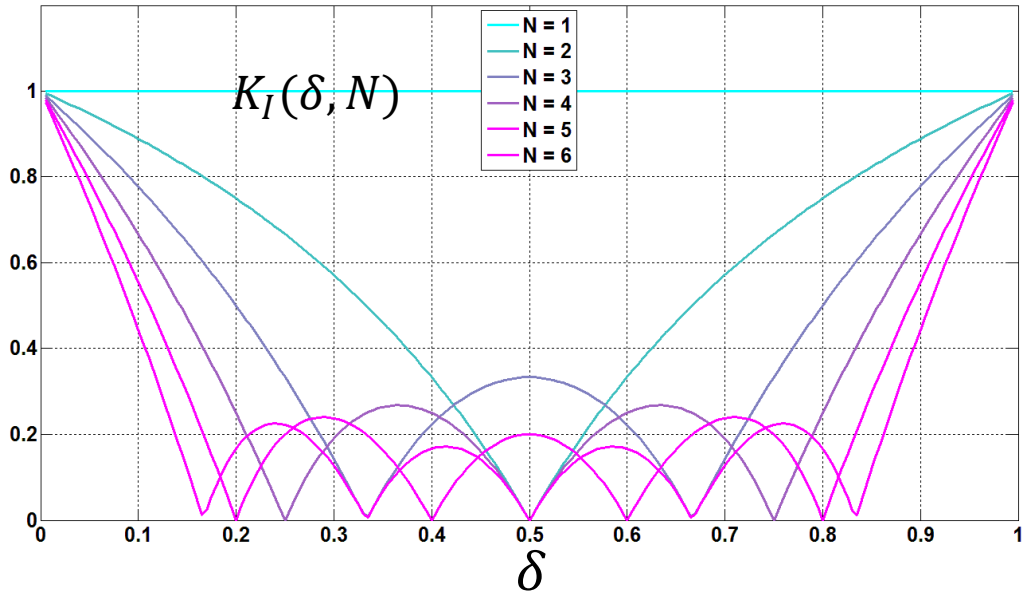


Fig. 5.5: Current ripple cancellation coefficient.

Coupled or independent phase design

The approach with independent phases is more efficient for low power conversion. The benefit is a considerable efficiency improvement in low-power region due a substantial reduction of fixed losses when several phases are disabled. A drawback of this approach is that the input/output filters must be designed for single-phase operation with high current ripples. On the other hand, the design with coupled inductors can reach power density as high

as two times that of the independent phase design. Therefore, the use of coupled inductors may be beneficial for space critical applications.

Soft-switching control

In order to achieve high-power density, the converter can be designed to operate in discontinuous conducting mode (DCM) such that the passive inductor can be minimized, affecting the converter size. The DCM operation introduces a large current ripple, so it is necessary to interleave multiple phases to cancel the high-frequency switching current ripple, as previously mentioned.

Another major advantage of this operation mode is that zero turn-on loss and thus low diode reverse recovery loss can be achieved. However, the DCM operation largely increases turnoff loss because the main switch is turned off at twice the load current or higher.

Another important issue is the inductor current parasitic ringing due to the inductor oscillation with the device output capacitance during turn-off. For those reasons in this section each phase has been realized by a synchronous buck converter composed by two complementary IGBTs with a snubber capacitor in parallel. In this case, the inductor current, rather than operating in a traditional DCM condition, goes from positive to negative direction and then swings back to positive. It is easily demonstrated that the diode turns off naturally without having reverse recovery loss and the parasitic ring is also fully avoided. **Fig. 5.6** shows the proposed complimentary gating control and inductor current waveform for one phase-leg operation.

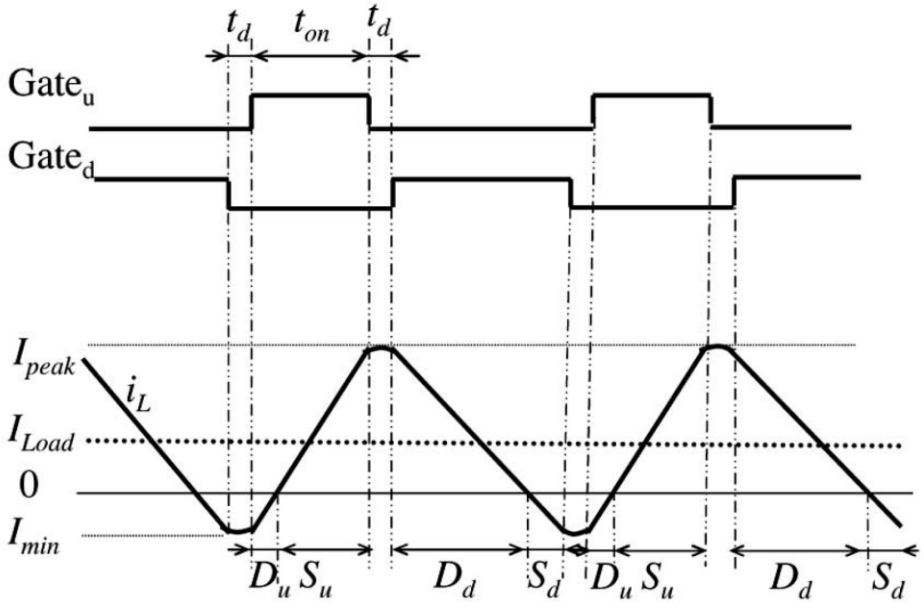


Fig. 5.6: Soft-switching buck operation mode.

Variable frequency operation

Normally, the induction value L is fixed to insure operation in soft-switching at the maximum power (at the highest load). When the load changes, the ZVRT condition cannot be guaranteed anymore resulting in a reduction of the converter efficiency.

A variable frequency control can be implemented taking into account possible variations of the output current in steady state conditions.

In the following equation the relationship between frequency and power/load has been derived:

$$f_{sw} = \frac{R}{2L \cdot V_{in}} \left(V_{in} - \sqrt{R \cdot P} \right) \tag{125}$$

In **Fig. 5.7** the switching frequency as a function of the load has been reported at different power levels. The dashed are lines are constant power lines, instead the solid lines are constant output voltage at $250\ V$ and $500\ V$.

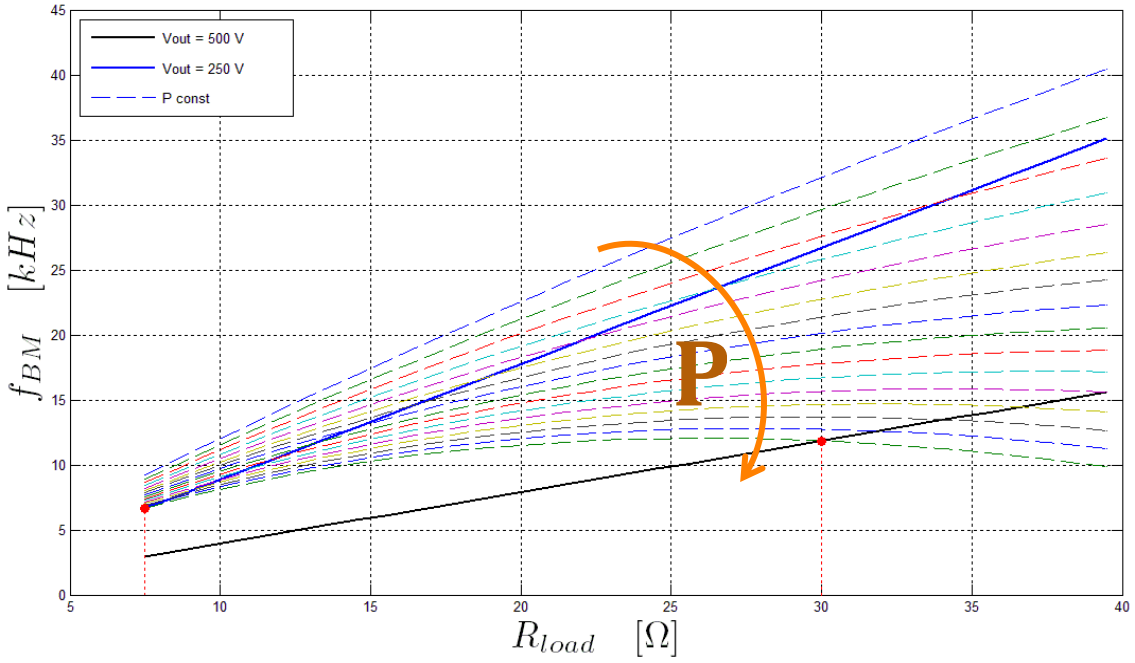


Fig. 5.7: Switching frequency as a function of the load at different power levels.

5.4 Compensation topology

The series-series compensation topology is presented in Fig. 5.8.

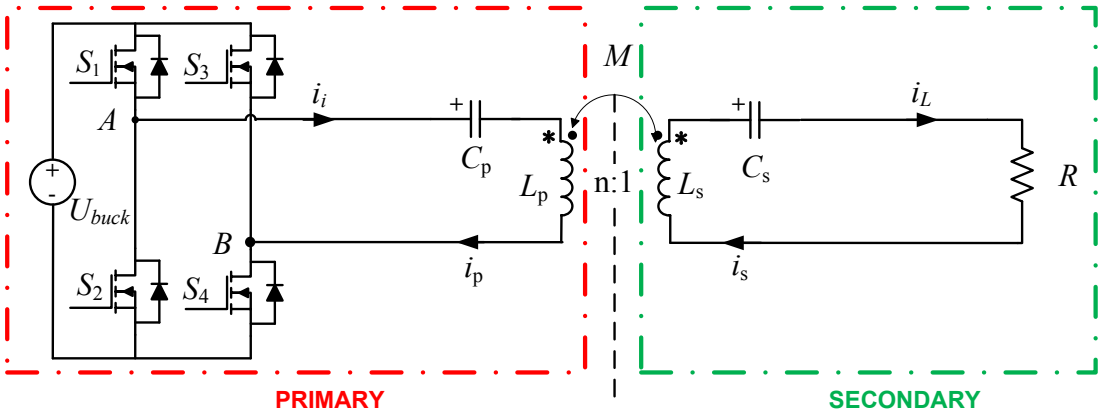


Fig. 5.8: Series-Series compensation topology.

The primary capacitance is deliberately to compensate both the primary self-inductance and the reflected impedance. This forces the zero angle frequency of the load model to equal the secondary resonant frequency. At this operating condition, maximum power transfer is achieved with minimum VA rating of the power supply. Using a standard mutual inductance coupling transformer model and assuming sinusoidal voltages and currents, the induced voltage in the secondary due to the primary current I_s is equal to $j\omega MI_s$, while the reflected voltage in the primary due to the secondary current I_p is equal to $-j\omega MI_p$, with M the mutual inductance between the primary and secondary and the operational frequency ω.

The load impedance of the secondary is calculated as a lumped impedance whose value depends on the secondary compensation as given by $Z_s = j\omega L_s + \frac{1}{j\omega C_s} + R$. The loading effect of the secondary on the primary circuit can represented as a reflected impedance Z_r (**Fig. 5.9**).

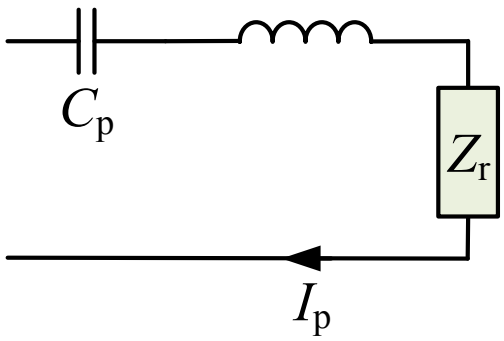


Fig. 5.9: Compensated primary.

This impedance depends on the transformer coupling and operating frequency, instead at the resonant frequency $\omega_0 = \frac{1}{\sqrt{C_s L_s}}$ depends only on ω_0, M and R, as shown in the following expressions:

$$\mathbf{Z_r} = \frac{\boldsymbol{\omega^2 M^2}}{\mathbf{Z_s}} \rightarrow \begin{cases} Re\{Z_r\} = \dfrac{\omega^4 C_s^2 M^2 R}{(\omega^2 C_s L_s - 1)^2 + \omega^2 C_s^2 R^2} \\ Im\{Z_r\} = \dfrac{-\omega^3 C_s M^2 (\omega^2 C_s L_s - 1)}{(\omega^2 C_s L_s - 1)^2 + \omega^2 C_s^2 R^2} \end{cases} \quad \textbf{(126)}$$

$$Z_{r_0} = Z_r(\omega = \omega_0) \rightarrow \begin{cases} Re\{Z_{r_0}\} = \dfrac{\omega_0^2 M^2}{R} \\ Im\{Z_{r_0}\} = 0 \end{cases} \quad \textbf{(127)}$$

The real and imaginary part of the reflected impedance as a function of the frequency are shown in Fig. 5.10, considering a resonant frequency equal to 69 kHz.

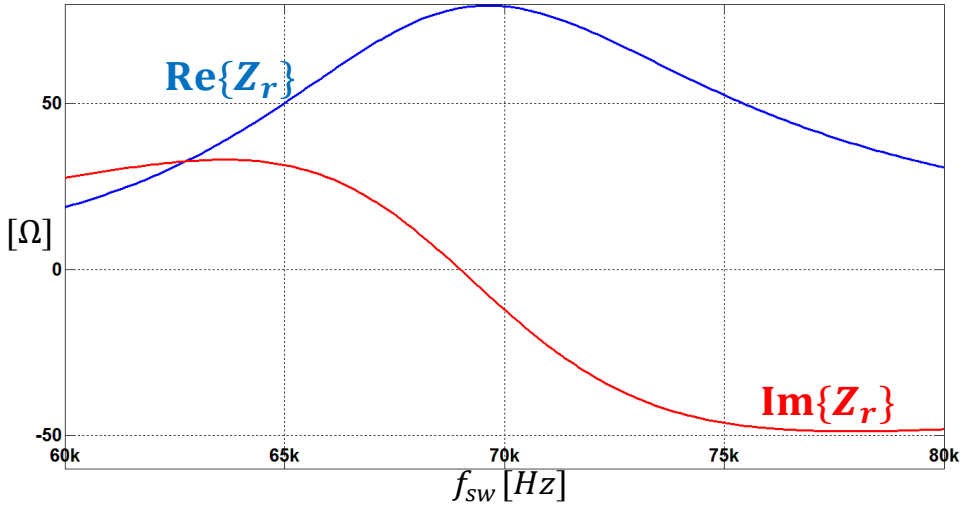


Fig. 5.10: Real and imaginary part of Z_r as a function of f_{sw}.

The power transferred from the primary to the secondary is then simply the reflected resistance multiplied by the square of the primary current as given by $P = \mathrm{Re}\{Z_r\} \cdot I_p^2$. There is theoretically no limit to the power transfer capability if the system is operated at the resonant frequency ω_0. It can be seen that both the reflected resistance and the power transfer capability assuming constant primary current for series compensation increase to infinity when the load resistance R is reduced to zero:

$$P(Z_{r_0}) = \frac{\omega_0^2 M^2}{R} \cdot I_p^2 \quad \textbf{(128)}$$

Thus, the primary current is:

$$I_p = \frac{\sqrt{P \cdot R}}{\omega_0 M} \tag{129}$$

The relationship between the power delivered to the load R and the reflected power is represented by the following expression:

$$R \cdot I_s^2 = Re\{Z_r\} \cdot I_p^2 \tag{130}$$

Thus, extracting I_p from (130), it's possible to derive the expression of the primary current as a function of the secondary circuit as:

$$I_p = \sqrt{\frac{R}{Re\{Z_r\}}} \cdot I_s \tag{131}$$

If the inverter works at the resonance frequency ω_0, equation (131) becomes:

$$I_{p_0} = \frac{R}{\omega_0 \cdot M} \cdot I_{s_0} \tag{132}$$

where I_{p_0} and I_{s_0} are the primary and secondary current at the resonance.

Meanwhile, the relationship between the input power and the reflected power is:

$$\frac{4}{\pi\sqrt{2}} V_{buck} \cdot I_p = Re\{Z_r\} \cdot I_p^2 \tag{133}$$

where V_{buck} is both the output voltage of the buck stage and the input voltage of the resonant inverter.

Equation (133) conducts to the following expression for the buck output voltage:

$$\begin{aligned} V_{buck} = \sqrt{Re\{Z_r\} \cdot R} \cdot I_s &= \frac{\pi\sqrt{2}}{4} \frac{\omega^2 \cdot C_s \cdot M \cdot R}{\sqrt{(\omega^2 C_s L_s - 1)^2 + \omega^2 C_s^2 R^2}} \cdot I_s \\ &= k(\omega, M, R) \cdot I_s \end{aligned} \tag{134}$$

where k is a coefficient depending on the resonance frequency, the mutual inductance and the compensation topology.

If the inverter works at the resonance frequency ω_0, the previous equation becomes:

$$V_{buck} = k_0 \cdot I_s = \frac{\pi\sqrt{2}}{4} \omega_0 \cdot M \cdot I_s \tag{135}$$

One can notice that in this case the coefficient k_0 is independent from the load. If a constant current charging strategy is adopted, the buck output voltage must be tuned in order to compensate variation on resonance frequency and mutual inductance due to parameters variation or misalignment.

A simple method for the dynamic identification of the mutual inductance is based on the voltage measure of three small coupled inductors with the primary coil and working in open circuit. By means of the voltage sense on these measuring inductors and using on a look-up table, the value of the mutual inductance will be estimated. This method will be analyzed in a future work.

5.5 Simulation results

A simulation model of the proposed wireless power transfer system has been implemented in the standalone PLECS tool, including all converter stages, coil section and conduction and switching loss models of the power devices. Extensive simulation have been performed in order to highlight the specific features of this wireless charging system. The main parameters used on the simulation scheme have been reported in **Tab. 7.5**.

In the simulation of **Fig. 5.11**, the primary and secondary currents of the wireless charger are presented while the load resistance is changed from a nominal value of 30 Ω to a value halved (15 Ω). As one can see, I_s is not affected by the load change but only by the resonance frequency and buck output voltage, confirming the validity of equation (135).

Another operating condition is considered in **Fig. 5.12**, where the mutual inductance value drops from the rated value M to a value halved. This situation can easily occur if a certain misalignment exists between the primary and the secondary coils. As shown by **Fig. 5.12**, both the primary and secondary side currents increase demonstrating the validity of equations (135) and (136).

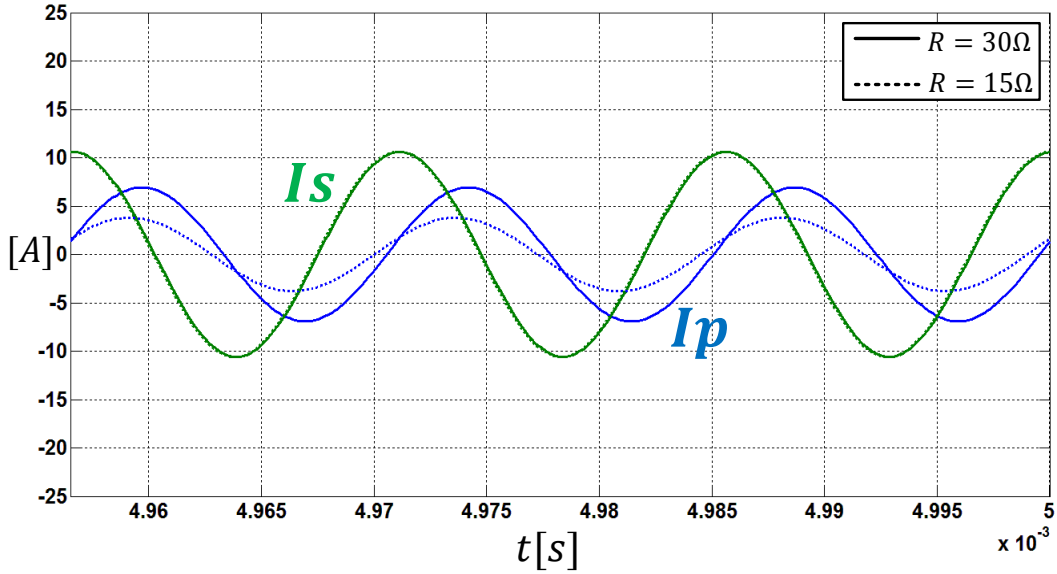


Fig. 5.11: Primary and secondary currents at two R values.

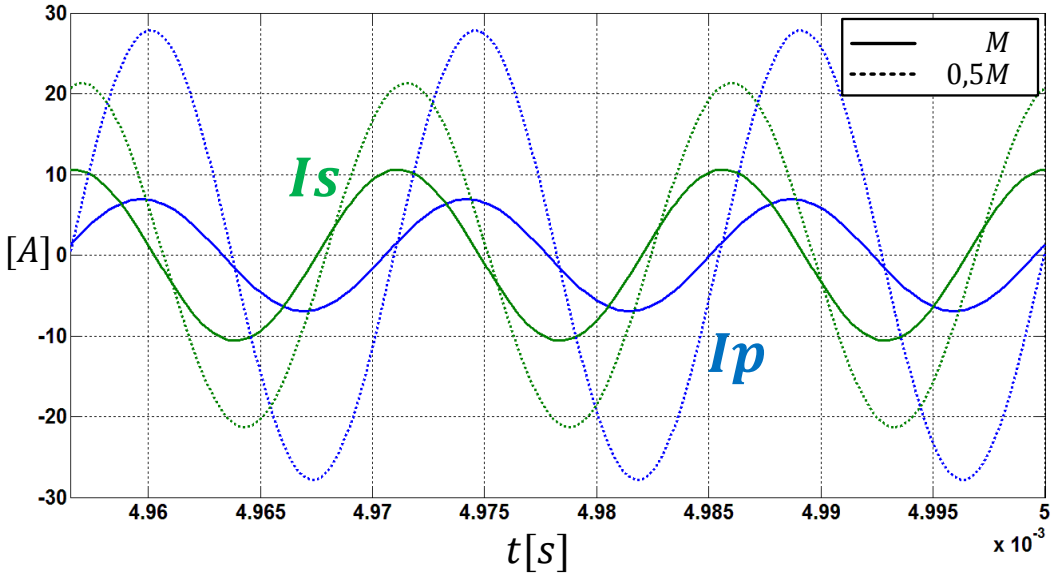


Fig. 5.12: Primary and secondary currents at two M values.

5.6 Prototype and experimental test bench

5.6.1 DC/DC converter

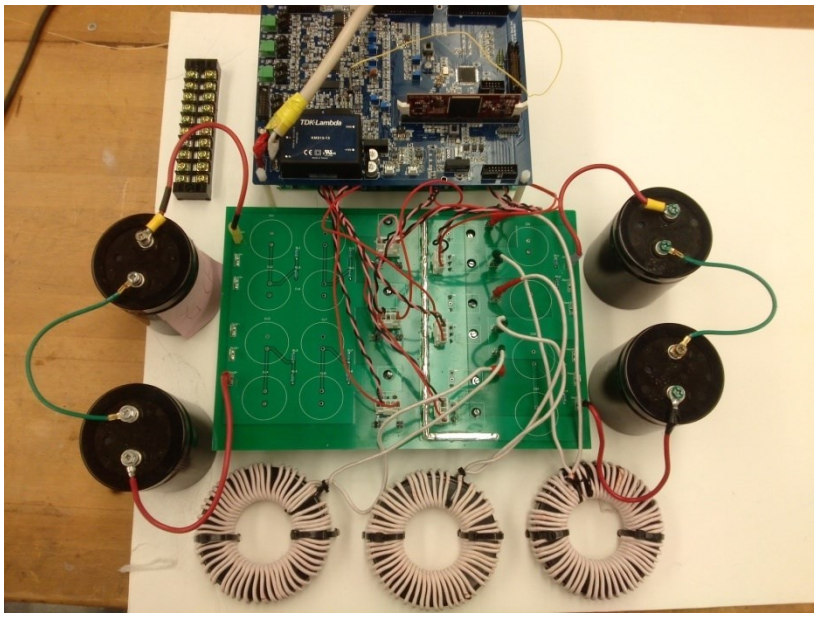


Fig. 5.13: Primary and secondary currents at two M values.

A 24 kW soft-switching bidirectional dc–dc converter prototype with six interleaved phases has been built. The converter is composed by two identical sub-modules delivering half of the total current. **Fig. 5.13** shows a photograph of the power stage sub-module prototype considering three buck phases with digital control based on a TMS320F28335 DSP. The rated switching frequency for the IGBTs has been fixed to 20 kHz, even though the converter can

work in variable switching mode depending on the load value as it will presented in the experimental results section.

5.6.2 Full-bridge resonant inverter

The resonant inverter has been realized with the standard full-bridge topology working with at fixed switching frequency equal to the resonance one and with duty cycle at 50%. The inverter is driven by the same digital control board of the DC/DC converter. Each physical switch has been realized with three SiC (Silicon Carbide) MOSFET SCT2080KE in parallel to achieve a rated 22 kW capability.

5.6.3 Coil structure parameters

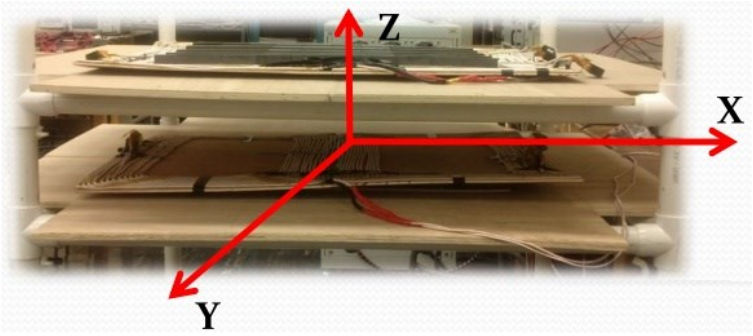


Fig. 5.14: Coils disposition along axis X,Y,Z.

The disposition of the coils along axis X, Y, Z is shown in **Fig. 5.14**. Since the ratio between the input voltage and the output voltage is 1, the transmitting and receiving coils are designed to have to same size. Both coils are made with the same double D (DD) type pad structure. The dimension is 800mm in length and 600 mm in width and the gap between the two coils is 200 mm. The compensation DD pads prototype is shown in **Fig. 5.15**.

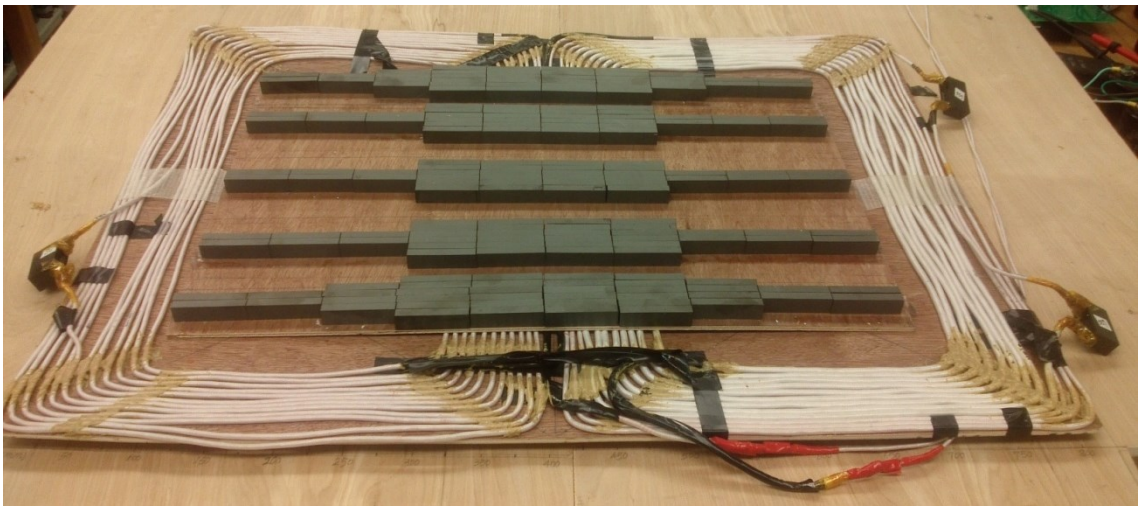


Fig. 5.15: Constructed compensation DD pads.

In wireless EV charging applications, the door-to-door misalignment (defined as X misalignment) usually holds the priority in the design consideration since it is harder for the driver to adjust it. The variations of the self and mutual inductances as a function of the misalignment along X axis and due to the presence or not of the ferrite bars are presented in **Fig. 5.16**. One can notice that in correspondence to 250 mm of misalignment the mutual inductance/coupling coefficient reaches the minimum value, nearly to zero. In this condition, no power can be transferred from the primary to the secondary side.

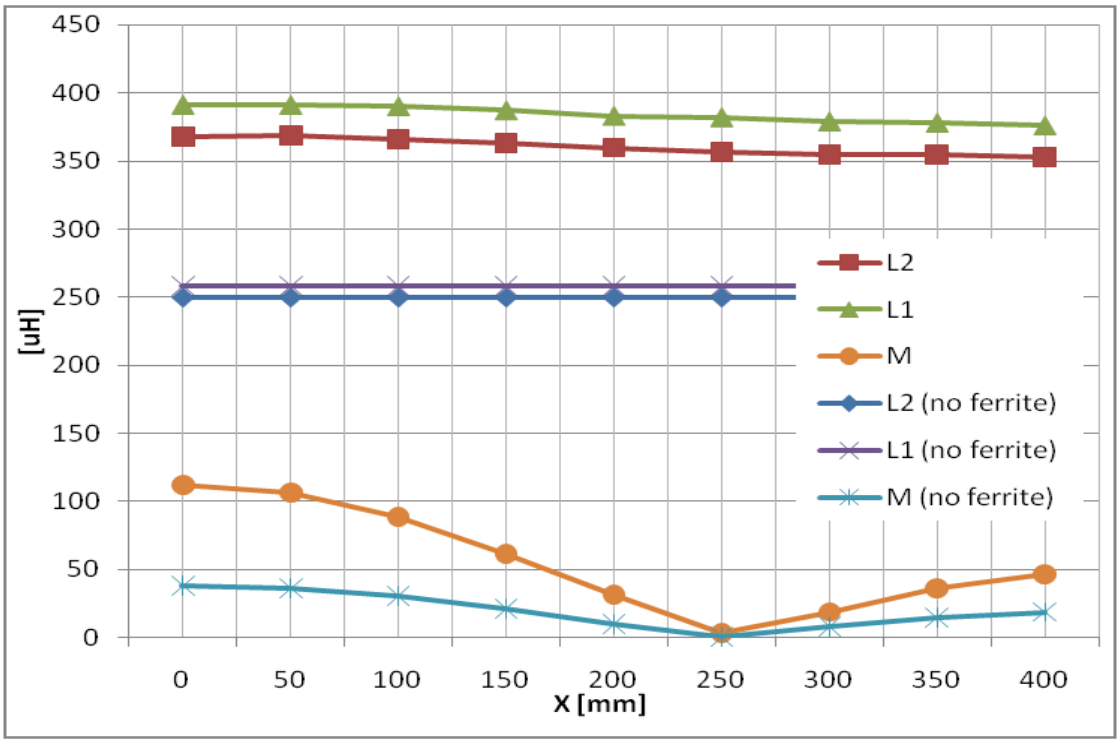


Fig. 5.16: Self and mutual inductance measurements as a function of "X" axis misalignment with and without ferrite.

Moreover, when the heavy ferrite bars are removed, the mutual inductance drops to half its nominal value, affecting the power transfer capability.

5.6.4 Experimental test-bench

Fig. 5.17 shows the experimental setup. The transmitting coil is connected to the input inverter and buck, whereas the receiver coil is connected directly with a resistive load.

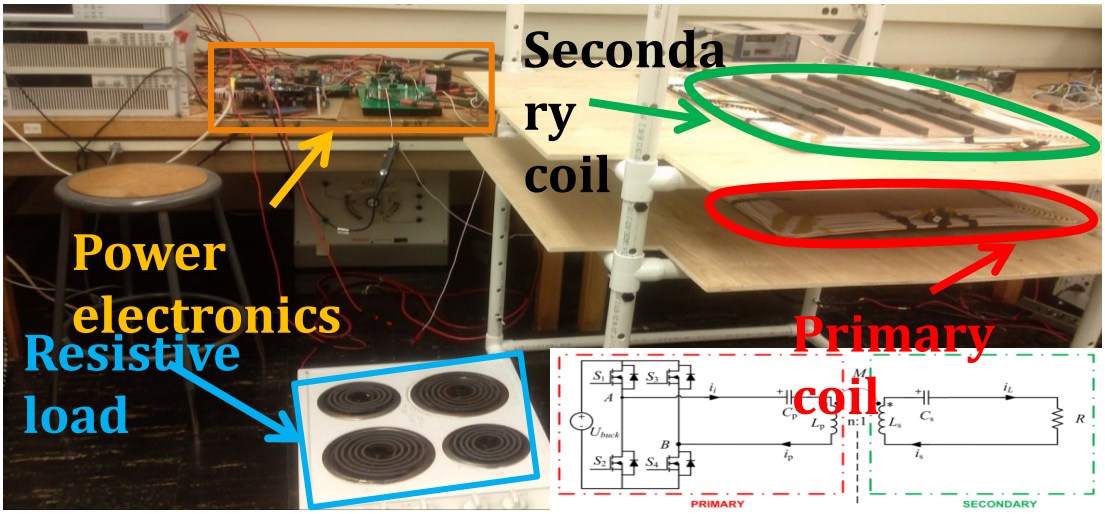


Fig. 5.17: Experimental test bench.

5.7 Experimental results

Extensive experiments have been conduct in order to validate the effectiveness of the proposed converter.

In the first experiment, an electronic load working in resistive mode was adopted to test the soft-switching buck as a standalone DC/DC converter.

Fig. 5.18 shows the first phase gate signal (red line), the output voltage of the second phase (violet line) and the inductor currents (green and blue lines) for the interleaved synchronous buck converter with only two active phases. In this condition the duty cycle of each phase is considered at 75 % and the switching frequency at 20 kHz. As one can notice by the currents shape, the convert realizes soft-switching inverting the current sign in order to switch off naturally the diode in parallel with the IGBT.

When the load changes, the current ripple on phase inductors experiences a variation too, since its dependency on the output current and the fact that the inductance value remains constant. For this reason, the soft-switching operation cannot be achieved in every working condition.

In the experiment of **Fig. 5.19**, a sweep of the switching frequency has been performed in two different load conditions, while the input/output voltage ration was fixed to 0,75. When the load is equal to 35 Ω, the maximum efficiency point is reached at 28 kHz. If the load changes to 50 Ω, the maximum efficiency is achieved working at a higher switching frequency, i.e. 32 kHz. A variable frequency control can be implemented in the buck converter, taking into account possible variations of the output current in steady state conditions. This feature will be examined in depth in a future work.

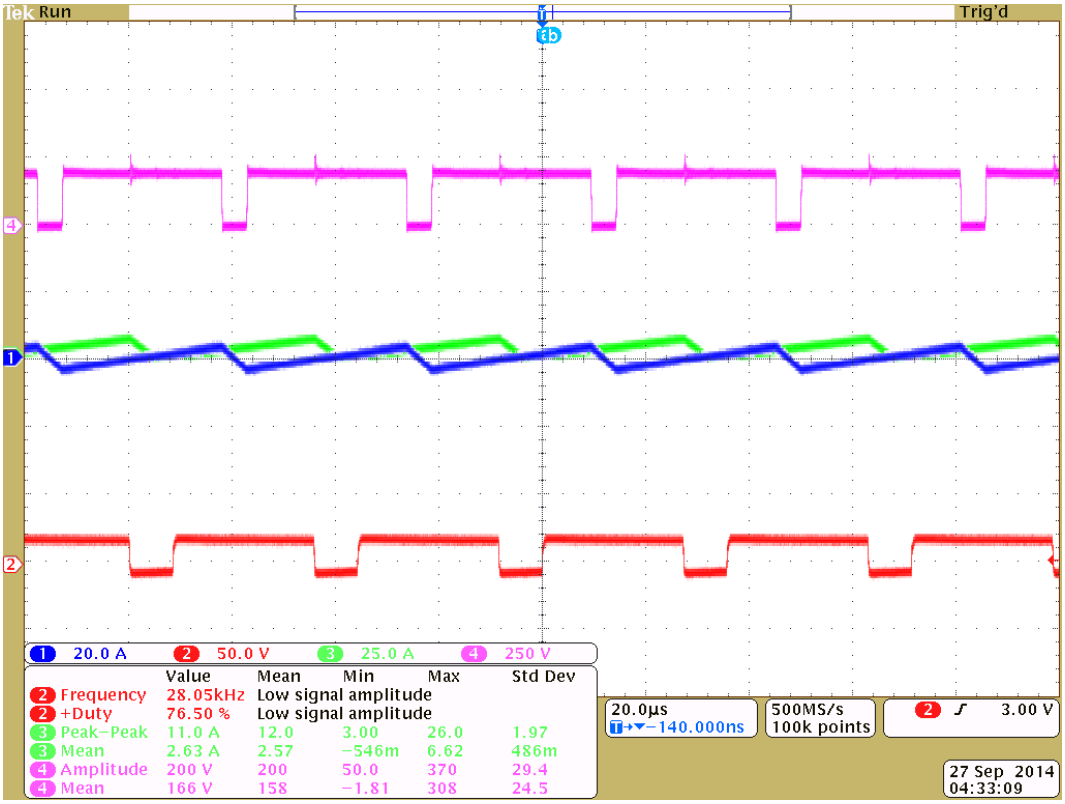


Fig. 5.18: Two phase interleaved synchronous buck experiment.

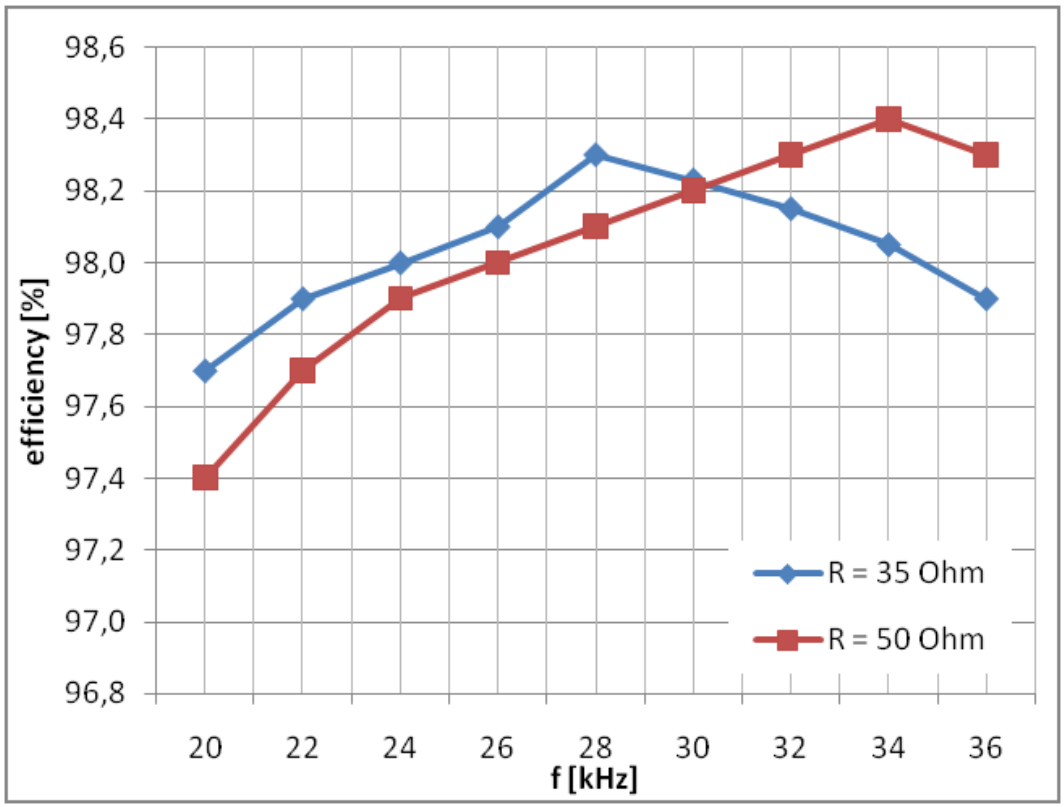


Fig. 5.19: Buck converter efficiency map as a function of the switching frequency for two load values.

A second experiment was related to the wireless power transfer considering the experimental setup of **Fig. 5.17**.

In this test, the input voltage of the full-bridge converter was fixed by the DC/DC converter around 400 V and the AC resistive load was around 30 Ω.. As shown by the screen shot from the power meter Yokogawa WT1600 (**Fig. 5.20**), the power transferred to the secondary side was 4,87 kW with an efficiency around 95 % from DC to AC. The resonance frequency has been tuned to 69 kHz in order to perform the maximum power transfer.

Fig. 5.21 presents the inverter output voltage and current together with one inverter leg gate commands. Experiments at different switching frequencies has been done. When the inverter doesn't work at the resonance, the power transfer efficiency decreases and the output voltage of the inverter experiences more oscillations during the switches. This phenomena happens due to the fact that no soft-switching is guaranteed in these conditions.

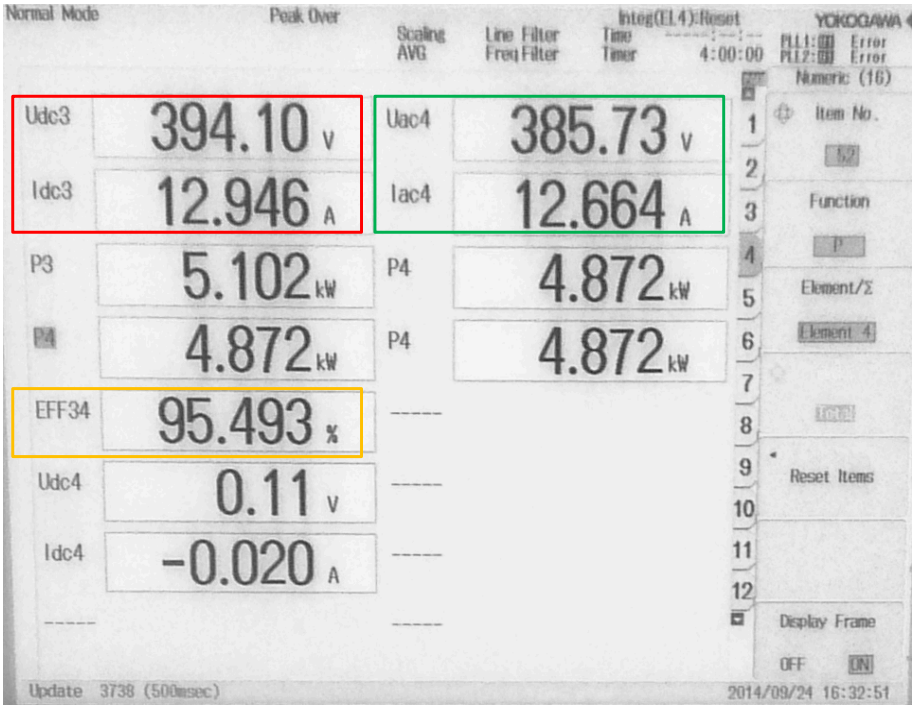


Fig. 5.20: Power transferring main parameters: inverter input voltage and current (red box), secondary side AC load voltage and current (green box), efficiency (yellow box).

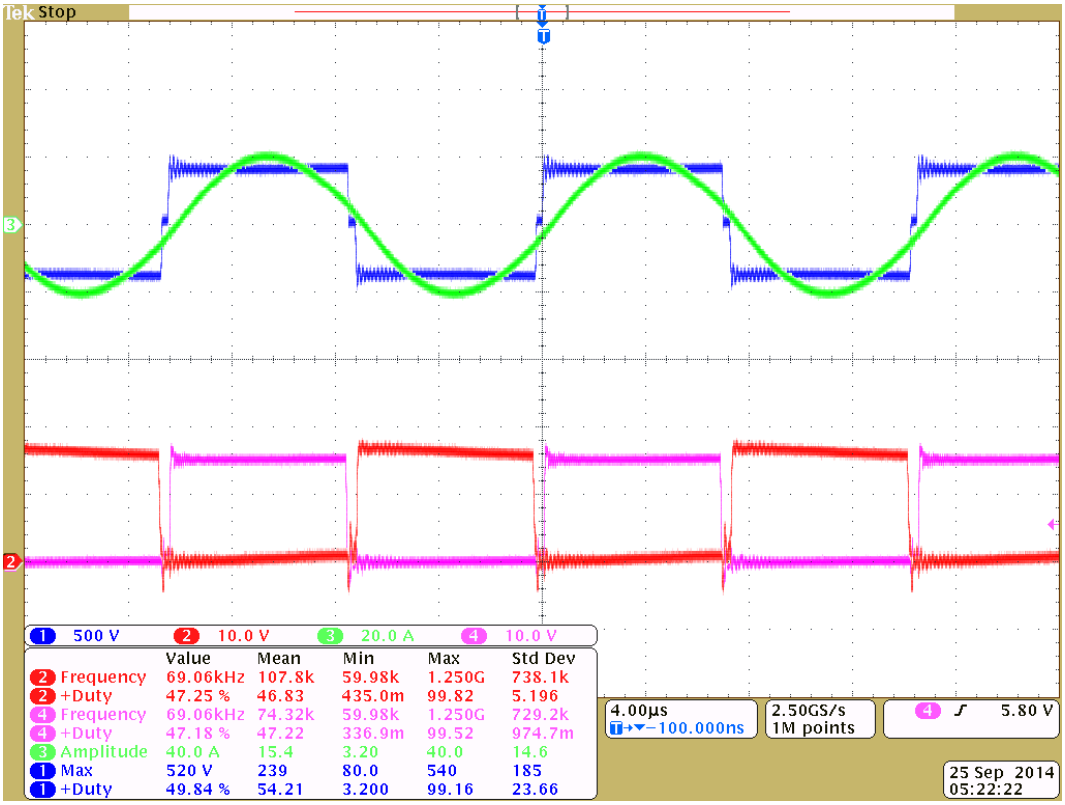


Fig. 5.21: Full-bridge output voltage and current and complementary gate signals.

6 CONCLUSIONS

In the last years environmental issues and constant increase of fuel and energy cost have been incentivizing the development of low emission and high efficiency systems, either in traction field or in distributed generation systems from renewable energy sources.

Moreover, along with the fast growing interest in EVs and PHEVs, wireless charging, as a new way of charging batteries, has drawn the attention of researchers, car manufacturers, and customers recently.

In this work, multiple aspects about power conversion and its applications on hybrid traction and wireless charging has been investigated, starting from the study of the state-of-the-art and then moving on with some original proposals.

In the first part of this dissertation, i.e. Chapter 2 and 3, theory and fundamental aspects of some power converters (DC/AC and DC/DC) has been illustrated.

Chapter 2 has focused the attention on the basic features of the three-level neutral-point-clamped inverter, presenting a review of the state-of-the-art of modulation strategies and proposing some original algorithms, i.e. discontinuous-hybrid, interleaved and adaptive interleaved modulations. Furthermore, an accurate model and compensation of the dead time for the 3L NPC inverter has been developed, including power device and output capacitance effects. Moreover, an analytical approach to power loss estimation based on fundamental equations and power device datasheets has been investigated, focusing in particular on the modulation type influence on switching losses.

In Chapter 3, some non-isolated DC/DC converter topologies has been presented, in particular a bidirectional half-bridge converter and a three level neutral point clamped buck converter. In addition, a novel proposal for a multiphase three-level buck converter has been developed by the author.

In the second part of the dissertation, i.e. Chapter 4 and 5, two real applications of the topologies, previously discussed, has been considered in the fields of hybrid traction and wireless charging.

In Chapter 4 the description, implementation and prototype development of a two stage bi-directional converter suitable for battery charging and mild hybrid traction systems has been reported.

Finally, in Chapter 5 he basics of the inductive power transfer has been illustrated and the design of a 22 kW wireless charger for electric vehicles fast charge has been proposed.

7 APPENDIX

APPENDIX 1

Tab. 7.1 Integrals for HPWM

I^{avg}	T_1
	$\frac{\pi}{6} < \varphi < \pi - D\frac{\pi}{6}$
I_1	0
I_2	0
I_3	$\frac{M}{4}\left\{2\cos\left(\varphi-\frac{\pi}{3}\right)\cdot\cos^2(\varphi)+\sin\left(\varphi-\frac{\pi}{3}\right)\cdot[\sin(2\varphi)-(\pi-2\varphi)]\right\}$
I_4	$\frac{M}{4}\left\{2\cos\left(\varphi-\frac{2}{3}\pi\right)\cdot\left[\cos^2\left(\frac{\pi}{2}-\varphi\right)-\cos^2\left(\frac{5}{6}\pi-\varphi\right)\right]-\sin\left(\varphi-\frac{2}{3}\pi\right)\cdot\left[\sin(\pi-2\varphi)-\sin\left(\frac{5}{3}\pi-2\varphi\right)+2\frac{\varphi}{3}\right]\right\}$
I_5	$\frac{M\sqrt{3}}{4}\left\{\cos(\varphi)\cdot\left[\sin\left(\frac{5}{3}\pi-2\varphi\right)-\sin\left(2\pi-\mathrm{D}\frac{\pi}{3}-2\varphi\right)+2\pi-(D+5)\frac{\pi}{3}\right]+2\sin(\varphi)\cdot\left[\cos^2\left(\frac{5}{6}\pi-\varphi\right)-\cos^2\left(\pi-\mathrm{D}\frac{\pi}{6}-\varphi\right)\right]\right\}$
I_6	$\frac{M}{4}\left\{2\cos\left(\varphi-\frac{2}{3}\pi\right)\cdot\left[\cos^2\left(\pi-\mathrm{D}\frac{\pi}{6}-\varphi\right)-\cos^2\left(\pi+\mathrm{D}\frac{\pi}{6}-\varphi\right)\right]-\sin\left(\varphi-\frac{2}{3}\pi\right)\cdot\left[\sin\left(\frac{5}{3}\pi-2\varphi\right)-\sin\left(2\pi-\mathrm{D}\frac{\pi}{3}-2\varphi\right)+2\pi-(D+5)\frac{\pi}{3}\right]\right\}$
	$D\frac{\pi}{6} < \varphi < \frac{\pi}{6}$
I_1	0
I_2	$\frac{M\sqrt{3}}{4}\left\{\cos(\varphi)\cdot\left[\frac{\pi}{3}-2\varphi-\sin\left(\frac{\pi}{3}-2\varphi\right)\right]+2\sin(\varphi)\cdot\sin^2\left(\frac{\pi}{6}-\varphi\right)\right\}$
I_3	$\frac{M}{4}\left\{2\cos\left(\varphi-\frac{\pi}{3}\right)\cdot\left[\cos^2\left(\frac{\pi}{6}-\varphi\right)-\sin^2(\varphi)\right]+\sin\left(\varphi-\frac{\pi}{3}\right)\cdot\left[\sin\left(\frac{\pi}{3}-2\varphi\right)-\sin(\pi-2\varphi)-\frac{2}{3}\pi\right]\right\}$

I_4	$\frac{M}{4}\left\{2\cos\left(\varphi-\frac{2}{3}\pi\right)\cdot\left[\cos^2\left(\frac{\pi}{2}-\varphi\right)-\cos^2\left(\frac{5}{6}\pi-\varphi\right)\right]-\sin\left(\varphi-\frac{2}{3}\pi\right)\cdot\left[\sin(\pi-2\varphi)-\sin\left(\frac{5}{3}\pi-2\varphi\right)+2\frac{\varphi}{3}\right]\right\}$
I_5	$\frac{M\sqrt{3}}{4}\left\{\cos(\varphi)\cdot\left[\sin\left(\frac{5}{3}\pi-2\varphi\right)-\sin\left(2\pi-\mathrm{D}\frac{\pi}{3}-2\varphi\right)+2\pi-(D+5)\frac{\pi}{3}\right]+2\sin(\varphi)\cdot\left[\cos^2\left(\frac{5}{6}\pi-\varphi\right)-\cos^2\left(\pi-\mathrm{D}\frac{\pi}{6}-\varphi\right)\right]\right\}$
I_6	$\frac{M}{4}\left\{2\cos\left(\varphi-\frac{2}{3}\pi\right)\cdot\left[\cos^2\left(\pi-\mathrm{D}\frac{\pi}{6}-\varphi\right)-\cos^2\left(\pi+\mathrm{D}\frac{\pi}{6}-\varphi\right)\right]-\sin\left(\varphi-\frac{2}{3}\pi\right)\cdot\left[\sin\left(2\pi-D\frac{\pi}{3}-2\varphi\right)-\sin\left(2\pi+\mathrm{D}\frac{\pi}{3}-2\varphi\right)+2D\frac{\pi}{3}\right]\right\}$
$\varphi<\frac{\pi}{6}$	
I_1	$\frac{M}{4}\left\{2\cos\left(\varphi-\frac{\pi}{3}\right)\cdot\sin^2\left(\mathrm{D}\frac{\pi}{6}-\varphi\right)-\sin\left(\varphi-\frac{\pi}{3}\right)\cdot\left[D\frac{\pi}{3}-2\varphi-\sin\left(D\frac{\pi}{3}-2\varphi\right)\right]\right\}$
I_2	$\frac{M\sqrt{3}}{4}\left\{\cos(\varphi)\cdot\left[\sin\left(D\frac{\pi}{3}-2\varphi\right)-\sin\left(\frac{\pi}{3}-2\varphi\right)+(1-D)\frac{\pi}{3}\right]+2\sin(\varphi)\cdot\left[\cos^2\left(D\frac{\pi}{6}-\varphi\right)-\cos^2\left(\frac{\pi}{6}-\varphi\right)\right]\right\}$
I_3	$\frac{M}{4}\left\{2\cos\left(\varphi-\frac{\pi}{3}\right)\cdot\left[\cos^2\left(\frac{\pi}{6}-\varphi\right)-\sin^2(\varphi)\right]-\sin\left(\varphi-\frac{\pi}{3}\right)\cdot\left[\sin\left(\frac{\pi}{3}-2\varphi\right)-\sin(\pi-2\varphi)-\frac{2}{3}\pi\right]\right\}$
I_4	$\frac{M}{4}\left\{2\cos\left(\varphi-\frac{2}{3}\pi\right)\cdot\left[\cos^2\left(\frac{\pi}{2}-\varphi\right)-\cos^2\left(\frac{5}{6}\pi-\varphi\right)\right]-\sin\left(\varphi-\frac{2}{3}\pi\right)\cdot\left[\sin(\pi-2\varphi)-\sin\left(\frac{5}{3}\pi-2\varphi\right)+2\frac{\varphi}{3}\right]\right\}$
I_5	$\frac{M\sqrt{3}}{24}\left\{\cos(\varphi)\cdot\left[12\sin\left(D\frac{\pi}{6}\right)\cos\left(D\frac{\pi}{6}\right)+2\pi-(D+5)\frac{\pi}{3}-3\sqrt{3}+(1-D)2\pi\right]+\sin(\varphi)\cdot\left[12\cos^2\left(D\frac{\pi}{6}\right)-9\right]\right\}$
I_6	$\frac{M}{4}\left\{2\cos\left(\varphi-\frac{2}{3}\pi\right)\cdot\left[\cos^2\left(\pi-\mathrm{D}\frac{\pi}{6}-\varphi\right)-1\right]-\sin\left(\varphi-\frac{2}{3}\pi\right)\cdot\left[\sin\left(2\pi-D\frac{\pi}{3}-2\varphi\right)+2D\frac{\pi}{3}+2\varphi\right]\right\}$

I^{avg}	T_2
	$\frac{\pi}{6} < \varphi < \pi - D\frac{\pi}{6}$
$I_1 + I_2$	0
$I_3 + I_4 + I_5$	$1 + \cos\left(D\frac{\pi}{6} + \varphi\right)$
I_6	$\cos\left(D\frac{\pi}{6} - \varphi\right) - \cos\left(D\frac{\pi}{6} + \varphi\right) - \frac{M}{4}\left\{2\cos\left(D\frac{\pi}{3} - \varphi\right) \cdot \left[\cos^2\left(D\frac{\pi}{6} + \varphi\right) - \cos^2\left(D\frac{\pi}{6} - \varphi\right)\right] + \sin\left(D\frac{\pi}{3} - \varphi\right) \cdot \left[2D\frac{\pi}{3} - \sin\left(D\frac{\pi}{3} + 2\varphi\right) - \sin\left(D\frac{\pi}{3} - 2\varphi\right)\right]\right\}$
I_7	$1 - \cos\left(D\frac{\pi}{6}\right) - \frac{M\sqrt{3}}{4}\left\{\cos(\varphi) \cdot \left[\frac{D\pi}{3} - 2\varphi + \sin\left(D\frac{\pi}{3} - 2\varphi\right)\right] + 2\sin\left(\varphi - \frac{\pi}{3}\right) \cdot \left[\cos^2\left(D\frac{\pi}{6} - \varphi\right) - 1\right]\right\}$
	$D\frac{\pi}{6} < \varphi < \frac{\pi}{6}$
$I_1 + I_2$	0
$I_3 + I_4 + I_5$	$1 + \cos\left(D\frac{\pi}{6} + \varphi\right)$
I_6	$\cos\left(D\frac{\pi}{6} - \varphi\right) - \cos\left(D\frac{\pi}{6} + \varphi\right) - \frac{M}{4}\left\{2\cos\left(D\frac{\pi}{3} - \varphi\right) \cdot \left[\cos^2\left(D\frac{\pi}{6} + \varphi\right) - \cos^2\left(D\frac{\pi}{6} - \varphi\right)\right] + \sin\left(D\frac{\pi}{3} - \varphi\right) \cdot \left[2D\frac{\pi}{3} - \sin\left(D\frac{\pi}{3} + 2\varphi\right) - \sin\left(D\frac{\pi}{3} - 2\varphi\right)\right]\right\}$
I_7	0
	$\varphi < \frac{\pi}{6}$
I_1	0

I_2	$\cos\left(D\frac{\pi}{6}-\varphi\right)-\cos\left(D\frac{\pi}{6}+\varphi\right)$ $-\frac{M}{4}\left\{2\cos\left(D\frac{\pi}{3}-\varphi\right)\cdot\left[\cos^2\left(D\frac{\pi}{6}+\varphi\right)-\cos^2\left(D\frac{\pi}{6}-\varphi\right)\right]\right.$ $+\sin\left(D\frac{\pi}{3}-\varphi\right)$ $\left.\cdot\left[2D\frac{\pi}{3}-\sin\left(D\frac{\pi}{3}+2\varphi\right)-\sin\left(D\frac{\pi}{3}-2\varphi\right)\right]\right\}$
I_3+I_4 $+I_5$	$\cos\left(D\frac{\pi}{6}-\varphi\right)+\cos\left(D\frac{\pi}{6}+\varphi\right)$
I_6	$\cos\left(D\frac{\pi}{6}-\varphi\right)-\cos\left(D\frac{\pi}{6}+\varphi\right)$ $-\frac{M}{4}\left\{2\cos\left(D\frac{\pi}{3}-\varphi\right)\cdot\left[\cos^2\left(D\frac{\pi}{6}+\varphi\right)-\cos^2\left(D\frac{\pi}{6}-\varphi\right)\right]\right.$ $+\sin\left(D\frac{\pi}{3}-\varphi\right)$ $\left.\cdot\left[2D\frac{\pi}{3}-\sin\left(D\frac{\pi}{3}+2\varphi\right)-\sin\left(D\frac{\pi}{3}-2\varphi\right)\right]\right\}$
I_7	0

Calculation steps

$$I_{T/D}^{avg}=\frac{1}{2\pi}\int_0^{2\pi} d_{T_1}(\alpha)i_L(\alpha)d\alpha = I_F{}^{max}\cdot\frac{1}{2\pi}\sum_{i=1}^{n} I_i \tag{136}$$

T_1

$$\begin{aligned} I_1 &= \int_{\varphi}^{D\pi/6} sin(\alpha-\varphi)\, M\, cos\left(\theta+\frac{5}{6}\pi\right)d\alpha \\ &= M\sqrt{3}\int_{\varphi}^{D\pi/6} sin(\alpha-\varphi)\, cos\left(\alpha-\frac{\pi}{3}\right)d\alpha \\ &= M\sqrt{3}\int_{0}^{D\pi/6-\varphi} sin(\gamma)\, cos\left(\gamma+\varphi+\frac{3}{2}\pi\right)d\gamma \end{aligned} \tag{137}$$

$$I_2 = \int_{\varphi}^{\pi/6} sin(\alpha-\varphi)\, M\sqrt{3}\, cos(\theta+\pi)\, d\alpha$$
$$= M\sqrt{3}\int_{\varphi}^{\pi/6} sin(\alpha-\varphi)\, cos\left(\alpha-\frac{\pi}{3}\right) d\alpha \quad (138)$$
$$= M\sqrt{3}\int_{0}^{\pi/6-\varphi} sin(\gamma)\, cos\left(\gamma+\varphi+\frac{3}{2}\pi\right) d\gamma$$

$$I_3 = \int_{\varphi}^{\frac{\pi}{2}} sin(\alpha-\varphi)\, M\, cos\left(\theta-\frac{\pi}{6}\right) d\alpha = M\int_{\varphi}^{\frac{\pi}{2}} sin(\alpha-\varphi)\, cos\left(\alpha-\frac{\pi}{3}\right) d\alpha$$
$$= M\int_{0}^{\frac{\pi}{2}-\varphi} sin(\gamma)\, cos\left(\gamma+\varphi-\frac{\pi}{3}\right) d\gamma \quad (139)$$

$$I_4 = \int_{\pi/2}^{5/6\pi} sin(\alpha-\varphi)\, M\, cos\left(\theta-\frac{\pi}{6}\right) d\alpha = M\int_{\pi/2}^{5/6\pi} sin(\alpha-\varphi)\, cos\left(\alpha-\frac{2}{3}\pi\right) d\alpha$$
$$= M\int_{0}^{\frac{\pi}{2}-\varphi} sin(\gamma)\, cos\left(\gamma+\varphi-\frac{2}{3}\pi\right) d\gamma \quad (140)$$

$$I_5 = \int_{5/6\pi}^{\pi-D\pi/6} sin(\alpha-\varphi)\, M\sqrt{3}\, cos(\theta)\, d\alpha$$
$$= M\sqrt{3}\int_{5/6\pi}^{\pi-D\pi/6} sin(\alpha-\varphi)\, cos\left(\alpha-\frac{2}{3}\pi\right) d\alpha \quad (141)$$
$$= M\sqrt{3}\int_{5/6\pi-\varphi}^{\pi-D\pi/6-\varphi} sin(\gamma)\, cos\left(\gamma+\varphi-\frac{\pi}{2}\right) d\gamma$$

$$I_6 = \int_{\pi-D\pi/6}^{\pi+D\pi/6} sin(\alpha-\varphi)\, M\, cos\left(\theta-\frac{\pi}{6}\right) d\alpha$$
$$= M\sqrt{3}\int_{\pi-D\pi/6}^{\pi+D\pi/6} sin(\alpha-\varphi)\, cos\left(\alpha-\frac{2}{3}\pi\right) d\alpha \quad (142)$$
$$= M\int_{\pi-D\pi/6}^{\pi+D\pi/6-\varphi} sin(\gamma)\, cos\left(\gamma+\varphi-\frac{\pi}{2}\right) d\gamma$$

T_2

$$I_1 = \int_{\varphi}^{\pi/6} 1 \cdot sin(\alpha - \varphi)\, d\alpha = 1 - cos\left(\frac{\pi}{6} - \varphi\right) \tag{143}$$

$$I_2 = \int_{D\pi/6}^{\pi/6} 1 \cdot sin(\alpha - \varphi)\, d\alpha = 1 - cos\left(D\frac{\pi}{6} - \varphi\right) \tag{144}$$

$$I_3 + I_4 + I_5 = \int_{\varphi}^{\pi - D\pi/6} 1 \cdot sin(\alpha - \varphi)\, d\alpha = 1 + cos\left(D\frac{\pi}{6} - \varphi\right) \tag{145}$$

$$\begin{aligned} I_6 &= \int_{\pi - D\pi/6}^{\pi + D\pi/6} \left[1 - M\left|cos\left(\alpha - \frac{2}{3}\pi\right)\right|\right] \cdot sin(\alpha - \varphi)\, d\alpha \\ &= \int_{\pi - D\pi/6 - \varphi}^{\pi + D\pi/6 - \varphi} sin(\gamma)\, d\gamma \\ &\quad - M\int_{\pi - D\pi/6 - \varphi}^{\pi + D\pi/6 - \varphi} \left|cos\left(\gamma + \varphi - \frac{2}{3}\pi\right)\right| sin(\gamma)\, d\gamma \end{aligned} \tag{146}$$

$$\begin{aligned} I_7 &= \int_{\pi + D\pi/6}^{\pi + D\pi/6} \left[1 - M\sqrt{3}\left|cos\left(\alpha - \frac{\pi}{2}\right)\right|\right] \cdot sin(\alpha - \varphi)\, d\alpha \\ &= \int_{\pi - D\pi/6 - \varphi}^{\pi + D\pi/6 - \varphi} 1 \cdot d\gamma - M\int_{\pi - D\pi/6 - \varphi}^{\pi + D\pi/6 - \varphi} \left|cos\left(\gamma + \varphi - \frac{2}{3}\pi\right)\right| sin(\gamma)\, d\gamma \end{aligned} \tag{147}$$

Appendix 2

Tab. 7.2 System Parameters in [Apec2013]

Parameter	*Symbol*	*Value*
Bus-DC voltage	V_{DC}	$650\ V$
Semi-bus capacitance	$C_1 = C_2$	$1880\ \mu F$
Modulation index	m	1
Modulating frequency	f_m	$50\ Hz$
Switching frequency	f_{sw}	$8\ kHz$
Nominal power	P_n	$10\ kW$
Power factor	PF	1
Switch dead-time	t_{dt}	$2\ \mu s$

Tab. 7.3 Parameters of the NPC inverter, load and SPM motor.

Parameter	**Symbol**	**Value**
DC link voltage	U_{dc}	150 $[V]$
DC link capacitance	C_i	2700 $[\mu F]$
PWM modulation period	T_{sw}	100 $[\mu s]$
Fundamental frequency	f_{fund}	50 $[Hz]$
Load resistance	R_{load}	3 [Ω]
Load inductance	L_{load}	6 $[mH]$
Pole pairs	pp	9
Stator slots	Q	27
External stator diameter	D_e	156 $[mm]$
Stack length	L_{stk}	35 $[mm]$
Rated torque	T_n	10 $[Nm]$
Rated phase current	$\|i\|_{n,rms}$	25 $[Arms]$
Rated speed	n_n	3000 $[rpm]$
Rated frequency	f_n	450 $[Hz]$
Rated phase voltage	U_n	60 $[Vrms]$
Stator resistance	R_s	75 $[m\Omega]$
Phase inductance	L_s	0.23 $[mH]$

Tab. 7.4 Parameters of the two-phase three-level Buck Converter.

Parameter	Symbol	Value
DC link voltage	U_{dc}	700 $[V]$
DC link capacitance	$C_1 = C_2$	120 $[\mu F]$
Phase inductance	$L_1 = L_2 = L_3 = L_4$	400 $[\mu H]$
Inductor resistance	R_L	40 $[m\Omega]$
Output capacitance	C_o	60 $[\mu F]$
Switching frequency	f_{sw}	10 $[kHz]$

Tab. 7.5 Parameters of the wireless charger.

Primary coil inductance	L_p	**390 μH**
Secondary coil inductance	L_s	**370 μH**
Mutual inductance	M	**112 μH**
Resonance frequency	ω_0	**69 kHz**
Primary capacitance	C_p	**14 nF**
Secondary capacitance	C_s	**15,1 nF**
Load resistance	R	**30,5 Ω**

Tab. 7.6 Interleaved half-bridge parameters for each phase.

Parameter	Symbol	Value
Number of phases	N	4
Switching frequency	F_{SW}	50 kHz
Maximum dc bus voltage	V_{DC}	150 V
Maximum battery voltage	V_{BAT}	30 V
Maximum battery current	I_{BAT}	32 A
Output Inductance	L_p	50 μH
Output Inductance Resistance	R_{L_p}	9 $m\Omega$

Tab. 7.7 Active NPC inverter parameters.

Parameter	Symbol	Value
Switching frequency	F_{SW}	20 kHz
Rated dc bus voltage	V_{DC}	150 V
Rated ac phase voltage	V_{AC}	60 V_{rms}
Rated ac phase current	I_{AC}	35 A_{rms}

Tab. 7.8 Electric machine parameters.

Parameter	Symbol	Value
Pole number	$2p$	18
Slot number	Q	27
External stator diameter	D_e	156 mm
Stack length	L_{stk}	35 mm
Rated torque	T_N	10 Nm
Rated phase current	I_N	25 A_{rms}
Rated phase voltage	V_N	60 V_{rms}
Phase resistance	R_s	75 $m\Omega$
Phase inductance	L_s	0.23 mH
Rated speed	n_{max}	4000 rpm

Tab. 7.9 Switch device parameters at 100°C.

Parameter	Value	
	dc/dc converter	NPC converter
Type of switch	Mosfet	Mosfet
Maximum voltage	200 V	100 V
Rated current	50 A	130 A
On resistance	35 $m\Omega$	6.5 $m\Omega$
t''_{rise}	0.8 ns/A	0.7 ns/A
t''_{fall}	1.8 ns/A	1.4 ns/A

Tab. 7.10 ICE model notations list.

Symbol	Definition
x	Cylinder axis
y	Axis perpendicular to the x-axis and crankshaft rotation axis
z	Horizontal axis coplanar with x and y-axes
x_{max}	Maximum distance between crankshaft rotation axis and the cylinder head
x_c	Distance between crankshaft rotation axis and the cylinder head
α	Angle between the crank axis and the x-axis, increasing clockwise
ϑ	Angle between x-axis and z-axis, increasing counterclockwise
β	Angle between the connecting rod axis and the x-axis, increasing counterclockwise
r	Crank length
d	Piston bore
c	Connecting rod length
a, b	coordinates of the connecting rod gravity center in relation to its extreme
G	Connecting rod mass center

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