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PHD THESIS

An isolated quasi-resonant multilevel dc-dc converter Multi-Phase Single-Stage Topology for 380 V VRM application

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Abstract

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The power supply evolution for data centers and networking applications demands a continuous improvement in the efficiency at system and converter levels. Higher voltage distribution system and less conversion steps are necessary to increase the efficiency of the overall distribution system. To implement more efficient power conversion systems 48 V dc at rack level recently has been adopted ensuring higher overall efficiency, isolation design and phase shedding in light load; but rack-level dc distribution can be performed at a higher level of dc voltage such as 380 V dc. An advantage over 48 V dc distribution is that a more efficient ac/dc converter may be used, resulting in higher overall efficiency. For higher voltage dc distribution system a voltage regulator modules (VRM) is currently realized using a two-stage approach, with an intermediate 12 V dc bus.

The challenge is to operate at high-efficiency with a single stage conversion directly from 380 V dc bus operating as high-voltage point-of-load (HV POL) converter, including a multi-phase approach and phase-shedding capabilities, maintaining high power density and dynamic performance comparable with 48 V VRM single-stage.

This dissertation presents an innovative single-stage approach for the 380 V VRM based on a quasi-resonant multilevel topology constant on-time (COT) operation. The proposed topology inherently integrates the multiphase approach, providing fast phase shedding and flat high efficiency curves even at light load conditions. This is a unique advantage, which is not possible to establish in the two stage approach, which is very important in server architectures, and where high efficiency is required even at light load conditions. This dissertation analyses different high step down topologies including the aforementioned multilevel one, comprising a control architecture for fast transient response, the current sharing capabilities, and a solution for implementing the integrated magnetics.

Experimental results show an efficiency of 93% for a 120 A, 380 V-1.8 V VRM power supply.

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Chapter 1

Introduction

This chapter presents the motivations, objectives and an overview of this dissertation. The challenges of the state-of-the-art of $Power\ Distribution\ System\ Architecture\ in\ Data\ Centers$ are investigated to determinate how they can fulfill the energy efficiency requirement and the power delivery demands of future microprocessors. This chapter provides a reviews of this field, followed by the scope of research.

1.1 Data Centers Energy Efficiency

Climate change is recognised as one of the key challenges that the modern society is facing. The Information Technology (IT) sector, including data centers, generates up to 2% of CO_2 emissions. Today 12 million computer servers in 3 million data centers deliver all United States on-line activities [1] and also we have been seeing a rapid increase of cloud computing and the high demand for digital content. In 2030 slightly 12% of the total electric power will be used to supply data centers [2] [3]. On the contrary, the progress in energy efficiency for data center power distribution system is slower than it needs to be.

Among the measures to mitigate the impact of climate change a key component is the energy efficiency of all systems. The energy consumption can be attributed primarily to the IT demands and cooling system but actually is not the only issue that a power distribution system is facing. Indeed, today in data centers, the most common operating points corresponds with the lowest energy-efficiency region [4], on the other hand the highest energy-efficiency region correspond with uncommon operating points. Most of servers in data centers are on 24/7 waiting to receive data just only because the processing power capacity of servers is typically planned to handle the peak annual traffic. This paradox will require significant rethinking of components and systems at power architecture level.

Power architecture should address between the energy-efficiency equipment used in data centers and the behaviour of server workloads. An ideally machine should consume zero power when idle and gradually more power proportionally with the activity level. Thus, new design rules should be based on assumptions: *without data to elaborate there is not energy consumption*. Actually it is not possible, but following this concept this dissertation would address these challenges.

1.1.1 Power Usage

Power usage is also an important concern in designing power delivery architecture. In a typical data center more or less than half of energy consumed is delivered to computer load, on the other hand the second half is lost in power conversion and cooling. As reported in section 1.1 this is partially due to the power delivery architecture which is not designed on the assumption that a lot of machines work in idle mode. In almost all data centers, all around the world, the hardware does not easily adapt its power usage at different load condition. This dilemma can be overcome by projecting the hardware with the concept of *energy proportionality* which is the only way to improve the overall efficiency. Indeed, energy optimization is a complex end to end problem, because is requiring an intricate coordination between hardware, software, applications, security rules and operations organizations.

Even if the overall power consumption will vary significantly depending on the power architecture system from the grid system to the motherboard, it is important to be aware how energy is used in a typical data center motherboard [5]. For a given workload the graph in Fig. 1.1 indicates the CPU as the dominator of energy consumption because has been adopted a better thermal management which allow to run the CPU to their maximum power envelope, whilst the memory consumption presents a reversed trend due to better energy management and new memory technology. In DRAM, voltage has dropped from 1.8 V down to 1.2 V

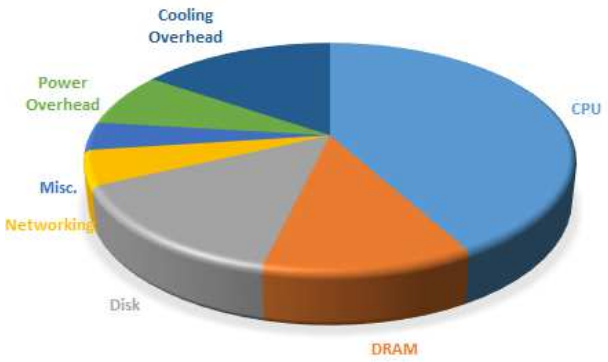


FIGURE 1.1: Approximate distribution of power usage in a modern data center.

1.1.2 Source of Efficiency losses in Data Centers and Energy-Proportional

As discussed earlier, energy management in data center is now one of the key issue for this business. In this scenario the reduction of all energy-related costs and environmental impact is very important. Many energy saving techniques have been developed in the last few decades to fill the gaps at all conversions level. Thus, it is important to be aware about these conversions step: from the grid the first two transformation steps from 100 kV to 10-15 kV and then down to typically 480 V are usually very efficiency around typically

half a percentage point. Inside the building the UPS causes most of the electrical losses (around 88% of efficiency), due to two steps conversion AC/DC DC/AC. After the UPS there is the power distribution unit with low losses, then down to the rack with a very long cable >100m. Typically the distribution energy usage in a conventional data center is 50% in the IT equipment whilst 25% comes from the cooling system which is historical due to lack of attention to efficiency [6]. A better power system architecture can greatly decrease the overall consumption because it can reduce at the same time cooling system power usage.

As reported in section 1.1.1 CPU is the dominator of energy consumption which historically have bad reputation regarding the power usage. Consequently, today in data centers one of the main problem is the *Energy Proportional* issue [4]. The mismatch between server workload and server energy efficiency, of the power delivery system, must be fixed at hardware level. The system are inefficient when lightly used because lack of attention from hardware engineers, about the importance of all energy efficiency region. In the last years the energy proportionality has been added as a design goal. The assumption of linearity between activity and power usage is one of the main reason of the research activities presented in this dissertation.

1.2 Power Distribution System Architecture in Data Center and New Proposed Architecture

The purpose of this section is to hand over a general background about the typical power distribution system architecture in data center. Before going deeply in details about power distribution system at rack level, it is important to clarify what is rack level and give a general overview of what there is from the grid system to the rack.

Power first enters at a utility station transforming the high voltage 110 kV to the medium voltage 50 kV. The medium voltage is used for the distribution in the site where there are unit substations for medium-to-low voltage transformation, typically bellow 1 kV. From here the low-voltage lines going to the uninterruptible-power-supply system (UPS) which in general take a second feed from a set of diesel generators. From the UPS the lines are routed to the data center floor and finally connected to Power Distribution Units (PDU). PDUs, in a typical power distribution system architecture are the last layer before the facility-level distribution system [5]. Existing power architectures may be divided into three categories: rack-level DC, facility-level DC and AC [7].

Through an analysis of several Power Distribution System at facility level in [8] is shown that different architectures give an important improvement for the overall power conversion efficiency.

Before explain what is a typical power distribution system at rack level it is important to understand what are the digital loads in data center and why their power consumption is increasing.

1.2.1 Evolution of Microprocessors

The central processing units CPU are the hear of computation in a server's motherboard. In order to achieve more powerful computation more and more transistor are integrated with higher clock frequency. In Fig. 1.2(a) are reported the number of transistors in a microprocessor. This number has been growing exponentially from 2300 to 1 billion transistor from 1974 to 2013 [9] [10]. Even the trend of the clock frequency, reported in Fig. 1.2(b) has been growing from 108 kHz to over 3 GHz. In general, the approximate power consumption of a typical CPU is proportional to the clock frequency.

From 2005 Intel and IBM has been adopted multi-core technology to boost the performance of the CPU without increasing the clock frequency, as is possible to get from Fig. 1.2(b). The core counts will keep increasing every year because of the general advantages in the computation performance [11]. Regarding the design of the thermal power the cores utilization have been become important, in fact, in order to further minimize the thermal dissipation each core has been powered by an individual voltage rail. The strategy, to save energy, is to adjust dynamically according to its computation demand. Thus, nowadays almost all CPUs are supplied by two stages: the fist is the classic $voltage\ regulator\ module$ (VRM) mounted on the motherboard whilst the second is a fully integrated voltage regulators (FIVR) inside the CPU which power each core in a CPU. The second stage (FIVR) needs to switch at very high frequency because an high bandwidth control are needed to keep a minimum number of output capacitors. In Haswell CPU the internal FIVR has a switching frequency of 140 MHz to reach 80 MHz of bandwidth [12]. Another drawback caused by multi cores architecture is that lover voltage external supply, from the first stage, are needed, increasing the current and transient requirement. Now the question is, why CPU and not something else? The new challenge is $ASIC\ Clouds$ whose are promise of accelerating computing performance with greatly improved power efficiency.

1.2.2 Specializing the ASIC Data Center

In the last ten years the services which are built around the Cloud model have been growing exponentially. For example, Facebook's face recognition system, Siri answer speech queries, YouTube videos, etc., etc [13]. At single node level is well known how ASICs can offer an improvements in energy-efficiency and elaboration performance, because it can work with specialized instructions. ASICs can achieve large reduction in silicon area which results in a general energy saving versus a typical CPUs. Moreover ASIC Clouds exploit a general optimization at rack level and motherboard level. At rack level the thermal dissipation of a typical ASIC results easier [13], comparing with typical application based on CPUs. More importantly, the specialization of ASIC reduces the overall Bill of Material (BOM) of the motherboard, resulting in a wider power delivery network. All such kind of application requires specialized VRM able to step current down to the 0.4-1.5 V ASIC core voltage, with a power level that can reach 600-800 W. In this scenario it is important to find an architecture which can optimize the VRM project

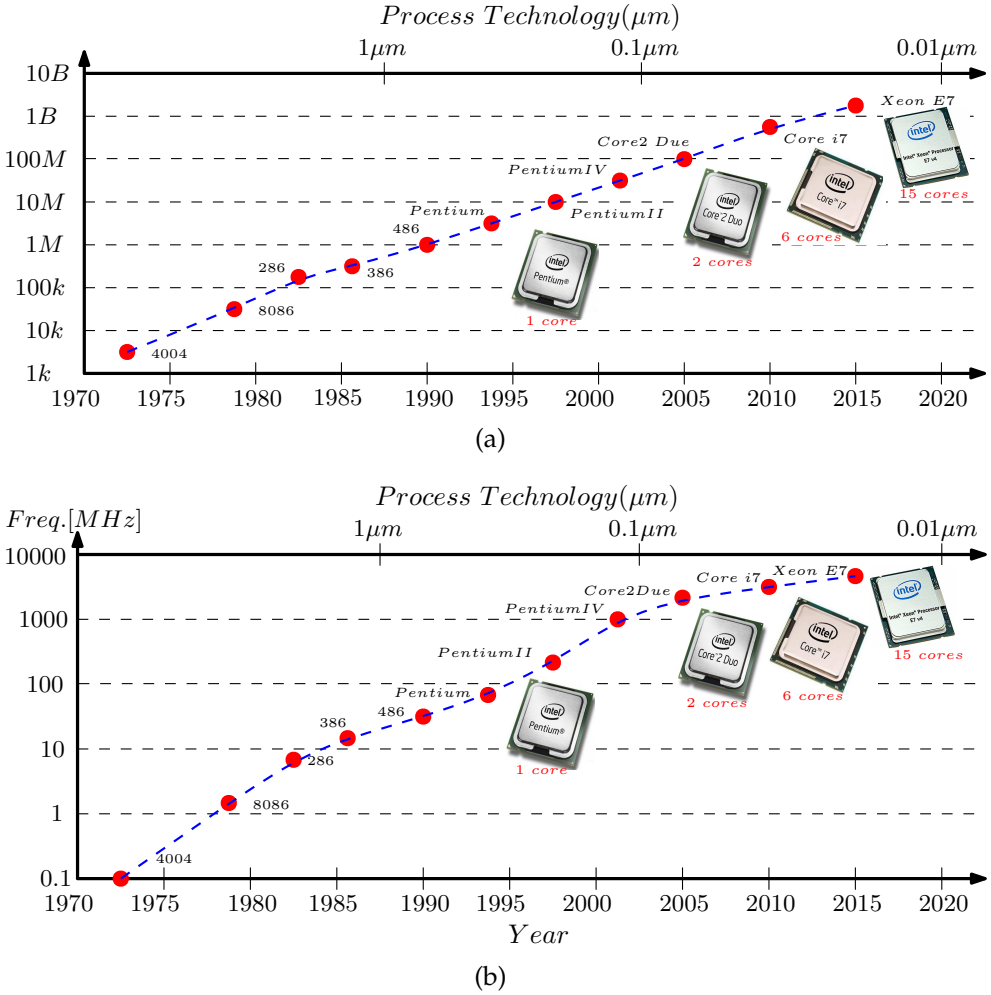


FIGURE 1.2: a) Trend in transistor integration on a CPU, b) trend in clock speed of CPU.

under different aspects, such as: impact on the RMS current in the bus of the rack, power density of the VRM, power delivery network, power efficiency of VRM and its dynamic performance.

1.2.3 From 12 V dc to 48 V dc bus

In Fig. 1.3 is depicted a typical power distribution architecture with a 12 V dc bus at rack level. The power architecture proposed in Fig. 1.3 is burdened with many conversion stages: inside the UPS the ac input is converted to dc voltage which is connected to an energy storage system, i.e. a battery, and then it is converted to ac. The ac output of the UPS is converted to dc voltage around 400 V dc. This dc voltage is stepped down with an isolated dc-dc converter to 12 V dc. Then VRs converters step the voltage down to main computing low voltage rails with high current consumption.

Nowadays the challenges of 12 V power delivery are becoming hard. Data centers today use more kilowatts per rack. In the past a typical rack was designed for 4 to 5 kW but now it can reach 10 kW and actually in the

future it could reach 30 kW [14], hence the current in the 12 V bus bar is causing high copper losses, while in the future will be unsustainable for low voltage bus. Thus, since the power losses increases by the square of the current (I2R), an higher voltage is required to limit distribution losses and even the amount of copper required to carry all current.

To implement more efficient power conversion systems it is mandatory to shift to higher bus voltage at rack-level dc like 48 V, instead of 12 V, which was recently proposed by $VICOR$ [15] and $STMicroelectronics$ (ST) [16]. 48 V dc enables higher overall efficiency and power supply volume reduction [17]. In Fig. 1.4 is proposed the Google data center power distribution architecture open compute racks [18], which introduces a new standard for data center. The transition from 12 V dc to 48 V dc at rack level provides several benefits: an overall reduction of power losses due to higher voltage bus, less conversion steps and better deployment flexibility. Moreover, the UPS is replaced by a battery bank placed at rack level leading to an optimized use of rack space and even reduce conversion stage.

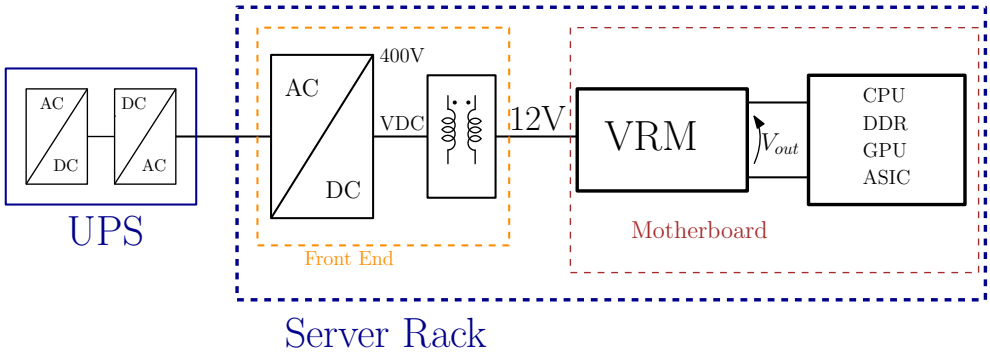


FIGURE 1.3: Power distribution architecture with a 12-V dc bus.

Due to the large conversion ratio from 48 V to PoL, the most common approach is the two-stage conversion system outlined in Fig. 1.5(a), in which an intermediate 12 V dc bus is used. The first stage is usually implemented using LLC resonant converters [19] [20] or Switched-capacitor dc-dc resonant converters [21] [22]. The second stage uses a multi-phase buck voltage regulation module (VRM) topology which is fed from the 12 V dc bus [23] [24] [25].

Nowadays, the bus converter is able to reach a peak efficiency of 96% or higher and the VRM can reach 94% or above, which results in an overall peak efficiency slightly around 90%. However, in VRM applications, the most relevant key performance index is not the peak efficiency, but a flat efficiency curve starting from light load to full load conditions. This is of paramount importance to consider, as the server processors always switch from light to heavy load conditions, remaining at light load for most of the time [4]. For these reasons, the controller of the second stage, i.e. the multiphase buck VRM, provides the phase shedding functionality to enable a flat efficiency for a wide load range. However, the first stage usually has a more conventional efficiency curve where the maximum peak is obtained only at medium load conditions. Thus, in the combined two-stage solutions the efficiency curve is

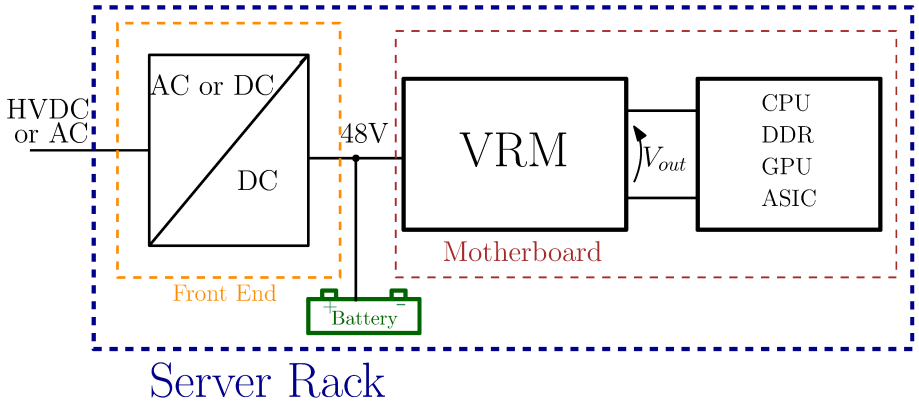


FIGURE 1.4: Power distribution architecture with a 48-V dc bus.

not as flat as desired. This situation is depicted in Fig. 1.5(a). Meanwhile, the desired operating conditions concept is outlined in Fig. 1.5(b), in which the employed single-stage multi-phase VRM enables a high and flat efficiency curve.

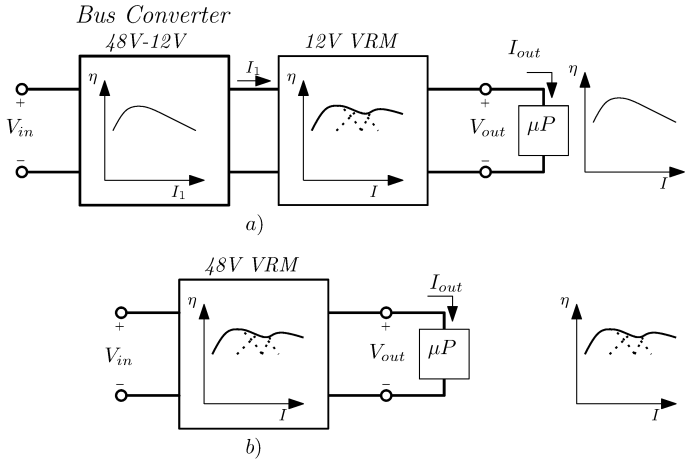


FIGURE 1.5: 48 V VRM architectures: (a) based on the two-stage approach with a multi-phase second stage converter, (b) based on the single stage approach.

1.2.4 New Proposed architecture

As highlighted in Section 1.2.3 the power supply evolution for data centers and networking applications demands a continuous improvement in the efficiency at system and converter levels. Higher voltage distribution system and less conversion steps are necessary to increase the efficiency of the overall distribution system. As reported in Section 1.2.3 48 V dc, in single stage VRM approach, enables higher overall efficiency, isolation design and phase shedding in light load; but rack-level DC distribution can be performed at a higher level of DC voltage such as 380 V dc [8] [26]. An advantage over 48 V DC distribution is that a more efficient AC/DC converter may be used,

resulting in higher overall efficiency. For higher voltage DC distribution system a voltage regulator modules (VRM) is currently realized using a two-stage approach, with an intermediate 12 V dc bus [8]. The first stage is commonly implemented with a resonant converter [27] while the second stage usually uses a multi-phase buck VRM topology that is fed from 12 V dc bus [23]. The overall efficiency power supply chain becomes the product of each power stages where, the Intermediate Bus Converter (IBC) 380V to 12V is able to reach 96.5% [27] or higher and the VRM of 94% [23] or bellow. However, in the VRM application, the desirable feature is a flat high efficiency curve over the entire load range as underlined in Section 1.2.3 for 48 V dc. The architecture proposed in this work is depicted in Fig. 1.6, where the only difference with Fig. 1.4 is the higher voltage bus used.

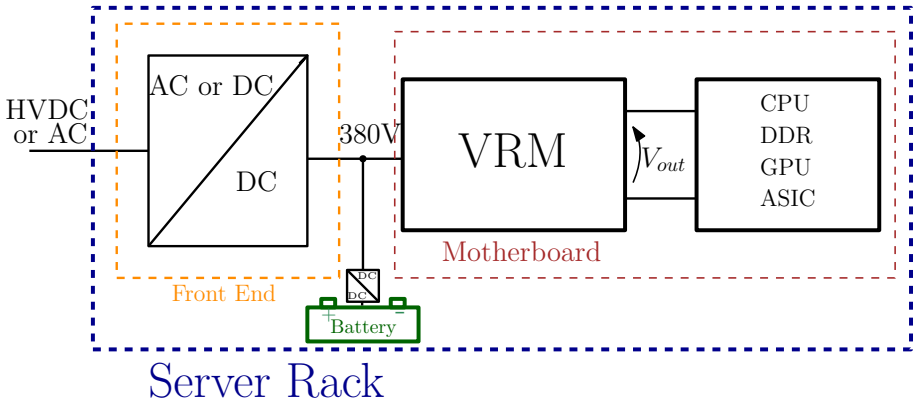


FIGURE 1.6: Power distribution architecture with a 380-V dc bus.

1.3 Voltage Regulators Module specification

In order to supply power to digital load, such as ASIC, CPU and GPU, with high current and low voltage, the VRM power supply is used. The main purpose of VRM is to maintain the voltage within the specification range during a transient event. Moreover, when the microprocessor switches between active mode and sleep mode, which is a very common behaviour for CPU, the VRM has to ensure high efficiency in all operating load conditions. The only way to meet these requirements is to use interleaving technology, such as parallel synchronous buck converter, which solve the large current requirement and even the transient specification. In this section the main VRM specifications are discussed in order to clarify how should be projected a VRM converter.

1.3.1 Efficiency Requirement for Voltage Regulators

Efficiency performance is the main requirement for such kind of applications. As previously reported the power consumption of a typical rack is around 10 kW and as depicted in Fig. 1.1 the CPU power usage in a typical

workload covers 40% of the overall consumption. Thus, even half a percentage point of higher efficiency is an important saving. The two-stage approach (i.e. VICOR [27] and Maxim Integrated [23]) can guarantee a good peak efficiency performance, but actually, as previously reported, the overall efficiency power supply chain becomes the product of each power stages. This is foremost important to consider, since server processors always switch from light to high load [4] [28]. The target is to project a power delivery system witch provides a flat efficiency curve. Shifting at higher bus voltage the overall efficiency can grow in all load conditions but actually can affect the thermal management closed the CPU. For this reason the dc-dc converter has to be projected with high peak efficiency, around 91%/92%.

1.3.2 Transient and Load Requirements for Voltage regulator

In the past, i.e. VRD 11.0 specification the maximum current slew rate was $300A/\mu s$, with a load line of $1m\Omega$, maximum continuous load current (I_{CCTDC}) of 130 A and maximum load current (I_{CCMAX}) of 150 A [30]. Nowadays, the VRM specification are getting stricter, a typical VRM application for CPU can reach a maximum load current of 240 A with a maximum slew rate of $750A/\mu s$. In Fig. 1.7 are reported the equation for the load-line specification. The vertical axis is the output voltage deviation from the voltage reference VID, and the horizontal axis is the output current of VRM. In Fig. 1.7 are defined the typical load-line $V_{typ_{LL}}$, the maximum voltage curve $V_{max_{LL}}$ and the minimum voltage curve $V_{min_{LL}}$, whilst TOB is the tolerance band. As reported, during a transient event the output voltage should be within the load line band for both dynamic and static transient operation. From the control point of view, the load-line dependence is achieve with an adaptive voltage positioning control (AVP) [31]. During a step-down transient, the output VRM voltage can be over the maximum voltage $V_{max:LL}$ load-line for $25\mu s$. The overshoot can not exceed the overshoot releif threshold which is $VID + \Delta_{max}$. The specification on the voltage undershoots is more stricter because may causes system lock-up.

1.3.3 Power Density and Power Delivery Requirements for Voltage regulator

The number of the CPUs per rack have been growing year by year and even the power delivery to the CPU is becoming more stricter due to less space for the VRM, causing thermal issue and higher power requirement for CPU. In the future, server microprocessors will have more power consumption and stricter transient requirements. In this scenario one of the main limitation comes from the power delivery network, in fact with higher current, the VRM has to be placed more closed to the CPU. More closer is, more difficult is to meet the occupation area requirement because of the digital interconnections. In fact, due to copper area limitation one main specification is the VRM power density. Thus, if isolated topology are adopted, magnetic integration structures can guarantee both high efficiency and high power density.

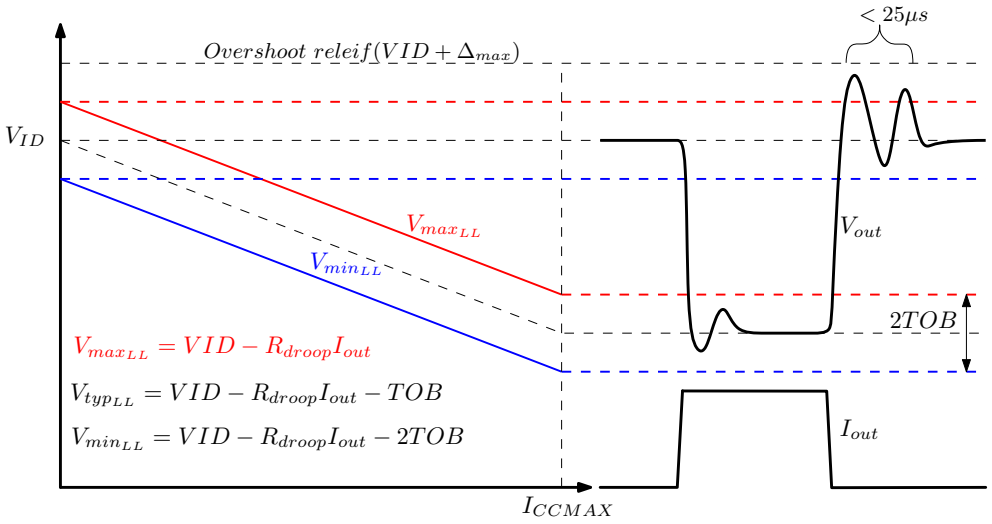


FIGURE 1.7: Relationship between load-line specification and time domain waveforms.

1.3.4 Challenges for VRM Design

As discussed in this section, power management for high current digital load will be much more critical for future microprocessor. As the transient is becoming higher, an higher bandwidth control loop is needed, which results in higher switching frequency. Not only VRM challenges, it is important to redraw the system at power architecture system level due to more power consumption and to meet the efficiency and power density requirement at all conversion stages. As discussed previously, higher single stage step down are needed because of the trend for the new power distribution system architecture [26] [8]. Shifting to higher bus voltage at rack-level like 48 V [18] enables in higher overall efficiency at power distribution system level. In this dissertation the main challenge is to ensure all of these requirements for a single stage working as, high-voltage point-of-load (HV POL).

1.4 Background of Point of Load (POL) Converters

Earlier VRM converter used a single conventional topology but actually with the increase of output current and with more strict transient requirement low output inductor where needed. However, small inductance results in large current ripple in steady-state operation causing high copper losses and a large turn off loss. To overcome this issue $CPES$ proposed an interleaving technology [32] [33] [34]. It consists of N buck converters with the inputs and outputs interconnected as depicted in Fig. 1.8. By interleaving N cells of the same buck converter the current ripple is greatly reduced because of the equivalent inductance $L_{out_{eq}} = L_{out}/N$. Interleaving VRMs can ensure high efficiency, high power density, good dynamic response and more distributed thermal dissipation. The interleaving concept was so successful and it has became a standard in VRM industry, reaching high efficiency even for a 12 V VRM [23].

Nowadays with the significant improvements in the MOSFETs technology the inductor is the barrier to higher power density. To overcome this problem in [35] was proposed a three level buck converter which offers high efficiency and power density. The gains is made by adding a flying capacitor that reduces the MOSFETs voltage stress by half, allowing to use low voltage devices and decreases the inductor size by reducing the volt-second across the inductor.

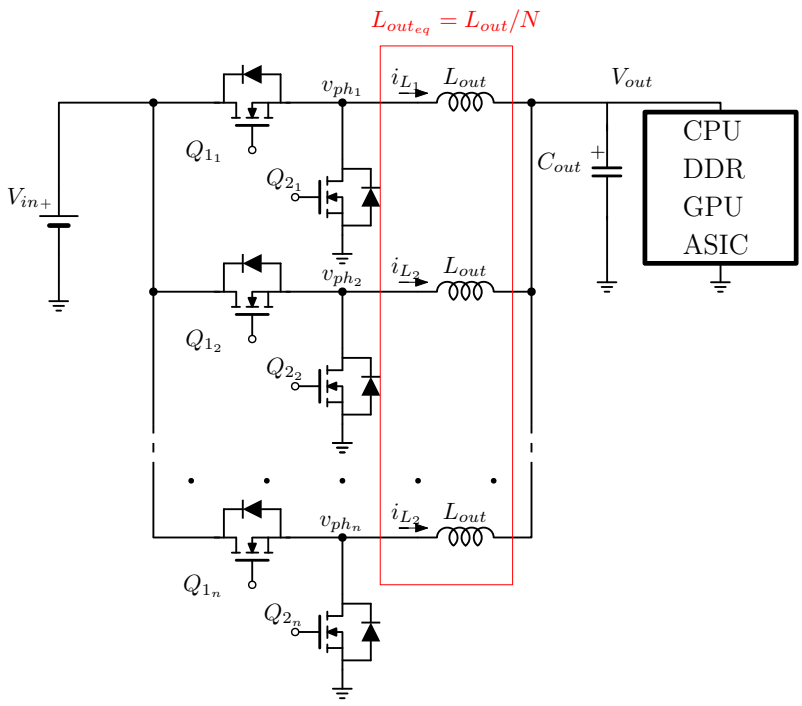


FIGURE 1.8: Interleaving synchronous Buck converter for VRM applications.

In recent years the VRM output currents has increased, while the output voltage has decreased. Conventional synchronous buck converter suffers a lot because of the small duty cycle, causing low efficiency and poor ripple cancellation. Moreover high power consumption for CPU results in high current in 12 V bus.

Today, one of the current trends in supplying high performance microprocessors is the adoption of the 48 V dc bus. To supply from 48 V dc the most common approach is the two-stage conversion system, as depicted in Fig. 1.5, in which an intermediate 12 V dc bus is used. But actually, as before reported and highlighted in Fig. 1.5 high step-down directly from 48 V are needed. The challenge is to operate at high-efficiency with a single stage conversion from the 48 V bus, including multi-phase and phase-shedding capabilities. There have been several research studies on the 48 V VRMs. Previous examples of dc-dc resonant topologies for VRM applications can be found in [36], [37], [38] and [39]. In [40], the 48 V VRM developed in [37] was analyzed including layout and thermal considerations for very high-frequency operation. A cascaded buck converter was proposed in [41] in order to reduce voltage stress across each cell of the cascaded converter. However, a

cascaded buck converter is very complex and eliminate the possibility of using DrMOS devices which is very beneficial for power density and high switching frequencies. In [42] a synchronous Buck converter using GaN is proposed with a very high ratio step down. Using the high switching speed of the GaN FET technology is possible to achieve a narrow duty cycle maintaining high efficiency.

Recently an high efficiency 48 V VRM dc-dc converter was introduced in [43], [44] and [45]. None of the previous attempts, however, are able to provide multiphase operation, phase-shedding and high efficiency compared to the two-stage solutions. An interesting single-stage alternative is recently investigated in [17] and [46] called Sigma converter. The first Sigma converter was proposed in [47] [48]. The basic idea is to deliver the power to the load in parallel using an high efficiency unregulated converter (i.e. LLC converter) to handle most part of the power. The regulated converter can be a classic buck converter which carries smaller part of the power. In order to have high efficiency, using Sigma converter, the input voltage across the unregulated converter shoul be as high as possible.

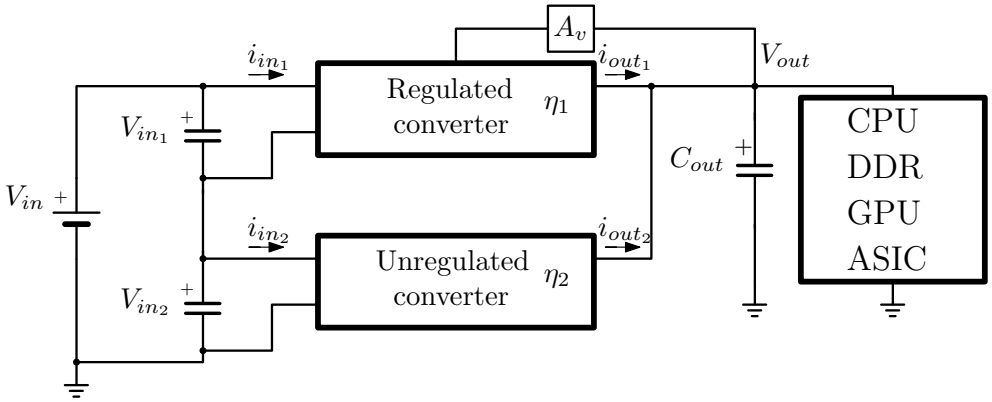


FIGURE 1.9: Main concept of Sigma converter.

For the unregulated converter, LLC converter topology should be the best candidate due to its properties, such as ZVS and ZCS for the secondary side rectifier and ZVS for the primary side switches.

Recently one stage direct power conversion from 54 V based on full-bridge current doubler is proposed in [49] where a prototype with a six transformer turns ratio and a maximum secondary side voltage of 10. An half bridge current doubler is proposed in [50] implemented with GaN technologies with a peak efficiency of 93.7%. In all of these solutions the transformer is used for achieving high step-down ensuring isolation.

1.5 380 V to POL VR technologies

The challenge now is to operate at high-efficiency with a single stage conversion directly from 380 V dc bus operating as HV POL converter, including a multi-phase approach and phase-shedding capabilities, maintaining high

power density and dynamic performance comparable with 48 V VRM single-stage. A conventional full-bridge that operates in phase-shifted (FBPS) with center tapped rectifier may be used for converting the energy from 380 V DC bus to microprocessor, as depicted in Fig. 1.10. In FBPS topology the key to zero voltage switching is the amount of energy stored in the primary inductance L_p [51] versus the energy required to charge and discharge the primary MOSFETs parasitic capacitance and the transformer stray capacitance. Moreover a dissipative RCD snubber is necessary to mitigate the voltage ringing across the rectifier MOSFETs.

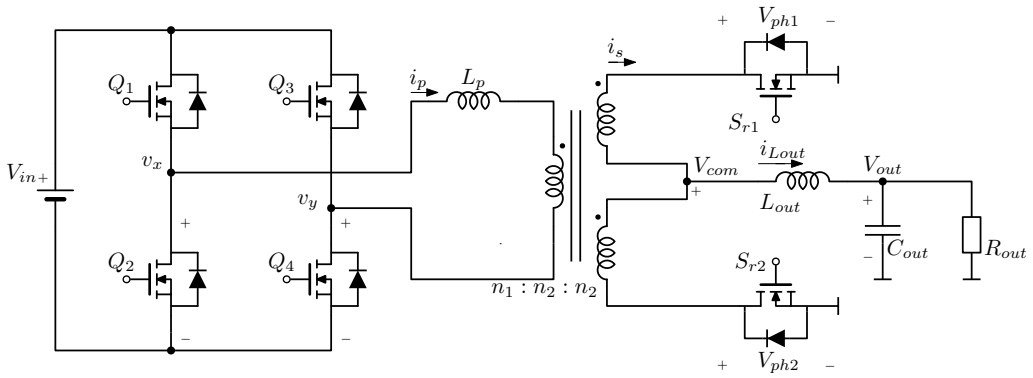


FIGURE 1.10: Circuit topology of FBPS converter with center tapped rectifier.

However, because of high voltage stress for primary MOSFETs and high transformer turns ratio, multi-phase primary side series and secondary side paralleled (ISOP) interleaved converter system is needed to mitigate the primary MOSFETs and transformer stress [52] [53] [54], as reported in Fig. 1.11.

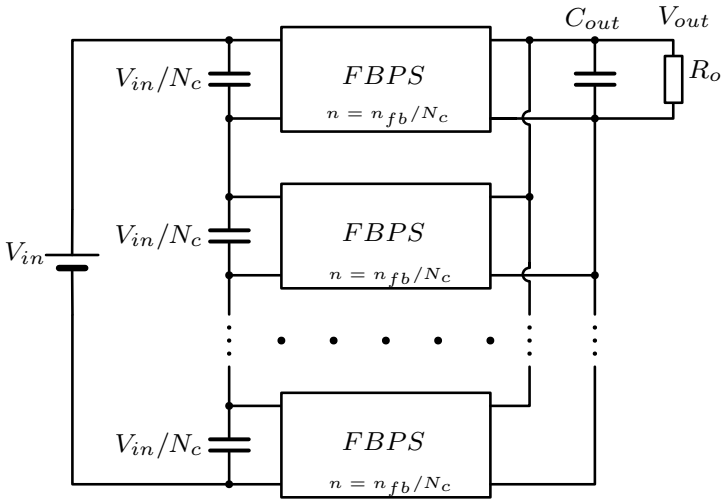


FIGURE 1.11: Input series and output parallel structure based on FBPS

In [55] and [56] an half-bridge current doubler is selected as HV POL converter because the voltage gain from output voltage to input voltage is half

comparing with the full bridge primary side [57]. Moreover in [56] a current doubler rectifier was selected to simplified the transformer realization. A symmetrical controlled half-bridge current doubler is proposed in an ISOP connected system for HV POL where a load-dependent zero-voltage switching ZVS method was proposed improving the efficiency in both heavy and light load conditions.

All the works presented in litterature can not ensure phase shedding operation eliminating the benefit which actually a single stage HV POL can ensure. Hence, it is important to find an optimal solution which can work as a synchronous buck converter, ensuring ZVS in both turn off and turn on maintaining high power density with good dynamic performance.

1.6 Dissertation Outline

The dissertation mainly focuses on the new single stage isolated VRM 380 V here proposed. To achieve this objective different topologies as high step down to POL are explored.

The dissertation consists of six chapters, organized as follows.

Chapter 1 gives an introduction of the research background. It highlighted the main challenges of data center power distribution system. The limitations of the existing power distribution architecture available nowadays are illustrated and is proposed our new architecture.

In Chapter 2 come up with a new single stage with high power density high efficiency for POL application based on the full-bridge phase-shifted quasi-resonant (FBPS-QR) converter that is the most suitable candidate for VRM applications as HV POL from 380 V voltage input. Experimental results are also reported for CPU and DDR VRM applications from 48 V. Then an IBC from 380 V to 12 V based on quasi-resonant converter is proposed, highlighting the trouble of poor switching performance for high voltage MOSFETs which appears at 380 V input. Then some different topologies architecture, based on FBPS-QR are presented in attempt to work as HV POL.

In Chapter 3, a novel multilevel topology for VRM application is proposed. Our 380 V VRM is based on half-bridge multilevel phase-shift current-doubler quasi-resonant (HBPS-QR) topology that enables ZVS operation both at primary side and secondary side. The voltage stress for the primary MOSFETs, in the proposed quasi-resonant multilevel topology, is half of the voltage input allowing to use lower voltage MOSFETs which are less affected from C_{oss} nonlinear behavior. Moreover, half of turns ratio, for the planar transformer, is needed comparing with FBPS-QR. The secondary side is implemented in current-doubler topology with both noncoupled version and coupled-inductor structure. A detailed analysis of the converter operations are presented including experimental results.

In Chapter 4, are proposed different magnetic structures for both FBPS-QR, presented in Chapter 2, and HBPS-QR accounted in Chapter 3. We will discuss first a different geometrical approach to integrate a current-doubler

with a transformer by using a planar technology and the second an innovative integration of the current-doubler, the output inductances and the external inductor connected to the primary side required for ZVS operation, using a single magnetic component. Moreover, two different transformer structure for HV POL are presented. Experimental results for integrated magnetics structures and HV POL transformers are presented.

Chapter 5 provides a summary of the dissertation highlighting the benefit of the proposed 380 V VRM over 48 V VRM.

Chapter 2

High conversion ratio isolated dc-dc converters for VRM application

High step down converter is the key for improving the overall performance of power distribution system in data center at rack level. In this chapter different topologies as high step down isolated dc-dc will be presented highlighting the major benefit and drawback of each topology.

2.1 Constrains for 380 V VRM conversion

VRM converter takes a variety of form factors for different digital load (i.e. GPU,CPU,AISCs etc) but actually the fundamental requirements for VRM conversion are generally the same. VRM converter as HV POL has to ensure the same fundamental requirements that a typical VRM from 12 V input voltage can guarantee, such as: efficiency, high step down, power density and dynamic performance. In order to avoid extremely conversion ratio of the converter higher turns ration n is normally selected. However, high turns ratio will complicate the design of the transformer, such as: primary side resistance, leakage inductance and inter-winding capacitance. Moreover, the volume of transformer becomes large affecting the power density of the converter. Another issue comes from the high input voltage of the application. The high voltage stress on the primary side switches will increase dramatically the power losses, so ZVS or zero current switches (ZCS) techniques are mandatory in this application. In particular, the benefit of ZVS in topology such as full-bridge phase shift, dual active-bridge are a well-known, which can ensure high-frequency operation showing significant improvements in efficiency from high voltage source. For the design and optimization of a converter system based on ZVS operation it is crucial to identify the conditions under which ZVS can be achieved. First of all the topology adopted, a basic requirement for ZVS operation is a half-bridge with an inductive element connected to its phase. Moreover, it is important to identify and calculate the required energy stored in the inductive element at the beginning of a switching transition. In this scenario, it is mandatory to analyze the soft switching behaviour in all operating load conditions especially in light load. Not only primary side switches, it is essential to study the impact of the transformer on

the ZVS functionalities and to meet EMI standards. In general inter-winding capacitance of transformer is a major path of CM noise causing also impact on the ZVS transition, so attention should be paid on this aspect.

In chapter 3 is introduces an analytical approach to specify the condition for ZVS and its impact on the overall efficiency due to the copper losses caused by the high energy for ZVS operation. A comparison between different topologies, different MOSFETs and different transformers will be carried out in this dissertation.

Primary side MOSFETs are important as secondary side MOSFETs. In general power converters which utilizing isolated topologies for low voltage high current applications are using synchronous rectifier (SR) to improve the overall performance. Attention should be paid on the selection of these MOSFETs because the high current and the voltage stress, which depends from the turns ratio of the transformer and the input voltage.

Another important constrains of 380 V VRM is the dynamic performance, as reported in section 1.3.2. The dynamic loading of the VRM represents a severe problem, because the high slew rate and the tighter voltage tolerance, which can be solve by using high frequency converter with high bandwidth control. Thus, low output inductance are mandatory to meet these requirements which actually affects the efficiency performance. All of these requirements pose serious design challenges.

2.2 High voltage to POL some proposal

In this section are discussed some general possible topology as high step down. All topologies should be transformer based with ZVS or ZCS operation at primary side and high output current range up to 60-70 A at 1.8 V for each phase ensuring current sharing.

2.2.1 Full-Bridge phase-shift

A full-bridge ZVS converter is displayed in Fig. 2.1 which can be a valuable topology as high step down, it has half the rms current at primary side compared to a half bridge, and also it can be implemented in phase-shift control which provides Zero Voltage Switching (ZVS) for all primary side MOSFETs. Double current rectifier is the most suitable for such high current application, since the current target is 60 A. Double current rectifier presents some advantages, such as: simpler transformer realization with one secondary winding, which results in a reduction of conduction losses at secondary side. Moreover current doubler provides ripple cancellation, since the output inductors are operating in parallel handling half the output current [58].

In [59] FBPS small signal model with current doubler (CD) rectifier is derived. By using the model proposed in [59] the averaged circuit model of the PWM converters can be directly used to derive the small signal model and as demonstrated, the small signal model of FBPS-CD can be described by a second-order transfer function as the classic buck converter.

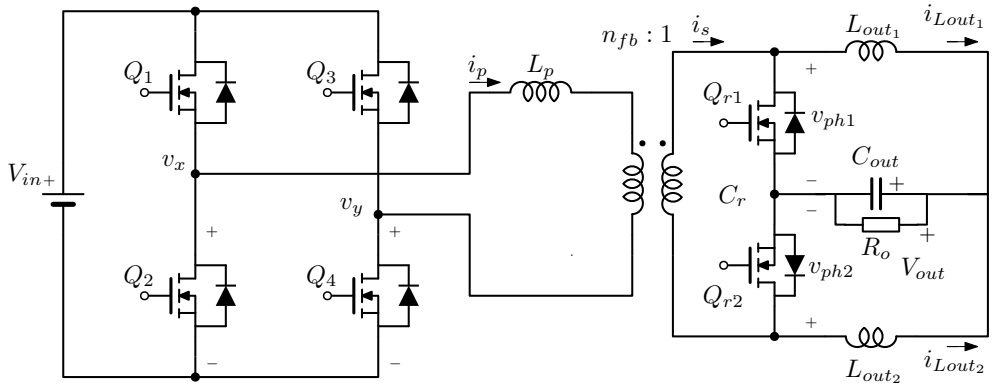


FIGURE 2.1: Phase-Shifted Full Bridge ZVS converter with double current rectifier.

To study the constraints considering the dynamic behaviour for FBPS-CD, we need to replace the converter in 2.1 with a simplified model. In Fig. 2.2 is illustrated the simplified model of FBPS-CD which shows that the current doubler rectifier can be simplified as one single LC filter, where $L_{out_{eq}}$ is the equivalent inductance $L_{out_{eq}} = L_{out_{1,2}}/2$ (i.e. $L_{out_1} = L_{out_2}$). In the model proposed in 2.1 is not reported the duty cycle loss behaviour which is the effective duty cycle d_e as defined in [60].

The circuit in Fig. 2.2 shows the major future of the CD rectifier: two inductors share the load current. Hence, the equivalent inductance design, and even the transformer turns ratio n have to be designed based on the transient and efficiency requirement.

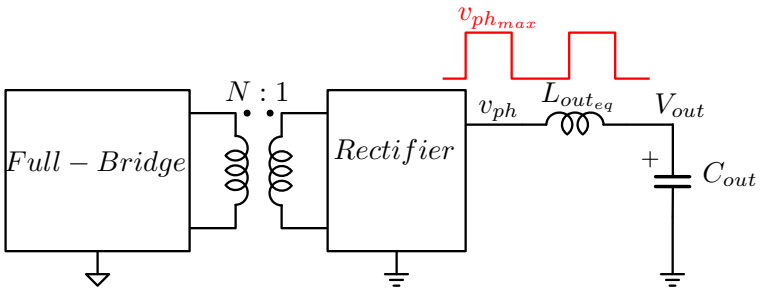


FIGURE 2.2: Simplified model for Full-Bridge phase-shift current doubler.

In a classic buck converter, to meet transient requirement an optimal design of the output inductances are needed as in FBPS-CD. During a transient the duty cycle increases as long as the duty cycle is not saturated. When the selected inductance value of $L_{out_{eq}}$ reaches a value such that the duty cycle is near saturation condition during the transient response. In this scenario the inductance is defined as the *crictical inductance*. In [61] a model for *crictical inductance* in multiphase VRM buck converter is proposed which can be adapted for FBPS-CD:

$$L_{crt} = \frac{\frac{\pi}{2} V_{ph_{max}} \Delta D_{max}}{\Delta I_{out} \omega_c}, \tag{2.1}$$

where ΔI_{out} is the maximum output current variation, ω_c is the control bandwidth, $V_{ph_{max}}$ is the maximum voltage on the secondary side (as depicted in Fig. 2.2) and ΔD_{max} is the maximum variation of duty cycle. ΔD_{max} depends on various parameters, such as the primary inductance L_p, the transformer turns ratio n, the output current I_{out} and the output inductances L_{out}.

As widely demonstrated in literature FBPS-CD ensure ZVS operation but attention should be posed on this aspect. ZVS is strongly subjected to variation with the load condition [51], moreover, an additional inductance is added at primary side to ensure ZVS operation. Another drawback of FBPS comes from the ringing effect across rectifier switches caused by a parasitic resonant transition between the primary inductance and the parasitic output capacitance of the rectifier MOSFETs C_{oss}. Thus, the peak voltage in the FB at secondary side is higher than V_{in}/n, if dissipative snubbers are not used. Moreover, considering Fig. 2.1 the two legs of the FB behave differently with reference to the ZVS. The left leg starts the transition of ZVS at the end of the circulating phase [62], whilst the right leg starts its transition at the end of the power phase, which means higher energy available.

Full-bridge phase-shift current doubler ZVS is not suitable for high step down operation from 380 V to POL because of hard switching operation at secondary side. In fact, high voltage MOSFETs rating are needed. Thus, the switching frequency of the topology will be limited, as well as the power density. Another important drawback is the high copper losses at primary side due to ZVS operation and high turns ratio requirement. Classic FBPS results in bigger size which is incompatible with motherboard placement.

2.2.2 Full-Bridge phase-shift double-current ISOP

Full-Bridge phase-shift converter proposed in section 2.2.1 is not a suitable candidate for VRM applications as HV POL from 380 V voltage input due to the trouble of poor switching performance for high voltage MOSFETs appears during 380 V input, reducing the overall efficiency. In addition in full-bridge topology the parasitic transformer stray capacitance comes as an important limitation for ZVS capability. In an attempt to improve the ZVS performance for primary side switches and reduce the necessary transformer turns ratio, here a multi phases primary side series and secondary side paralleled (ISOP) interleaved converter system [63] is used to mitigate the transformer stress [52] as shown in Fig. 1.11. Each box in Fig. 1.11 represents a FBPS-CD converter.

The proposed structure ensure ZVS with less energy stored in the leakage inductance compared with full-bridge in Fig. 2.1 and even the transformer turns ratio requirement is less compared with FBPS ($n = n_{fb}/N_c$, where N_c are the number of converter in series at primary side), which results in an higher peak efficiency. However, in VRM applications, the most relevant key performance index is not the peak efficiency but actually a flat high efficiency in the entire load range. In fact, in the proposed architecture is not possible to use phase shedding technique.

2.2.3 Full-Bridge phase-shift series approach

Another appealing topology can be a series approach at primary side without using parallel configuration at secondary side, ensuring phase shedding functionality. As mentioned in section 2.2.2 the ISOP configuration can mitigate the voltage conversion ration and the voltage stress on primary side MOSFETs. However, due to less efficiency in light load the ISOP architecture is not suitable for HV POL VRM applications. In attempt to reduce the transformer turns ratio at primary side, compared to FBPS approach, in Fig. 2.3 a primary side series approach is proposed. Compared with FBPS this converter can ensure higher ZVS capability, moreover less voltage related MOSFETs are used.

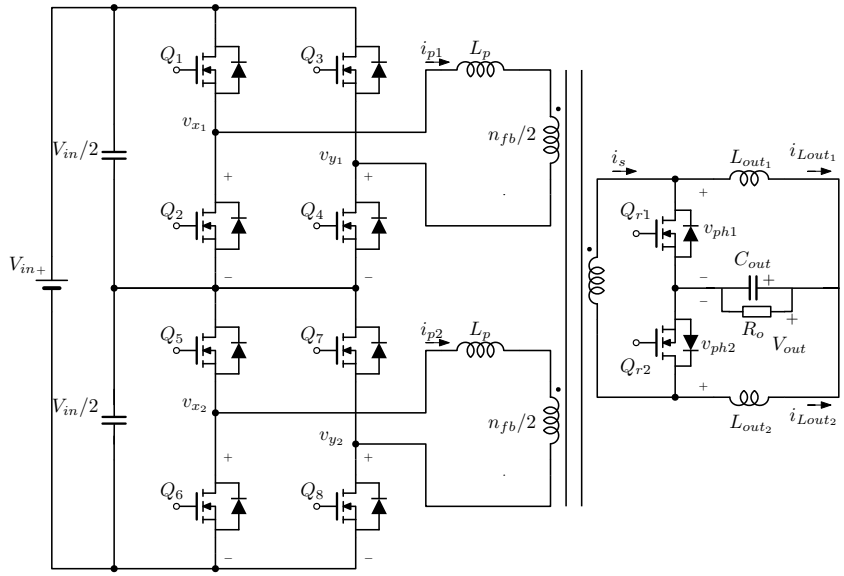


FIGURE 2.3: Full-bridge phase-shift with double current with series apporach at primary side with one transformer.

The full-bridge primary side series approach presents several advantages such as: same transformer size comparing with FBPS, less total resistance of transformer due to internal series parallel winding arrangement, half of voltage MOSFETs related at primary side, higher ZVS capability and less duty cycle losses. However, still, this topology suffer from hard switching at secondary side and even 8 MOSFETs are used at primary side. So, the switching frequency of the topology will be limited.

2.3 Full-Bridge phase-shift quasi-resonant double-current

In section 2.2 are presented some different converters suitable for HV POL VRM application. The main limitations for such of topologies where: duty cycle loss which could be very limited for dynamic performance, ZVS operation limitation in light load and hard switching operation at secondary side causing maximum frequency limitation.

The conventional ZVS phase-shift full-bridge topology presented in Fig. 2.1 presents some fundamental limits. The first limit is the difficulties to reach ZVS transition at primary side in light load, because the energy stored in the leakage inductance of the transformer can not ensure ZVS operation. The main method of expanding the ZVS range is to add an additional inductance in series at primary side [64], however, it would increase the duty cycle loss [59]. Other solutions have been proposed to address this issue. In [65] an additional active switch ensure ZVS transition in all load conditions, however the efficiency benefit is not considerable and the circuit control becomes more complicated. In [66] a passive auxiliary branch is added for ZVS operation, reducing the RMS current but the drawbacks are high cost and volume of the solution.

To increase the switching frequency operation and improve the ZVS capability a modified operation of the phase shifted full-bridge at the primary side and of the current doubler rectifier at the secondary side, in [67] we have presented a full-bridge phase-shift quasi-resonant double-current (FBPS-QR), which performs a VRM from 48 V. FBPS-QR is the most suitable candidate for VRM applications as HV POL from 380 V voltage input. In this section is studied the proposed solution for a 48 V VRM application useful to clarify what are the main advantages and disadvantages of FBPS-QR for HV POL applications.

The proposed solution is based on an isolated converter, which comprises a full-bridge at the primary side and a current-doubler (CD) rectifier at the secondary side as shown in Fig. 2.4. The primary side full-bridge operates in phase-shifted COT [68], as shown in Fig. 2.5. The secondary side current-doubler rectifier uses synchronous rectifiers that comprises Q_{r1} and Q_{r2}. Due to resonant transitions, both Q_{r1} and Q_{r2} are on at zero voltage (ZVS). This is obtained by generating a zero current detection (ZCD) signal on the voltage across the synchronous rectifier switches (i.e. v_{ph1} and v_{ph2}).

This discussion of FBPS-QR is organized as follows: firstly a presentation of the proposed converter, with the detailed analysis of operation, is carried out in section 2.3.1 and section 2.3.2. In section 2.3.3, the control system structure is analyzed including the current sharing control, while the small-signal model is discussed in section 2.3.4. Two solutions for the magnetic integration are proposed in section 4.2. Finally, section 2.4 reports experimental results for both the processor power supply and the DDR power supply for 48 V VRM applications.

Compared to the conventional full-bridge phase-shifted converter, the proposed solution presents an additional capacitance C_r at secondary side and an innovative driving scheme to enable ZVS operation. To simplify the analysis, the magnetizing current is neglected and the leakage inductance is included in the external inductance L_r. Thus, each resonant transition includes L_r, C_r and one of the output inductances $L_{out1,2}$, depending on the primary voltage polarity. The main property of the proposed solution is that the circulating current at the primary side is kept almost constant, ensuring soft-switching at the primary side at any load conditions. This is a unique advantages of the proposed FBPS-QR overcoming the ZVS capability limitation

of a classic FBPS.

The proposed dc-dc converter has two different modes of operation: when the voltage on the resonant capacitor C_r reaches zero during the input powering phase (when Q_1 and Q_4 are on or when Q_3 and Q_2 are on) and when the voltage on the resonant capacitor C_r reaches zero during the freewheeling phase (when Q_1 and Q_3 are on or when Q_2 and Q_4 are on). The two operating modes are denoted as $Operation\ Mode\ A$ and $Operation\ Mode\ B$, respectively, and occur at increasing level of load power, i.e. $Mode\ A$ is for lighter load conditions and $Mode\ B$ for heavier load conditions.

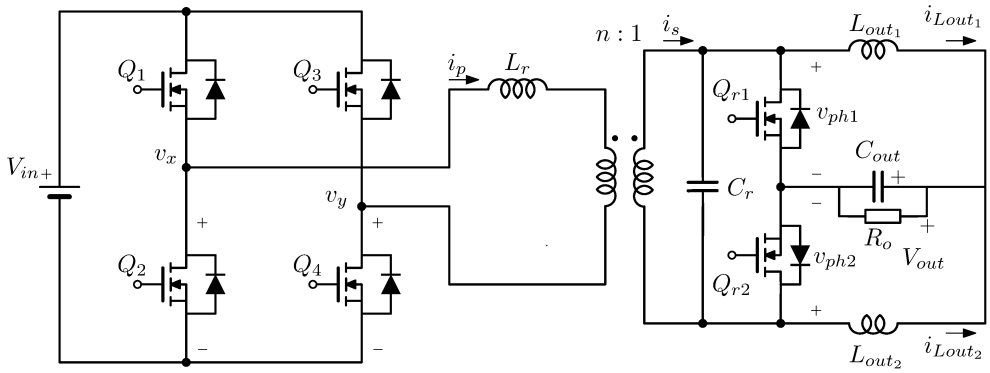


FIGURE 2.4: 48 V VRM based on a full-bridge at the primary side and a current doubler with resonant capacitor C_r at the secondary side.

2.3.1 Operation Mode A: Resonant Transition during the powering phase

Following the converter waveforms shown in Fig. 2.5, the converter operation in one switching cycle T_{sw} is described in twelve subintervals that correspond to the topological states shown in Fig. 2.6. For the purpose of explanation, we will denote $L_{out} = L_{out_1} = L_{out_2}$. The twelve subintervals are described as follows:

1) $\boldsymbol{t_0 - t_1}$: at $t = t_0$, switch Q_4 is turned on, the primary current i_p freewheels through switches Q_2 and Q_4, and both Q_{r1} and Q_{r2} are on. The topological state is shown in Fig. 2.6(a).

2) $\boldsymbol{t_1 - t_2}$: at $t = t_1$, switch Q_2 is turned off, and the primary current i_p discharges the capacitance of Q_1 and charges the capacitance of Q_2. When capacitance of Q_1 is discharged to zero, its body diode conducts to enable ZVS turn-on of Q_1. This is a well-known operation in full-bridge phase-shifted (FBPS) converters. Both Q_{r1} and Q_{r2} are on and the topological state corresponding to this subinterval is reported in Fig. 2.6(b). The current $i_p(t_1)$ that enable ZVS operation of Q_1 is denoted as circulating current I_{cir} (i.e. $I_{cir} = -i_p(t_1) = -i_s(t_1)/n$), as shown in Fig. 2.5, and it is almost constant within the interval $(t_0 - t_1)$.

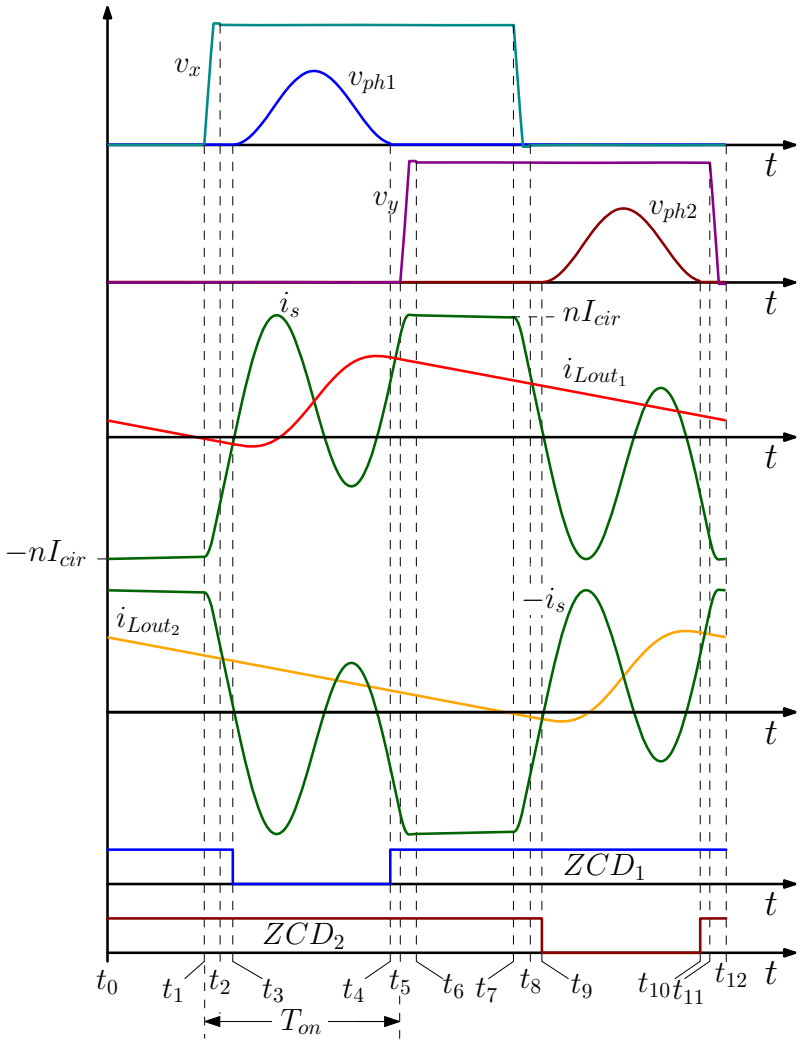


FIGURE 2.5: Main converter waveforms for Operation Mode A. From top to bottom: primary side voltages (v_x and v_y), voltages ($v_{ph1,2}$), secondary side transformer current i_s and inductor currents ($i_{L_{out1}}$ and $i_{L_{out2}}$), and zero current detection (ZCD) signals ($ZCD_{1,2}$)

3) $\boldsymbol{t_2 - t_3}$: at $t = t_2$, switch Q_1 is turned on with ZVS and both secondary side rectifiers Q_{r1} and Q_{r2} remain conducting, as shown in Fig. 2.6(c). After $t = t_1$, the primary current i_p increases with a slope that can be approximated as V_{in}/L_r.

4) $\boldsymbol{t_3 - t_4}$: at $t = t_3$, the secondary current i_s reaches i_{Lout1} (i.e. $i_s(t_3) = i_{Lout1}(t_3)$), Q_{r1} is turned off, and Q_{r2}, Q_1 and Q_4 are conducting. The topological state is shown in Fig. 2.6(d). Indeed, Q_{r1} is turned off when the ZCD_1 signal is low. Signal ZCD_1 is theoretically obtained measuring the voltage across Q_{r1}, comparing with zero (or with a threshold close to zero) and thus detecting when the current on Q_{r1} changes sign. In practice, ZCD_1 signal is obtained with a more complicated procedure also to enable current sharing, as outlined in section III. In this subinterval, the resonance between L_r, C_r and L_{out} takes place and the equivalent resonant circuit is shown in Fig. 2.7 case a).

5) $\boldsymbol{t_4 - t_5}$: at $t = t_4$, the resonant voltage reaches zero volt, ZCD_1 signal becomes high and switch Q_{r1} is turned on, while at the primary side switches Q_1 and Q_4 are still conducting. The topological state is reported in Fig. 2.6(c).

6) $\boldsymbol{t_5 - t_6}$: at $t = t_5$, switch Q_4 is turned off, i_p charges the capacitance of switch Q_4 and discharges the parasitic capacitance of switch Q_3 in order to achieve ZVS. The topological state is now represented in Fig. 2.6(e). The current that enables ZVS of Q_3 is $i_p(t_5)$ and it is only slightly smaller than I_{cir}. Thus, I_{cir} is still a good index to establish when turn-on ZVS is achieved for all switches. At $t = t_6$, Q_3 is turned on at ZVS and i_p freewheels through switches Q_1 and Q_3, as shown in Fig. 2.6(f).

7) $\boldsymbol{t_6 - t_7}$: at $t = t_6$, the positive half-cycle of the switching period is completed (i.e. $t_6 = t_0 + \frac{T_{sw}}{2}$), and the topological state of Fig. 2.6(f) is the first one of the negative half-cycle and corresponds to the one of Fig. 2.6(a) for subinterval $t_0 - t_1$, the primary current i_p freewheels through switches Q_1 and Q_3, and both Q_{r1} and Q_{r2} are on.

8) $\boldsymbol{t_7 - t_8}$: at $t = t_7$, switch Q_1 is turned off, i_p charges the capacitance of switch Q_1 and discharges the parasitic capacitance of switch Q_2 in order to achieve ZVS. The current that enables ZVS of Q_2 is $i_p(t_7)$ and it is I_{cir}. The topological state is reported in Fig. 2.6(g).

9) $\boldsymbol{t_8 - t_9}$: at $t = t_8$, switch Q_2 is turned on with ZVS and both secondary side rectifiers Q_{r1} and Q_{r2} remain conducting, as shown in Fig. 2.6(h). After $t = t_8$, the primary current i_p increases with a slope that can be approximated as V_{in}/L_r.

10) $\boldsymbol{t_9 - t_{10}}$: at $t = t_9$, the secondary current $-i_s$ reaches i_{Lout2} (i.e. $-i_s(t_9) = i_{Lout2}(t_9)$), Q_{r2} is turned off, and Q_{r1}, Q_2 and Q_3 are conducting. The topological state is shown in Fig. 2.6(i). Q_{r2} is turned off when the ZCD_2 signal is low. In this subinterval, the resonance between L_r, C_r and L_{out2} takes place and the equivalent resonant circuit is shown in Fig. 2.7 case a).

11) $\boldsymbol{t_{10} - t_{11}}$: at $t = t_{10}$, the resonant voltage reaches zero volt, ZCD_2 signal becomes high and switch Q_{r2} is turned on, while at the primary side switches Q_2 and Q_3 are still conducting. The topological state is reported in Fig. 2.6(h).

12) $\boldsymbol{t_{11} - t_{12}}$: at $t = t_{11}$, switch Q_3 is turned off, i_p charges the capacitance of switch Q_3 and discharges the parasitic capacitance of switch Q_4 in order to achieve ZVS. The current that enables ZVS of Q_4 is $i_p(t_{11})$ and it is slightly I_{cir}. The topological state is reported in Fig. 2.6(j). Now the switching period is completed (i.e. $t_{12} = t_0 + T_{sw}$).

As previously highlighted in a classic FBPS 2.2.1 the voltage reflected at secondary side depends from the turns ratio n and the load condition. In FBPS-QR due to resonant operation the phases voltage $v_{ph1,2}$ is slightly complicated: taking into account that the average voltage of $v_{ph1}(t)$ is equal to the output voltage V_{out}, the voltage conversion ratio in Mode A is evaluated deriving $v_{ph1}(t)$ and then averaging it over the switching period. The analytical expression of $v_{ph1}(t)$ is obtained solving the equivalent resonant circuit of

Fig. 2.7 case a). By solving in S-domain it is derived $v_{ph1}(t)$ from $V_{ph1}(s)$:

$$V_{ph1}(s) = \frac{(V_{out}L_p + nV_{in}L_{out})}{L_p + n^2L_{out}} \frac{1}{s} \frac{1}{1 + \frac{s^2}{\omega_r^2}}. \tag{2.2}$$

From 2.2 and applying a step variation of $v(t)$ equal to V_{in}/n it is possible to derive the analytical expression of $v_{ph1}(t)$. Assuming $v_{C_r}(t_3) = 0$ and $i_{L_{out}}(t_3) = i_s(t_3)$, for $t_3 < t < t_4$, $v_{ph1}(t)$ can be derived as follows:

$$v_{ph1}(t) = \frac{V_{out}L_r + nV_{in}L_{out}}{L_r + n^2L_{out}} \left(1 - cos(\omega_r(t - t_3))\right), \tag{2.3}$$

where the resonant angular frequency $\omega_r = \sqrt{\frac{L_r + n^2L_{out}}{L_{out}L_rC_r}}$. Averaging $v_{ph1}(t)$ over the switching period T_{sw}, the output voltage V_{out} is therefore given by:

$$\begin{aligned} V_{out} &= \frac{1}{T_{sw}} \int_{t_0}^{t_0+T_{sw}} v_{ph1}(\tau)d\tau \\ &= \frac{V_{out}L_r + nV_{in}L_{out}}{L_r + n^2L_{out}} \frac{f_{sw}}{f_r}, \end{aligned} \tag{2.4}$$

where $f_r = \omega_r/(2\pi)$ and $f_{sw} = 1/T_{sw}$. Since $V_{out} \ll V_{in}$, $L_r/n^2 < L_{out}$, and $n > 1$, also $V_{out}L_r \ll nV_{in}L_{out}$. Thus, term $V_{out}L_r$ can be neglected in eq. (2.4) and the converter voltage conversion ratio (V_{out}/V_{in}) is approximated by:

$$\frac{V_{out}}{V_{in}} \approx \frac{nL_{out}}{(L_r + n^2L_{out})} \frac{f_{sw}}{f_r}. \tag{2.5}$$

As can be seen, the output voltage V_{out} is directly controlled by the switching frequency f_{sw}. Thus, the proposed solution is inherently a constant-on time modulation, where the *constant phase-shift*, here denoted also as *constant on-time* T_{on}, is determined by the resonant transition, while the output voltage regulation is obtained by varying the switching frequency. The constant on-time T_{on}, as depicted in Fig. 2.5, is equal to $t_5 - t_1$. During time T_{on}, the secondary current i_s varies from $i_s(t_1) = -nI_{cir}$ to $i_s(t_5) \approx nI_{cir}$. Moreover, the voltage applied across L_r at the primary side, assuming negligible the time interval $t_1 - t_2$, is $V_{in} - nv_{ph1}(t)$. Thus, the primary current variation during T_{on} is:

$$\begin{aligned} i_p(t_5) - i_p(t_1) &= \frac{1}{L_r} \int_{t_1}^{t_5} (V_{in} - nv_{ph1}(\tau))d\tau \\ &= \frac{V_{in}T_{on} - nV_{out}T_{sw}}{L_r} \\ &\approx 2I_{cir}. \end{aligned} \tag{2.6}$$

The circulating current I_{cir} can therefore be expresses as:

$$I_{cir} \approx \frac{V_{in}T_{on} - nV_{out}T_{sw}}{2L_r}. \tag{2.7}$$

As can be seen, the circulating current I_{cir}, that enables ZVS operation, is independent on the load conditions, as the voltage conversion ratio and therefore also T_{sw} are not dependent on I_{out} if the converter works in $Mode\ A$. This in an important feature of our solution and it is valid also for $Mode\ B$ for a wide range of operating conditions.

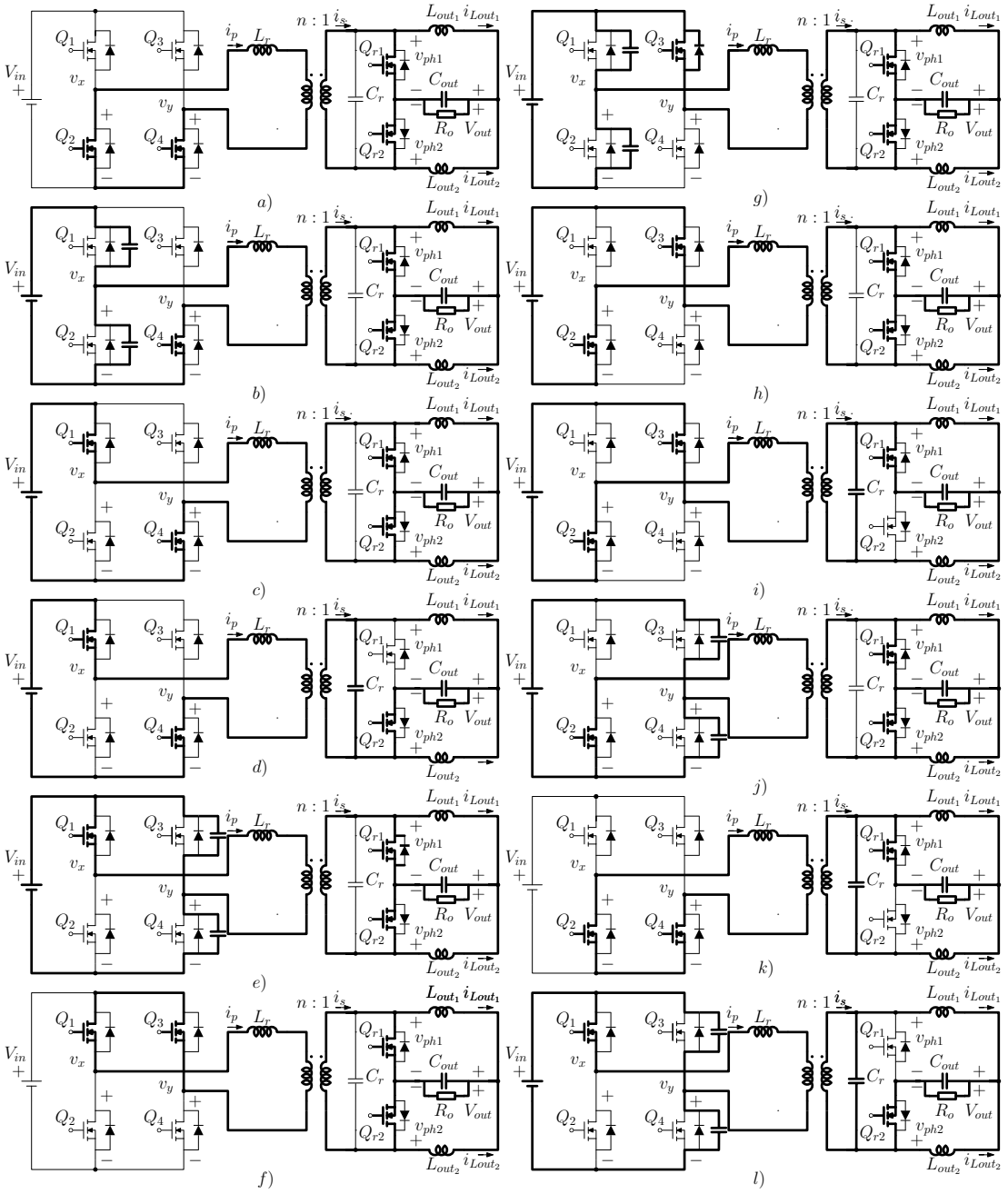


FIGURE 2.6: Switch configuration during each subinterval in $Mode\ A$ and $Mode\ B$: $Mode\ A$ (a) $t_0 - t_1$, b) $t_1 - t_2$, c) $t_2 - t_3$, d) $t_3 - t_4$, c) $t_4 - t_5$, e) $t_5 - t_6$ f) freewheeling subinterval $t_6 - t_7$ g) $t_7 - t_8$ h) $t_8 - t_9$ i) $t_9 - t_{10}$ h) $t_{10} - t_{11}$) j) $t_{11} - t_{12}$) and $Mode\ B$ (g) $t_0 - t_1$, a) $t_1 - t_2$, b) $t_2 - t_3$, c) $t_3 - t_4$, d) $t_4 - t_5$, h) $t_5 - t_6$).

2.3.2 Operation Mode B: Resonant Transition During the Freewheeling Phase

Fig. 2.8 reports the main converter waveforms during $Operating\ Mode\ B$, where the resonant voltage reaches zero during the freewheeling subinterval. The operation on $Mode\ B$ can be explained by analyzing the following subintervals:

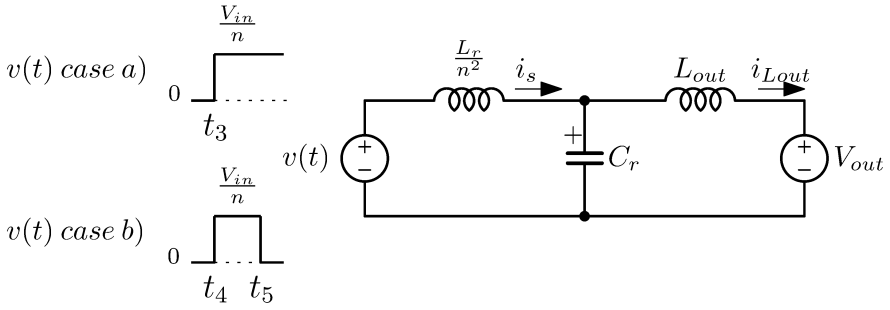


FIGURE 2.7: Equivalent resonant circuits for converter analysis: case a) equivalent circuit in $Mode\ A$, case b) equivalent circuit in $Mode\ B$.

1) $\boldsymbol{t_0 - t_1}$: switch Q_4 is turned on with ZVS and the primary current i_p freewheels through Q_2 and Q_4. Differently from Mode A, during this interval the synchronous rectifier switch Q_{r2} is still off, as the resonant voltage transition of $v_{ph2}(t)$ started on the negative half-cycle is still not completed as shown in Fig. 2.6(k).

2) $\boldsymbol{t_1 - t_2}$: at t_1, $v_{ph2}(t)$ reaches zero, ZCD_2 signal becomes high and Q_{r2} is turned on. The topological state is now depicted in Fig. 2.6(a).

3) $\boldsymbol{t_2 - t_3}$: this interval is the same as the interval $t_1 - t_2$ of $Mode\ A$.

4) $\boldsymbol{t_3 - t_4}$: this interval is the same as the interval $t_2 - t_3$ of $Mode\ A$. At $t = t_4$, i_s reaches i_{Lout1}.

5) $\boldsymbol{t_4 - t_5}$: at $t = t_4$, Q_{r1} is turned off and the resonance takes place between L_r, C_r and L_{out}. The topological state is now depicted in Fig. 2.6(e) .The duration of this mode, denoted as T_ϕ (i.e. $T_\phi = t_5 - t_4$), is a subinterval of T_{on} and it can be expressed as follows:

$$T_\phi = T_{on} - T_{ch}, \tag{2.8}$$

being T_{ch} the pre-charging time required to increase the secondary current i_s from $-nI_{cir}$ to $i_{Lout1}(t_4)$, i.e. when the resonant transition starts. Thus, the pre-charging time T_{ch} can be expressed by

$$\begin{aligned} T_{ch} &= (nI_{cir} + I_{Lout}(t_4))\frac{L_r}{nV_{in}} \\ &\approx (nI_{cir} + \frac{I_{out}}{2} - \frac{\Delta I_{Lout}}{2})\frac{L_r}{nV_{in}} \end{aligned} \tag{2.9}$$

where ΔI_{Lout} is the peak-to-peak current ripple and $i_{Lout}(t_4)$ is approximated as the minimum value of the inductor current i_{Lout1}. Thus, using (2.7) and (2.8), T_ϕ is given by:

$$T_\phi = \frac{1}{2}(T_{on} + \frac{nV_{out}}{V_{in}}T_{sw} - \frac{(I_{out} - \Delta I_{Lout})L_r}{nV_{in}}). \tag{2.10}$$

6) $\boldsymbol{t_5 - t_6}$: at $t = t_5$, Q_4 is turned off, i_p charges the capacitance of switch Q_4 and discharges the parasitic capacitance of switch Q_3. The topological state is now depicted in Fig. 2.6(l). At $t = t_6$, Q_3 is turned on in ZVS conditions and the positive half-cycle of the switching period is completed (i.e. $t_6 = t_0 + \frac{T_{sw}}{2}$).

During the negative half-cycle of a switching period, the behavior of the circuit is the same as the one described during the positive half-cycle, as depicted in Fig. 2.8.

Similarly to $Mode\ A$, the output voltage is derived averaging $v_{ph1}(t)$ over the switching period T_{sw}. In this case, however, the analytical derivation of $v_{ph1}(t)$ is slightly more complex, as the equivalent resonant circuit, shown in Fig. 2.7 case b), is excited by two voltage steps of $v(t)$, the first one at t_4 from zero to V_{in}/n and the second one at t_5 when $v(t)$ returns back to zero. Applying the superposition effects of the two voltage steps, $V_{ph1}(s)$ can be expressed as:

$$V_{ph}(s) = \frac{(V_{out}L_p + nVinL_{out})}{L_p + n^2L_{out}}\frac{1}{s}\frac{1}{1+\frac{s^2}{\omega_{cc}^2}} - \frac{nV_{in}L_{out}}{L_p + n^2L_{out}}\frac{e^{-T_\phi s}}{s}\frac{1}{1+\frac{s^2}{\omega_{cc}^2}}, \tag{2.11}$$

from 2.11 it is possible to derive the analytical expression of $v_{ph1}(t)$ in $Mode\ B$:

$$\begin{aligned} v_{ph1}(t) = {} & \frac{V_{out}L_r + nV_{in}L_{out}}{L_r + n^2L_{out}}\left(1 - cos(\omega_r(t - t_4))\right) - \\ & \frac{nV_{in}L_{out}}{L_r + n^2L_{out}}H\left(t - t_5\right)\left(1 - cos\left(\omega_r(t - t_5)\right)\right), \end{aligned} \tag{2.12}$$

where $H(t)$ is the Heaviside function (i.e. $H(t) = 1$, for $t \geq 0$ and $H(t) = 0$ for $t < 0$). In order to determine the resonant transition time during $Mode\ B$, denoted as T_{rB}, it is sufficient to impose $v_{ph1}(t_4 + T_{rB}) = 0$ and solve the equation for T_{rB}. Assuming $V_{out}L_r << nV_{in}L_{out}$, from (2.12), $cos(\omega_r T_{rB}) = cos(\omega_r(T_{rB} - T_\phi))$ or $\omega_r T_{rB} = -\omega_r(T_{rB} - T_\phi) + 2\pi$. Thus, T_{rB} can be written as:

$$T_{rB} = \frac{T_\phi + T_r}{2}. \tag{2.13}$$

The output voltage V_{out} is derived averaging (2.12) over T_{rB}. It can be shown that V_{out}/V_{in} can be expressed as (all demonstration in appendix A.1):

$$\frac{V_{out}}{V_{in}} = \left(\frac{\omega_r T_\phi + 2\sin\left(\omega_r\frac{T_\phi}{2}\right)}{2\pi}\right)\frac{nL_{out}}{L_r + n^2L_{out}}\frac{f_{sw}}{f_r}. \tag{2.14}$$

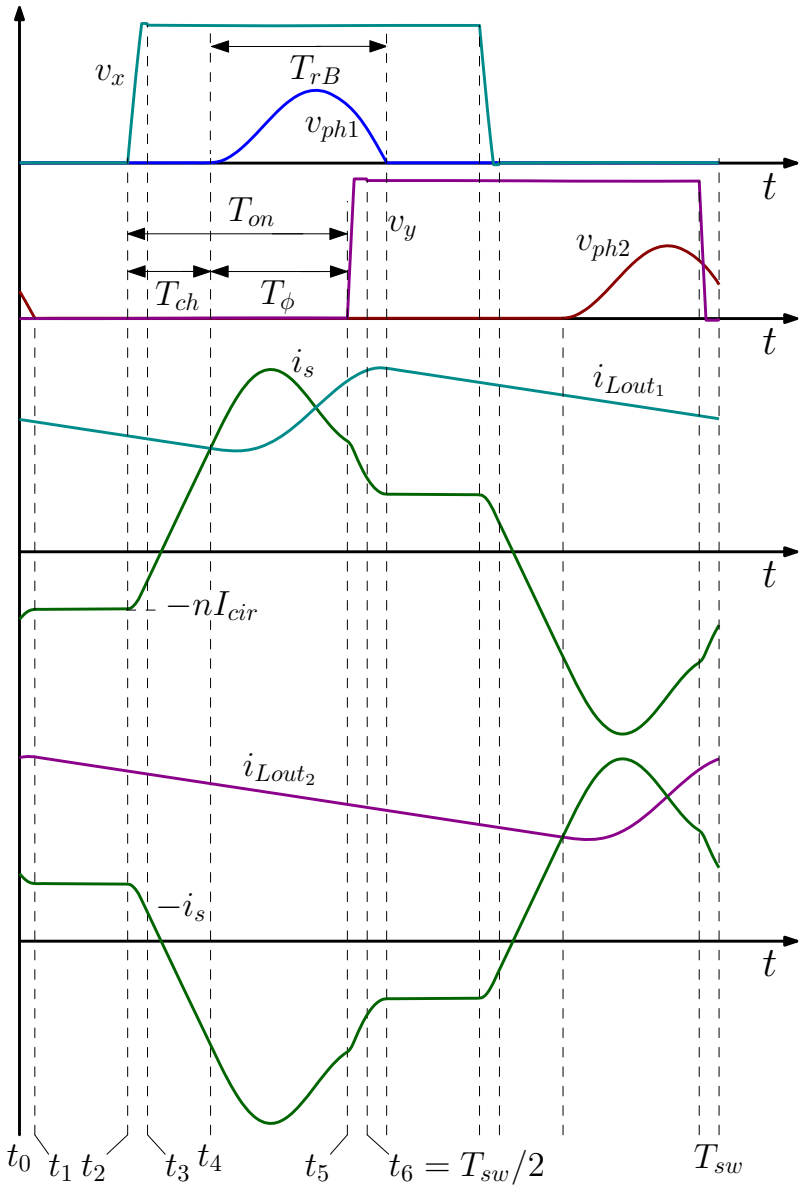


FIGURE 2.8: Main converter waveforms for Operation Mode B. From top to bottom: primary side voltages (v_x and v_y), voltages ($v_{ph1,2}$), secondary side transformer current i_s and inductor currents ($i_{L_{out1}}$ and $i_{L_{out2}}$)

It is worth noting that equation (2.14) differs from equation (2.5) only in the factor between the brackets and the output voltage V_{out} is still controlled by the switching frequency f_{sw} even in *Mode B*. In fact, looking at (2.10), T_ϕ decreases when the load current I_{out} increases. Thus, from (2.14), the output voltage V_{out} decreases and the control system imposes the reference voltage V_{ref} by increasing f_{sw}.

For any load operating condition, the maximum output voltage is obtained when the resonant transition is completed at the end of the freewheeling period, as depicted in Fig. 2.9. This is obtained at the maximum switching frequency, which is given by

$$f_{sw,max} = \frac{1}{2(T_{ch} + T_{rB})} \tag{2.15}$$

Using (2.10), (2.14) and (2.15), it is possible to obtain the relation between the maximum output voltage V_{out}, obtained with the maximum switching frequency, and the converter output current I_{out}. This relation is denoted as *current capability* $V_{out,max}(I_{out})$ and indicates the maximum power capability for given converter parameters. An example is reported in Fig. 2.10 using the parameters of Table 2.1.

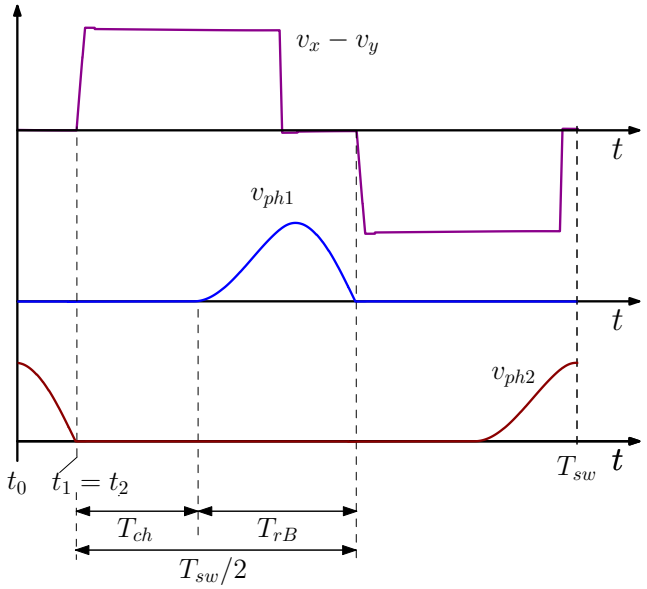


FIGURE 2.9: Converter operating waveforms at $f_{sw,max}$: difference between v_x and v_y and the secondary side voltages $v_{ph1,2}$.

TABLE 2.1: Converter parameters

Input voltage	$V_{in} = 54\ V$
Output inductances	$L_{out} = 110\ nH$
External inductance	$L_r = 1.7\ \mu H$
Resonance capacitance	$C_r = 233\ nF$
Transformer turns-ratio	$n = 7$
Constant on-time	$T_{on} = 515\ ns$
Output capacitance	$C_{out} = 470\ \mu F$

Fig. 2.10 shows the *current capability* curve $V_{out,max}(I_{out})$ and output characteristic (V_{out}-I_{out}) as a function of switching frequency f_{sw}. As can be seen, all the curves are almost flat for a wide range of output current. Thus, the

regulation of the output voltage is obtained with a small frequency variation. This is an important property of the proposed solution. Finally, Fig. 2.10 shows also the boundary between $Mode\ A$ and $Mode\ B$. As can be seen, the converter works mainly in $Mode\ B$ because of the edge between the operating modes of this converters depends from the resonant on time and the on-time. The first is a project parameter which depends from the resonant tank components, whilst the second depends from the ZVS capability; in fact as demonstrated in eq. (2.7), the circulating current which ensure ZVS at primary side is strongly depends from the on-time. As a result, if the on-time is high the copper losses at primary side will increase and even the dynamic performance will be deteriorated.

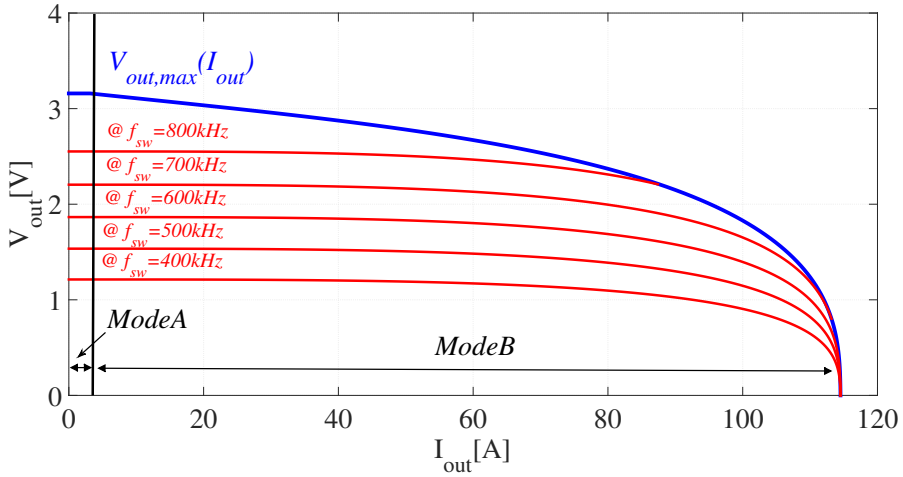


FIGURE 2.10: Current capability: maximum output voltage V_{out}, obtained at the maximum switching frequency, as a function of the converter output current I_{out}. All possible converter operating points are below this curve.

Finally, it is important to note the difference between this architecture and the ZVS full-bridge (FB) converter proposed in section 2.2.1. Both converters need an additional inductance to reach ZVS conditions at the primary side. The main difference between the two architectures is the circulating current at the primary side. In ZVS FB, the primary circulating current strongly depends on the load current [51]. In the proposed solution, the circulating current is almost independent on the load conditions. In fact, T_{on} is constant and T_{sw} has a small variation, as outlined in Fig. 2.10. Thus, looking at eq. (2.7), I_{cir} is almost constant.

On the other hand, the voltage rating of the proposed solution at the secondary side is higher due to quasi-resonant operation. In the practice case, however, even in the FB, there is a resonant transition between the primary inductance and the parasitic output capacitance of the rectifier switches C_{oss}. Thus, the peak voltage in the FB at the secondary side is almost the same, if dissipative snubbers are not used.

2.3.3 Control System and Current Sharing

The controller block diagram of the multi-phase dc-dc converter is reported in Fig. 2.11, where only two interleaved phases, indicated as $CELL_{1,2}$, are shown. The voltage loop controller implements the load line, as required by VRM specifications, imposing a resistive output impedance equal to R_{ll}, i.e. $V_{ref} = V_{out} - R_{ll} I_{cellT}$. This is obtained calculating the voltage error by the difference between the reference voltage V_{ref}, determined by the voltage identification (VID) code, and the sum of voltage v_{out} and of the total cell current i_{cellT} multiplied by the load line resistance R_{ll} [31]. As in any VRM applications, the inductor current is senses and used instead of the output current. The voltage error is then processed by the PID controller that drives the voltage controlled oscillator (VCO), the frequency of which is multiplexed for each of the interleaved cells. From each cell, two PWM signals with a duty cycle of 50% are generated at the primary side with programmed time shift equal to T_{on}.

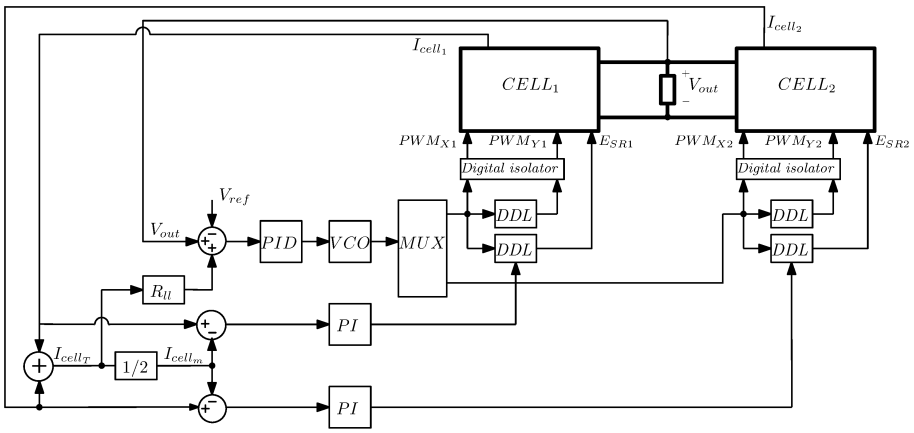


FIGURE 2.11: Block diagram of the multi-phase control architecture with two phases, indicated as $CELL_{1,2}$.

Fig. 2.11 also reports the block diagram for the current sharing loop needed to ensure the current balancing in presence of mismatches in the resonant components. This additional loop regulates the delay of the turn-off of the synchronous rectifier switches $Q_{r1,2}$ respect to the commutation instant determined by ZCD signal. The principle of operation is explained in Fig. 2.12 for mode A: synchronous rectifier switch Q_{r1} is turned off when ZCD signal is low and the enable signal E_{SR} is high. Signal E_{SR} is enabled with a delay equal to ΔT_{SR} respect to the natural zero current detection instant t_3. With this delay, the secondary current i_s increases by term ΔI before the resonance occurs, boosting the resonant voltage $v_{ph1}(t)$. If the current of this cell is lower than the mean cell current I_{cell_m}, the current sharing controller increases the delay ΔT_{SR} of the digital delay line (DDL) of the secondary side switches. As a consequence, the corresponding phase voltage increases, thus reducing the current unbalance.

To understand the new current sharing system here proposed is important to study the average output voltage of each phase with the current sharing loop, evaluated in $Mode\ A$. In $Mode\ A$, the expression of the resonant

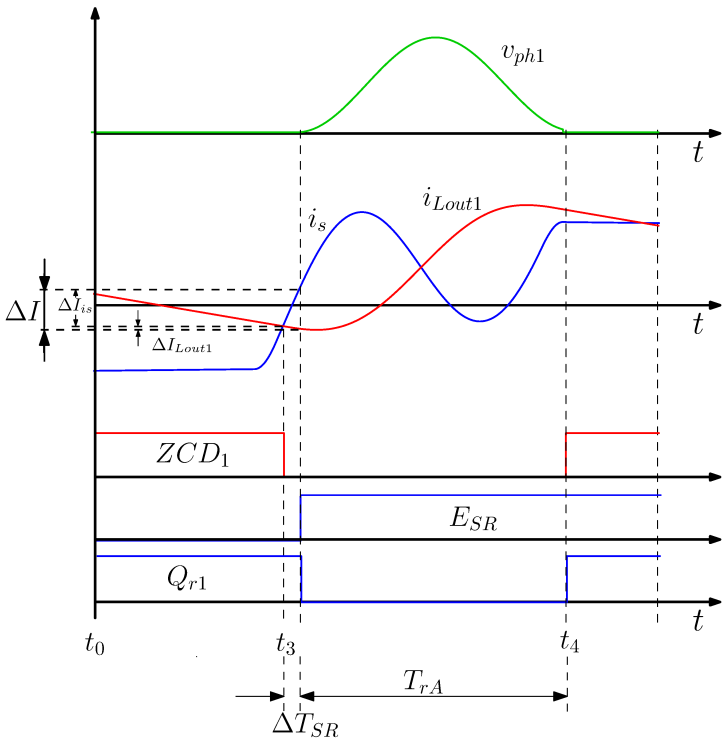


FIGURE 2.12: Main converter voltage and current waveforms at secondary side with $\Delta T_{SR} > 0$.

transition that start at $t_3 + \Delta T_{SR}$ is obtained solving the equivalent circuit of Fig. 2.13, where the generator in series with the resonant inductance represents the stored energy. Then applying a step variation of $v(t)$ equal to V_{in}/n. Assuming $v_{C_r}(t_3) = 0$ and $i_{L_{out}}(t_3) = i_s(t_3) + \Delta I$, for $t_3 + \Delta T_{SR} < t < t_4$.

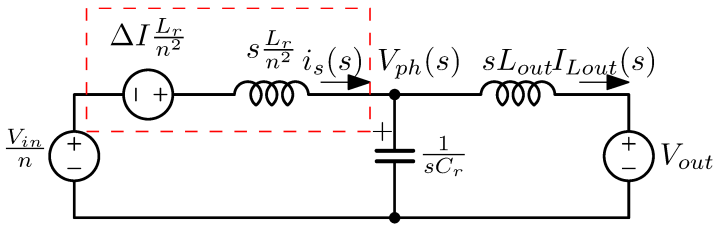


FIGURE 2.13: Equivalent cicrcuit in S when $\Delta T_{SR} > 0$.

Applying the superposition effects of the two voltage steps, considering the equivalent circuit in S-domain in Fig. 2.13, $V_{ph}(s)$ can be expressed as:

$$V_{ph}(s) = \frac{(V_{out}L_p + nVinL_{out})}{L_p + n^2L_{out}} \frac{1}{s} \frac{1}{1 + \frac{s^2}{\omega_{cc}^2}} + \frac{L_rL_{out}\Delta I\omega r}{L_r + n^2L_{out}} \frac{\omega_r}{s^2 + \omega_r^2}, \quad (2.16)$$

from 2.16 in S-domain is possible to get the $v_{ph1}(t)$:

$$\begin{aligned} v_{ph1}(t) = {} & \frac{V_{out}L_r + nV_{in}L_{out}}{L_r + n^2L_{out}} (1 - cos(\omega_r(t - t_3 - \Delta T_{SR}))) + \\ & + \frac{L_rL_{out}\Delta I\omega_r}{L_r + n^2L_{out}} sen(\omega_r(t - t_3 - \Delta T_{SR})), \end{aligned} \quad (2.17)$$

where ΔI is given by

$$\begin{aligned}\Delta I &= \Delta I_{i_s} + \Delta I_{i_{Lout1}} \\ &= \Delta T_{SR}\left(\frac{nV_{in}}{L_r} + \frac{V_{out}}{L_{out}}\right),\end{aligned} \tag{2.18}$$

where ΔI_{i_s} and $\Delta I_{i_{Lout1}}$ are the variations on i_s and i_{Lout1}, respectively, due to delay ΔT_{SR}. In order to derive the mean value of V_{ph1}, the value of resonant transition T_{rA} ($T_{rA} = t_4 - t_3 - \Delta T_{SR}$), also shown in Fig. 2.12, is needed. From equations (2.17) and (2.18) T_{rA} can be expressed as follows:

$$T_{rA} = \frac{2\pi - arccos\left(\frac{1-\omega_r^2\Delta T_{SR}^2}{1+\omega_r^2\Delta T_{SR}^2}\right)}{\omega_r}. \tag{2.19}$$

By averaging $v_{ph1,2}$ over the switching period T_{sw}, the following expression is obtained:

$$V_{ph1,2} = \frac{f_{sw}}{f_r}\frac{V_{out}L_r + nV_{in}L_{out}}{L_r + n^2L_{out}} \cdot K_{cs}, \tag{2.20}$$

where the current sharing factor K_{cs} is

$$K_{cs} = \frac{\left(2\pi - arccos\left(\frac{1-\omega_r^2\Delta T_{SR}^2}{1+\omega_r^2\Delta T_{SR}^2}\right) + 2\omega_r\Delta T_{SR}\right)}{2\pi}. \tag{2.21}$$

From (2.20) and (2.21), if ΔT_{SR} is increased when the phase current is below the average current I_{cel_m}, K_{cs} increases and V_{ph1} increases, reducing the current unbalance. Eqs (2.20) and (2.21) are also needed for the derivation of the small-signal model of the current sharing loop.

Considering now the converter in $Mode\ B$ is possible to get the voltage resonant $v_{ph1}(t)$ considering the resonant transition out from the diagonal power at primary side with $\Delta T_{SR} > 0$. From equations (2.12) and (2.17) is possible to derive the following relation:

$$\begin{aligned}v_{ph1}(t) = &\frac{V_{out}L_r + nV_{in}L_{out}}{L_r + n^2L_{out}}\left(1 - cos(\omega_r(t - t_3 - \Delta T_{SR}))\right) + \\ &+\frac{L_rL_{out}\Delta I\omega_r}{L_r + n^2L_{out}}sen(\omega_r(t - t_3 - \Delta T_{SR})) \\ &- \frac{nV_{in}L_{out}}{L_r + n^2L_{out}}H\left(t - t_5\right)\left(1 - cos\left(\omega_r(t - t_5)\right)\right),\end{aligned} \tag{2.22}$$

which is the actual $v_{ph1}(t)$ expression in a nominal operating condition under hypothesis that $\Delta T_{SR} > 0$ due to different discrete resonant parameters between each cells. In fact, as graphically demonstrated in Fig. 2.10 the converter works almost in $Mode\ B$.

2.3.4 Small Signal Model of FBPS-QR

The small signal model is based on the well-known ac averaging technique [69]. The converter is a buck-derived topology as FBPS [59], [70], [71] and the linearization of the average voltage $V_{ph1,2}$ is obtained deriving the partial derivative of $V_{ph1,2}$ of (2.20) respect to f_{sw}, ΔT_{SR}, V_{out} and the output current I_{out}.

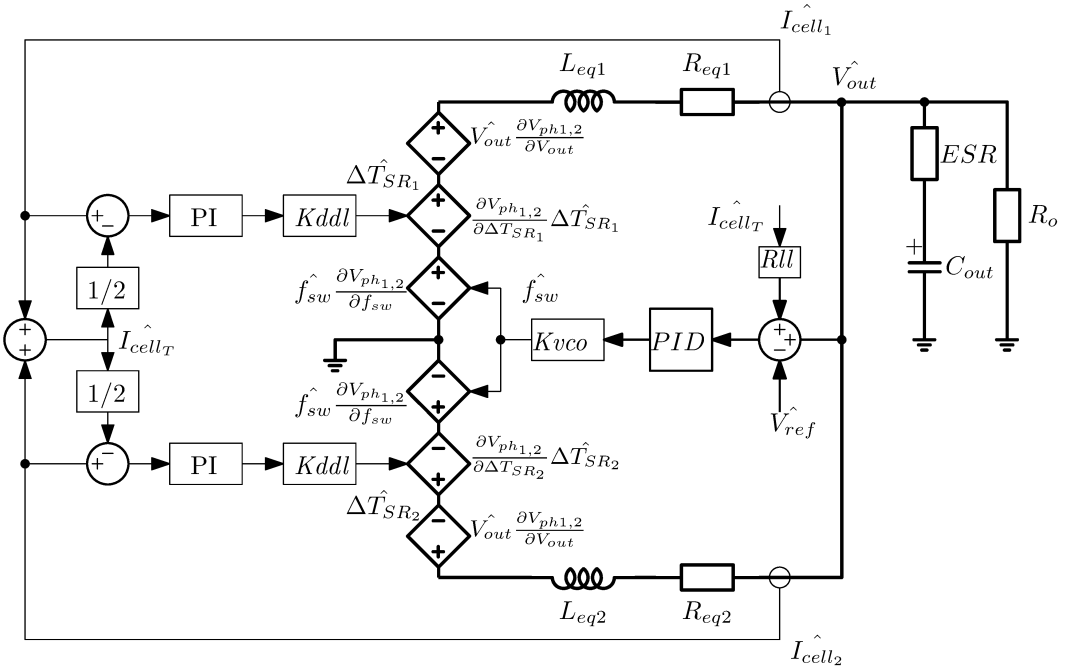


FIGURE 2.14: Two cells small-signal model.

To develop the small signal model for FBPS-QR converter with CDR, a block diagram of the small-signal are needed. The block diagram of the small-signal model of a 2-phase converter is reported in Fig. 2.14. For the case where a current doubler rectifier is used, the inductance L_{eq} equal to $L_{out}/2$. The most relevant parameters to be derived are the two equivalent voltage sources of Fig. 2.14 and the equivalent resistance R_{eq} which accounts for the variation of $V_{ph1,2}$ due to the variation of the output current I_{out}. R_{eq} is an important parameter in modelling FBPS-QR, its derivation will be given here which basically is based on duty cycle loss concept proposed in [59] for a classic full-bridge phase shift converter.

Using (2.8), (2.9) and (2.14) and deriving (2.14) with respect to I_{out}, R_{eq} is given by and demonstrated in Appendix A.2.

$$R_{eq} = f_{sw}\frac{L_{out}\cdot L_r}{2\left(L_r + n^2 L_{out}\right)}\left(1 + cos\left(\frac{\omega_r T_\phi}{2}\right)\right). \tag{2.23}$$

From the R_{eq} model, it is seen that when $T_\phi = T_{res}$, which means that the converter is still in $Mode\ A$, and the equivalent resistance R_{eq} equal zero, in fact the model proposed is valid only for $Mode\ B$. Indeed, in $Mode\ A$ the resonant voltage is into the input power transferring phase (section 2.3.1) and there is no voltage drop due to the output current I_{out}. Using the parameters

of Table I, several load points are reported in Fig. 2.15. It is evident that the later the resonant voltage reaches zero during the freewheeling mode, the higher R_{eq} is.

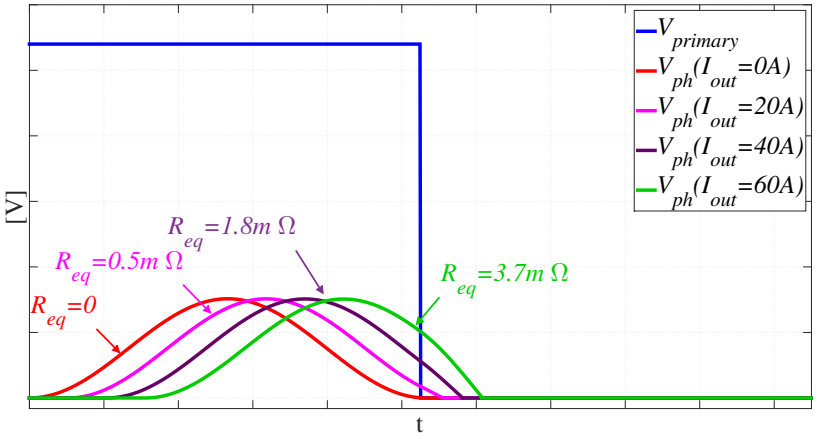


FIGURE 2.15: Resonant voltage loss at secondary side using the parameters of Table I.

Take the inductor's current $\widehat{I_{cell_1}}$ and the voltage capacitor $\widehat{V_{C_{out}}}$ as the state variables, and the switching frequency f_{sw} and the delay ΔT_{SR} as the inputs. The state-space equation for the circuit in Fig. 2.14 are:

From the model of Fig. 2.14, the controlled voltage sources are obtained as:

$$\frac{\partial V_{ph1,2}}{\partial f_{sw}} = \frac{(nV_{in}L_{out} + V_{out}L_r)}{(L_r + n^2 L_{out})\, f_r} K_{cs}, \tag{2.24}$$

and

$$\frac{\partial V_{ph1,2}}{\partial \Delta T_{SR}} = f_{sw} \frac{2\,(nV_{in}L_{out} + V_{out}L_r)}{L_r + n^2 L_{out}} \cdot \left(\frac{\omega_r^2 \Delta T_{SR}^2}{\omega_r^2 \Delta T_{SR}^2 + 1} \right). \tag{2.25}$$

while the terms $\frac{\partial V_{ph1,2}}{\partial V_{out}}$ is directly derived from (2.20) (demonstration reported in A.3) and it is usually negligible. As a second order effect, it should be also noted that the time interval between two resonance on $V_{ph1,2}$ is not strictly defined by the controller but is also affected by the intersection of $i_{Lout_{1,2}}$ and i_s of Fig. 2.5 for the $Mode\ A$ operation, or Fig. 2.8 for the $Mode\ B$. More precisely, the mismatch of the switching period between the secondary side of the converter and the control system can be seen as the variation of T_{ch} with respect to previous switching period. Thus, such second order effect can be written as:

$$\begin{aligned} \hat{T}_{sw}[k] &= T_{ch}[k] - T_{ch}[k-1] \\ &= \frac{I_{Lout_{1,2}}[k] - I_{Lout_{1,2}}[k-1]}{\frac{nV_{in}}{L_r} + \frac{V_{out}}{L_{out}}} \end{aligned} \tag{2.26}$$

reported in the continuous time domain the expression can be rewritten as:

$$\hat{T}_{sw} \approx \frac{L_r T_{sw}}{2nV_{in}} \frac{d\hat{I}_{cell}(t)}{dt} \tag{2.27}$$

where $\hat{I}_{cell}$ is the small signal averaged value of the sum of inductor currents $i_{Lout_{1,2}}$. This variation in term of frequency can be expressed as

$$\hat{f}_{sw} \approx -\frac{L_r f_{sw}}{2nV_{in}} \frac{d\hat{I}_{cell}(t)}{dt} \tag{2.28}$$

Since the $V_{ph1,2}$ of (2.20) is proportional to the switching frequency and a positive slew rate of I_{cell} increases the period, as reported in (2.28), this effect acts as an inductive contribution L_{ch}, i.e.

$$L_{ch} \approx \frac{L_r f_{sw}}{2nV_{in}} \frac{\partial V_{ph1,2}}{\partial f_{sw}} \tag{2.29}$$

In order to take into account of this effect, L_{ch} shall be be added to L_{eq}.

Thus, all the parameters of the model of Fig. 2.14 are now available and the relevant transfer function, can be evaluated. For example, for each cell, the transfer functions from f_{sw} to V_{out}, without considering the negligible feedback effect of $\frac{\partial V_{ph1,2}}{\partial V_{out}}$, can be expressed as

$$\begin{aligned} G_{v_{out}f_{sw}}(s) &= \frac{\hat{V}_{out}(s)}{\hat{f}_{sw}(s)} \\ &= \frac{\partial V_{ph1,2}}{\partial f_{sw}} \frac{R_o}{R_o + R_{eq}} \frac{(1 + ESR \cdot C_{out}s)}{p(s)}, \end{aligned} \tag{2.30}$$

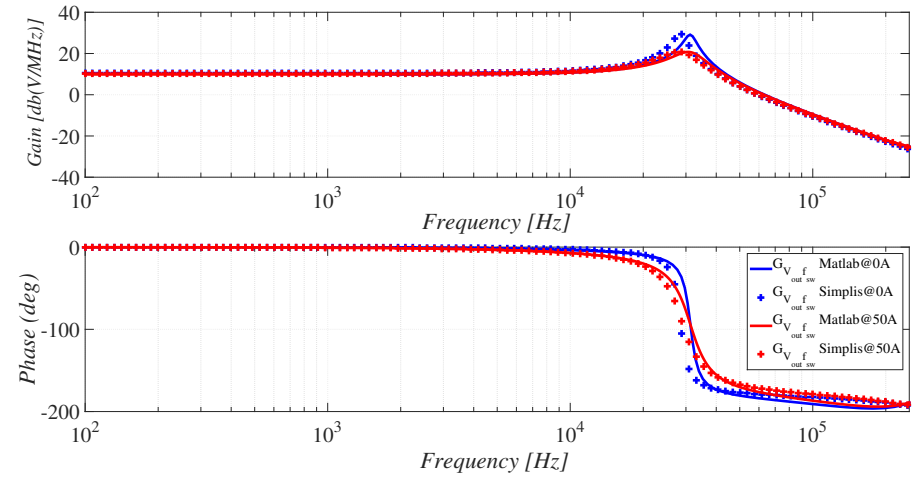
where $p(s)$

$$p(s) = s^2 \frac{L_{eq} C_{out} R_{os}}{R_{eq} + R_o} + s \frac{C_{out}\left(ESR \cdot R_o + R_{eq} R_{os}\right) + L_{eq}}{R_{eq} + R_o} + 1 \tag{2.31}$$

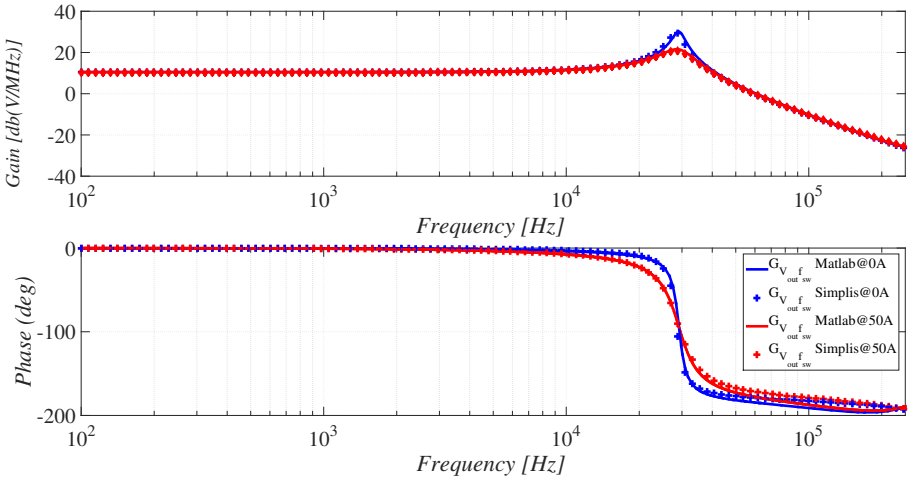
being $R_{os} = R_o + ESR$.

Similarly, the transfer function from the delay ΔT_{SR} to V_{out}, needed for the current sharing loop, is given by

$$\begin{aligned} G_{v_{out}\Delta T_{SR}}(s) &= \frac{\hat{V}_{out}(s)}{\Delta\hat{T}_{SR}(s)} \\ &= \frac{\partial V_{ph1,2}}{\partial \Delta T_{SR}} \frac{R_o}{R_o + R_{eq}} \frac{(1 + ESR \cdot C_{out}s)}{p(s)}. \end{aligned} \tag{2.32}$$



(a)



(b)

FIGURE 2.16: a) Comparison between the transfer function Simulated with Simplis and calculated neglecting the gain $\frac{\partial V_{ph1,2}}{\partial V_{out}}$ and L_{ch} b) Comparison between the complete transfer function and Simplis

Fig. 2.16 shows the control to output transfer function calculated by Simplis simulation, i.e. the transfer function between the switching frequency $d\hat{f}_{sw}$ and the output voltage $d\hat{V}_{out}$. In the figure is reported the typical second-order transfer function of the buck converter in which R_{eq} influences the damping of the second order filter. In fact for $I_{out} = 50A$ the equivalent resistance is $R_{eq} = 2.9\ m\Omega$ increasing the dumping factor of the complex poles. Moreover in Fig. 2.16 is reported the comparison between the theoretical transfer function calculated a) neglecting the gain $\frac{\partial V_{ph1,2}}{\partial V_{out}}$ and L_{ch} and b) considering all the terms.

2.3.5 Small Signal Analysis of Cells Current Sharing

In section 2.3.4 is studied the small signal model of FBPS-QR demonstrating that is a derived buck converter topology. In general, FBPS-QR can be duplicated and connected in parallel with an interleaving technique as demonstrated in section 2.3.3. However, an in-depth mathematical model and analysis for the current sharing of multiphase FBPS-QR has not yet curried out.

Considering two cells these equations are always valid:

$$C\frac{dv_c(t)}{dt} = i_{cell1}(t) + i_{cell2}(t) - i_{out}(t) \tag{2.33}$$

$$\begin{aligned} L\frac{di_1(t)}{dt} = &-v_c(t) - (R_{s1} + ESR)\, i_{L1}(t) - ESRi_{L2}(t) \\ &+ ESRi_{out}(t) + K_{f_{sw1}} f_{sw} + K_{Tst1}\Delta_{Tst1} \end{aligned} \tag{2.34}$$

where $R_{s1} = R_{eq1} + DCR_1$, $K_{f_{sw1}}$ depends from the converter parameters and input voltage instead K_{Tst1} depends from ΔT_{SR}.

The state-space variables are defined as follows:

$$\hat{x(t)} = \left[\hat{v_c(t)} \;\; \hat{i_{cell1}} \;\; \hat{i_{cell2}}\right]^T \tag{2.35}$$

$$x(t) = \left[v_c(t) \;\; i_{cell1} \;\; i_{cell2}\right]^T \tag{2.36}$$

$$u(t) = \left[i_{out}(t) \;\; f_{sw1} \;\; \Delta_{Tst1} \;\; f_{sw2} \;\; \Delta_{Tst2}\right]^T \tag{2.37}$$

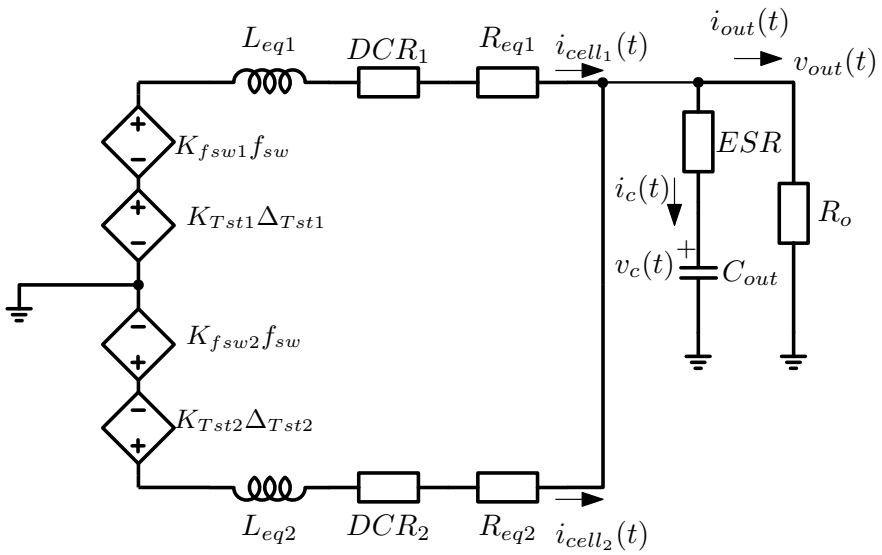


FIGURE 2.17: Two-phases FBPS-QR semplified model.

Considering the simplified circuit in Fig. 2.17 the state-space matrices of the system $\hat{x(t)} = Ax + Bu$ are:

$$A = \begin{bmatrix} 0 & \frac{1}{C_{out}} & \frac{1}{C_{out}} \\ -\frac{1}{L_{eq1}} & -\frac{R_{s1}+ESR}{L_{eq1}} & -\frac{ESR}{L_{eq1}} \\ -\frac{1}{L_{eq2}} & -\frac{ESR}{L_{eq2}} & -\frac{R_{s2}+ESR}{L_{eq2}} \end{bmatrix} \tag{2.38}$$

$$B = \begin{bmatrix} \frac{1}{C_{out}} & 0 & 0 & 0 & 0 \\ \frac{ESR}{L_{eq1}} & K_{f_{sw1}} & K_{Tst1} & 0 & 0 \\ \frac{ESR}{L_{eq2}} & 0 & 0 & K_{f_{sw2}} & K_{Tst2} \end{bmatrix} \tag{2.39}$$

To study the dynamic model of the current-sharing, here the differential state variables model are derived. Hence, the average current value and the error between each cells is useful to derive such model. Considering N cells the average current is defined as:

$$\overline{I(t)} = \frac{1}{N}\sum_{k=1}^{N} i_{cell_k}(t), \tag{2.40}$$

whilst the $average\ input\ voltage$ can be expressed by:

$$\overline{K_{f_{sw}} f_{sw}(t)} = \frac{1}{N}\sum_{k=1}^{N} K_{f_{sw_k}} f_{sw}(t). \tag{2.41}$$

Thus, each cell's current can be defined by the following relation:

$$i_{cell_k} = \overline{I(t)} + \delta i_{cell_k}, \tag{2.42}$$

it easy to demonstrate that $\sum_{k=0}^{N} \delta i_{cell_k} = 0$.

Considering the system defined in equations (2.35), (2.36), (2.37), (2.38) and (2.39) it is possible to arrange the matrix system in another way. The common component of the system is $K_{f_{sw}} f_{sw}$, instead the differential component is $K_{Tst}\Delta_{Tst2}$.

Considering two cells the following state-space system is obtained, with the state-space variables defined as follows:

$$x(t) = \begin{bmatrix} v_c(t) & \overline{I(t)} & \delta i_{cell_1} & \delta i_{cell_2} \end{bmatrix}^T \tag{2.43}$$

$$u(t) = \begin{bmatrix} f_{sw} & i_{out} & \Delta_{Tst1} & \Delta_{Tst2} \end{bmatrix}^T \tag{2.44}$$

where the equivalent matrices are defined as:

$$A = \begin{bmatrix} 0 & \frac{2}{C_{out}} & 0 & 0 \\ -\frac{1}{L_{eq}} & -\frac{R_0+2ESR}{L_{eq}} & 0 & 0 \\ 0 & 0 & -\frac{R_0}{L_{eq}} & 0 \\ 0 & 0 & 0 & -\frac{R_0}{L_{eq}} \end{bmatrix} \tag{2.45}$$

$$B = \begin{bmatrix} 0 & \frac{1}{C_{out}} & 0 & 0 \\ \frac{K_{fsw}}{L_{eq}} & \frac{ESR}{L_{eq}} & 0 & 0 \\ 0 & 0 & \frac{K_{Tst1}}{L_{eq}} & 0 \\ 0 & 0 & 0 & \frac{K_{Tst2}}{L_{eq}} \end{bmatrix}, \tag{2.46}$$

Considering matrices (2.45) and (2.46) it is noticed that are block diagonal matrix. Thus, it is possible to derive the equivalent common system between two cells:

$$\dot{x_{cm}}(t) = A_{cm}x_{cm}(t) + B_{cm}u_{cm}(t), \tag{2.47}$$

the common system is descripted by the following matrices:

$$A_{cm} = \begin{bmatrix} 0 & \frac{2}{C_{out}} \\ -\frac{1}{L_{eq}} & -\frac{R_0+2ESR}{L_{eq}} \end{bmatrix}, \tag{2.48}$$

and

$$B_{cm} = \begin{bmatrix} 0 & -\frac{1}{C_{out}} \\ \frac{K_{fsw}}{L_{eq}} & \frac{ESR}{L_{eq}} \end{bmatrix} \tag{2.49}$$

According to (2.47), (2.48) and (2.49) the following time-domain relation is derived:

$$\dot{\delta i_{cell}}(t) = -\frac{R_0}{L_{eq}}\delta i_{cell}(t) + \frac{K_{Tst}\Delta_{Tst}}{L_{eq}}. \tag{2.50}$$

From eq. 2.50 here is derive the transfer function between the variation of the current in each cell and the variation of the rectifier delay Δ_{Tst}.

$$\frac{\delta I_{cell}(s)}{K_{Tst}\Delta_{Tst}} = \frac{1}{L_{eq}}\frac{1}{\frac{R_0}{L_{eq}} + s}. \tag{2.51}$$

2.3.6 Critical inductance for FBPS-QR

In VRM application the multichannel interleaving synchronous buck topology has been widely discussed as the best way to ensure high dynamic performance maintaining high efficiency. In multichannel buck converter the current ripple in the output inductance can be greatly reduced. However, nowadays, the slew rate requirement for such kind of application is around $750A/\mu s$ to $1000A/\mu s$, hence a smaller inductance value and high bandwidth control loop are needed. The low value of inductance causes large current ripples a so extra conduction losses. The main purpose of this section is to find out an analytical model to calculate the critical inductance for FBPS-QR as for the buck converter.

The slew rate of the output current i_{out} is much faster than $i_{L_{out}}$. In a typical buck converter the waveform which represents the inductor current is close to the step response of a typical second-order system. As simplification the average inductor current slew rate during the transient response can be approximated as follow [61]:

$$\frac{di}{dt}_{avg} = \frac{\Delta I_{out}}{t_r}. \tag{2.52}$$

where t_r is the rise time of the current.

The relationship between rise time and control bandwidth ω_c can be approximated as:

$$t_r = \frac{T_c}{4} = \frac{\pi/2}{\omega_c}. \tag{2.53}$$

The average current slew rate needed for ensuring the transient response can be derived from equations (2.52) and (2.53):

$$\frac{di}{dt}_{avg} = \frac{\Delta I_{out}\omega_c}{\pi/2}. \tag{2.54}$$

Assuming that the switching frequency has an increment of Δf_{sw} during a transient event it is possible to derive the relation for the inductor average current slew rate during the transient response:

$$\frac{di}{dt}_{avg} = \frac{\Delta f_{sw}}{f_r}\frac{nL_{out}V_{in} + V_{out}L_p}{L_p + n^2 L_{out}}\frac{1}{L_{out}}. \tag{2.55}$$

Thus, considering eq. (2.54) it follows that by designing the control bandwidth as high as possible the average current slew rate can increase proportionally with it. Hence, for a small variation of the switching frequency, ω_c can also be considered constant. Considering now eq. (2.55) it is always true that during a transient event Δf_{sw} increases and the average model is still valid. In this scenario the average inductor current slew rate is determined by eq. (2.54). Let's suppose to increase the output inductance L_{out}, Δf_{sw} also increases due to mainly two mechanisms: one is the effect of the transient, while, the other, is the $Mode\ B$ effect. In general it is always true that the average model analysis is valid until the frequency is not saturated. When the value of inductance reaches such value, where the switching frequency is saturated, for a fixed load transient, the inductance is defined as the "$critical\ inductance$" which is given by the following equation:

$$\begin{aligned} L_{crt} &= \frac{\frac{\pi}{2}\left(nL_{out}V_{in} + V_{out}L_p\right)}{f_r\left(L_p n^2 L_{out}\right)\Delta I_{out}\omega_c}\Delta f_{sw_{max}} \\ &\approx \frac{\frac{\pi}{2}V_{in}}{f_r L_p n \Delta I_{out}\omega_c}\Delta f_{sw_{max}}, \end{aligned} \tag{2.56}$$

eq. 2.56 is derived considering the converter working in $Mode\ A$.

If the inductance value increases beyond the value calculated in eq. (2.56), the switching frequency become saturated and its value is defined by the following equation:

$$f_{sw_{maxCI}} = \frac{1}{2T_{on}}. \tag{2.57}$$

where T_{on} is the fixed on-time.

Once the switching frequency is saturated, the inductor average current slew rate cannot be no longer determined by (2.54). Thus, inductor average current slew rate is determined by eq. 2.55.

In general, considering the converter in $Mode\ A$, it is possible to derive the equation definition for $\Delta f_{sw_{max}}$ in eq. (2.56). Considering eq. (2.4) (2.57) $\Delta f_{sw_{max}}$ is defined by the following equation:

$$\begin{aligned}\Delta f_{sw_{maxCI}} &= f_{sw_{maxCI}} - f_{sw_{MODE_A}} \\ &= \frac{1}{2T_{sh}} - \frac{f_r\left(L_p + n^2 L_{out}\right)}{nL_{out}V_{in} + V_{out}L_p}V_{out},\end{aligned} \tag{2.58}$$

where $f_{sw_{MODE_A}}$ is derived from eq. (2.4).

Equation (2.58) is not always valid, since the converter, as reported in Fig. 2.10, is working mainly in $Mode\ B$ operations. However, considering the worst case of transient response, from light load to heavy load, eq. (2.58) comes as a good reference in designing the converter.

2.4 Experimental Results of 48 V VRM based on FBPS-QR

The proposed topology and control system have been tested by the implementation of three test chip on $0.16\ \mu$ lithography. One chip implements a driving system of secondary side synchronous rectifier ensuring zero-voltage and zero-current switching conditions. The second chip implements a control scheme for primary side full-bridge in COT and an adjustable dead-time control, while the third is a multiphase digital controller based on the architecture of Fig. 2.11.

The proposed system has been tested for VRM and DDR applications. This section presents the experimental results for both solutions.

2.4.1 VRM power supply

As shown in Fig. 2.20, a test board (in chapter 4 is reported the transformer realization for 48 V VRM FBPS-QR) with 4 cells and $I_{out} = 220\ A$ has been realized to experimentally validate the performance of proposed topology. The total space of the test board is $72mmX43mm$.

The primary side full-bridge is implemented with STL35N75F3. The secondary side are BSZ013NE2LS5I. The main passive elements parameters are as follows: $L_r = 1.7\ \mu H$, $L_{out} = 120\ nH$ (EATON FP0906R1 R12R), $C_r = 233\ nF$ and the transformer is made by planar core with a turns ratio of 7:1. The switching frequency is about $560\ kHz$ for each phase.

Efficiency measurements, including converter, driving and control losses, at nominal output voltage $V_{out} = 1.8\ V$ and $V_{in} = 54\ V$, are shown in Fig. 2.18. The peak efficiency is equal to 93.1% and it is maintained high by using phase shedding.

The single-cell loss breakdown at the peak efficiency (i.e. at $I_{out} = 120A$) is shown in Fig. 2.19. The losses are evaluated analytically and they match the experimental measurements with an error of 10%. As can be seen in Fig. 2.19, the major contribution is coming from the transformer, where the

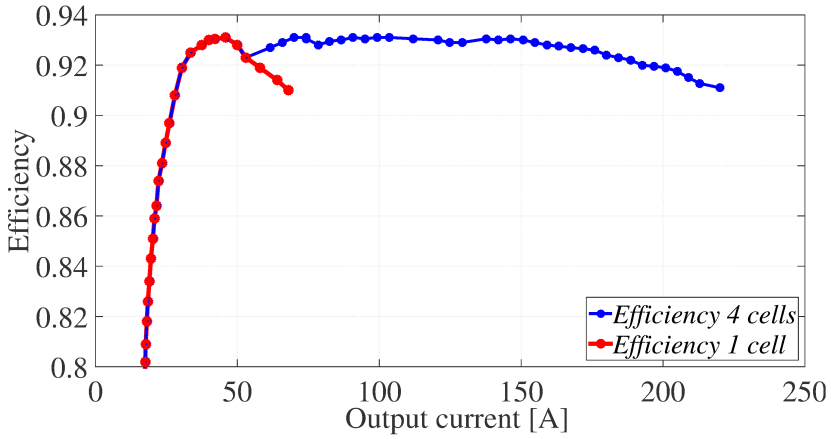


FIGURE 2.18: Total system efficiency over the total load range.

conduction losses are dominant, and in the other magnetic elements. Moreover, the loss contribution of the output synchronous rectifiers. The losses on the secondary side MOSFETs are considerable because of the voltage rating of the secondary side MOSFETs (25 V with $R_{ds,ON} = 1.3m\Omega$). In fact, as demonstrated in section 2.5.1, the resonant voltage peak is double than the ratio between the input and the transformer ratio, due to resonant transition. Instead, the losses in the resonant capacitor are small, having adopted COG dielectric in order to reduce ESR value. In FBPS-QR the main drawback is the need to adopt higher voltage secondary side MOSFETs comparing with an hard switching solution, such as classic full-bridge phase-shift current doubler.

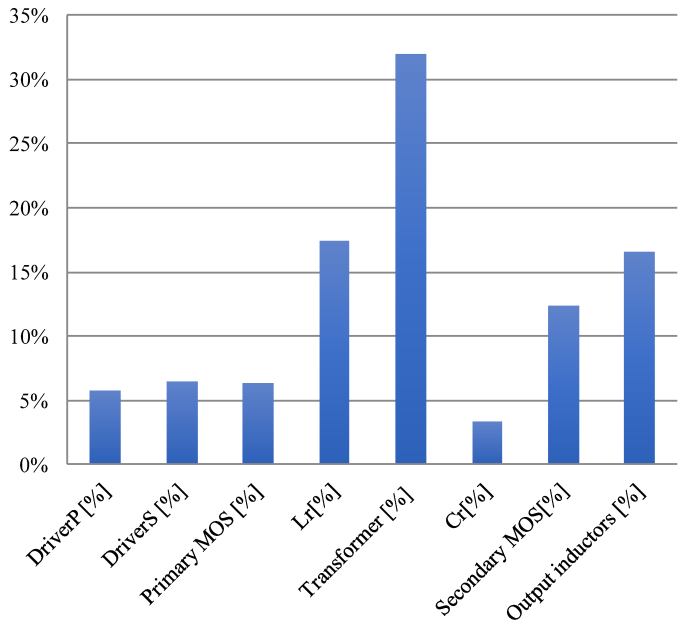


FIGURE 2.19: Loss breakdown of the single cell at the peak efficiency point.

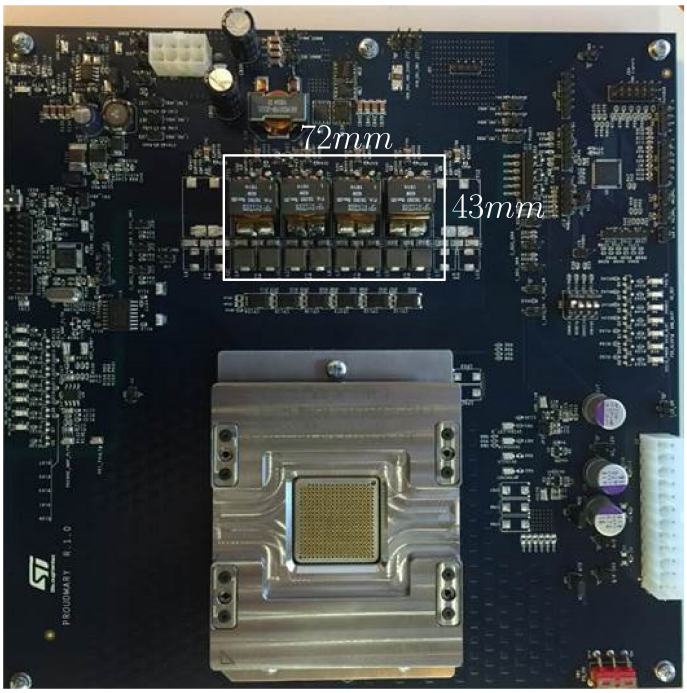


FIGURE 2.20: Test board providing VR13.0 specifications from 48 V.

Transient-response measurements obtained at $V_{in} = 51\ V$ and $V_{out} = 1.8\ V$ are shown in Fig. 2.21, 2.22 and 2.23. In Fig. 2.21 the output voltage transient response in presence of a load step variation from 41A to 228 A, with a slew rated of $750A/\mu s$, is reported. The output voltage has a resistive behavior without overshoot or undershoot. Fig. 2.22 displays the transient performed by the voltage transient tool (VTT) with $900\ kHz$ of load step from $60\ A$ to $220\ A$.

To validate the effectiveness of the ZVS strategy at primary side, in Fig. 2.24 is reported the ZVS transition corresponding with the time interval $t_5 - t_6$ of the circuit configuration depicted in Fig. 2.6(e).

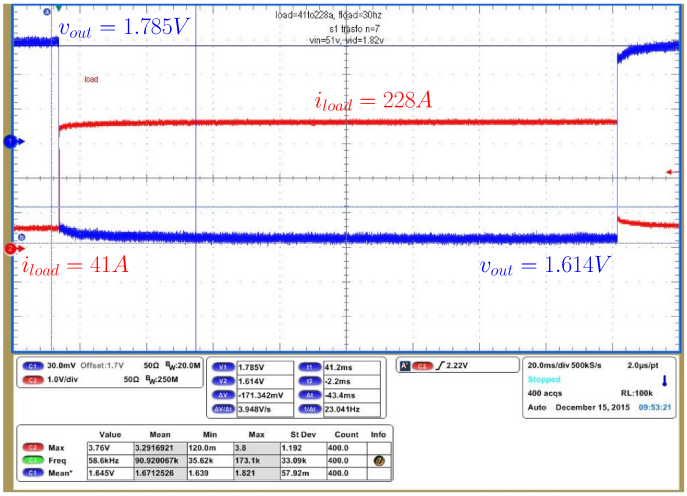


FIGURE 2.21: Transient response from $41\ A$ to $228\ A$ load step.

Finally, Fig. 2.23 shows a voltage identification (VID) transition.

The proposed converter fully meets the voltage deviation at VRM output that is compatible with $1\ m\Omega$ load line requirement. Moreover, Fig. 2.22 shows that the output impedance is mainly resistive for a wide range of frequency, as required by Intel specifications.

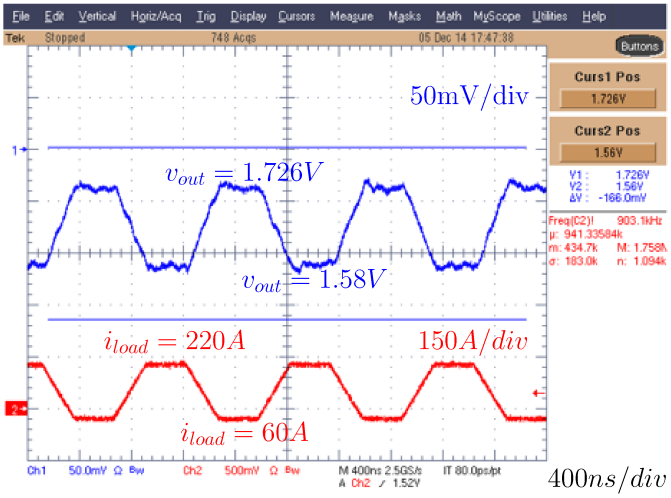


FIGURE 2.22: Output voltage behavior with 900 kHz load step from 60 A to 220 A.

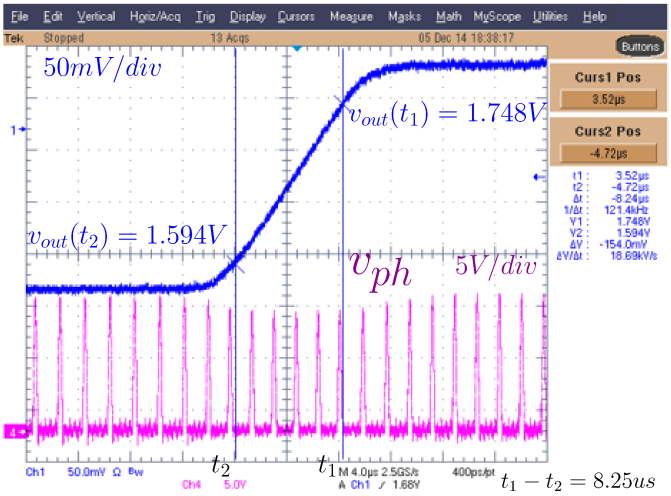


FIGURE 2.23: VID transition: output voltage (upper trace), v_{ph} (lower trace).

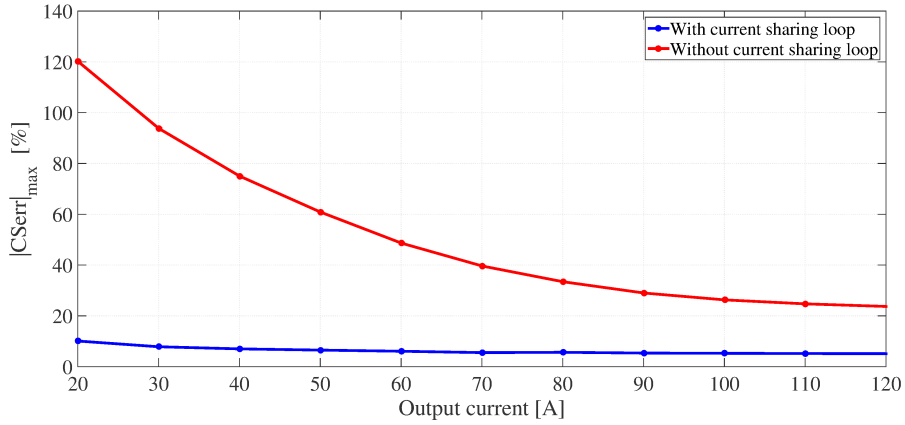


FIGURE 2.25: Current sharing error with and without current sharing control loop

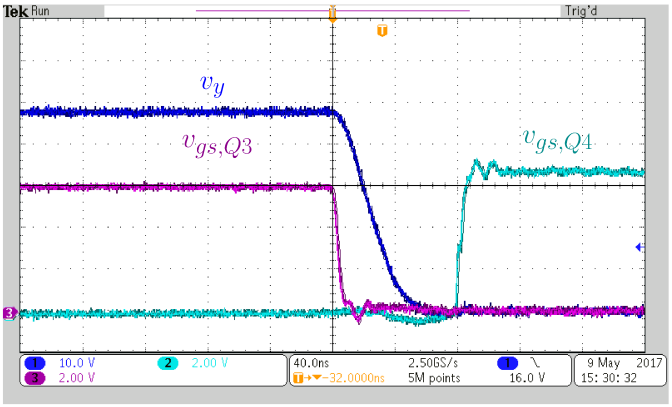


FIGURE 2.24: An example of ZVS turn on for Q_4: voltage at node y (v_y), driving voltage for Q_3 (v_{gsQ3}) and Q_4 (v_{gsQ4}).

Finally, Fig. 2.25 reports the current sharing error, defined as the relative error of the current of each phase respect to the ideal case of perfect matching. Only the value of the phase with the highest mismatch is shown. As can be seen, the measured improvement obtained with the current sharing loop demonstrates the effectiveness of the proposed approach reported in section 2.3.3.

2.4.2 DDR power supply

As mentioned in section 1.1.1 the memory power usage, for a given workload of a data-center's motherboard, is almost 25 % of the overall consumption. In this scenario it is important to validate the proposed converter even for different voltage rail, to prove the effectiveness of the proposed converter for all digital load applications. Here a prototype based on the proposed FBPS-QR is depicted in Fig. 2.27 for DDR application.

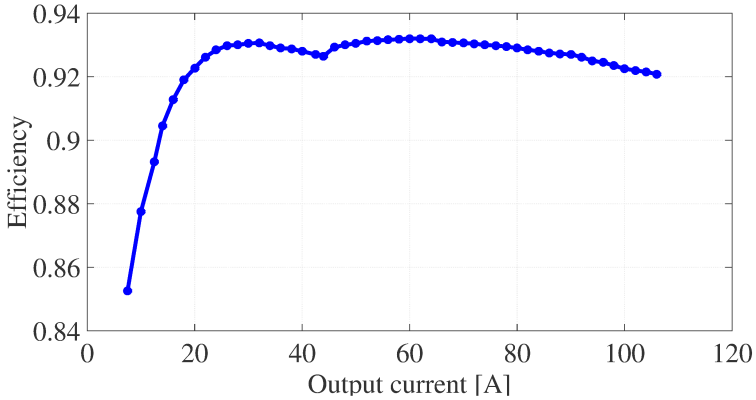


FIGURE 2.26: System efficiency over the total load range for the DDR power supply.

The output voltage specification is $V_{out} = 1.2\ V$ with a maximum current of $I_{out} = 105\ A$. The prototype was built using two cells; the primary side MOSFETs are STL35N75F3, while the secondary side ones are BSZ013NE2LS5I. The main passive parameters are: L_r = 3.3 μH, $L_{out} = 220\ nH$, $C_r = 600\ nF$ and the transformer is made by a planar core with a turns ratio 9:1. The switching frequency is about $250\ kHz$ for each phase.

Efficiency measurement, including converter, driving and control losses, at nominal output voltage $V_{out} = 1.2V$ and $V_{in} = 54V$, is shown in Fig. 2.26. The peak efficiency is 93.2%.

Comparing with the CPU application the proposed DDR power supply presents higher peak efficiency even if the voltage rail is 600mV less. The main reason is because of lower dynamic performance requirement allowing to use higher output inductance and higher transformer turns ratio.

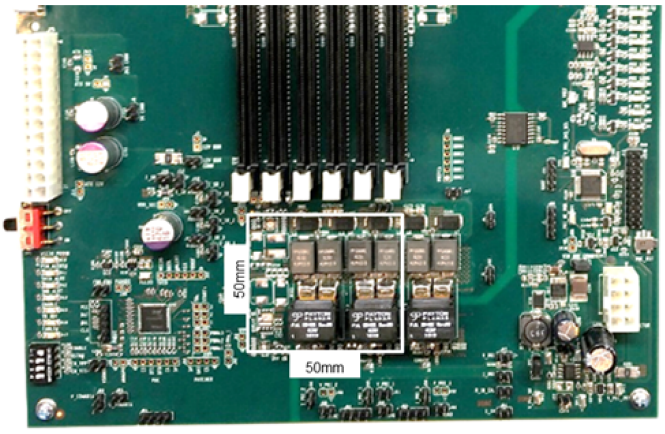


FIGURE 2.27: Test board of the DDR power supply.

The voltage regulation for the DDR power supply does not require a load line implementation. The transient response obtained at nominal input voltage and output voltage of 1.2 V is shown in Fig. 2.28 with load step from 15 A to 65 A. The load step transient response is fast and well damped. From Fig. 2.28 it follows also that the voltage peak of the resonant transition is less in high load condition, as discussed in section 2.3.2.

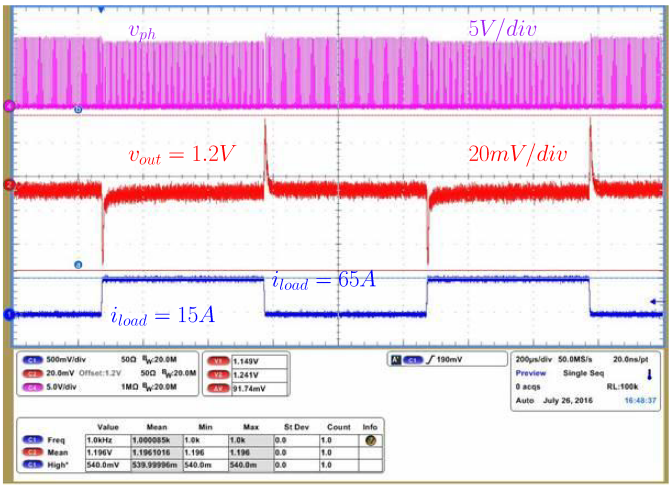


FIGURE 2.28: Load step change from 15A to 65A: V_{ph} (upper trace), V_{out} (middle trace) and I_{load} (lower trace).

FBPS-QR has been proven to perform a VRM function for the VR13.0 specification and provides a microprocessor core voltage rail directly from the 48 V bus. By using ZVS and ZCS both at primary side and secondary side, this converter is able to achieve high efficiency with high performance. This is also obtained by using a multiphase approach that implements a novel current sharing technique. The proposed solution was tested both for VRM and DDR applications, showing good dynamic performance and high efficiency, reaching 93.1% and 93.2% efficiency for VRM and DDR power supply, respectively, including control and driving losses and using SiMOSFETs. The proposed dc-dc resonant converter fully meets the goals of providing a direct conversion from 48 V to main computing low voltage rails with high current consumption.

2.5 Full-Bridge phase-shift center-tapped quasi resonant converter

As previously highlighted in Chapter 1 the high-voltage dc distribution power architecture has been drawing attention due to its lower copper losses. In Fig. 1.5(a) is reported a VRM two stage approach where a *Intermediate Bus Converter* (IBC) are needed from 380 V to 12 V bus dc. The power conversion IBC has to be very efficient with a good power density to be compatible with the motherboard placement.

For data-centers most of the power goes to CPUs and memory and the power level can reach over 600 W per power module. Unregulated LLC converter for IBC helps to improve the efficiency and simplify the control of the IBC stage. LLC has been widely demonstrated as a good power supplies for telecommunication an data centers applications because of the high efficiency, high capability with high frequency operation [72]. However 380 V

dc bus presents a wide range, in this scenario the 12 V VRM has to be designed with a wide input voltage range affecting the overall efficiency of the two stage approach.

In this section will be presented an IBC based on FBPS-QR which works as a buck type voltage regulator.

In section 2.3 is widely discussed and demonstrated the advantages of the new topology based on a quasi-resonant converter which ensure ZVS transition for the primary and secondary switches, enabling high efficiency with high power density. FBPS-QR is realized with current doubler rectifier which is more suitable for low voltage high current applications due to simpler transformer realization, where both output inductors are operating in parallel handling half the output current each inductor.

In attempt to improve the power density, maintaining high performance, in this section is proposed a Full-Bridge phase-shift center-tapped quasi resonant converter. The proposed converter is depicted in Fig. 2.29 where the only difference with FBPS-QR, reported in Fig. 2.4, is the rectifier replaced with a center-tapped. FBPS-QR with center-tapped presents 3 magnetics components instead of 4. However, although the center-tapper rectifier presents only one output inductor, it operates at doubler the switching frequency of the semiconductors, as depicted in Fig. 2.30. The center pin V_{COM}, reported in Fig. 2.29, is switching with one double of the switching frequency respect standard solution with current doubler [73]. During the resonance V_{COM} shows half of the resonance in v_{ph1} and v_{ph2} that allows to use an inductance with half of value comparing with a current doubler solution but with one double of saturation current.

The new structure is shown in Fig. 2.29, where a single phase is represented. The primary-side full-bridge operates in phase-shift, the secondary-side center-tapped rectifier uses synchronous rectifiers Q_{r1} and Q_{r2}. This configuration increases the output inductor equivalent value during the resonance transition at secondary side, replacing the previous current-doubler rectifier proposed in section 2.3, [58], [67], [73] and thus reducing magnetic component size. The resonant tank is formed by an external inductor L_r, in series with the transformer at primary side, an external capacitance C_r in parallel with both switches at secondary side and the output inductance L_{out}. The topology here presented is typically used to obtain stabilized output voltages [67] and [73].

To simplify the analysis the magnetizing current is neglected and the leakage inductance is included within the external inductance L_r. Considering the condition in which Q_1 and Q_4 are in the on-state and Q_2 and Q_3 are off (or when Q_2 and Q_3 are on and Q_1 and Q_4 are off), the total primary inductance L_r generates a resonance with the capacitor C_r causing a voltage oscillation on the secondary side node V_{ph1}, reflected on V_{COM}. This voltage oscillation can reach zero while the state of the primary switches does not change. The control signals for this converter are the two primary side PWMs for the full bridge and a signal called enable rectifier ESR that enables the turn off of the switches $Q_{r1,2}$ in the synchronous rectifier as for FBPS-QR based on current doubler rectifier.

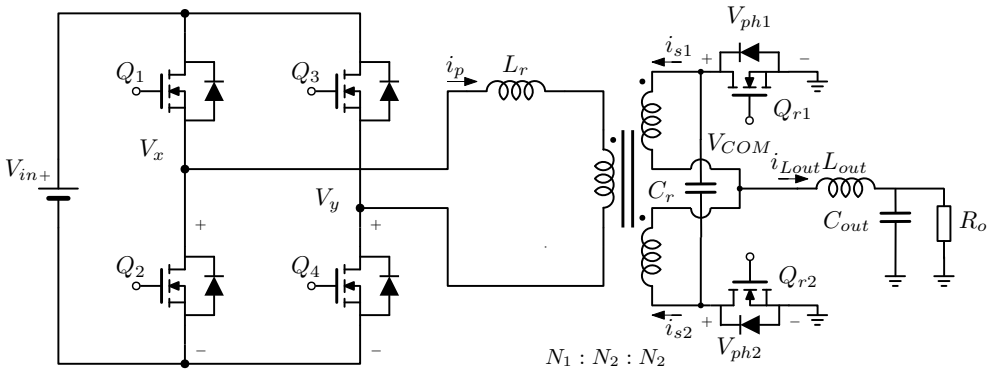


FIGURE 2.29: Full-Bridge phase-shift quasi resonant converter with center tapped rectifier for IBC application.

The proposed dc-dc converter has two different modes of operation: when the voltage on the resonant capacitor C_r reaches zero during the input powering phase (when Q_1 and Q_4 are on or when Q_3 and Q_2 are on) and when the voltage on the resonant capacitor C_r reaches zero during the freewheeling phase (when Q_1 and Q_3 are on or when Q_2 and Q_4 are on). In this work is discussed only the first mode of operation (i.e. when the voltage on the resonant reaches zero during the input powering phase). For further details on the converter behavior in the other mode of operation the interested reader should refer to the $Mode\ B$ of FBPS-QR reported in section 2.3.2.

The six subintervals are described as follows:

1) $\boldsymbol{t_0 - t_1}$: at $t = t_0$, switch Q_4 is turned on in ZVS, current i_p freewheels through switches Q_2 and Q_4; both Q_{r1} and Q_{r2} keep carrying current. The topological state is shown in Fig. 2.33(a).

2) $\boldsymbol{t_1 - t_2}$: at $t = t_1$, switch Q_2 is turned off, and the primary current i_p discharges the capacitance of Q_1 and charges the capacitance of Q_2. When capacitance of Q_1 is discharged to zero, its body diode conducts and ZVS is achieved. Both Q_{r1} and Q_{r2} are still conducting. The current $i_p(t_1)$ that enable ZVS operation of Q_1 is denoted as circulating current $I_{cir_{CT}}$, as shown in Fig. 2.30. This subinterval is reported in Fig. 2.33(b)

2) $\boldsymbol{t_2 - t_3}$: at $t = t_2$, switch Q_1 is turned on with ZVS and both secondary side rectifiers Q_{r1} and Q_{r2} remain conducting, as depicted in Fig. 2.33(c). After $t = t_1$, the primary current i_p increases with a slope that can be approximated as V_{in}/L_r.

3) $\boldsymbol{t_3 - t_4}$: at $t = t_3$, the secondary current i_{s2} reaches i_{Lout}, Q_{r1} is turned off, while Q_{r2}, Q_1 and Q_4 are conducting. In this subinterval the resonance between L_r, C_r and L_{out} takes place. The equivalent resonant circuit is depicted in Fig. 2.31(a) and the equivalent resonant circuit reflective at primary side is shown in 2.31(b). The topological state is represented in Fig. 2.33(d).

4) $\boldsymbol{t_4 - t_5}$: at $t = t_4$, the resonant voltage reaches zero volt ZCD_1 signal becomes high and switch Q_{r1} is turned on, while at the primary side switches Q_1 and Q_4 are still conducting as shown in Fig. 2.33(c).

5) $\boldsymbol{t_5 - t_6}$: at $t = t_5$, switch Q_4 is turned off, i_p charges the capacitance of switch Q_4 and discharges the parasitic capacitance of switch Q_3 in order to achieve ZVS. The topological state is now represented in Fig. 2.33(e). At

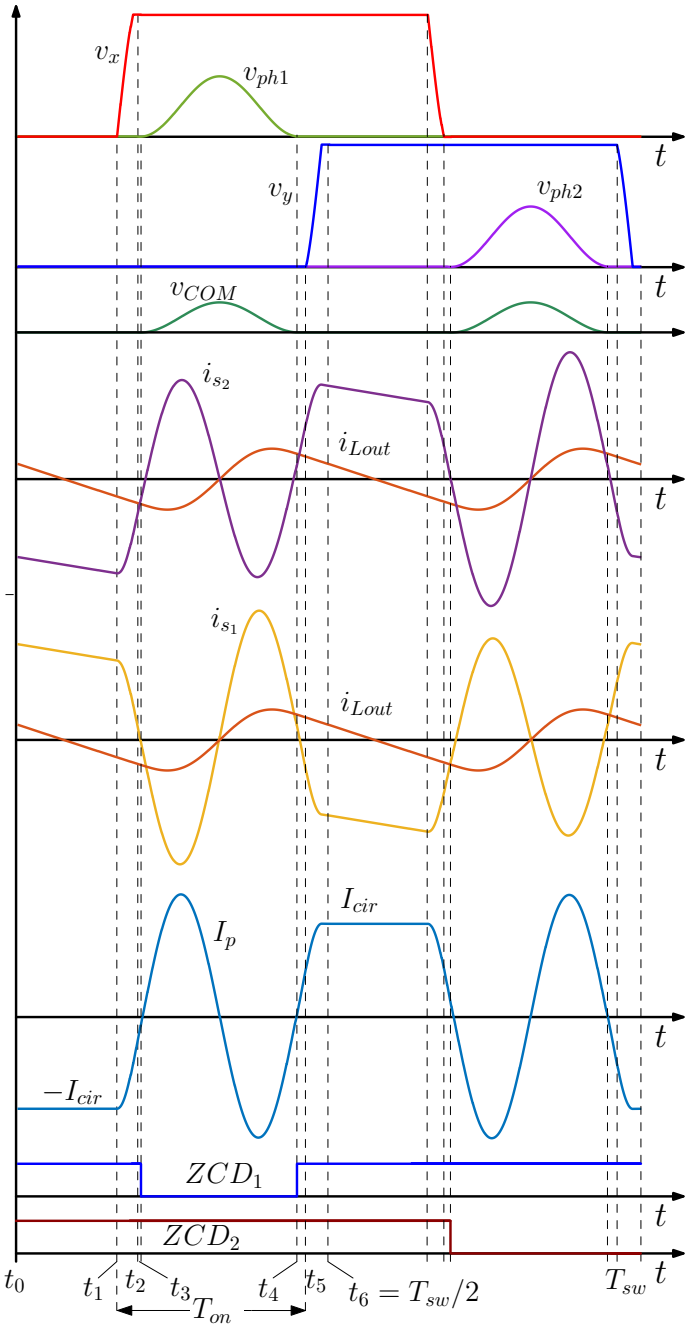


FIGURE 2.30: Main operation waveforms. From top to bottom: primary side voltages (v_x and v_y), voltages ($v_{ph1,2}$), voltages (v_{COM}), secondary side transformer current i_{s2} and inductor currents ($i_{L_{out1}}$ and i_{s1}), and zero current detection (ZCD) signals ($ZCD_{1,2}$)

$t = t_6$, the positive half-cycle of the switching period is completed (i.e. $t_6 = t_0 + \frac{T_{sw}}{2}$), and the topological state of Fig. 2.33(f) is the first one of the negative half-cycle.

During the negative half-cycle of a switching period, the behavior of the circuit is the same as the one described during the positive half-cycle, as shown in Fig. 2.30, in which the output inductance operates at double of the switching frequency.

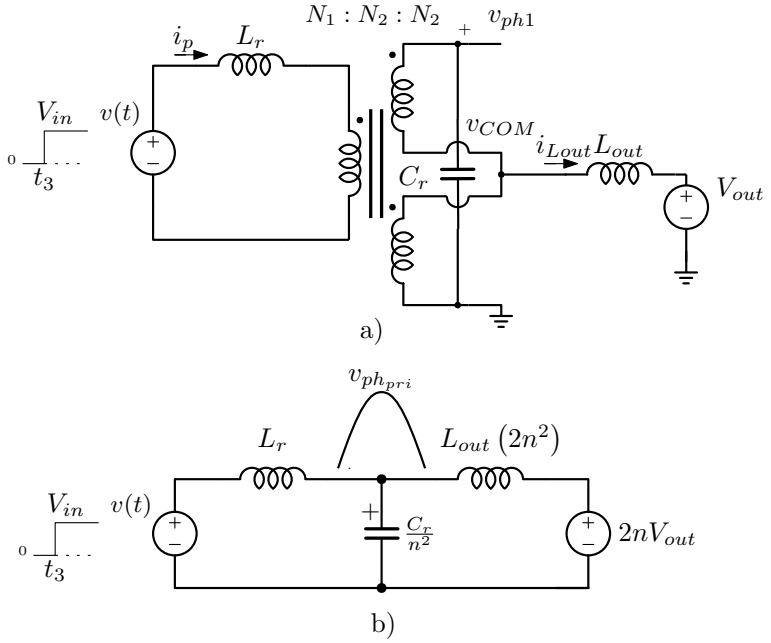


FIGURE 2.31: Equivalent circuit during resonant transition, a) equivalent circuit during the resonant transition, b) equivalent resonant circuit reflected at primary side.

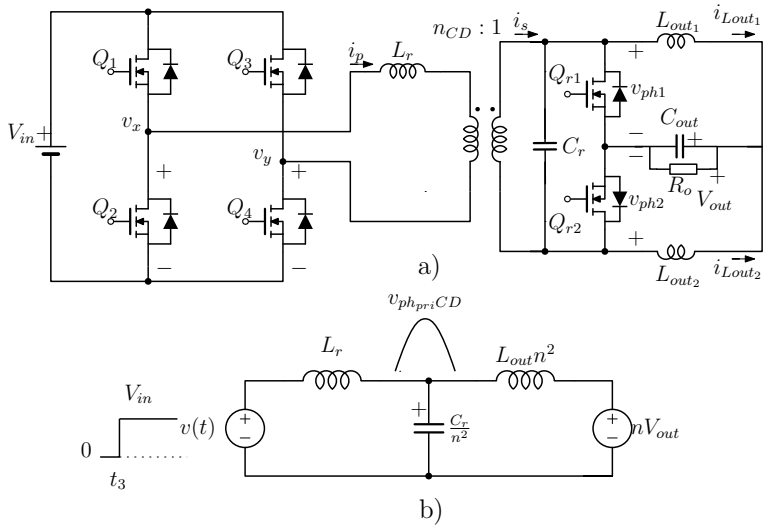


FIGURE 2.32: a) quasi resonant FBPS with current doubler rectifier, b) equivalent resonant circuit reflected at primary side.

The analytical expression of v_{ph} is obtained by solving the equivalent resonant circuit depicted in Fig. 2.31(b). Considering C_r discharges (i.e. $v_{Cr}(t_3) = 0$), v_{ph} is obtained from $v_{ph_{pri}}$:

$$v_{ph}(t) = \frac{2V_{out}L_r + 4n_{CT}V_{in}L_{out}}{L_r + 4n_{CT}^2 L_{out}} \left(1 - cos(\omega_r(t - t_3))\right), \tag{2.59}$$

where the resonant angular frequency $\omega_r = \sqrt{\frac{L_r + 4n^2 L_{out}}{4L_{out}L_r C_r}}$ is the resonance frequency of the network during the phase from $(t_2 - t_3)$ and $n_{CT} = \frac{N_1}{2N_2}$ is the equivalent turns ratio of center tapped transformer.

Hence the mean output voltage in stationary condition is:

$$\begin{aligned} V_{out} &= \frac{1}{T_{sw}} \int_{t_0}^{t_0+T_{sw}} v_{COM}(\tau) d\tau \\ &= \frac{1}{T_{sw}} \int_{t_0}^{t_0+T_{sw}} \left(\frac{v_{ph1}}{2}(\tau) + \frac{v_{ph2}}{2}(\tau) \right) d\tau \\ &= \frac{1}{T_{sw}} \int_{t_0}^{t_0+T_{sw}} v_{ph}(\tau) d\tau d\tau \\ &= \frac{2V_{out}L_r + 4n_{CT}V_{in}L_{out}}{L_r + 4n_{CT}^2 L_{out}} \frac{f_{sw}}{f_r}. \end{aligned} \tag{2.60}$$

From the equation (2.60) it can be seen that the behavior of this converter is similar to a buck converter controlled by a constant on-time regulator. In fact, each single full bridge is equivalent to a couple of phases with a fixed on-time PWM that has the same mean voltage of equation (2.60). This topology can be easily controlled by changing the switching frequency in order to obtain the output current regulation.

As described in previously in section 2.3.1 the circulating current that enables ZVS transition for the primary switches is given by the following equations for FBPS-QR with center-tapped rectifier:

$$\begin{aligned} i_p(t_5) - i_p(t_1) &= \frac{1}{L_r} \int_{t_1}^{t_5} (V_{in} - 2n_{CT} v_{ph}(\tau)) d\tau \\ &= \frac{V_{in}T_{on} - 2n_{CT}V_{out}T_{sw}}{L_r} \\ &\approx 2I_{cir_{CT}}, \end{aligned} \tag{2.61}$$

it follows that:

$$I_{cir_{CT}} \approx \frac{V_{in}T_{on} - 2n_{CT}V_{out}T_{sw}}{2L_r}. \tag{2.62}$$

As reported in section 2.3.1, the circulating current that enables ZVS is independent on the load conditions, that means the unique parameters to consider for ZVS operations are parasitic capacitance C_{oss} for primary MOSFETs, the transformer inter-winding capacitance C_w and the resonant inductor L_r value.

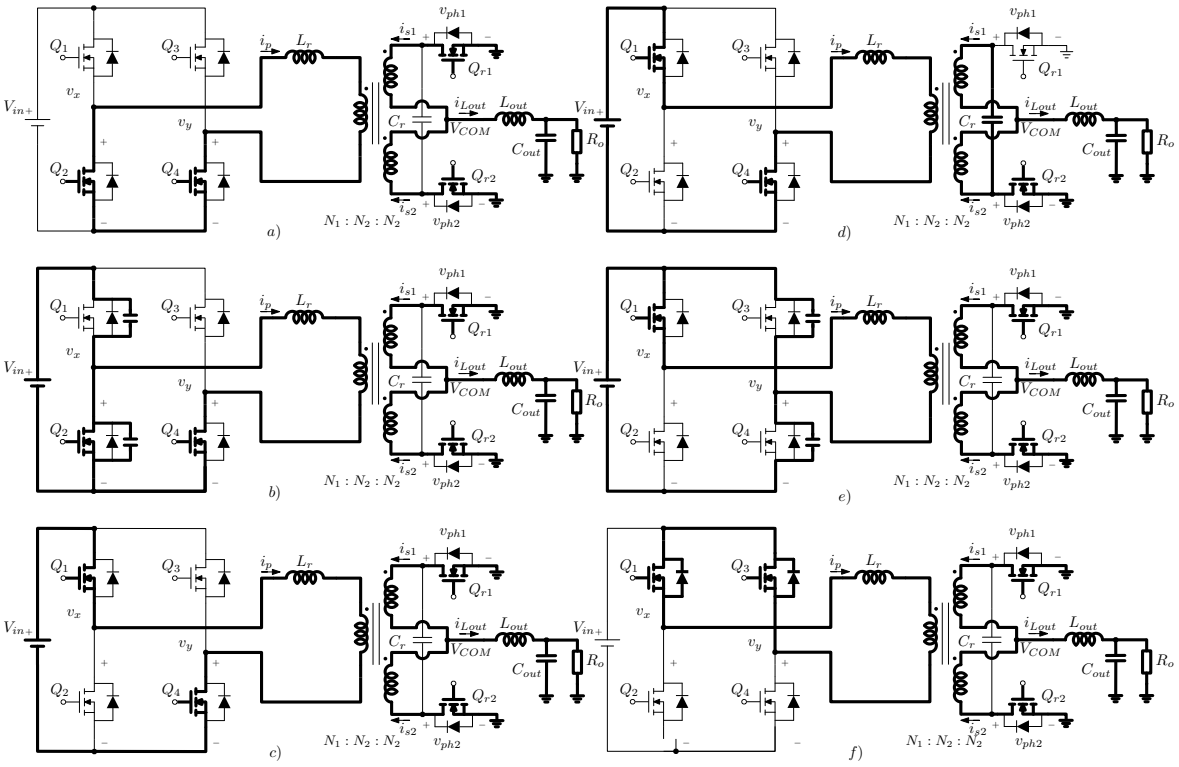


FIGURE 2.33: Switch configuration during each subinterval: a) $t_0 - t_1$, b) $t_1 - t_2$, c) $t_2 - t_3$, d) $t_3 - t_4$, c) $t_4 - t_5$, e) $t_5 - t_6$ f) freewheeling subinterval after t_6 .

2.5.1 Comparison of Current Doubler Rectifier and Center Tapped Rectifier for quasi-resonant FBPS

Considering a quasi-resonant FBPS with current doubler rectifier, as depicted in Fig. 2.32(a), it is possible to quantify the main differences between FBPS-QR based on center-tapped and current doubler rectifier. From Fig. 2.32(b), considering C_r discharges the resonant transition at secondary side in current doubler configuration, v_{phCD}, is obtained from $v_{ph_{pri}CD}$:

$$v_{phCD}(t) = \frac{V_{out}L_r + n_{CD}V_{in}L_{out}}{L_r + n_{CD}^2 L_{out}} \left(1 - cos(\omega_r(t - t_3))\right), \tag{2.63}$$

where the resonant angular frequency $\omega_r = \sqrt{\frac{L_r + n^2 L_{out}}{L_{out}L_r C_r}}$ n_{CD} is the turns ratio of the transformer.

The comparison between the Center-Tapped and the Current-Doubler rectifier is carried out in respect the following conditions: 1) same resonant frequency for equations (2.59) and (2.63) (i.e. by changing C_r so as to obtain the same resonant frequency $f_r = \omega_r/(2\pi)$), 2) primary MOSFETs operate at the same switching frequency in both rectification stage, 3) same equivalent turns ratio for both transformer (i.e. $n_{CD} = n_{CT}$), 4) equal input voltage and same output voltage.

Voltage resonance peak voltage

From equations (2.59) and (2.63) the resonant peak voltage value on the secondary MOSFETs, for both solution, is given by the following expressions:

$$\begin{aligned} V_{peakCT} &= 2\frac{2V_{out}L_r + 4n_{CT}V_{in}L_{out}}{L_r + 4n_{CT}^2 L_{out}} \\ &\approx \frac{2V_{in}}{n_{CT}} \end{aligned} \tag{2.64}$$

$$\begin{aligned} V_{peakCD} &= 2\frac{V_{out}L_r + n_{CD}V_{in}L_{out}}{L_r + n_{CD}^2 L_{out}} \\ &\approx \frac{2V_{in}}{n_{CD}} \end{aligned} \tag{2.65}$$

Assuming $V_{out}L_r << nV_{in}L_{out}$ and $L_r << n^2 L_{out}$.

Indeed, equations (2.64) and (2.65) highlight that the voltage stress for rectifier MOSFETs are almost the same for a quasi-resonant FBPS converter in both rectifier configuration.

Output inductance

The converter depicted in Fig. 2.29 has an output inductor which handles all the output current and operates at double the switching frequency as reported in Fig. 2.30. While, the current doubler, has the inductances operating at the same MOSFET frequency and handles half the output current each inductor, as reported in Fig. 2.5. However, the main difference with FBPS-QR current-doubler is that the output inductor works with a lower voltage so it is possible to use half of the inductance value in center tapped rectifier. It is evident that current ripple, through current-dobuler in quasi-resonant FBPS, is higher, increasing the skin effect and fringing flux effect in the conductors. The unique advantage of the current doubler rectifier in quasi-resonant FBPS converter is that the dc current is half of the output current, which means the saturation current for center tapped topology is doubler respect current-doubler. With center tapped rectifier the system has almost the same performance but the total size of output inductance is half than current doubler rectifier solution [73].

Transformer and high voltage transformer effect

The current doubler transformer for this application is slightly less complex to realize, its presents lower dc resistance and ac resistance due to easier interleaving structure realization and half of turns at primary side, comparing with center-tapped transformer. Another important key to consider is that the transformer inter-winding capacitance, between primary and secondary secondary windings C_w, must be charged and discharged [74]. Transformer with center-tapped rectifier has one double of the inter-winding capacitance, between primary and secondary secondary windings C_w, comparing with

transformer realized for current-doubler rectifier that is mandatory for ZVS operation at primary side.

Primary switches and secondary switches

Comparing the quasi-resonant FBPS current doubler rectifier with quasi-resonant FBPS center-tapped rectifier the voltage stress and current stress for primary switches and secondary switches are very similar as previously described in equations (2.65) and (2.64). As anticipated, this dc-dc establish ZVS operations both at primary side and secondary side. Primary side ZVS is ensured with a well-known operation in full-bridge FBPS converters. The key to zero voltage switching, at primary side, is the amount of energy stored in the primary inductance L_p (i.e. $L_r = L_k + L_{res}$ where L_k is the leakage inductance and L_{res} is an addition inductance in series with the transformer at primary side). The store inductive energy required for ZVS operation is obtained from the following equation:

$$E_L \approx \frac{1}{2} L_p I_{ric}^2. \tag{2.66}$$

To reach the ZVS condition the inductive energy E_L needs to be higher than the capacitive energy E_C, which is given by:

$$E_C \approx \frac{1}{2} \left(2C_{oss_{avg}} + C_w\right) V_{in}^2, \tag{2.67}$$

where C_w is the interwindings capacitance, and $C_{oss_{avg}}$ is given by:

$$C_{oss_{avg}} = \frac{1}{V_{ds_{max}}} \int_0^{V_{ds_{max}}} C_{oss}(V_{ds}) dV_{ds}, \tag{2.68}$$

where $V_{ds_{max}}$ is the input voltage.

As previously reported the proposed FBPS-QR with center tapped rectifier is recommended for IBC applications and as widely discussed the main benefit comes from the power density. In fact, at medium current the center tapped topology is more appropriate due to lower losses and less space occupation [58]. The unique problem regarding center tapped topology is the transformer realization. The current doubler transformer is simpler since it only has one secondary winding or two, depending on the core size and the output voltage. Instead, center tapped transformer presents double of turns ratio. The only way to reduce the overall ac resistance is to adopt a fully-interleaved winding arrangement incrementing the stray capacitance C_w increasing the energy required as reported in equation (2.67). What can be done is to increase the circulating current I_{ric} by modulating the on-time T_{on} in equation (2.62), increasing the overall copper losses.

2.6 Experimental Results FBPS-CT quasi-resonant as IBC from 380 V

In order to prove the effectiveness of the proposed FBPS-QR with center-tapped rectifier, in this section experimental results are presented, highlighting the advantages for a IBC application and the possible disadvantages for a VRM application. Moreover, it is interesting to analyse the ZVS operation at primary side for the FBPS-QR with a 380 V input voltage using SiMOS.

A prototype has been built to validate the proposed architecture. As shown in Fig. 2.34, a test board with $I_{out} = 50\ A$ and $V_{out} = 12\ V$ has been realized. The total space occupation of the test board is $100\ mm\ X\ 130\ mm$. The primary side full-bridge MOS are STL33N60DM2, the secondary side ones are STL100N12F7. The primary inductance L_r is $48\ \mu H$, L_{out} is $1.8\ \mu H$, C_r is 127 nF and the transformer is made by planar core 8.5:1 of equivalent turns-ratio. The secondary turns ratio is 2 to reach high power density containing the cross section area of the core. The phase switching frequency range is 165 kHz - 185 kHz.

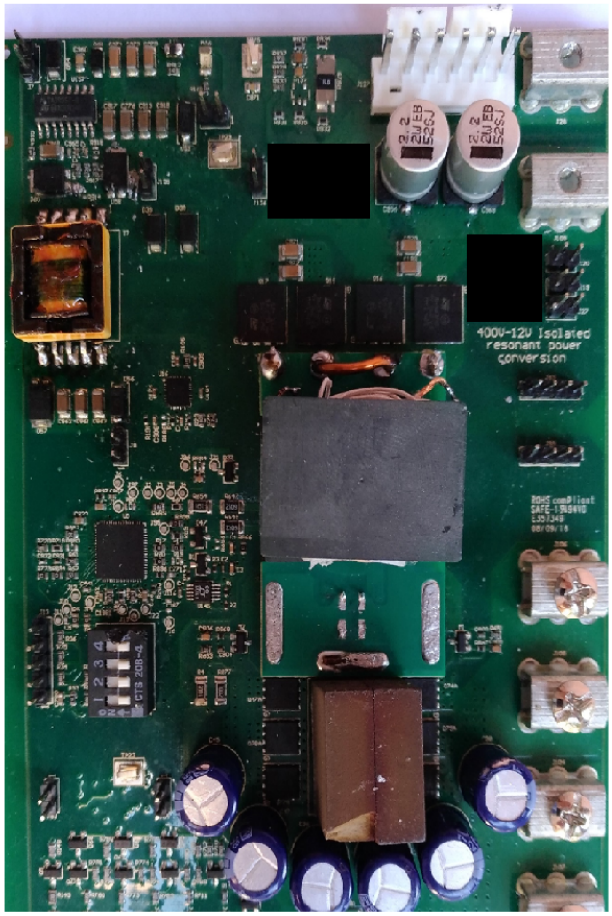


FIGURE 2.34: Test board 380 V to 12 V 50 A

In Fig. 2.35(a) and 2.35(b) are shown respectively the ZVS transition at primary side and secondary side in light load, whilst in 2.35(c) and 2.35(d)

are reported the same waveforms in high load condition. As previously highlighted FBPS-QR based on center-tapped presents the same ZVS functionality of FBPS-QR based on current-doubler proposed in section 2.3. As can be seen from Fig. 2.35(a) and Fig. 2.35(b) the circulating current from light load to high load is slightly the same, however the value of such current is very high to ensure ZVS transition. In fact, the recirculating current is around 2 A. The required energy for ZVS transition is very high due to the high charge stored in parasitic capacitances of the MOSFETs. Moreover, as reported in eq. 2.67, the parasitic stray capacitance of the transformer C_w increases the energy required for ZVS operation at primary side. In Fig. 2.36 are accounted the parasitic C_{oss} capacitance of the MOSFETs tested for the primary side (STL33N60DM2 and ST36N55M5).

In Fig. 2.37 are displayed the efficiency measurement comparison using STL33N60DM2 ($R_{ds_{on}} = 140\ m\Omega$ and $C_{oss_{avg}} = 218\ pF$) and ST36N55M5 ($R_{ds_{on}} = 90\ m\Omega$ and $C_{oss_{avg}} = 218\ pF$) as primary side MOSFETs. From Fig. 2.37 it follows that the prototype built with STL33N60DM2 gives higher efficiency in all entire load regardless higher on-resistance.

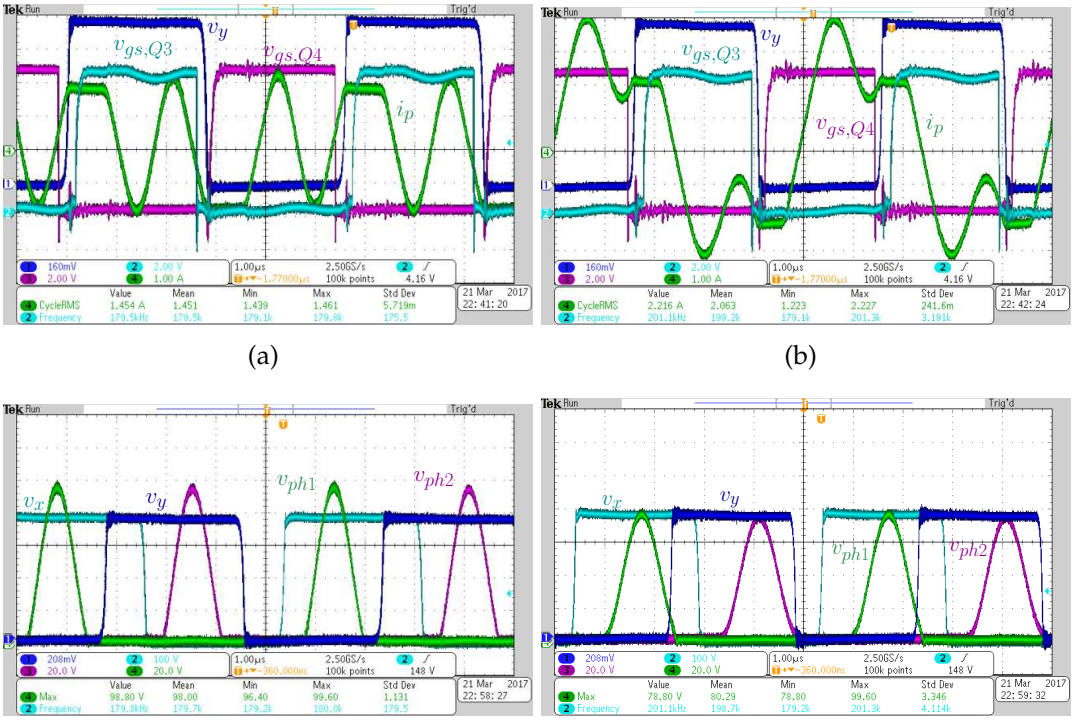


FIGURE 2.35: (a) An example of ZVS turn on and turn off for Q_4: voltage at node V_y driving voltage for Q_3 (Vgs_{Q_3}) and Q4 (Vgs_{Q_4}) in light load and (b) in high load. () Resonant transition at secondary side V_{ph1} and V_{ph2}, and the voltage node V_v and V_y at primary side in light load and (d) in high load.

The peak efficiency is 95.5% as reported in Fig. 2.37 and in light load the losses are around 12 W due to high recirculating current. In fact, as reported

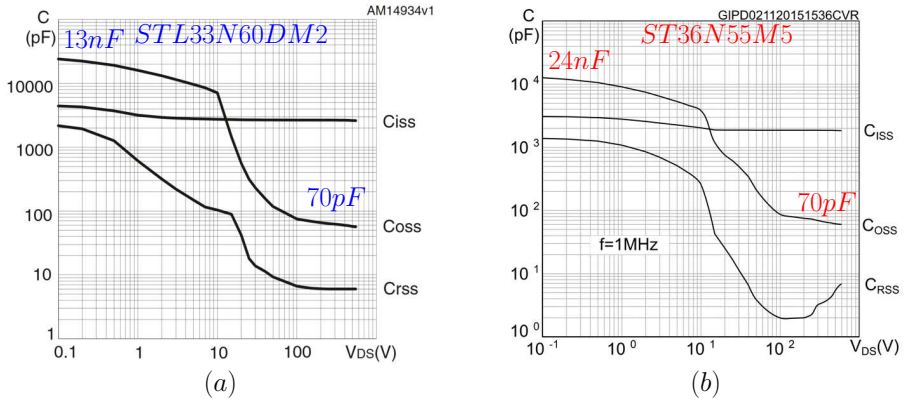


FIGURE 2.36: Capacitance C_{oss} over V_{ds} from datasheet rispectively (a) STL33N60DM2 and (b) ST36N55M5.

in Fig. 2.37 the efficiency presents a dominated bias losses from the light load.

Finally, in Fig. 2.38(a) and 2.38(b) are reported the thermal images respectively at 0 A and 50 A. The dissipation in light load are dominated by the core losses and by the primary side copper losses. In fact, as previously discussed the ZVS functionality are strongly influenced by the primary side MOSFETs and transformer realization. Instead, in high load the losses are dominated by the secondary side MOSFETs because the 150 V rating are adopted due to resonant operation at secondary side. Another issue at high load comes from the transformer, in fact comparing with current doubler transformer the RMS current through the secondary winding is higher since all output current is circulating.

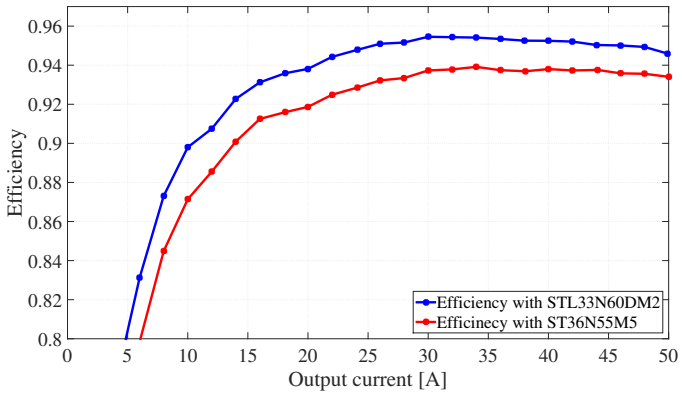
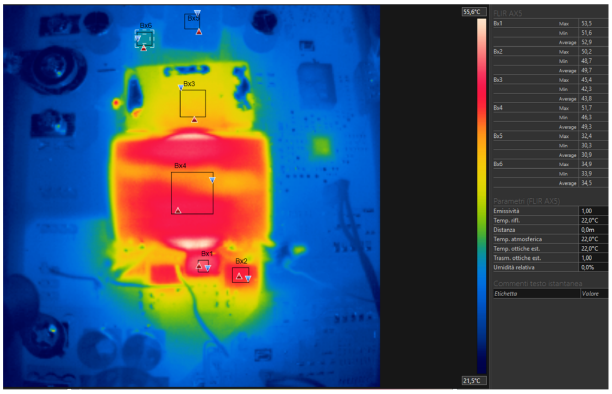


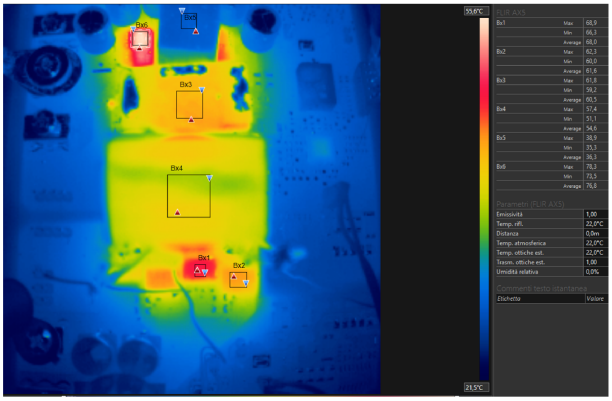
FIGURE 2.37: System efficiency comparison between STL33N60DM2 and ST36N55M5 over the total load range.

The proposed solution would be higher performed if Gallium Nitride (GaN) at primary side is adopted. GaN is an enabling technology with high figure of merit compared with traditional silicon devices. In fact, in the proposed application the main limitations comes from the high energy for ZVS which increases the copper losses at primary side. By adopting GaN devices such as PGA26E19BA the energy for ZVS decreases exponentially. From PGA26E19BA datasheet it is possible to derive the average parasitic output

capacitance of the device C_{avg} which is around 30 pF. This is a paramount importance to consider since the main limitation for this application comes from the dissipation at primary side.



(a)



(b)

FIGURE 2.38: Thermal images at different load conidition for 1 phase prototype for the converter proposed in 2.34: (a) $I_{out} = 0A$, (b) $I_{out} = 50A$.

2.7 Full-Bridge phase-shift quasi-resonant as HV POL

As previously mentioned FBPS-QR (proposed in section 2.3) is a buck-derived topology which we proposed as a 48 V VRM high step down converter down to the main low voltage high current rails [67]. Considering now the main functionalities introduced in section 2.3.1 it is possible to rethink the converter from 380 V input voltage. In general there are several constraints for VRM specification but actually the most important is the output inductance which affect the transient response and the efficiency (the maximum value should be around 170 nH). Moreover the transformer realization comes as an important limitation. In 48 V VRM the turns ratio requirement oscillates from 5 to 9 depending on the maximum output voltage and the transient requirement, thus the turns ratio for 380 V VRM bases on FBPS-QR has to

be at least 40. However, 40 as turns ratio will complicate the design of the transformer.

TABLE 2.2: Converter parameters FBPS-QR for 380 V VRM.

Input voltage	$V_{in} = 380\ V$
Output inductances	$L_{out} = 110\ nH$
External inductance	$L_r = 120\ \mu H$
Resonance capacitance	$C_r = 132\ nF$
Transformer turns-ratio	$n = 40$
Output capacitance	$C_{out} = 470\ \mu F$

In FBPS-QR the key for high efficiency and high frequency operation are the selection of an optimum MOSFET for primary side full-bridge. To select carefully the best solution there are some considerations to be taken into account: low FOM $R_{on}C_{oss}$ for improving ZVS functionality and low dissipation at primary side, fast turn-off switching (which means low gate resistance and low Q_g), V_{ds} rating to handle overshoots and robust body diode with fast reverse recovery.

Thus, it is important to study the ZVS capability of primary MOSFETs, by studying the non-linear behaviour of parasitic capacitance C_{oss}, in order to find out the energy required for ZVS transition. From eq. (2.68) it is possible to derive the actual value of $C_{oss_{avg}}$ (i.e. for STL33N60DM2 is 218 pF). Moreover, considering the stray capacitance of the transformer (i.e. 800 pF for fully interleaved transformer using E22 core or 100 pF in a semi-interleaved arrangement) the actual energy for ZVS is increased as it is possible to get from eq. (2.67).

Considering equations (2.68), (2.67) and the converter parameters of table 2.2, the actual circulating current required for ZVS transition is given by the following equation:

$$I_{cir_{ER}} \geq \sqrt{\frac{\left(2 \cdot C_{oss_{avg}} + C_w\right) V_{in}^2}{L_r}}. \tag{2.69}$$

From eq. (2.69) and the parameters of table 2.2 it follows that the required circulating current for STL33N60DM2 FET in ZVS, considering fully-interleaved transformer arrangement, is 1.35 A whilst for a semi-interleaved arrangement is 0.87 A. In this scenario the on-time for semi-interleaved structure should be around 950 ns while for fully-interleaved will be 1250 ns.

As graphically demonstrated in Fig. 2.39 the converter is not able to reach the nominal output voltage due to the switching frequency limitation caused by the high on-time required for ZVS capability. Here is demonstrated how FBPS-QR is a good step-down converter, but actually the technology limitations for primary MOSFETs restricts its functionalities. In order to fully meet the requirements for a converter working as HV POL, ensuring high

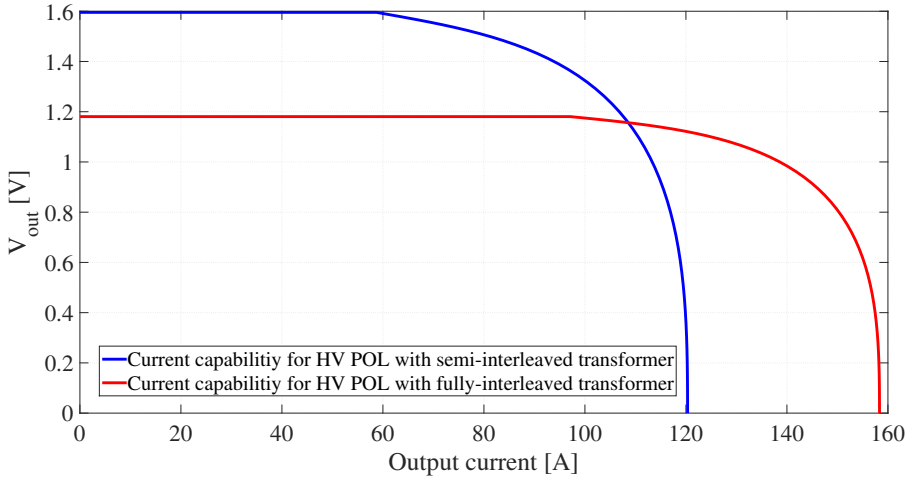


FIGURE 2.39: Current capability comparison for FBPS-QR as HV POL using converter parameters of table 2.2 with a semi-interleaved and fully-intrleaved transformer.

dynamic performance, some primary side multilevel topologies will be proposed in this dissertation. The main concept is to find out a FBPS-QR derived topologies, exploiting the main advantages of FBPS-QR overcoming its drawback.

2.8 Multilevel structures based on FBPS-QR

Multilevel converters were principally developed as a result of a growing need for higher power converters [75] [76]. In order to achieve higher power capability, the voltage and current capabilities of the MOSFETs used in the converter need to be increased. Topology converters whose make use of a series connection of switches, can allow for the use of MOSFETs with reduced voltage ratings and higher current capability. Lower voltage MOSFETs have lower switching losses and can switch at a higher frequency [77]. In a multilevel converter the medium voltage can be clamped using diode-clamped or flying capacitor topologies.

The diode-clamped converters [78] is also knows as the neutral point clamped converter. The half-bridge leg with a clamped diode consists of two pairs of series switches in parallel with two series capacitors where the anode of the upper diode is connected to the neutral point. One of the main benefit is that the capacitors can be pre-charged without external auxiliary circuit, however it can not reach high efficiency. As an alternative to the diode clamped multilevel is to replace the diode with a flying capacitor.

The flying capacitor multilevel converters is an attractive choice to reduce the voltage stress increasing the overall efficiency of the converter. The voltage of the flying capacitor is typically naturally balanced, this is achieved by applying a phase shifted control [79] [80]. But actually, these converters have an important drawback coming from the start-up procedure, which makes

this topology not so attractive for VRM applications. It is this section's goal to show how multilevel topology can be suitable as HV POL.

2.8.1 Multilevel double Half-Bridge Phase-Shift Quasi-Resonant

In section 2.3 is widely discussed how FBPS-QR can be used as high step down converter ensuring all VRM functionalities, but the poor switching performance at higher voltage makes FBPS-QR not so efficient as HV POL. In this section a new multilevel topology based on double half bridge multilevel quasi-resonant (2HBPS-QR) is presented in Fig. 2.40. The main difference from 2.4 is the double multilevel half bridge at primary side which ensure higher ZVS capability and higher current capability.

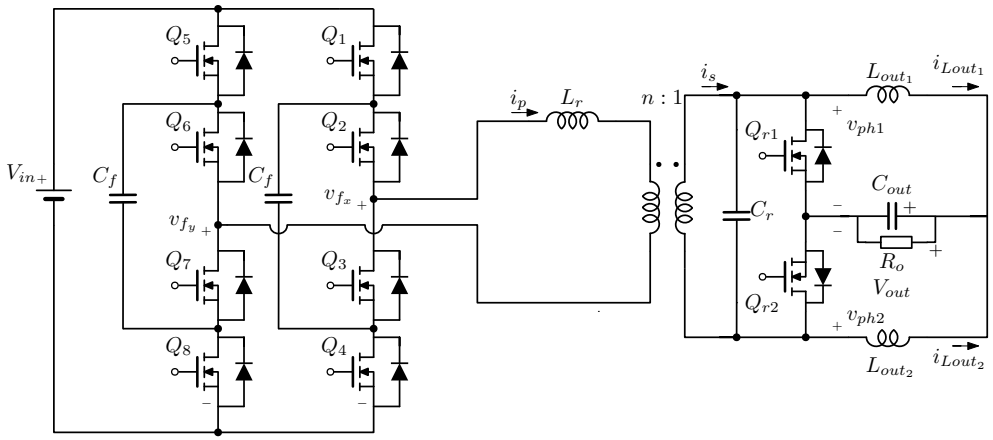


FIGURE 2.40: Multilevel double half-bridge phase-shift quasi-resonant double current converter scheme.

As was done for FBPS-QR, to simplify the analysis the magnetizing current is neglected and the leakage inductance is included within the external inductance L_r. Considering the condition in which Q_1 and Q_4 are in the on-state and Q_2 and Q_3 are off (or when Q_2 and Q_3 are on and Q_1 and Q_4 are off), the total primary inductance L_r generates a resonance with the capacitor C_r causing a voltage oscillation on the secondary side node V_{ph1} or V_{ph2}. This voltage oscillation can reach zero while the state of the primary switches does not change.

The proposed dc-dc converter has two different modes of operation: when the voltage on the resonant capacitor C_r reaches zero during the input powering phase (when Q_1, Q_2, Q_5 and Q_7 are on or when Q_5, Q_6, Q_1 and Q_3 are on) and when the voltage on the resonant capacitor C_r reaches zero during the freewheeling phase (when Q_1, Q_3, Q_5 and Q_7 are on). For this converter is discussed only the first mode of operation (i.e. when the voltage on the resonant reaches zero during the input powering phase).

The eight subintervals are described as follows:

1) $\boldsymbol{t_0 - t_1}$: at $t = t_0$, switch Q_4 is turned on, the primary current i_p freewheels through switches Q_2 and Q_4, and both Q_{r1} and Q_{r2} are on. The topological state is shown in Fig. 2.41(a).

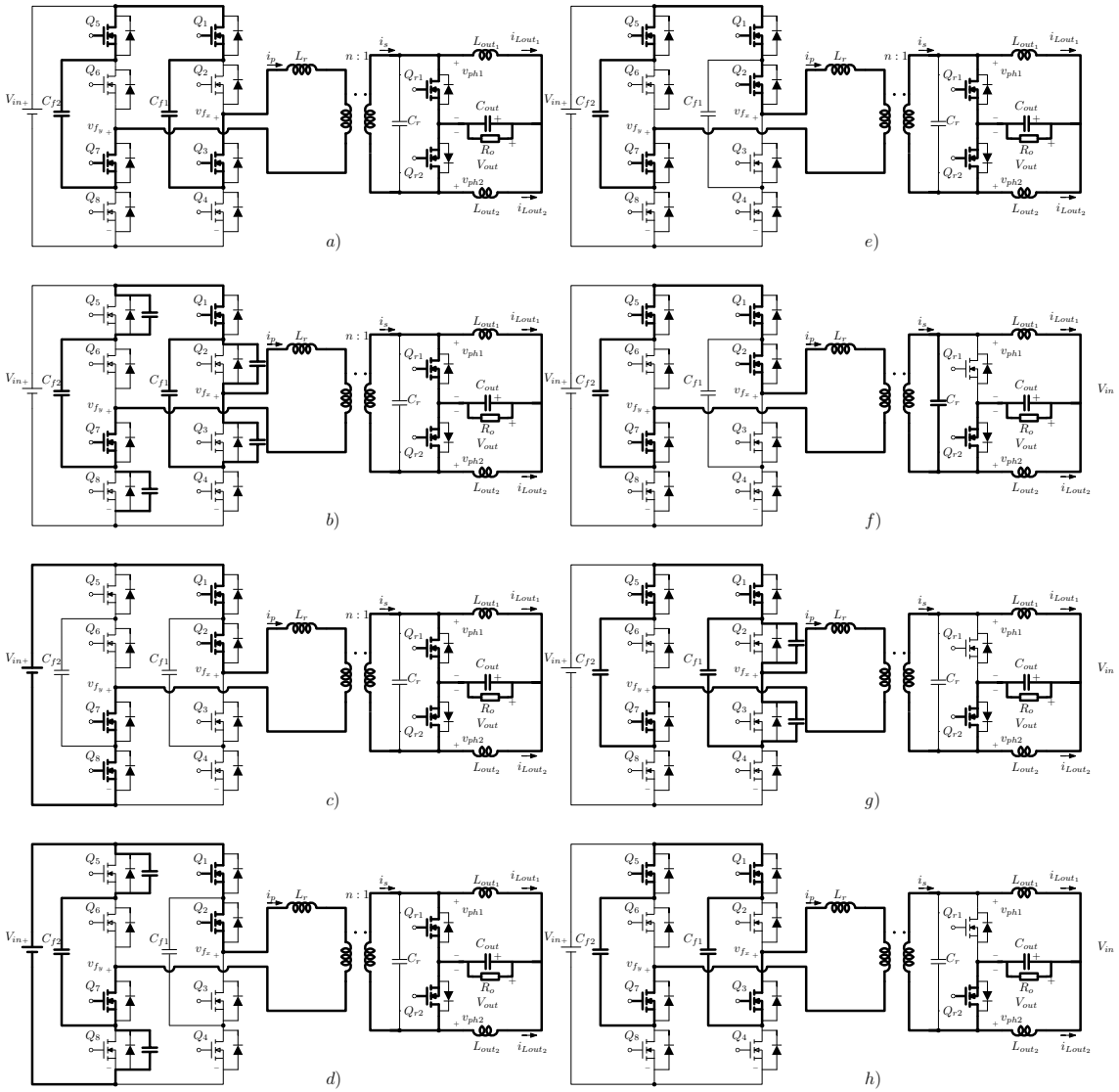


FIGURE 2.41: Switch configuration during each subinterval in *Mode A* for 2HBPS-QR: a) $t_0 - t_1$, b) $t_1 - t_2$, c) $t_2 - t_3$, d) $t_3 - t_4$, e) $t_4 - t_5$, f) $t_5 - t_6$ e) $t_6 - t_7$ g) $t_7 - t_8$ h) $t_8 - t_9$.

2) $\boldsymbol{t_1 - t_2}$: at $t = t_1$, switches Q_3 and Q_5 are turned off, and the primary current i_p discharges the capacitance of Q_3 and Q_5 and charges the capacitance of Q_2 and Q_8. When capacitance of Q_3 and Q_5 are discharged to zero, their body diode conducts to enable ZVS turn-on of Q_2 and Q_8. Both Q_{r1} and Q_{r2} are on and the topological state corresponding to this subinterval is reported in Fig. 2.41(b). The current $i_p(t_1)$ that enables ZVS operation of Q_2 and Q_8 is denoted as circulating current $I_{cir_{2HB}}$ (i.e. $I_{cir_{2HB}} = -i_p(t_1) = -i_s(t_1)/n$), as shown in Fig. 2.42, and it is almost constant within the interval $(t_0 - t_1)$. I_{cir} for double half-bridge quasi-resonant converter is given by the following equation:

$$I_{cir_{2HB}} \approx \frac{\frac{V_{in}(T_{on}+T_{on_{HV}})}{2} - nV_{out}T_{sw}}{2L_r}. \tag{2.70}$$

3) $\boldsymbol{t_2 - t_3}$: at $t = t_2$, switches Q_2 and Q_8 are turned on with ZVS and both secondary side rectifiers Q_{r1} and Q_{r2} remain conducting, as shown in Fig. 2.41(c). After $t = t_1$, the primary current i_p increases with a slope that can be approximated as V_{in}/L_r.

4) $\boldsymbol{t_3 - t_4}$: at $t = t_3$, switch Q_8 is turned off, and the primary current i_p discharges the capacitance of Q_5 and charges the capacitance of Q_8. When capacitance of Q_5 is discharged to zero, its body diode conducts to enable ZVS turn-on of Q_5. Both Q_{r1} and Q_{r2} are on and the topological state corresponding to this subinterval is reported in Fig. 2.41(d). The current $i_p(t_3)$ that enables ZVS operation of Q_8 is not the circulating current $I_{cir_{2HB}}$ but depends from the high voltage mode duration $T_{on_{HV}}$, its value is denoted as $I_{HV_{ZVS}}$ (i.e. $I_{HV_{ZVS}} = -i_p(t_3) = -i_s(t_3)/n$), as shown in Fig. 2.42. Again, the value of $I_{HV_{ZVS}}$ does not depend from the load condition and is given by the following equation:

$$\begin{aligned} I_{HV_{ZVS}} &\approx -I_{cir_{2HB}} + \frac{V_{in}T_{on_{HV}}}{L_r} \\ &= \frac{-\frac{V_{in}T_{on}}{2} + \frac{3V_{in}T_{on_{HV}}}{2} + nV_{out}T_{sw}}{2L_r}. \end{aligned} \tag{2.71}$$

5) $\boldsymbol{t_4 - t_5}$: at $t = t_4$, switch Q_5 is turned on with ZVS and both secondary side rectifiers Q_{r1} and Q_{r2} remain conducting, as shown in Fig. 2.41(e). After $t = t_4$, the primary current i_p increases with a slope that can be approximated as $V_{in}/2L_r$.

6) $\boldsymbol{t_5 - t_6}$: at $t = t_5$, the secondary current i_s reaches i_{Lout1} (i.e. $i_s(t_5) = i_{Lout1}(t_5)$), Q_{r1} is turned off, and Q_{r2}, Q_1, Q_2, Q_5 and Q_7 are conducting. The topological state is shown in Fig. 2.41(f). In this subinterval, the resonance between L_r, C_r and L_{out_1} takes place and the equivalent resonant circuit is shown in Fig. 2.7 case a) as in FBPS-QR (in this case the reflected voltage at secondary side is half comparing with FBPS-QR).

7) $\boldsymbol{t_6 - t_7}$: at $t = t_6$, the resonant voltage reaches zero volt, and Q_{r1} is turned on, while at the primary side switches Q_1, Q_2, Q_5 and Q_7 are still conducting. The topological state is reported in Fig. 2.41(e).

8) $\boldsymbol{t_7 - t_8}$: at $t = t_7$, switch Q_2 is turned off, i_p charges the capacitance of switch Q_2 and discharges the parasitic capacitance of switch Q_3 in order

to achieve ZVS. The topological state is now represented in Fig. 2.41(g). The current that enables ZVS of Q_3 is $i_p(t_7)$ and it is only slightly smaller than $I_{cir_{2HB}}$. Thus, $I_{cir_{2HB}}$ and $I_{HV_{ZVS}}$ are a good index to establish when turn-on ZVS is achieved for all switches. At $t = t_8$, Q_3 is turned on at ZVS and i_p freewheels through switches Q_1, Q_3, C_{f_1}, Q_7, Q_7 and C_{f_2} as shown in Fig. 2.41(h). At $t = t_8$, the positive half-cycle of the switching period is completed (i.e. $t_8 = t_0 + \frac{T_{sw}}{2}$).

During the negative half-cycle of a switching period, the behavior of the circuit is the same as the one described during the positive half-cycle, as shown in Fig. 2.42, in which the output inductance operates at double of the switching frequency.

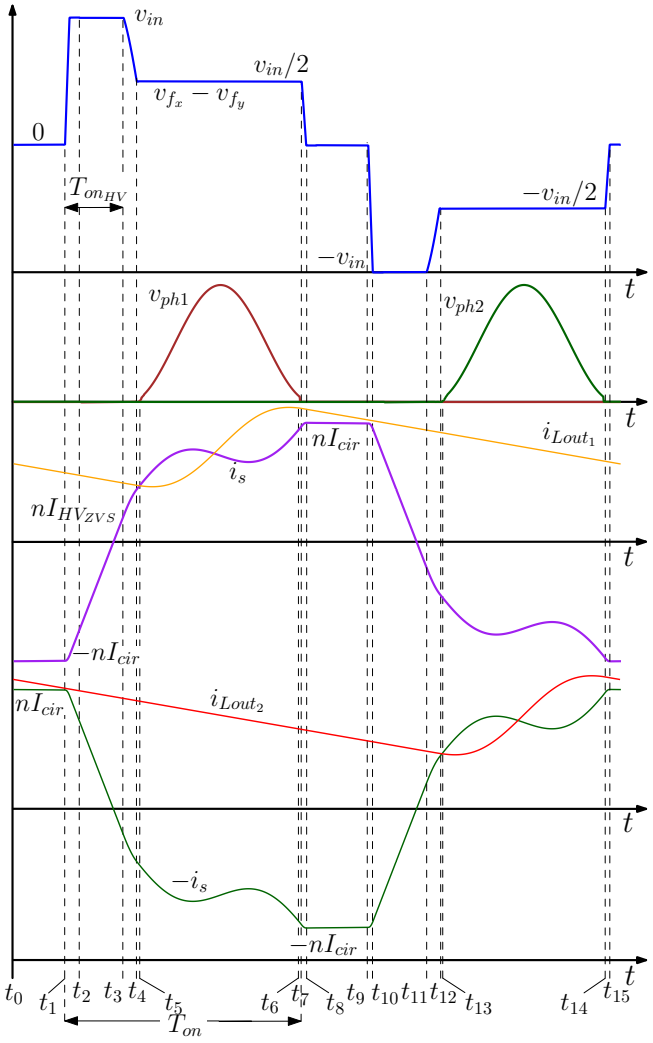


FIGURE 2.42: Main converter waveforms for Operation Mode A of multilevel double half-bridge phase sfhift current doubler. From top to bottom: primary side voltage ($v_{f_x} - v_{f_y}$), voltages ($v_{ph1,2}$), secondary side transformer current i_s and inductor currents ($i_{L_{out1}}$ and $i_{L_{out2}}$).

Comparison between FBPS-QR and multilevel double half-bridge quasi-resonant

The proposed 2HBPS-QR works in COT as FBPS-QR (section 2.3), but in the new multilevel topology the constant on time presents two different phases. The first phase is called $high\ voltage\ phase$ and its duration is $T_{on_{HV}}$, in this phase the primary side inductance is charged with all the input voltage. The second phase is called $powering\ phase$ and its duration is $T_{on} - T_{on_{HV}}$, in this phase takes place the resonant transition. However, since the pre-charging time of the primary inductance depends on the load condition, is not always true that the beginning of the second phase corresponds with $powering\ phase$, but actually, depends on the load condition. In fact, is still needed a pre-charging of the resonant inductance with half of the input voltage. The benefit of a constant $T_{on_{HV}}$ is that the $Mode\ A$ operation is extended comparing with the classic FBPS-QR, when in 2HBPS-QR is used half of the transformer turns ratio.

In order to make a fair comparison between FBPS-QR and 2HBPS-QR, in Table 2.3 are reported converters parameters for both topologies, where the equivalent resonant tank are kept as the same. In Fig. 2.43 are reported the two current capabilities of FBPS-QR and 2HBPS-QR, considering negligible the parasitic C_{oss} capacitance. The main difference between those converters is that the second presents and extended $Mode\ A$ operation region. This is a paramount importance to consider, since , as reported in section 2.3.2 in $Mode\ A$ the frequency does not change, whilst in $Mode\ B$ changes to control the output voltage.

TABLE 2.3: Converters parameters of FBPS-QR and 2HBPS-QR used for the capability comparison in Fig. 2.43

	FBPS-QR	2HBPS-QR
Output inductances	$L_{out} = 170\ nH$	$L_{out} = 170\ nH$
External inductance	$L_r = 120\ \mu H$	$L_r = 30\ \mu H$
Resonance capacitance	$C_r = 132\ nF$	$C_r = 132\ nF$
Transformer turns-ratio	$n = 40$	$n = 20$
Constant on-time	$T_{on} = 800\ ns$	$T_{on} = 800\ ns\ T_{on_{HV}} = 200\ ns$

Multilevel topology gives higher capability, as demonstrated, but actually it presents an high numbers of switches which are eight in the proposed 2HBPS-QR that means 4 MOSFETs on during each phases.

As described in section 2.3.1, the ZVS operation of leading-leg switches of FBPS-QR is achieved over whole load conditions using the stored energy in the resonant inductance during the freewheeling phase. As demonstrated the freewheeling current ensures the ZVS transition and as indicated in eq. (2.62) does not depend from the load condition. In 2HBPS-QR the operation principle of the ZVS functionality is slightly the same but presents two different ZVS phases. In 2HBPS-QR the lagging-leg switches can achieve ZVS

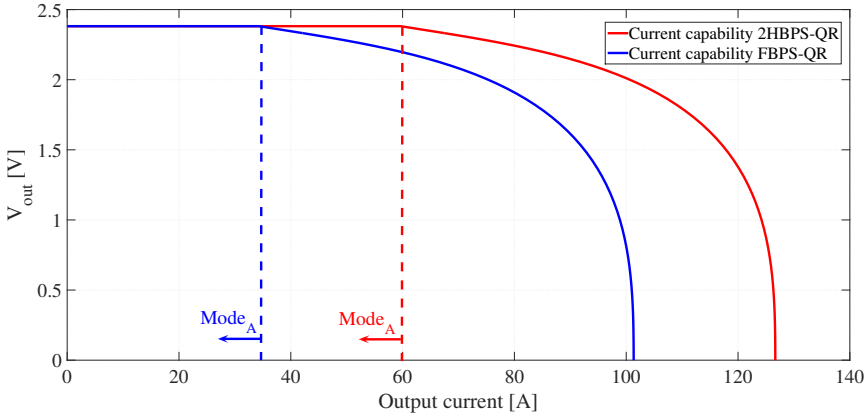


FIGURE 2.43: Current capability comparison between FBPS-QR and 2HBPS-QR without considering parassitic MOSFET capacitance effect on ZVS capability.

from light-load to heavy-load with the same energy capability as in FBPS-QR, but actually, by looking at Fig. 2.44, it is possible to get the main differences between FBPS-QR and 2HBPS-QR ZVS transitions. Considering the ZVS transition of FBPS-QR at $t = t_1$, as reported in Fig. 2.44(a), and comparing with the ZVS of 2HBPS-QR at $t = t_1$ (depicted in 2.44(c)) it is possible to get how the equivalent resonant circuit during the ZVS transition in 2HBPS-QR presents two more MOSFET's parasitic capacitance as depicted in Fig. 2.44(b)) and Fig. 2.44(d)).

However, the main difference is that at $t = t_3$ in 2HBPS-QR the circuit configuration is as depicted in Fig. 2.44(e), whilst the equivalent resonant circuit during the ZVS transition is reported in Fig. 2.44(f). $I_{HV_{ZVS}}$ current ensures ZVS transition without varying with the load condition as demonstrated in eq. (2.71). Hence, to ensure ZVS even in the transition between $high\ voltag\ phase$ to half of the input voltage it is important to derive a efficacious relation between the on-time T_{on} and the high voltage on time $T_{on_{HV}}$.

Thus, considering the stray capacitance of the transformer C_w negligible comparing with the MOSFETs parasitic capacitance C_{oss} and by studying the circuits in Fig. 2.44(d) and Fig. 2.44(f), hence the energy needed for the ZVS transition is half at $t = t_3$ comparing with the energy necessary at $t = t_1$. Thus, the relation between the high voltage on time $T_{on_{HV}}$ and the on-time T_{on} are given by:

$$T_{on_{HV}} \geq T_{on} - 2n\frac{V_{out}}{V_{in}}. \tag{2.72}$$

Eq. 2.72 is obtained from $I_{HV_{ZVS}} = \frac{1}{\sqrt{2}} I_{cir_{2HB}}$ accomplished from the constrains for the same ZVS operations in both phases.

The proposed 2HBPS-QR can overcome the limitation of FBPS-QR and can work as HV POL, but the implementation of 2HBPS-QR is slightly complicated for two main reasons. The first comes from the control system. $T_{on_{HV}}$ has to be dependent with the load, and has to satisfy the relation in eq. (2.72) in all operating load conditions. The second is the operation in light load. In light load the pre-charging time can be less than the duration of $T_{on_{HV}}$, thus,

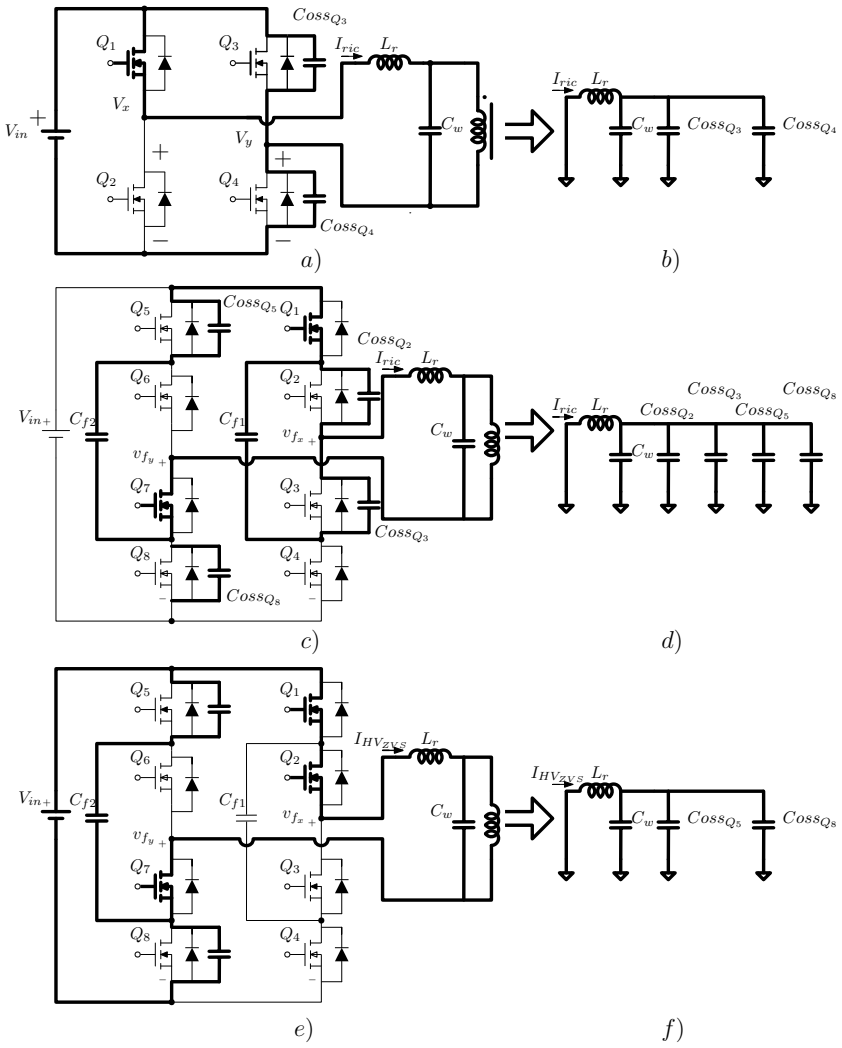


FIGURE 2.44: (a) Equivalent circuit in ZVS full-bridge at t_1, (b) Equivalent resonant circuit in ZVS transition mode for full-bridge topology, (c) Equivalent circuit in ZVS double half-bridge multilevel at t_1, (d) Equivalent resonant circuit in ZVS transition mode for double half-bridge multilevel at t_1 (e) Equivalent circuit in ZVS double half-bridge multilevel at t_3, (d) Equivalent resonant circuit in ZVS transition mode for double half-bridge multilevel at t_3.

the resonant tank has to be designed to meet this requirement, otherwise the voltage rating of the secondary side MOSFETs has to to be higher, affecting the overall efficiency.

Chapter 3

Multilevel Half-Bridge Phase-Shift Quasi-Resonant converter for VRM Applications

This chapter presents a single-stage approach for the 380 V VRM based on a quasi-resonant multilevel topology constant on-time (COT) operation. The proposed topology inherently integrates the multi-phase approach, providing fast phase shedding and flat high efficiency curves even at light load conditions. The chapter analyses the circuit topology and proposes a control architecture for fast transient response, including the current sharing capabilities and finally a current doubler coupling inductor for the proposed architecture is presented.

3.1 Analysis of the Proposed Converter

The proposed solution is based on an isolated converter, which comprises half-bridge three-level on the primary side and a current-doubler (CD) rectifier on the secondary side as shown in Fig. 3.1. The primary side half-bridge three-level operates in phase-shifted COT [68] [81], as shown in Fig. 3.2. The secondary side current-doubler rectifier uses synchronous rectifiers comprising Q_{r1} and Q_{r2}. Due to resonant transitions, both Q_{r1} and Q_{r2} are on at zero voltage (ZVS). This is obtained by generating a zero current detection (ZCD) signal on the voltage across the synchronous rectifier switches (i.e. v_{ph1} and v_{ph2}).

The proposed solution presents an additional capacitance C_r on the secondary side and an innovative driving scheme to enable ZVS operation. To simplify the analysis, the magnetizing current is neglected, the leakage inductance is included in the external inductance L_r and the divided capacitors C_1 and C_2 are large enough to be treated as a voltage source (i.e. $Vc_{C_1} = Vc_{C_2} = V_{in}/2$). Thus, each resonant transition includes L_r, C_r and one of the output inductances $L_{out1,2}$, depending on the v_f voltage value.

As before reported the proposed HBPS-QR converter, depicted in Fig. 3.1, is implemented in a multilevel structure which is the main differences with FBPS-QR proposed in section 2.3. FBPS-QR has at least one switching node which is exposed to the transformer stray capacitance [67]. In the FBPS-QR topology, the parasitic stray capacitance of the transformer is an important

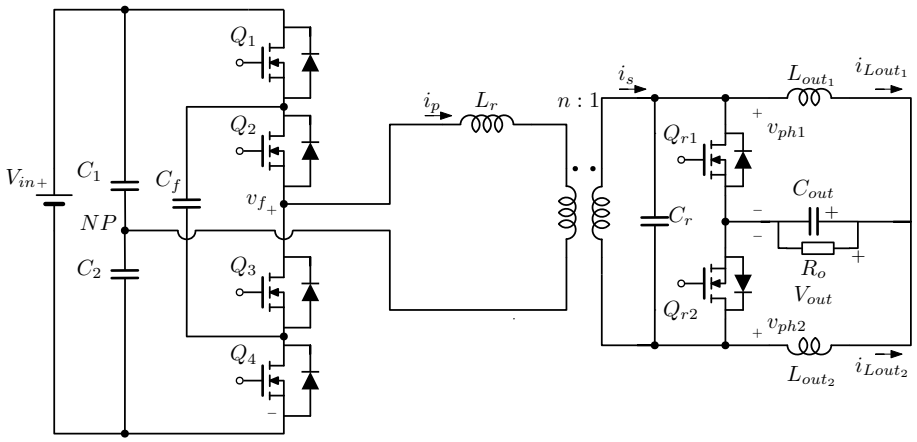


FIGURE 3.1: 380 V VRM based on a half-bridge three-level on the primary side and a current doubler with resonant capacitor C_r on the secondary side.

limitation in high voltage operation. On the other hand, HBPS-QR does not present a switching node directly exposed to the transformer stray capacitance, since the resonant inductance is placed in between the switching node and the transformer. This is of paramount importance to consider, as the transformer does not affect the ZVS capability. In this scenario the transformer can be realized in fully interleaved configuration. Secondary, another important advantage is that the voltage stress on the primary MOSFETs is decreased by half of the input voltage. This results in lower energy stored in the primary inductance L_r for ZVS operation together with lower copper losses at primary side compared with FBPS-QR topology.

The proposed dc-dc converter has two different modes of operation: when the voltage on the resonant capacitor C_r reaches zero during the input powering phase (when Q_1 and Q_2 are on or when Q_3 and Q_4 are on) and when the voltage on the resonant capacitor C_r reaches zero during the freewheeling phase (when Q_2 and Q_3 are on). The two operating modes are denoted as $Operation\ Mode\ A$ and $Operation\ Mode\ B$, respectively, and occur at increasing level of load power, i.e. $Mode\ A$ is for lighter load conditions and $Mode\ B$ for heavier load conditions.

3.1.1 Operation Mode A for HBPS-QR: Resonant Transition during the powering phase

Following the converter waveforms shown in Fig. 3.2, the proposed converter in PS control mode has twelve operation stages during a switching cycle that correspond to the topological states shown in Fig. 3.3.

For the simplicity of explanation, we will denote $L_{out} = L_{out_1} = L_{out_2}$. The twenty subintervals are described as follows:

1) $\boldsymbol{t_0 - t_1}$: at $t = t_0$, switch Q_2 is turned on, the primary current i_p freewheels through switches Q_2, Q_4 and the flying capacitor C_f, and both Q_{r1} and Q_{r2} are on. The topological state is shown in Fig. 3.3(a).

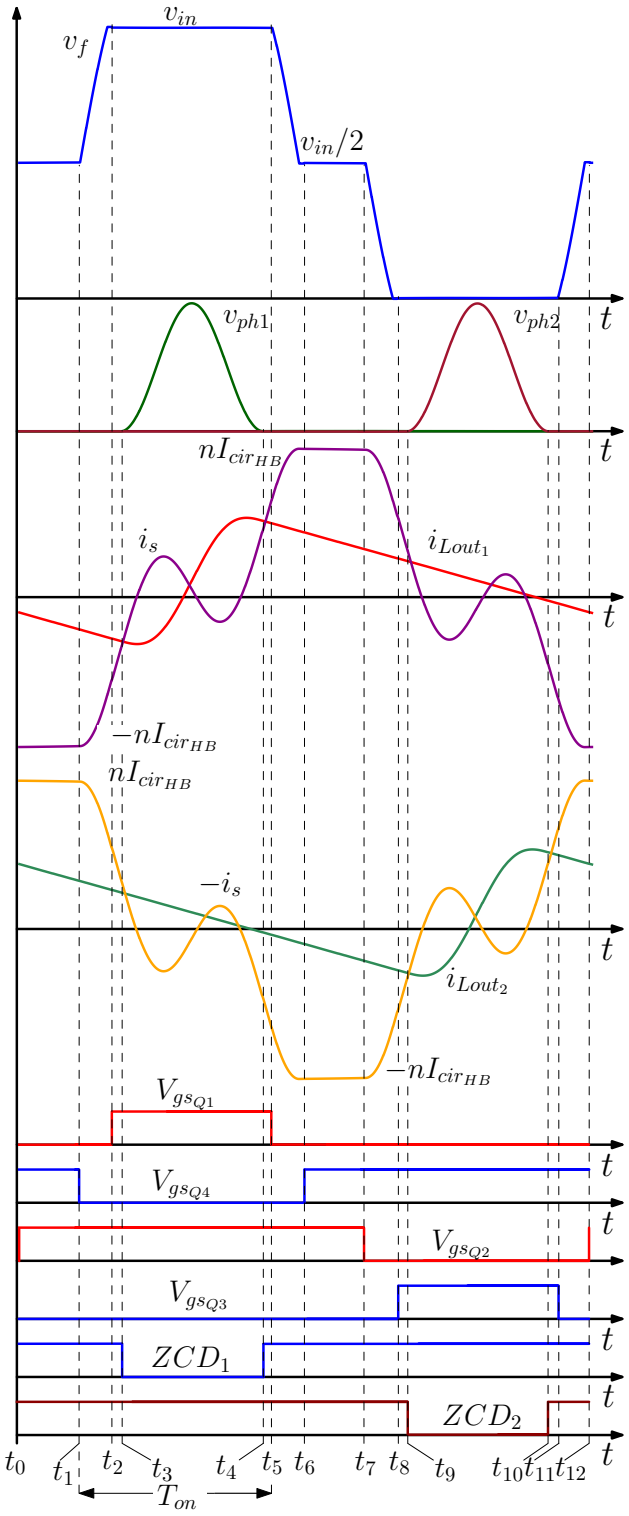


FIGURE 3.2: Main converter waveforms for Operation *Mode A*. From top to bottom: primary side voltages (v_f), voltages ($v_{ph1,2}$), secondary side transformer current i_s and inductor currents ($i_{L_{out1}}$ and $i_{L_{out2}}$), gate-source voltage MOSFETs ($V_{gs_{Q1}}$, $V_{gs_{Q4}}$, $V_{gs_{Q2}}$ and $V_{gs_{Q3}}$) and zero current detection (ZCD) signals ($ZCD_{1,2}$)

2) $\boldsymbol{t_1 - t_2}$: at $t = t_1$, switch Q_4 is turned off, and the primary current i_p discharges the capacitance of Q_1 and charges the capacitance of Q_4. When capacitance of Q_1 is discharged to zero, its body diode conducts to enable ZVS turn-on of Q_1. Both Q_{r1} and Q_{r2} are on and the topological state corresponding to this subinterval is reported in Fig. 3.3(b). The current $i_p(t_1)$ that enable ZVS operation of Q_1 is denoted as circulating current $I_{cir_{HB}}$ (i.e. $I_{cir_{HB}} = -i_p(t_1) = -i_s(t_1)/n$), as shown in Fig. 3.2, and it is almost constant within the interval $(t_0 - t_1)$.

3) $\boldsymbol{t_2 - t_3}$: at $t = t_2$, switch Q_1 is turned on with ZVS and both secondary side rectifiers Q_{r1} and Q_{r2} remain conducting, as shown in Fig. 3.3(c). After $t = t_1$, the primary current i_p increases with a slope that can be approximated as $V_{in}/2L_r$.

4) $\boldsymbol{t_3 - t_4}$: at $t = t_3$, the secondary current i_s reaches i_{Lout1} (i.e. $i_s(t_3) = i_{Lout1}(t_3)$), Q_{r1} is turned off, and Q_{r2}, Q_1 and Q_2 are conducting. The topological state is shown in Fig. 3.3(d). Indeed, Q_{r1} is turned off when the ZCD_1 signal is low. Signal ZCD_1 is theoretically obtained by measuring the voltage across Q_{r1}, compared with zero (or with a threshold close to zero) and thus detecting when the current on Q_{r1} changes sign. In practice, ZCD_1 signal is obtained with a more complicated procedure also to enable current sharing, as outlined in section 2.3.3. In this subinterval, the resonance between L_r, C_r and L_{out1} occurs and the equivalent resonant circuit is shown in Fig. 3.4 case a).

5) $\boldsymbol{t_4 - t_5}$: at $t = t_4$, the resonant voltage reaches zero volt, ZCD_1 signal becomes high and switch Q_{r1} is turned on, while at the primary side switches Q_1 and Q_2 are still conducting. The topological state is reported in Fig. 3.3(c).

6) $\boldsymbol{t_5 - t_6}$: at $t = t_5$, switch Q_1 is turned off, i_p charges the capacitance of switch Q_1 and discharges the parasitic capacitance of switch Q_4 in order to achieve ZVS. The topological state is now represented in Fig. 3.3(b). The current that enables ZVS of Q_4 is $i_p(t_5)$ and it is only slightly smaller than $I_{cir_{HB}}$. Thus, $I_{cir_{HB}}$ is still a good index to establish when turn-on ZVS is achieved for all switches.

7) $\boldsymbol{t_6 - t_7}$: at $t = t_6$, Q_4 is turned on at ZVS and i_p freewheels through switches Q_2, Q_4 and C_f, as shown in Fig. 3.3(a). At $t = t_6$, the positive half-cycle of the switching period is completed (i.e. $t_6 = t_0 + \frac{T_{sw}}{2}$).

8) $\boldsymbol{t_7 - t_8}$: at $t = t_7$, switch Q_2 is turned off, i_p charges the capacitance of switch Q_2 and discharges the parasitic capacitance of switch Q_3 in order to achieve ZVS. The topological state is now represented in Fig. 3.3(e).

9) $\boldsymbol{t_8 - t_9}$: at $t = t_8$, switch Q_3 is turned on with ZVS and both secondary side rectifiers Q_{r1} and Q_{r2} remain conducting, as shown in Fig. 3.3(f). After $t = t_7$, the primary current i_p decreases with a slope that can be approximated as $V_{in}/2L_r$.

10) $\boldsymbol{t_9 - t_{10}}$: at $t = t_9$, the secondary current i_s reaches i_{Lout2} (i.e. $-i_s(t_9) = i_{Lout2}(t_9)$), Q_{r2} is turned off, and Q_{r1}, Q_3 and Q_4 are conducting. The topological state is shown in Fig. 3.3(g). Similar to stage $(t_3 - t_4)$ the principle operation of this phase is the same, except for different polarities across the primary side transformer and still the resonance takes place between L_r, C_r and L_{out2}.

11) $\boldsymbol{t_{10} - t_{11}}$: at $t = t_{10}$, the resonant voltage reaches zero volt, ZCD_1 signal becomes high and switch Q_{r2} is turned on, while at the primary side switches Q_3 and Q_4 are still conducting. The topological state is reported in Fig. 3.3(f).

12) $\boldsymbol{t_{11} - t_{12}}$: at $t = t_{11}$, switch Q_3 is turned off, i_p charges the capacitance of switch Q_3 and discharges the parasitic capacitance of switch Q_2 in order to achieve ZVS. The topological state is now represented in Fig. 3.3(e). The current that enables ZVS of Q_4 is $i_p(t_{11})$ and it is only slightly higher than $-I_{cir_{HB}}$. At $t = t_{11}$ when switch Q_2 is turned on and the primary current i_p freewheels through Q_2, Q_4 and the flying capacitor C_f as reported in Fig. 3.3(a). Now the switching period is completed (i.e. $t_{12} = t_0 + T_{sw}$).

Taking into account that the average voltage of $v_{ph1}(t)$ is equal to the output voltage V_{out}, the voltage conversion ratio in Mode A is evaluated deriving $v_{ph1}(t)$ and then averaging it over the switching period. The analytical expression of $v_{ph1}(t)$ is obtained solving the equivalent resonant circuit of Fig. 3.4 case a) and applying a step variation of $v(t)$ equal to $V_{in}/2n$. Assuming $v_{C_r}(t_3) = 0$ and $i_{L_{out}}(t_3) = i_s(t_3)$, for $t_3 < t < t_4$, $v_{ph1}(t)$ can be derived as follows:

$$v_{ph1}(t) = \frac{V_{out}L_r + \frac{nV_{in}L_{out}}{2}}{L_r + n^2 L_{out}} \left(1 - cos(\omega_r(t - t_3))\right), \tag{3.1}$$

where the resonant angular frequency $\omega_r = \sqrt{\frac{L_r + n^2 L_{out}}{L_{out} L_r C_r}}$. Averaging $v_{ph1}(t)$ over the switching period T_{sw}, the output voltage V_{out} is therefore given by

$$\begin{aligned} V_{out} &= \frac{1}{T_{sw}} \int_{t_0}^{t_0 + T_{sw}} v_{ph1}(\tau) d\tau \\ &= \frac{V_{out}L_r + \frac{nV_{in}L_{out}}{2}}{L_r + n^2 L_{out}} \frac{f_{sw}}{f_r}. \end{aligned} \tag{3.2}$$

where $f_r = \omega_r/(2\pi)$ and $f_{sw} = 1/T_{sw}$. Since $V_{out} \ll V_{in}$, $L_r/n^2 < L_{out}$, and $n > 1$, also $V_{out}L_r \ll nV_{in}L_{out}/2$. Thus, term $V_{out}L_r$ can be neglected in (3.2) and the converter voltage conversion ratio (V_{out}/V_{in}) is approximated by:

$$\frac{V_{out}}{V_{in}} \approx \frac{nL_{out}}{2\left(L_r + n^2 L_{out}\right)} \frac{f_{sw}}{f_r}. \tag{3.3}$$

As can be seen, the output voltage V_{out} is directly controlled by the switching frequency f_{sw}. Thus, the proposed solution is inherently a constant-on time modulation, where the *constant phase-shift*, here denoted also as *constant on-time* T_{on}, is determined by the resonant transition, while the output voltage regulation is obtained by varying the switching frequency. From eq. (2.7), the circulating current $I_{cir_{HB}}$ for HBPS-QR is given by:

$$I_{cir_{HB}} \approx \frac{\frac{V_{in}T_{on}}{2} - nV_{out}T_{sw}}{2L_r}. \tag{3.4}$$

As can be seen, the circulating current $I_{cir_{HB}}$, that enables ZVS operation, is independent on the load conditions, as the voltage conversion ratio and

therefore also T_{sw} are not dependent on I_{out}. This in an important feature of our solution and it is valid also for $Mode\ B$ for a wide range of operating conditions.

3.1.2 Operation Mode B: Resonant Transition During the Freewheeling Phase

Fig. 3.5 reports the main converter waveforms during $Operating\ Mode\ B$, where the resonant voltage reaches zero during the freewheeling subinterval. The converter operation in the first half of the switching cycle T_{sw} is described in six subintervals that correspond to the topological states shown in Fig. 3.3. The operation on $Mode\ B$ can be explained by analyzing the following subintervals:

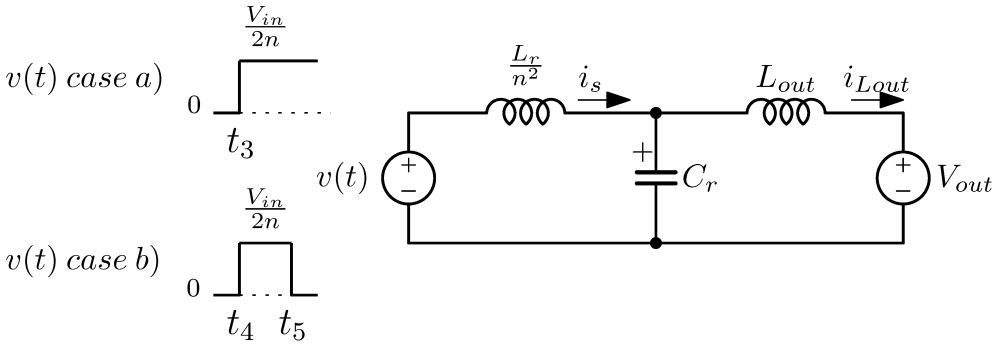


FIGURE 3.4: Equivalent resonant circuits for converter analysis: case a) equivalent circuit in $Mode\ A$, case b) equivalent circuit in $Mode\ B$.

1) $\boldsymbol{t_0 - t_1}$: switch Q_4 is turned on with ZVS and the primary current i_p freewheels through Q_2, Q_4 and C_f. Differently from $Mode\ A$, during this interval the synchronous rectifier switch Q_{r2} is still off, as the resonant voltage transition of $v_{ph2}(t)$ started on the negative half-cycle is still not completed as shown in Fig. 3.3(h).

2) $\boldsymbol{t_1 - t_2}$: at t_1, $v_{ph2}(t)$ reaches zero, ZCD_2 signal becomes high and Q_{r2} is turned on, while at primary side Q_2 and Q_4 are still. The topological state is now depicted in Fig. 3.3(a).

3) $\boldsymbol{t_2 - t_3}$: this interval is the same as the interval $t_1 - t_2$ of $Mode\ A$.

4) $\boldsymbol{t_3 - t_4}$: this interval is the same as the interval $t_2 - t_3$ of $Mode\ A$. At $t = t_4$, i_s reaches i_{Lout1}.

5) $\boldsymbol{t_4 - t_5}$: at $t = t_4$, Q_{r1} is turned off and the resonance takes place between L_r, C_r and L_{out}. The topological state is now depicted in Fig. 3.3(e). The duration of this mode, denoted as T_ϕ (i.e. $T_\phi = t_5 - t_4$), is a subinterval of T_{on} and it can be expressed as follows:

$$T_\phi = T_{on} - T_{ch}, \tag{3.5}$$

being T_{ch} the pre-charging time required to increase the secondary current i_s from $-nI_{cir_{HB}}$ to $i_{Lout1}(t_4)$, i.e. when the resonant transition starts. Thus, the pre-charging time T_{ch} can be expressed by

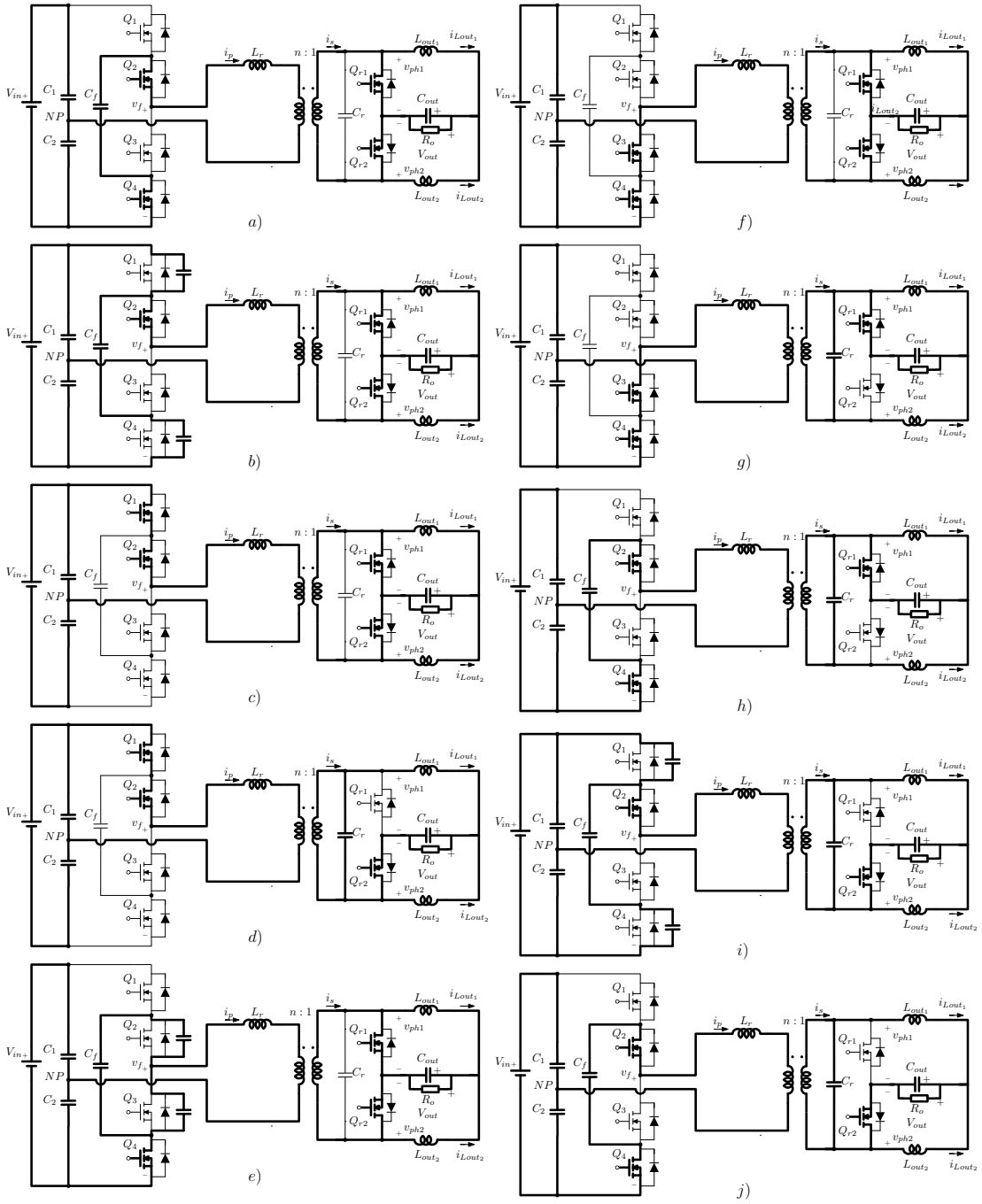


FIGURE 3.3: Switch configuration during each subinterval in $Mode\ A$ and $Mode\ B$: $Mode\ A$ (a) $t_0 - t_1$, b) $t_1 - t_2$, c) $t_2 - t_3$, d) $t_3 - t_4$, c) $t_4 - t_5$, b) $t_5 - t_6$ a) $t_6 - t_7$ e) $t_7 - t_8$ f) $t_8 - t_9$ g) $t_9 - t_{10}$ f) $t_{10} - t_{11}$ e) $t_{11} - t_{12}$) and $Mode\ B$ (g) $t_0 - t_1$, a) $t_1 - t_2$, b) $t_2 - t_3$, c) $t_3 - t_4$, d) $t_4 - t_5$, h) $t_5 - t_6$, j) $t_5 - t_6$).

$$\begin{aligned} T_{ch} &= (nI_{cir_{HB}} + I_{Lout}(t_4))\frac{2L_r}{nV_{in}} \\ &\approx (nI_{cir_{HB}} + \frac{I_{out}}{2} - \frac{\Delta I_{Lout}}{2})\frac{2L_r}{nV_{in}} \end{aligned} \tag{3.6}$$

where ΔI_{Lout} is the peak-to-peak current ripple and $i_{Lout}(t_4)$ is approximated as the minimum value of the inductor current i_{Lout1}. Thus, using (3.4) and (3.5), T_ϕ is given by:

$$T_\phi \approx \frac{1}{2}(T_{on} + \frac{2nV_{out}}{V_{in}}T_{sw} - \frac{2(I_{out} - \Delta I_{Lout})L_r}{nV_{in}}) \tag{3.7}$$

6) $\boldsymbol{t_5 - t_6}$: at $t = t_5$, Q_1 is turned off, i_p charges the capacitance of switch Q_1 and discharges the parasitic capacitance of switch Q_4. The topological state is now depicted in Fig. 3.3(i). At $t = t_6$, Q_4 is turned on in ZVS conditions and the positive half-cycle of the switching period is completed (i.e. $t_6 = t_0 + \frac{T_{sw}}{2}$) and the topological state of Fig. 3.3(j) is the first one of the negative half-cycle.

During the negative half-cycle of a switching period, the behavior of the circuit is the same as the one described during the positive half-cycle, as depicted in Fig. 3.5.

Similarly to $Mode\ A$, the output voltage is derived averaging $v_{ph1}(t)$ over the switching period T_{sw}. From [67], the voltage $v_{ph1}(t)$ in this mode can be expressed as:

$$\begin{aligned} v_{ph1}(t) = &\frac{V_{out}L_r + \frac{nV_{in}L_{out}}{2}}{L_r + n^2L_{out}}\left(1 - cos(\omega_r(t - t_4))\right) - \\ &\frac{nV_{in}L_{out}}{2(L_r + n^2L_{out})}H\left(t - t_5\right)\left(1 - cos\left(\omega_r(t - t_5)\right)\right), \end{aligned} \tag{3.8}$$

where $H(t)$ is the Heaviside function (i.e. $H(t) = 1$, for $t \geq 0$ and $H(t) = 0$ for $t < 0$) and the duration of the resonant voltage is T_{rB} as reported in Fig. 3.5. In eq. (3.8) the unique difference with FBPS-QR is that due to multilevel topology here the input voltage for the resonant tank is one half.

As described in section 2.3.2 V_{out}, in $Mode\ B$, is given by the following equation:

$$\frac{V_{out}}{V_{in}} = \left(\frac{\omega_r T_\phi + 2\sin\left(\omega_r \frac{T_\phi}{2}\right)}{2\pi}\right)\frac{nL_{out}}{2(L_r + n^2L_{out})}\frac{f_{sw}}{f_r}. \tag{3.9}$$

It is worth noting that equation (3.9) differs from equation (3.3) only in the factor between the brackets and the output voltage V_{out} is still controlled by the switching frequency f_{sw} even in *Mode B*. In fact, looking at (3.7), T_ϕ decreases when the load current I_{out} increases. Thus, from (3.9), the output voltage V_{out} decreases and the control system imposes the reference voltage V_{ref} by increasing f_{sw}.

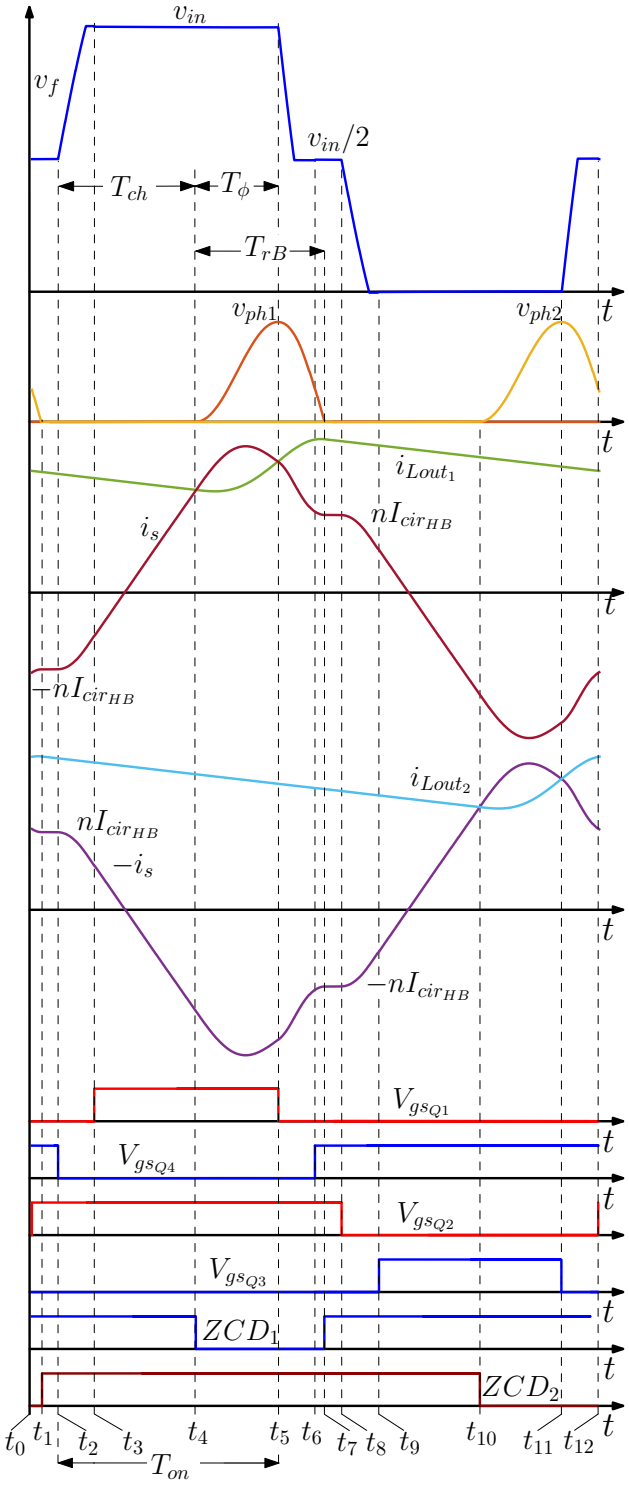


FIGURE 3.5: Main converter waveforms for Operation $Mode\ B$. From top to bottom: primary side voltages (v_x and v_y), voltages ($v_{ph1,2}$), secondary side transformer current i_s and inductor currents ($i_{L_{out1}}$ and $i_{L_{out2}}$)

3.2 Differences between FBPS quasi-resonant and HBPS multilevel quasi-resonant converter

To demonstrate the comparability in power density and efficiency between between FBPS quasi resonant 48 V VRM showed in section 2.4 and HBPS multilevel quasi-resonant converter 380 V VRM, in this section the fundamental metrics are calculated.

In order to make a fair VRM comparison between the three topologies (48 V quasi resonant FBPS, 380 V quasi-resonant multilevel HBPS and FBPS), the main converters are kept as similar as possible, designing both with the same equivalent resonant tank, in order to obtain the same switching frequency, as reported in table 3.1.

ZVS condition at primary side

ZVS at primary side in the proposed version, as in the 48 V case for FBPS-QR has been widely discussed as a way to ensure high frequency operation and high efficiency. As reported in section 3.1 the recirculating current, equation 3.4, enables ZVS operation and, as demonstrated, it is load-independent. In order to make a fair comparison, a common on-time-dependent model for the inductive energy is described for the three topologies. The following equation is useful to show the impact of the ZVS capability between the 48 V, the 380 V FBPS-QR converter and the 380 V HBPS-QR one:

$$E_L = \frac{1}{2} L_p I_{ric}^2 = \frac{1}{8L_p} \left(V_{in} T_{on} - n T_{sw} V_{out} \right)^2 , \tag{3.10}$$

where I_{ric} is the circulating current in FBPS-QR case and HBPS-QR case as given by equations (2.7) and (3.4).

TABLE 3.1: Comparison between FBPS and HBPS for the proposed quasi-resonant converter

	48 V FBPS-QR	380 V FBPS-QR	380 V HBPS-QR
FET($C_{oss_{avg}}$)	BSC042NE7NS3 (1.4nF)	IPL60R299CP (228pF)	BSZ42DN25NS3 (72pF)
Turns ratio n	n_{nom}	$8n_{nom}$	$4n_{nom}$
L_p	$L_{p_{nom}}$	$64L_{p_{nom}}$	$16L_{p_{nom}}$
Ip_{ric}	$Ip_{ric_{nom}}$	$>> Ip_{ric_{nom}}/16$	$\approx p_{ric_{nom}}/8$
Ip_{pk}	$Ip_{pk_{nom}}$	$Ip_{pk_{nom}}/16$	$Ip_{pk_{nom}}/8$
Ip_{rms}	$Ip_{rms_{nom}}$	$> Ip_{rms_{nom}}/16$	$Ip_{rms_{nom}}/8$

From equation 3.10 it is possible to obtain the graph reported in Fig. 3.6 where it is shown (in red), as function on T_{on}, the stored energy that actually determines the recirculating current at primary side. The red curve in Fig. 3.10 is plotted using the following data: $n_{nom} = 5$, $L_{p_{nom}} = 1.7\mu H$, $C_{res} = 130nF$, $L_{out} = 170nH$ and $V_{out} = 1.8V$. The comparison made in Fig. 3.6 is consistent since the equivalent resonant tank reported at secondary side is kept a as the same for all converters compared. It is necessary to create an

accurate model to predict the large-signal C_{oss} value for all MOSFETs under evaluation [82], so as to predict the ZVS boundary for each MOSFETs for the different VRMs here compared. As reported in [82], the large signal C_{oss} provide a practical and accurate tool for fast switching loss evaluation of WBG power MOSFETs, while the small signal based C_{oss} datasheet parameters can be misleading. In table 3.1 are reported three different MOSFETs and their average MOSFET parasitic capacitance calculated using equation (2.68).

In eq. (2.68) $V_{ds_{max}}$ depends from the topology (48 V VRM based on FBPS is 48 V, whilst in 380 V VRM based on FBPS is 380 V and finally in 380 V VRM HBPS is 190 V). In regards to ZVS for the three VRMs, in Table 3.1, in Fig. 3.6 are reported the ZVS boundaries calculated using equation (2.67) and considering C_w as parasitic transformer stray capacitance, .

As reported in equation (2.67) C_w is important once the transformer is implemented in planar structure and, as investigate in [83] is in parallel with the MOSFETs parasitic capacitance. For the sake of explanation in Fig. 3.7(a) and 3.7(b) report respectively the circuit during the ZVS mode for FBPS-QR and its equivalent resonant circuit during ZVS transition mode. In general FBPS-QR has at least one switching node which is directly exposed to the transformer stray capacitance since the resonant inductance position (under hypotheses that $L_r >> L_k$) can be either connected directly to the Vx or Vy net. This results in a higher energy for ZVS transition for FBPS-QR. On the contrary, in HBPS-QR the switching node that can be exposed directly to the transformer stray capacitance C_w is V_f, that can actually be separated with the resonant inductance, as reported in Fig. 3.1. In Fig. 3.7(c) the primary side circuit configuration during ZVS transition and its equivalent resonant circuit are reported. From Fig. 3.7(c) and 3.7(d) it is possible to understand how the HBPS-QR ZVS transition does not depend on transformer stray capacitance: this is of foremost importance to consider. Thus, the minimum energy stored in the resonant inductance, during ZVS operation, has to be higher than the value obtained from the following equation:

$$E_C \approx \frac{1}{2}\left(2C_{oss_{avg}}\right)\left(\frac{V_{in}}{2}\right)^2, \tag{3.11}$$

In FBPS-QR the transformer stray capacitance needs to be limited preventing an interleaved winding arrangement, thus increasing ac resistance.

By looking at the diagram in Fig. 3.6 it can be noticed that the technology of the MOSFETs and transformer becomes crucial for achieving ZVS. In Fig. 3.6, in blue, the ZVS condition for 48 V VRM based on FBPS-QR without considering C_w is reported. In fact, at this voltage the transformer parasitic stray capacitance can be neglected. Instead, in green, is highlighted the ZVS boundary condition for HBPS-QR 380 V VRM considering only the FETs parasitic capacitance. Finally, the cyan and magenta lines correspond to the ZVS boundary condition respectively for FBPS-QR 380 V VRM with ($C_W = 800pF$) and without considering the transformer parasitic stray capacitance.

In the multilevel quasi-resonant HBPS topology, overcoming the constraint of containing stray capacitance, a fully interleaved windings planar structure

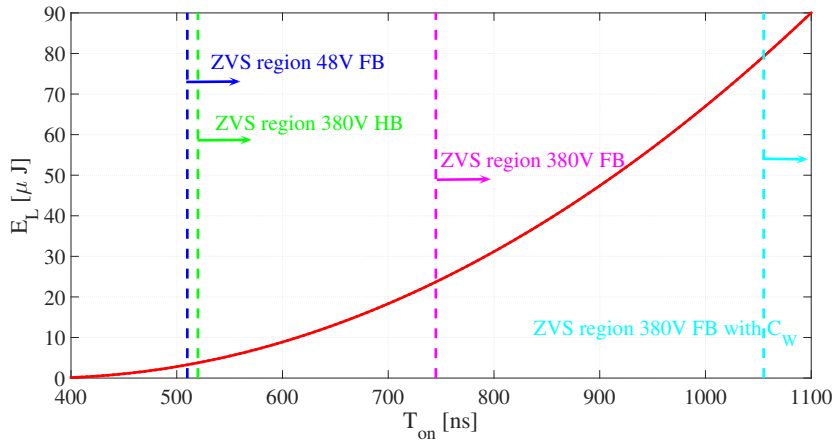


FIGURE 3.6: Stored energy in the resonant inductance during ZVS transition (in red) vs ZVS regions for 48V FB (blu), 380V HB (green), 380V FB (magenta) and 380V FB considering parasitic windings capacitance C_w (cyan).

is used to allow high switching frequency operation. However, the proposed planar structure is not implemented in a fully interleaved structure but in a semi-interleaved arrangement in order to suppress the CM noise in the transformer, which is one of the main sources of the EMI noise. The proposed planar transformer was designed to find a balance between the stray transformer capacitance C_w and the ac resistance R_{ac}. In the FBPS-QR the transformer would have been critical due to higher transformer turns ratio so as higher R_{dc} and R_{ac} and also higher CM noise. Thus, the proposed solution results in high efficiency and high power density as HV POL converter.

In section 4.4 the transformer realization for HBPS-QR is presented for both semi and fully interleaved windings arrangement.

Power density

The following equation gives the equivalent cross section area A_e for the transformer:

$$A_e = \frac{\int_{t_3}^{t_4} V_{ph1}(t)dt}{2B} \tag{3.12}$$

where B is the flux density and V_{ph1} is given by eq. (3.1) and the secondary windings turns are $N_s = 1$. From eq. (3.12) it follows that both converter FBPS-QR and HBPS-QR multilevel have the same equivalent core cross section area, and so the same transformer volume. The output inductance L_{out} are the same in both solution assuming that both converters cell are carrying the same current. This is of paramount importance to consider, because the power density is dominated by the transformer volume.

The primary inductance volume for FBPS-QR and even in HBPS-QR depends from the peak current and also from the RMS current as described by the following relation:

$$L_{r_{volume}} \propto I_{p_{RMS}} * I_{p_{PK}} * L_r. \tag{3.13}$$

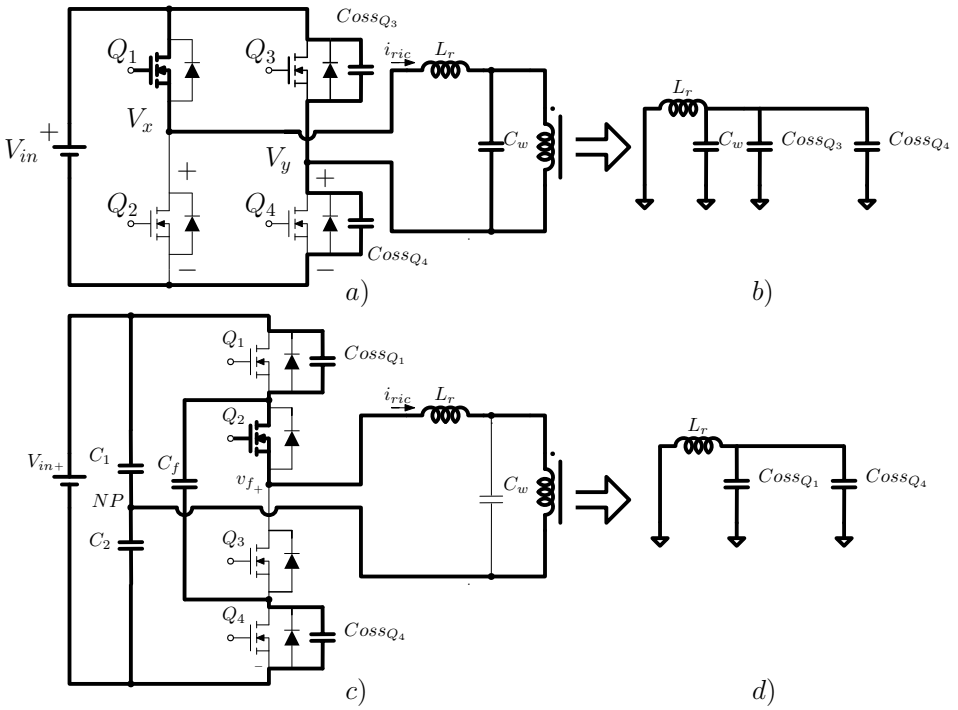


FIGURE 3.7: (a) Equivalent circuit in ZVS full-bridge, (b) Equivalent resonant circuit in ZVS transition mode for full-bridge topology, (c) Equivalent circuit in ZVS half-bridge multilevel, (d) Equivalent resonant circuit in ZVS transition mode for half-bridge multilevel topology proposed.

Hence, considering equation (3.13), the total volume does not depend only from the peak current, so, it is important to consider even the ZVS capability comparison from the technology point of view. Thus, it is useful to calculate the peak current and RMS current at primary side for both 380 V VRM based on HBPS-QR and 48 V VRM based on FBPS-QR.

$$I_{Cres_{pk,380V}} = C_{res}\frac{V_{out}L_r + 4n_{48}\frac{380L_{out}}{2}}{L_r + 16n_{48}^2 L_{out}}\omega_{res} \tag{3.14}$$

$$I_{Cres_{pk,48V}} = C_{res}\frac{V_{out}L_r + n_{48}48L_{out}}{L_r + n_{48}^2 L_{out}}\omega_{res} \tag{3.15}$$

$$I_{p_{pk,380V}} = \left(\frac{I_{out}}{2} - \frac{\Delta I_{Lout}}{2} + I_{Cres_{pk,380V}}\right)/4n_{48} \tag{3.16}$$

$$I_{p_{pk,380V}} = \left(\frac{I_{out}}{2} - \frac{\Delta I_{Lout}}{2} + I_{Cres_{pk,48V}}\right)/n_{48} \tag{3.17}$$

Considering equations (3.14), (3.15), (3.16) and (3.17) it is easy to demonstrate (table 3.2) that the peak current is 8 times larger in 48 V VRM FBPS-QR comparing with 380 V VRM HBPS-QR. This is actually as expectation, since

the transformer turns ratio in HBPS-QR is 4 times larger than in FBPS-QR. Moreover, the RMS current scales with the turns ratio of the transformer. This is confirmed by the graph reported in Fig. 3.6, where the energy for ZVS for FBPS-QR 48 V VRM and HBPS-QR 380 V VRM are almost the same. Thus, 380 V VRM HBPS-QR has the same power density of 48 V VRM FBPS-QR, making our proposed solution suitable for all POL applications as HV POL. As here demonstrated the primary RMS current in HBPS-QR 380 V VRM is very low which reduces the conduction losses in the primary MOSFETs and transformer, making it theoretically more efficient than FBPS-QR 48 V VRM.

Finally, it is also interesting to compare the power density between HBPS-QR and FBPS-QR, both for 380 V VRM application, in order to validate our proposed topology, as done for 48 V VRM application by using equations (3.14), (3.15), (3.16) and (3.17). The only difference between FBPS-QR and HBPS-QR for VRM application is a technology issue as demonstrated before and explained in Fig. 3.6. The ZVS capability of FBPS-QR for high voltage is limited by technology MOSFETs. Thus, the primary resonant inductance would be bigger as clarified in table 3.2.

3.3 Control System, Current Sharing and Dynamic Performance

The controller block diagram of the multi-phase dc-dc converter 380 V VRM is reported in Fig. 3.8, where two interleaved phases, indicated as $CELL_{1,2}$, are shown. The voltage loop controller implements the load line, as required by VRM specifications, imposing a resistive output impedance equal to R_{ll}, i.e. $V_{ref} = V_{out} - R_{ll}I_{cellT}$. This is obtained by calculating the voltage error by the difference between the reference voltage V_{ref}, determined by the voltage identification (VID) code, and the sum of voltage v_{out} and of the total cell current i_{cellT} multiplied by the load line resistance R_{ll} [31]. As in any VRM applications, the inductor current is detected and used instead of the output current. The voltage error is then processed by the PID controller that drives the voltage controlled oscillator (VCO), the frequency of which is multiplexed for each of the interleaved cells. From each cell, two PWM signals with a duty cycle of 50% are generated on the primary side with programmed time shift equal to T_{on}.

Fig. 3.8 also reports the block diagram for the current sharing loop needed to ensure the current balancing in presence of mismatches in the resonant components. This additional loop regulates the delay (of the digital delay line (DDL)) of the turn-off of the synchronous rectifier switches $Q_{r1,2}$ with respect to the commutation instant determined by ZCD signal. Instead from the control prospective as was demonstrated in section 2.3.4 the converter presented in this paper is a buck derived topology. Fig. 3.9 shows the control to output transfer function calculated by Matlab simulation (using the parameters of Table 3.2) where is reported the typical second-order transfer function of the buck converter. For further details on the current sharing

functionality and the small signal analysis the interested reader should refer to the FBPS-QR functionalities presented in section 2.3.

TABLE 3.2: Converter parameters

Input voltage	$V_{in} = 380\ V$
Output inductances	$L_{out} = 110\ nH$
External inductance	$L_r = 28.8\ \mu H$
Resonance capacitance	$C_r = 132\ nF$
Transformer turns-ratio	$n = 20$
Constant on-time	$T_{on} = 725\ ns$
Output capacitance	$C_{out} = 470\ \mu F$

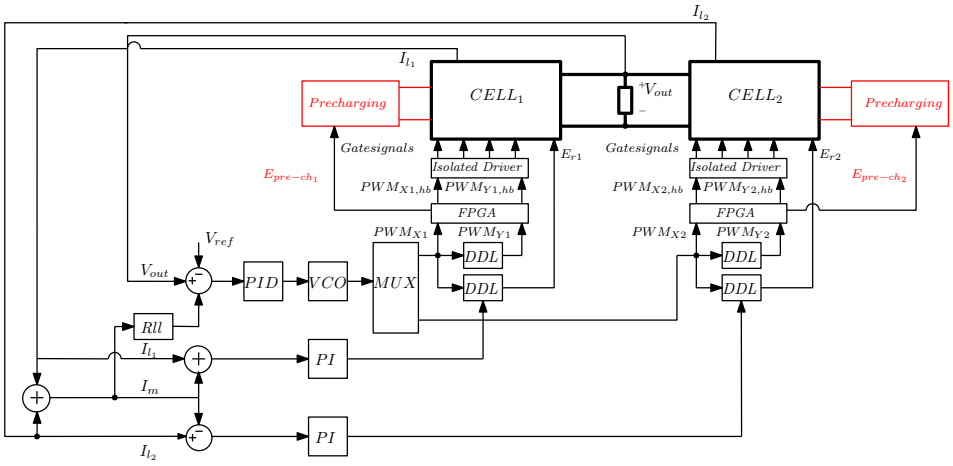


FIGURE 3.8: Block diagram of the multi-phase control architecture with two phases, indicated as $CELL_{1,2}$.

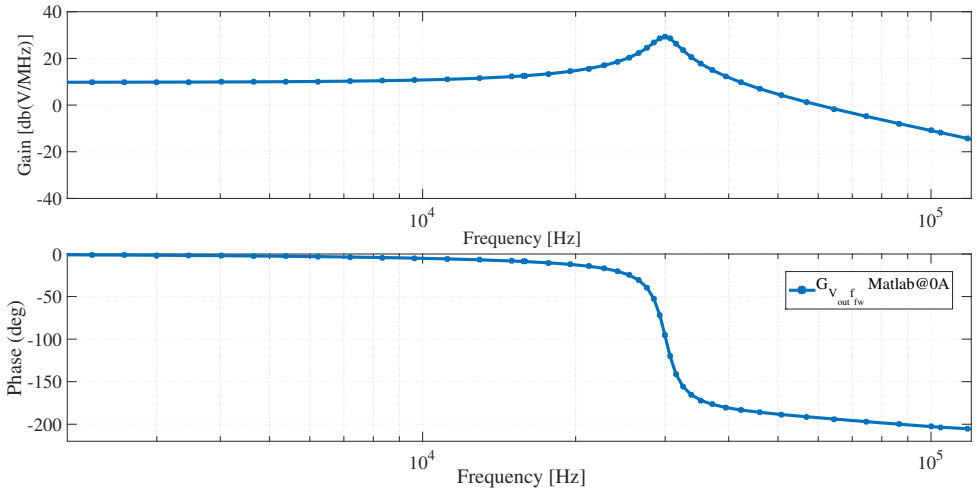


FIGURE 3.9: Control to output transfer function calculated with Matlab using the parameters reported in Table 3.2.

3.4 Startup 380 V VRM HBPS-QR

Start-up is also a concern for the proposed 380 V VRM based on multilevel topology [35] [84] at primary side. Initially the flying capacitor is uncharged, in this scenario if the converter is started up Q_1 and Q_4 will see the full input voltage. This will not allow to used reduced voltage rated device and even the functionality of the converter will be compromised, until the flying capacitor naturally reached the half of the input voltage due to phase-shift operation. A precharging method of the flying capacitor is shown in Fig. 3.10. The startup circuit operates through two signal MOSFETs in series with the flying capacitor. The value of the zener in parallel with the V_{sg} of the P-MOS fixed the precharging current. Key waveforms during the proposed start up procedure for HBPS-QR are shown in Fig. 3.11. The proposed start-up can be divided in two phases. In the first phase, during the precharging time T_{pre}, the flying capacitor C_f is charged. When the flying capacitor voltage V_{C_f} reached V_z ((with $V_z = V_{in_{max}}/2$+5 V)) the zener diode starts to conduct to keep the flying capacitor voltage slightly above half of the input voltage. During the precharging time all power MOSFETs are off. In the second phase, when the VRM is enabled, the converter is started up and the flying capacitor falls naturally at half of the input voltage during the second phase.

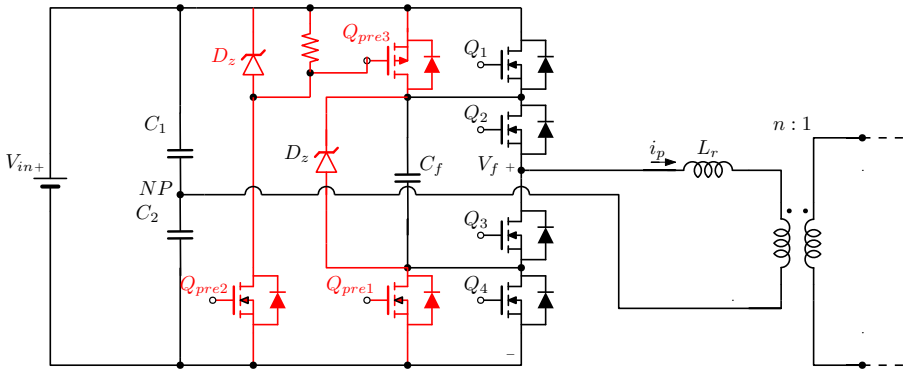


FIGURE 3.10: Startup circuit of HBPS-QR in red.

The proposed start-up circuit depicted in Fig. 3.10 ensure even the functionality during phase shedding procedure. In fact, all cells are started up all together during the precharging mode, and if shaded, their flying capacitor are kept charged with a pulsed charged.

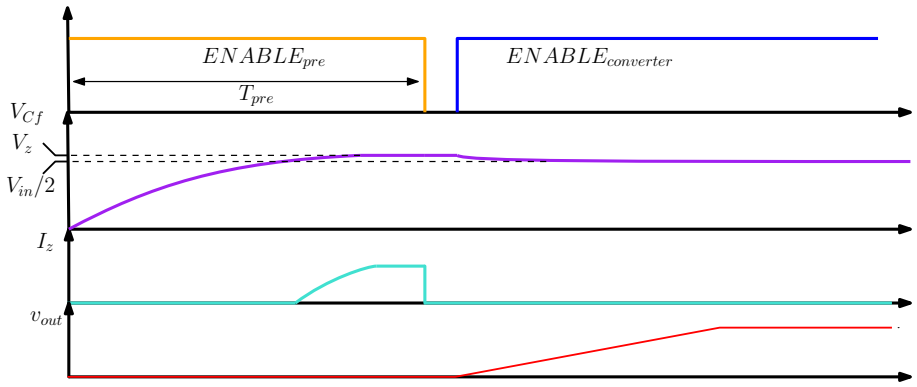


FIGURE 3.11: Conceptual Startup waveforms of the circuit reported in Fig. 3.10.

3.5 Coupling inductor in HBPS-QR

Fig. 3.12(a) shows the proposed coupled-inductor scheme for HBPS-QR with double current rectifier, where M is the coupling inductance between the output inductances that represents the coupling effect and L_0 is the self inductance. Because the coupling inductor effect between the two output inductances cannot be considered as two individual inductors, as described in [85] [86] [87], the electrical model of coupled-inductor is equivalent as in Fig. 3.12 where $L = L_0 - M$.

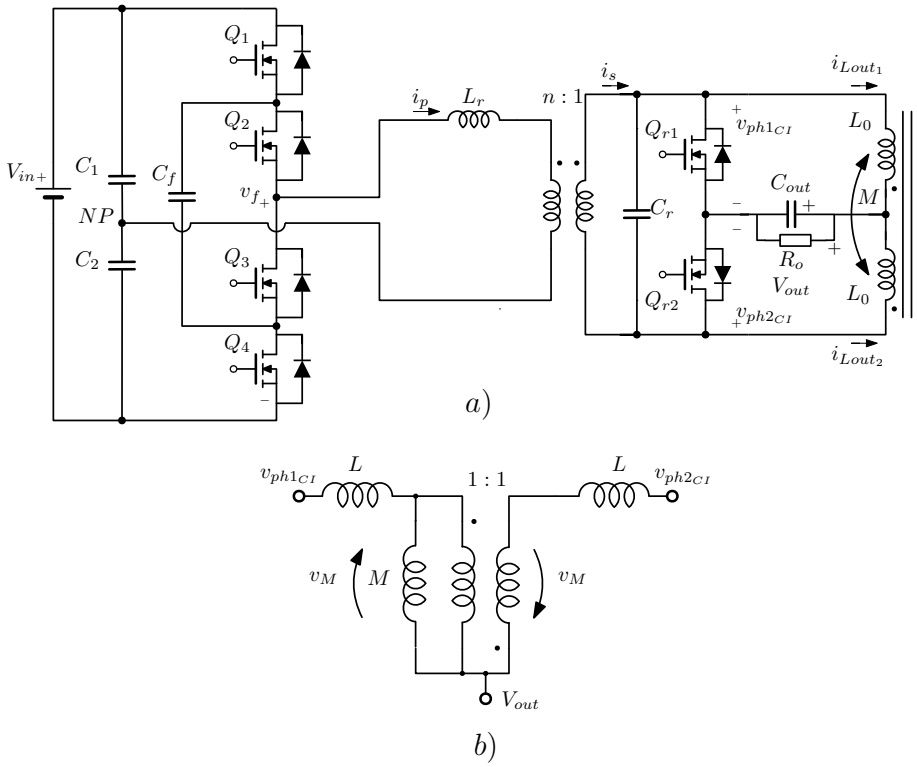


FIGURE 3.12: HBPS-QR multilevel with coupling inductor double current a) 380 V VRM schematic with coupled inductor double current, (b) equivalent electrical circuit for coupled inductor.

The analysis of coupling inductor in HBPS-QR is carried out considering the converter in $Mode\ A$ and the switching configuration as depicted in Fig. 3.3(d), corresponding at subinterval $t_3 - t_4$, where the resonance between L_r, C_r and $L_{out_{CI}}$ (i.e. the equivalent output inductance for the current doubler coupling inductor) takes place. Now the analytical expression of $v_{ph_{1_{CI}}}$ considering the coupling inductor is given by the following equation:

$$v_{ph1_{CI}}(t) = \frac{V_{out}L_r\left(1+\frac{M}{L+M}\right)+\frac{nV_{in}L_{out_{CI}}}{2}}{L_r+n^2L_{out_{CI}}}\left(1-cos(\omega_{r_{CI}}(t-t_3))\right), \quad (3.18)$$

were the equivalent output inductance for the resonant tank in coupled inductor current doubler is $L_{out_{CI}} = \frac{L^2+2\cdot L\cdot M}{L+M}$, whilst the resonant angular frequency is $\omega_{r_{CI}} = \sqrt{\frac{L_r+n^2L_{out_{CI}}}{L_{out_{CI}}L_rC_r}}$.

Averaging $v_{ph1_{CI}}(t)$ over the switching period T_{sw}, the output voltage V_{out} is given by:

$$\frac{V_{out}}{V_{in}} = \frac{V_{out}L_r\left(1+\frac{M}{L+M}\right)+\frac{nV_{in}L_{out_{CI}}}{2}}{L_r+n^2L_{out_{CI}}}\frac{f_{sw}}{f_{r_{CI}}}, \quad (3.19)$$

where $f_{r_{CI}} = \omega_{r_{CI}}/2\pi$.

Considering the converter in $Mode\ A$ and the switching configuration as depicted in Fig. 3.3(d), corresponding at subinterval $t_3 - t_4$ the following equations are valid for the current doubler coupling inductor:

$$L\frac{di_{L_{out1}}}{dt} = v_{ph_1} - v_{out} - v_M, \quad (3.20)$$

where $v_M = \frac{M}{L+2M}v_{ph1_{CI}}$.

Thus, expression for the current increment of $i_{L_{out1}}$ during subinterval $t_3 - t_4$ in $Mode\ A$ is derived by substituting eq. (3.20) into eq. (3.19):

$$\triangle I_{Lout1_{t_3-t_4}CI} \approx \frac{1}{f_{r_{CI}}L}\left(\frac{V_{out}L_r\left(1+\frac{M}{L+M}\right)+\frac{nV_{in}L_{out_{CI}}}{2}}{L_r+n^2L_{out_{CI}}}\left(1-\frac{M}{L+2M}\right)-V_{out}\right). \quad (3.21)$$

Equation 3.21 is derived considering double current implemented with coupled inductor, whilst the incremental current component during the power phase (subinterval $t_3 - t_4$), obtained considering non-coupled inductors, is given by the following equation:

$$\triangle I_{Lout1_{t_3-t_4}} \approx \frac{1}{f_rL_{out}}\left(\frac{V_{out}L_r+\frac{nV_{in}L_{out}}{2}}{L_r+n^2L_{out}}-V_{out}\right). \quad (3.22)$$

In order to make fair comparisons, the converter with non-coupled and inverse coupling inductors is kept as similar as possible. Designing both converters with the same transient equivalent inductance (i.e. L_{out}, in non-coupled double current referred to Fig. 3.1), and keeping the same switching

frequency, increasing C_{res} in the non-coupled converter due to lower equivalent inductance for the resonant tank, as reported in Fig. 3.13. Considering $M > L$ it is possible to demonstrate analytically that the current ripple in the current-doubler coupling inductor is slightly half compared with non-coupled configuration. From eqs. (3.2), (3.19), (3.21) and (3.22) the following expression is always true:

$$\frac{\triangle I_{Lout1_{t_3-t_4}CI}}{\triangle I_{Lout1_{t_3-t_4}}} \approx \frac{1}{2}, \tag{3.23}$$

as graphically demonstrate also in Fig. 3.13. Furthermore, coupling inductor offers unique advantages over non-coupled inductor in a HBPS-QR. As previously reported the equivalent output inductance for the resonant tank is higher compared with the equivalent transient inductance. Thus, and considering the same switching frequency for both solutions, by reducing the resonant time for non-coupled configuration, the coupling inductor configuration gives higher current capability (in section 2.3.2 are reported the current capability concept for FBPS-QR) than is reachable using non-coupled configuration. This is a unique advantage that gives higher dynamic performance and also higher efficiency in entire load range adopting coupled inductor in HBPS-QR.

Finally as described in section 2.3.2 it is possible to derive the relation between the maximum output voltage V_{out}, obtained at the maximum switching frequency expressed by eq. (2.15), and the converter output current I_{out} using coupling inductor for the current doubler. This relation is denotated as $current\ capability\ V_{out,max}(I_{out})$ which indicates the maximum theoretical power capability for a given converter parameters. To derive the relation $V_{out}I_{out}$ for HBPS-QR (would be the same for FBPS-QR) implemented with coupling inductor it comes useful to highlight the differences between HBPS-QR implemented with and without coupling-inductor. Firstly, as depicted in Fig. 3.13, for a fixed switching frequency for both coupling and non-coupling solution, the resonant time is $150\ ns$ less in coupling inductor solution which gives an important advantages since the degradation of the resonant voltage depends from both the on-time (T_{sh}) and the resonant time (T_{res}). Lower resonant time gives higher current capability, since the RMS value for both resonant transition is the same. Secondary, the pre-charging time, equation (2.9) for FBPS-QR, required to increase the secondary current i_s from $-nI_{cir_{HB}}$ to $i_{Lout1}(t_4)$, i.e. when the resonant transition starts, is higher in coupling inductor topology. In fact, combining equation (2.9) with equation (3.23) it is possible to derive the pre-charging time for HBPS-QR implemented with coupling inductor:

$$T_{ch} \approx (nI_{cir_{HB}} + \frac{I_{out}}{2} - \frac{\Delta I_{Lout_{NC}}}{4})\frac{2L_r}{nV_{in}}. \tag{3.24}$$

The last important difference between coupled and non-coupled current doubler is the maximum voltage for the resonant voltage that can be analytically described from the following equations:

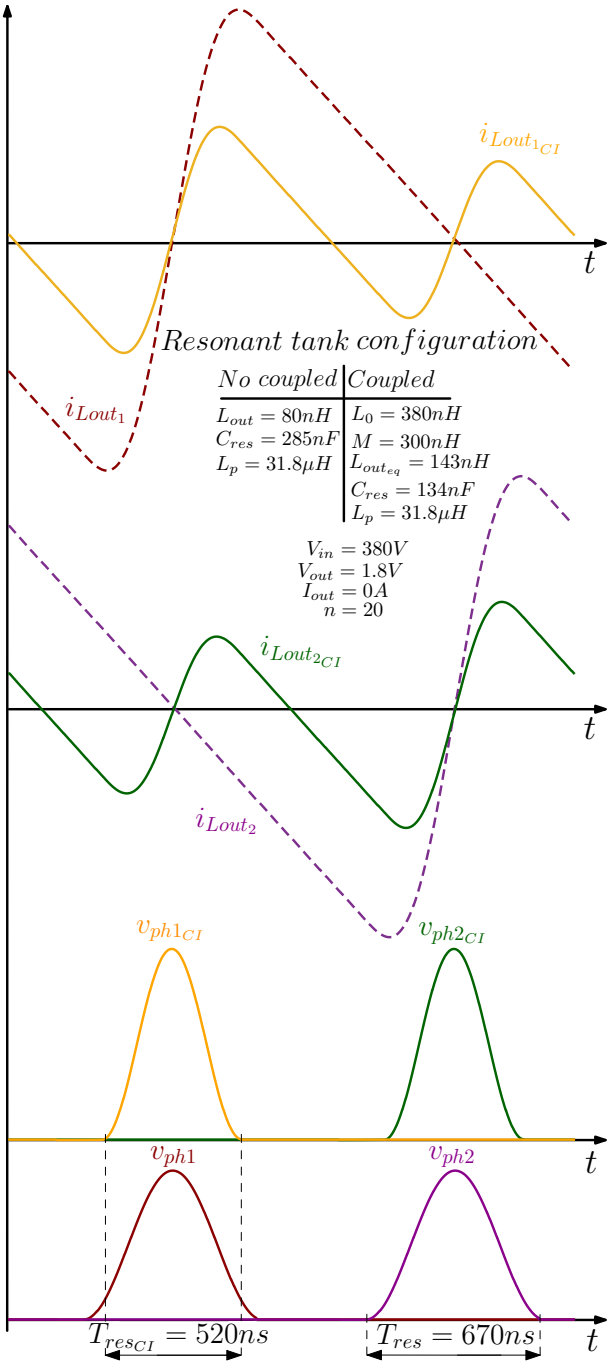


FIGURE 3.13: Inductor current waveforms with a without coupling inductor maintaining the same switching frequency and same equivalent transient inductance, simulated with Simplis.

$$V_{peakNCI} = 2\frac{V_{out}L_r + \frac{nV_{in}L_{out}}{2}}{L_r + n^2 L_{out}}, \tag{3.25}$$

$$V_{peakCI} = 2\frac{V_{out}L_r\left(1 + \frac{M}{L+M}\right) + \frac{nV_{in}L_{outCI}}{2}}{L_r + n^2 L_{outCI}}. \tag{3.26}$$

Since $L_{outCI} = L_{out}$ it follows that $V_{peakCI} > V_{peakNCI}$.

Considering the differences between coupling a non coupling inductor, equation (3.24) and the demonstration of *current capability* described in section 2.3.2, it is possible to derive the graph in Fig. 3.14. In Fig. 3.14, in blue, is depicted the current capability (maximum output voltage V_{out} obtained at the maximum switching frequency, as a function of the converter output current I_{out}) for the coupled solution compared at the same V_{out} in no-load condition for both current doubler rectifier. From Fig. 3.14 it follows that the current capability for coupled inductor configuration is higher for almost all entire load. Another advantages of HBPS-QR implemented with coupled-inductor is that the converter works in $Mode\ A$ until 20A. This is of paramount to consider since the efficiency degradation at medium and high load mainly depends from the higher switching frequency and also from the RMS current in the output inductances. With coupling inductor it is possible to mitigate both effects reaching higher efficiency in all operating loads.

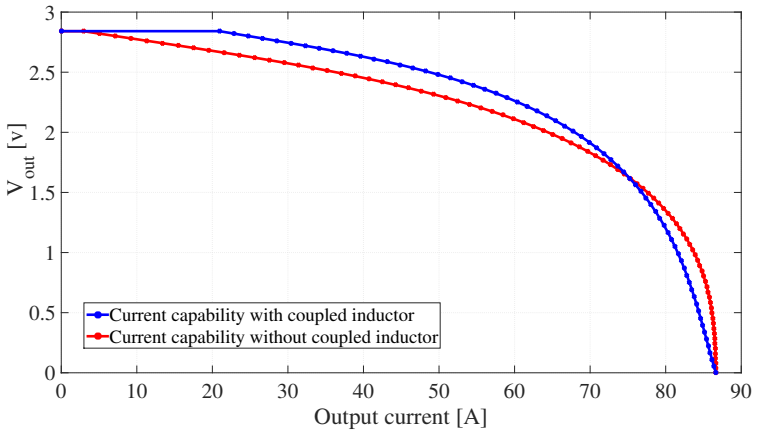


FIGURE 3.14: Current capability: maximum output voltage V_{out} obtained at the maximum switching frequency, as a function of the converter output current I_{out}, comparison between coupled and noncoupled inductor configuration.

Furthermore, it is interesting to notice in Fig. 3.14 how the degradation of the output voltage is faster in coupling inductor configuration. This is due to lower resonant time for coupled inductor solution. In general this behaviour does not affect the coupling inductor capability since the maximum current for each cell is around 60-70A.

Finally, from Fig. 3.15 it is possible to derive the relation between V_{out} and I_{out} as a function of switching frequency f_{sw}. As obtained in Fig. 3.15, in coupled inductor solution all the curves are almost flat for a wider range

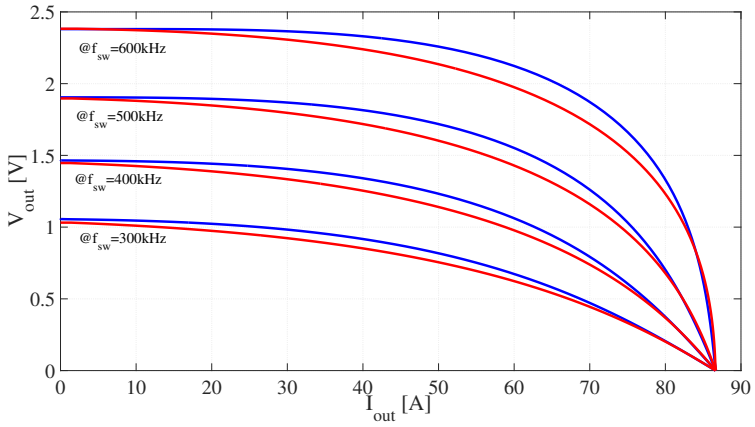


FIGURE 3.15: Possible operating points at fixed frquency. Comparison between noncoupled (red) e coupled (blue) indcutor.

of output current comparing with non-coupled solution. Thus, the regulation of the output voltage is obtained with a small frequency variation in coupled inductor. This is an important property that gives higher dynamic performance even if the equivalent output inductance is the same for both solution.

3.6 Design of HBPS-QR

There are several ways to design the proposed HBPS-QR converter. In general there are not a specific design flow to make the best solution, since the converter proposed in this research is slightly complicate. In this section is carried out a general procedure useful from the design point of view and even useful to clarify how this converter is definitely a best solution as HV POL with high dynamic performance. Before proposing a design example, are specified the main losses which affect HBPS-QR and layout consideration. Moreover at the end of this section there will be demonstrated the robustness of the proposed HBPS-QR.

3.6.1 Losses in HBPS-QR and design layout consideration

HBPS-QR is in ZVS both at primary side and secondary side and the transformer core losses depends from the resonant voltage and frequency.

As previously highlighted the proposed converter are under ZVS turn-on, however if the driver is not as much fast there will be a turn-off MOSFETs losses of each leg. The model of estimation of the turn-off losses is slightly complicated and depends on many factors, however if strong driver are used these losses can be reduced near zero.

Gate losses can be estimated according with [88] using the following equation:

$$P_{gate} = V_g \cdot Q_g \cdot f_{sw}, \tag{3.27}$$

where V_g is the gate voltage and Q_g the total gate charge.

As a transformer based topology, HBPS-QR is affected by core losses, which can be estimated using Steinmetz's equation [89]:

$$P_{core} = k \cdot Vol \cdot B_{pk}^{\beta} \cdot f_{sw}^{\alpha}, \tag{3.28}$$

where k, β and α can be estimated form the core material datasheet. To calculate the peak magnetic flux when the converter is in $Mode\ A$ are needed the following equation:

$$B_{pk} = \frac{\int_{t_3}^{t_3+T_{res}} v_{ph(t)dt}}{2 \cdot A_e} \tag{3.29}$$

where A_e is the equivalent core cross section area.

3.6.2 Design procedure

Step 1

Firstly it is important to clarify the specification of the converter such as: total occupation area of the converter A_{tot}, maximum output current $I_{out_{max}}$, output voltage range, output voltage tolerance band and maximum load slew rate.

Step 2

The rectifier current doubler of the converter proposed in this work and depicted in Fig. 3.1 is composed by two MOSFETs. To select the number of the MOSFET for each phases at secondary side it is important to consider the $R_{ds_{ON}}$ of the MOSFET. Thus, has highlighted, the resonant behaviour is the main limitation of the proposed solution because higher voltage MOSFETs are needed, therefor the voltage peak is established by the technology. To mitigate this issue more rectifier MOSFETs in parallel are placed finding the optimal number between power density, gate driver losses and conduction losses.

$$V_{ph_{PK}} = 2\frac{V_{out}L_r + \frac{nV_{in}L_{out}}{2}}{L_r + n^2 L_{out}} \approx \frac{V_{in}}{n}. \tag{3.30}$$

Thus, the minimum transformer ratio, considering the MOSFET's technology constrain ($V_{ph_{pk}}$) is given by the following equation:

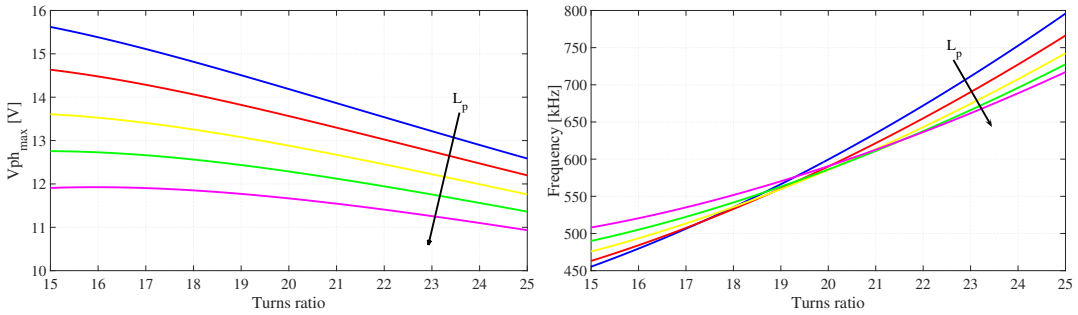
$$n_{min} \approx \frac{V_{in_{MAX}}}{V_{ph_{pk}}}. \tag{3.31}$$

Equation (3.31) is not always a consistent approximation. Considering eq. (3.30) it is possible to generate the graph in Fig. 3.16(a). Hence, equation (3.31) does not give an adequate simplification. In fact, the dependence of the peak voltage with the primary inductance is considerable. But actually is acceptable as second step for designing the converter.

Step 3

HBPS-QR is mainly designed to ease the transformer design as an evolution from FBPS-QR converter. However, still, the transformer needs to be carefully designed because it affects the performance both at primary and secondary side of the converter. From eq. (3.31) the constrain on the minimum transformer turns ratio is given considering the maximum voltage on the secondary MOSFETs selected. To calculate the maximum transformer turns ratio the following consideration can indirectly define its value.

In general, in HBPS-QR converter the switching frequency depends mainly on the transformer turns ratio. From Fig. 3.16(b) and eq. 3.2 it follows that the impact of the turns ratio on the switching frequency is a first order effect. Thus, it is possible to derive the maximum turns n_{max} ratio from the maximum switching frequency specification.



(a) (b)

FIGURE 3.16: a) variation of the maximum resonant voltage on secondary side $V_{ph_{max}}$ vs turns ratio, b) variation of the switching frequency vs turns ratio, based on the parameters reported in Table 3.2 except for L_p ($L_p(blue) = 20\mu H$, $L_p(red) = 24\mu H$, $L_p(yellow) = 29\mu H$, $L_p(green) = 34\mu H$ and $L_p(magenta) = 39\mu H$).

From (2.56) the critical inductance relationship for HBPS-QR $L_{crt_{HBPS-QR}}$ is given by the following equation:

$$L_{crt_{HBPS-QR}} = \frac{\frac{\pi}{2}\left(\frac{nL_{out}V_{in}}{2} + V_{out}L_p\right)}{f_r\left(L_p n^2 L_{out}\right)\Delta I_{out}\omega_c} \approx \frac{\pi V_{in}}{4 f_r L_p n_{max}\Delta I_{out}\omega_c}, \tag{3.32}$$

where $f_r \approx 4f_{sw_{min}}$ as a conceivable approximation, whilst ω_c depends from the loop bandwidth that can be $\omega_c = 2\pi 70k$.

Consequently, considering eq. (3.32), the maximum turns ratio limits the transient response of the converter.

Step 4

After selected the turns ratio of the transformer and the maximum output inductance it is possible to calculate the primary inductance. Considering

equations (3.30) and approximating $V_{out}L_r << \frac{nV_{in}L_{out}}{2}$, the primary inductance can be calculated using the following relation:

$$L_p \approx \frac{nL_{out}V_{in}}{V_{ph_{max}}} - n^2 L_{out}. \tag{3.33}$$

Finally, to obtain the resonant capacitance C_{res} a good rule of thumb is to derive it from the minimum switching frequency and obtain C_{res} from eq. (3.2).

Thus, all the resonant tank parameters are selected and it is possible to calculate the current capability from eq. (3.9), as done for FBPS-QR in section 2.3.1. Using the parameters of Table 3.2, several capabilities are reported in Fig. 3.17. Firstly, it is essential to verify that the converter has not a wide output peak current range, adopting nominal resonant tank parameters with different input voltage. The actual peak current variation for different input voltages are depicted in Fig. 3.17(a), thus the peak current variation is around 18 A. The purpose of this graph is to underline how the switching frequency can change significantly at different input voltages.

Fig. 3.17(b) shows the comparison between capability using nominal tank components and worst case, when all tank components are at their maximum value (i.e. all resonant tank components have an high tolerance between 10% to 20%). As reported in Fig. 3.17(b) the actual peak current in the worst case should not be inside the VRM constrains which typically is around 50 A to 60 A for each cell.

To design HBPS-QR converter it is important to be confident with the effect on the current capability caused by the variation of the resonant tank parameters. The capability variation with different resonant capacitance C_{res} are outlined in Fig. 3.17(c), thus, high value of C_{res} can change considerably the maximum switching frequency in light load, since the converter can supply higher voltage with higher C_{res}. Moreover, high value of C_{res} can slightly increase the maximum output current but on the other hand this actually makes higher frequency variation on the entire output current load, resulting in worse dynamic response. Fig. 3.17(d) reports the capability variation at different resonant inductance L_p which yields two important informations: the actual output voltage does not change consistently, thus the resonant transition in $Mode\ A$ is not affected by the inductance value. On the other hand, the maximum current depends on the primary inductance value because the pre-charging time. Instead L_{out} variation, on the current capability, produces two main effects: switching frequency variation and maximum current capability as reported in Fig. 3.17(e). Finally considering the on-time variation T_{on} on the current capability, Fig. 3.17(f), it follows that it does not affect the maximum output current. Instead, T_{on} is an important parameter to achieve ZVS condition at primary side.

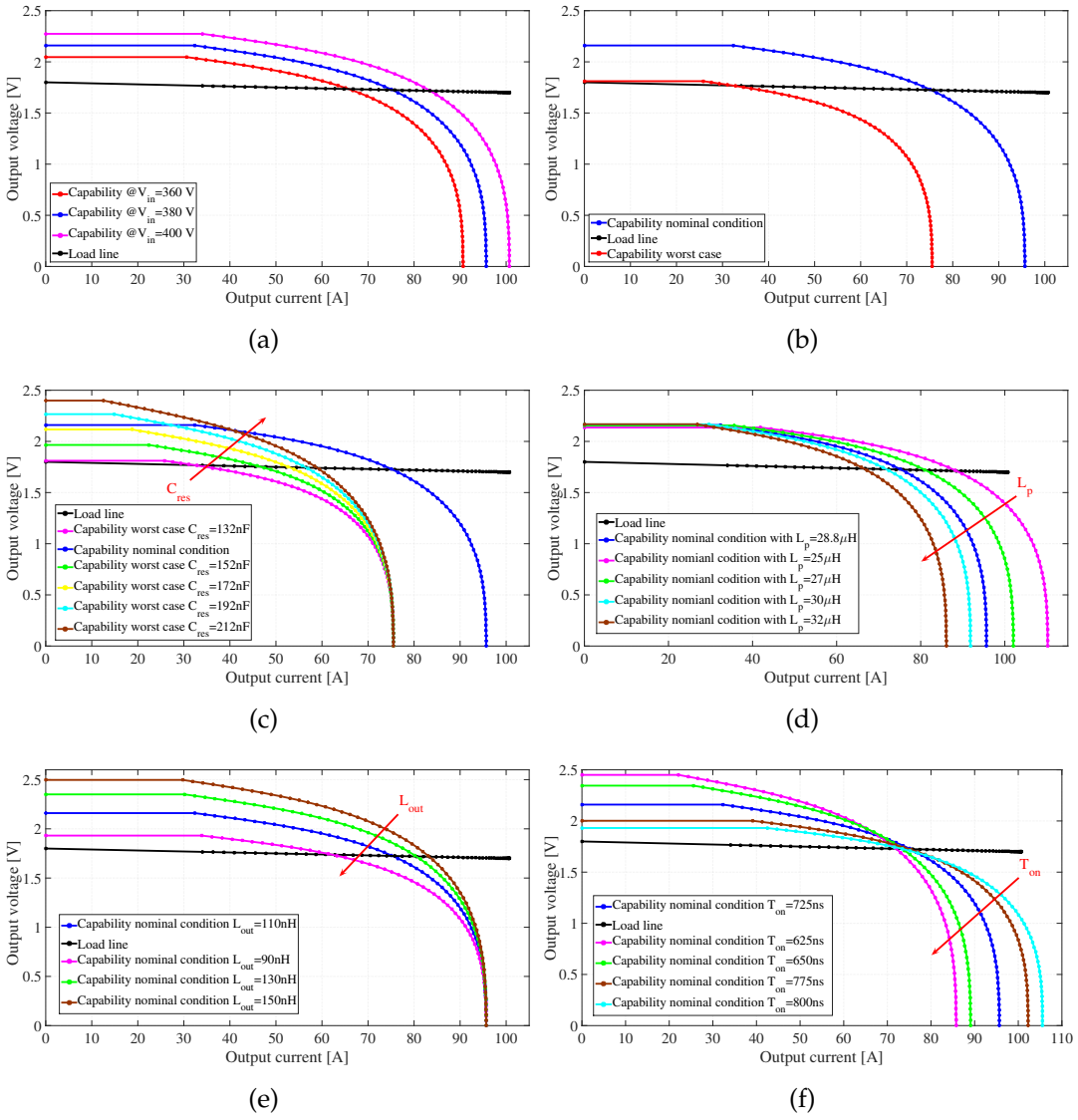


FIGURE 3.17: Capabilities for different scenarios using the value from Table 3.2: a) capability comparison with nominal parameter for resonant tank at different input voltage V_{in}, b) capability comparison from the nominal condition and worst case as input voltage and resonant tank parameters ($L_{out} = L_{out_{nom}} * 0.8$, $L_p = L_{p_{nom}} * 1.2$, $C_{res} = C_{res_{nom}} * 0.9$ and $V_{in} = 360V$), c) capability comparison in nominal condition with different resonant inductance C_{res}, d) capability comparison in nominal condition with different resonant inductance L_p e) capability comparison in nominal condition with different resonant inductance L_{out} and f) capability comparison in nominal condition with different on-times T_{on}

Step 5

In section 3.2 the actual ZVS transition has been explained and the benefit of HBPS-QR in such techniques. In this dissertation has been widely discussed how to improve the zero voltage range by using HBPS-QR resonant converter, however some important design equations have not reported yet. As before explained in Fig. 3.7(c) and 3.7(d) the key of zero voltage switching is the amount of energy stored in the resonant inductance L_p versus the energy required to charge and discharge the circuit capacitances formed by two parasitic capacitance $2C_{oss}$. To improve the ZVS capability there are three key techniques: chose MOSFETs with less parasitic output capacitance C_{oss}, increase the primary inductance L_p and increase the actual current before ZVS transition [90]. The energy needed for ZVS is required at the end of the free-wheeling phases (t_0-t_1 and t_6-t_7) as reported in Fig. 3.18(a), where the actual current which performs ZVS transition is $I_{cir_{HB}}$, obtained from eq. (3.4). However there are other two ZVS transitions (t_5-t_6 and t_{11}-t_{12}) where the current, which ensure ZVS operation is not $I_{cir_{HB}}$, but actually is the primary current at $t = t_5$ or $t = t_{11}$, which is slightly less than $I_{cir_{HB}}$, as highlighted in section 3.1.1. Moreover, since the circuit during the ZVS transition is a resonant circuit, as reported in Fig. 3.7(d), its resonant frequency may be useful to estimate the dead time.

$$f_{res_{ZVS}} = \frac{1}{2\pi\sqrt{2L_pC_{oss}}}. \tag{3.34}$$

The time condition for achieving ZVS is one fourth the resonant period $T_{res_{ZVS}}$, obtained in eq. (3.34). Hence, dead time is given by the following equation:

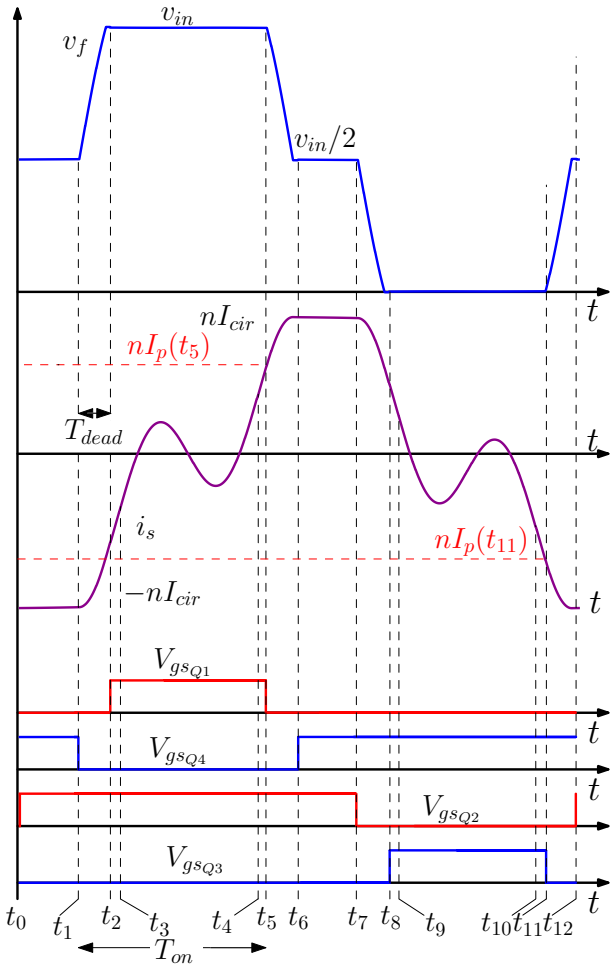
$$T_{dead} \geq \frac{\pi\sqrt{2L_pC_{oss_{avg}}}}{2}, \tag{3.35}$$

where $C_{oss_{avg}}$ is given by equation (2.68).

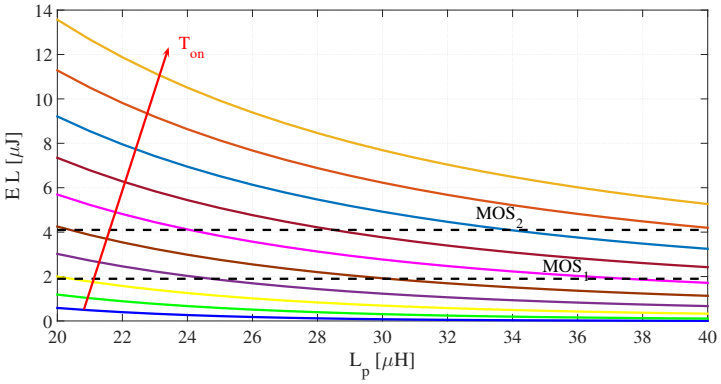
If we consider both energy and resonant time for ZVS transition, respectively eq. (3.10) and eq. (3.35), it follows that the leakage inductance can increase the energy for ZVS transition, on the other hand it increases the dead time required, which is not compatible in high switching frequency application as VRM. Thus, it is mandatory to chose low parasitic capacitance related MOSFETs. Furthermore, it is also important to consider the amplitude of the resonant voltage transition during ZVS phase which depends from the primary current stored in the resonant inductance and the LC network's characteristic impedance. Considering the worst case at $t = t_5$ or $t = t_{11}$, the following relation is mandatory to reach ZVS transition in all conditions.

$$I_p(t_5) \approx |I_p(t_{11})| > \frac{V_{in}}{2}\sqrt{\frac{2C_{oss_{avg}}}{L_p}} \tag{3.36}$$

Note that equation (3.36) is the same as eq. (3.10), however it estimates the actual energy for ZVS transition in the worst case. In order to find out the



(a)



(b)

FIGURE 3.18:
Actual ZVS operation: a)Main waveforms during ZVS transitions b) the actual energy store in L_p at $t = t_5$ or $t = t_{11}$ (worst case) for different T_{on} (from $625ns$ to $850ns$), in black the predicted energy required, for MOS_1 (BSZ42DN25NS3) and MOS_2 (BSZ16DN25NS3) to ensure ZVS transition.

optimal condition for ZVS operation, keeping low RMS at primary side, it is essential to derive the primary current at $t = t_5$ from the following equation:

$$I_p(t_5) \approx -I_p(t_{11}) \approx I_{cir_{HB}} - \frac{V_{in} T_{dead}}{2L_p} \tag{3.37}$$

In Fig. 3.18(b) are depicted the energy stored in the resonant inductance at $t = t_5$ or $t = t_{11}$ in function of primary inductance L_p at different T_{on} (from $625ns$ to $850ns$). Fig. 3.18(b) gives a general understanding regarding the impact of the primary inductance and the on-time on the ZVS capability, considering also its effect on the dynamic response.

Step 6

The basic operating principles discussed in Section 3.1.1 are based on the assumption that the flying capacitor is balanced to half of the input voltage, keeping a DC value.

The peak to peak capacitor voltage ripple is given by:

$$\begin{aligned} \Delta V_{C_f pk-pk} &= \frac{I_{cir_{HB}} \left(\frac{T_{sw}}{2} - T_{on}\right)}{C_f} \\ &= \frac{\left(\frac{V_{in}}{2} T_{on} - n V_{out} T_{sw}\right) \left(\frac{T_{sw}}{2} - T_{on}\right)}{2 L_p C_f} \end{aligned} \tag{3.38}$$

where $I_{cir_{HB}}$ is given by eq. (3.4).

To keep a small voltage ripple, a large enough flying capacitor must be selected. For lower switching frequency the flying capacitor requirement needs to be larger increasing the occupation area of the converter. Moreover, an interesting proprieties of HBPS-QR is that voltage ripple is grater at zero load, because the converter is switching at lower frequency. Considering $C_f = 300\ nF$ and the switching frequency $f_{sw} = 400\ kHz$ and a circulating current $I_{cir_{HB}} = 750\ mA$, from Fig. 3.19, the voltage ripple on the flying capacitor is around 1.2 V, which is acceptable for the proposed topology. Another important concern about the flying capacitor comes at the start-up. After the pre-charging mode (Section 3.4) the converter starts to switch at low frequency for a normal operation of the start-up, causing high voltage ripple on the flying capacitor.

Small voltage ripple will ensure proper converter operation even during start-up procedure.

3.6.3 Robust design of HBPS-QR

In designing HBPS-QR, selecting proper values of primary inductance, output inductance and resonant capacitance are important for determining the performance of the system. As reported in Section 3.1.1 the circulating current $I_{cir_{HB}}$ is an important design parameter to validate the actual ZVS performance at primary side and actually it is strongly dependent on the resonant tank parameters. However, if the circulating current is too high, efficiency will be lower, as highlighted in Section 3.2. We need to create a model

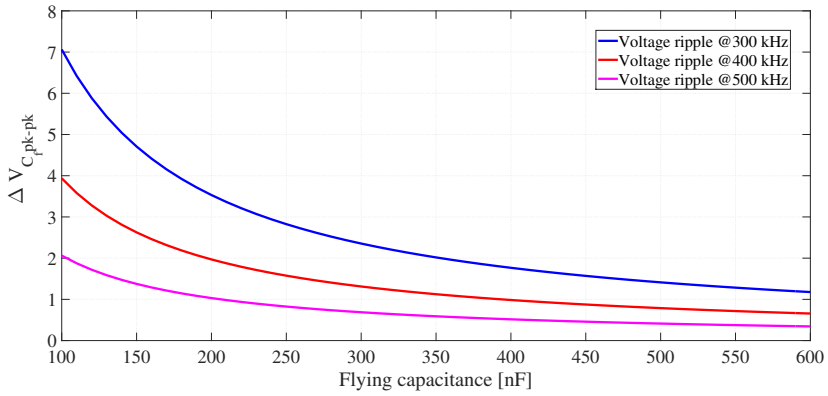


FIGURE 3.19: Flying capacitor voltage ripple varying flying capacitor capacitance with a fixed circulating current $I_{cir_{HB}} = 750mA$.

to predict the ZVS capability considering the tolerance of the resonant tank component and the input voltage range.

Before studying the hard switching behaviour it is important to define an accurate model for the voltage transition on each MOSFETs during ZVS operation.

Considering the equivalent resonant circuit during ZVS transition, depicted in Fig. 3.7(d), for HBPS-QR, it is possible to derive the behaviour of the resonant ZVS transition. Thus, with $I_{cir_{HB}}$ as stored current in L_p, the following expression in S-domain is obtained:

$$\begin{aligned} V_{ZVS}(s) &= \frac{1}{s \cdot C_{out_{eq}}} L_r I_{cir_{HB}} \frac{sC_{oss_{eq}}}{1 + s^2 C_{oss_{eq}} L_r} \\ &= \frac{\frac{1}{\omega_r} \cdot I_{cir_{HB}} \cdot \omega_r}{s^2 + \omega_r^2} \end{aligned} \tag{3.39}$$

where $C_{oss_{eq}} = C_{oss_{Q_1}} + C_{oss_{Q_4}}$ and $\omega_r = \sqrt{\frac{1}{L_r C_{osseq}}}$ is the resonant angular frequency of the resonant ZVS circuit.

From S-domain eq. (3.39), the time-domain one can be expressed as:

$$v_{zvs}(t) = \sqrt{\frac{L_r}{C_{out_{eq}}}} I_{cir_{HB}} \cdot sin\left(\omega_r (t - t_1)\right) \tag{3.40}$$

If the circulating current is enough to discharge and charge the output capacitance of MOSFETs during ZVS operation, the turn-on does not presents hard switching event, supposing the right T_{dead} from eq. (3.35). On the contrary if the energy in the resonant inductance is not enough ($E_L < E_c$) there will be a certain level of hard switching, which can be obtained from the following equation:

$$V_{Hsw} = V_{in} - \sqrt{\frac{L_r}{C_{out_{eq}}}} I_{cir_{HB}}, \tag{3.41}$$

where equation (3.41) is derived from eq. (3.40).

From eq. 3.41 the hard switching voltage level can be plotted in Fig. 3.20(a), for different tank parameters, considering as nominal value: $L_r = 30\ \mu H$, $L_{out} = 220\ nH$, $C_{res} = 172\ nF$ (with transformer parasitic effect of $40\ nF$ on the resonant capacitance C_{res} i.e. $C_w = 100pF$ with turns ratio $n = 20$), $V_{out} = 1.8\ V$, transformer turns ration $n = 20$ and $V_{in} = 380\ V$ with the tolerance of 10% for the capacitance and 20% for inductance. The graphs in Fig. 3.20(a) and Fig. 3.20(b) are obtained considering the converter in $Mode\ A$. In almost all cases, ZVS can be achieved. The worst case occurs when the resonant tank components are at their maximum value and the input voltage is at its minimum value. Even if the hard switching occurs there will be a minor impact on the efficiency. This means that the tank resonance design is very robust for ZVS range, making the propose HBPS-QR converter suitable for the production.

Finally it is also relevant to calculate the ZVS capability at different input voltage. In Fig. 3.20(b) are reported the hard switching voltage level for different input voltages, supposing nominal resonant tank parameters. From Fig. 3.20(b) it follows that the impact on the ZVS capability at different input voltages has a minor impact on the ZVS functionality. This is a paramount important to consider since the 380 V bus presents an important voltage variation.

3.6.4 Driving system

The top-level view of the driver architecture is reported in Fig. 3.21, where each cell are driven by 3 drivers, one for the rectifier MOSFETs and two for the multilevel half-bridge.

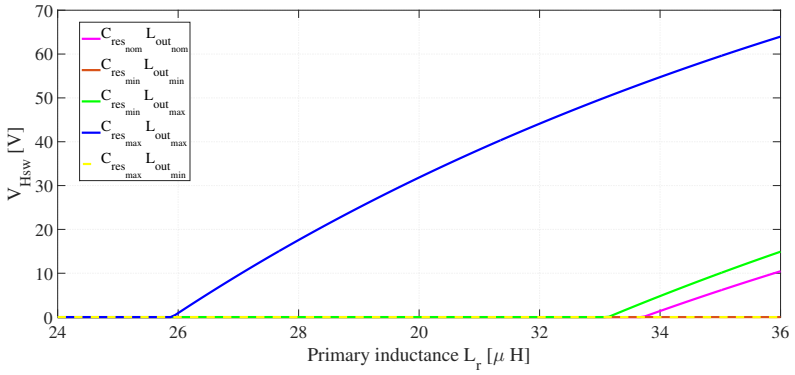
At primary side the circuit is made by two isolated driver (SI827X) whom have to ensure an high common mode transient immunity [91]. Common mode transient immunity (for SI827X is $350KV/\mu s$) is an important parameter, of a isolated gate driver, to consider, especially when operating at high frequency as in the proposed converter. Fig. 3.21 shows that there are three floating domains with a voltage slew rate of 190 V during the dead time (around 100ns). The most noticeable drawback of the proposed driving system is that Q_1 gate's supply has two diodes in between the voltage driver supply and the auxiliary supply.

At secondary side the driver ensure ZVS transition, as described in section 3.1.1, by observing the resonant voltage of each phase.

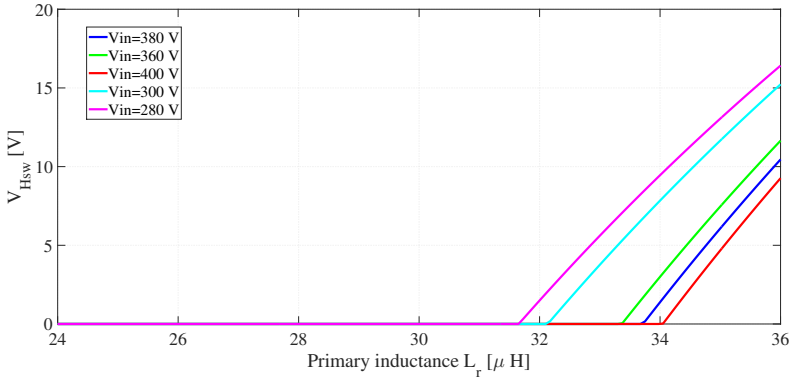
3.7 Experimental Results HBPS-QR 380 V VRM

The proposed system has been tested for VRM application. This section presents the experimental results.

As shown in Fig. 3.22 a test board with 2 cells and $I_{out} = 120A$ has been realized to experimentally validate the performance of proposed topology. The total space of the test board is $44mmX43mm$. The primary side half-bridge multilevel is implemented with BSZ42DN25NS3. The secondary side



(a)



(b)

FIGURE 3.20: Modeled hard switching voltage considering: a) resonant tank tolerance, b) variation of the input voltage.

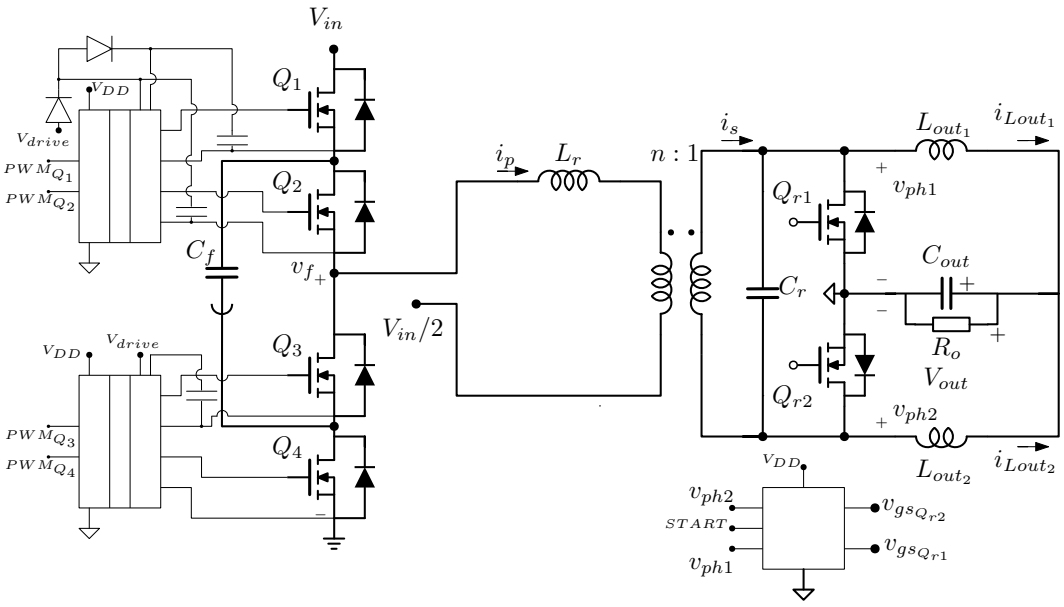


FIGURE 3.21: Driving system at primary and secondary side.

are FDMC8010. The main passive elements parameters are as follows: $L_r = 28.8\mu H$, $L_{out} = 220nH$ (FP1008R1-R220-R), $C_r = 176nH$ and the transformer is constructed by planar core (E22/6/16 FERROXCUBE 3F4) with a turns ratio of 20:1. The switching frequency is about 440 kHz for each phase.

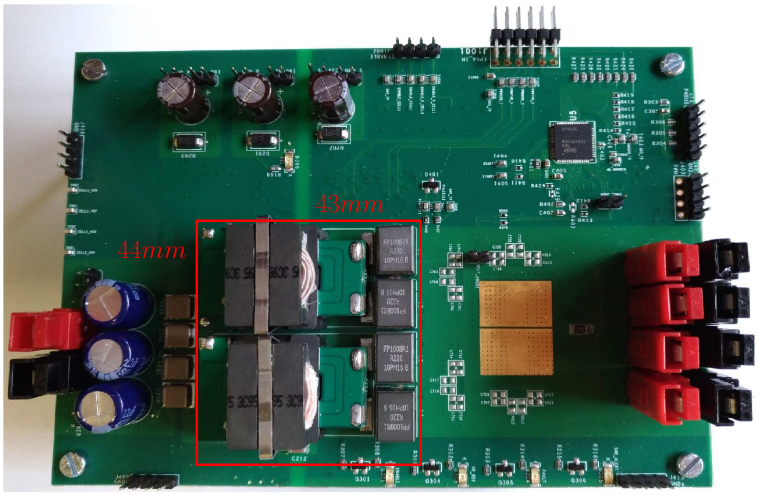


FIGURE 3.22: Test board VRM from 380V to 1V8 with noncoupled inductor.

Efficiency measurements, including converter and driving losses, at nominal output voltage $V_{out} = 1.8V$ and $V_{in} = 380V$, are shown in Fig. 3.23. Moreover, to demonstrate the wide input range operating condition, is reported in Fig. 3.23 the efficiency at nominal output voltage $V_{out} = 1.8V$ and $V_{in} = 360V$. The peak efficiency is equal to 93% and it is maintained high by using phase shedding. Comparing with the two stage approach, the overall efficiency is higher in a 380 V VRM in the all entire operating load, especially in light load, where, in the two stage approach the overall losses are dominated by the first stage (7W at no load in the IBC [27] whilst the proposed solution is 2.2W).

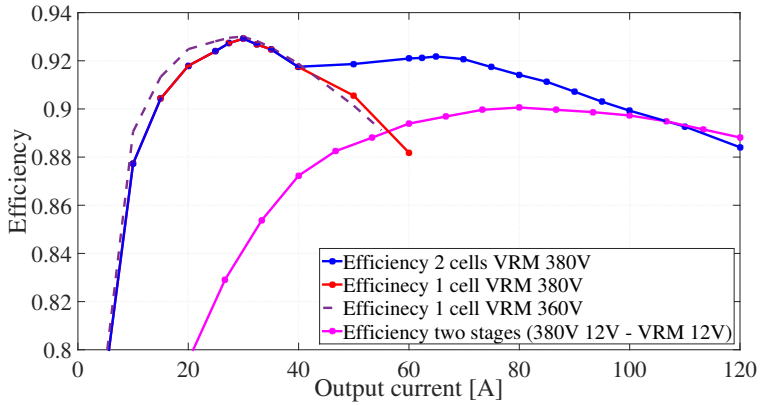


FIGURE 3.23: Total system efficiency: in red for 1 cell VRM 380V single stage proposed, in blue 2 cells VRM 380V single stage proposed, in magenta for the two stages approach (data from [27] and [23]) and in violet dashed line for 1 cell VRM 360 V single stage.

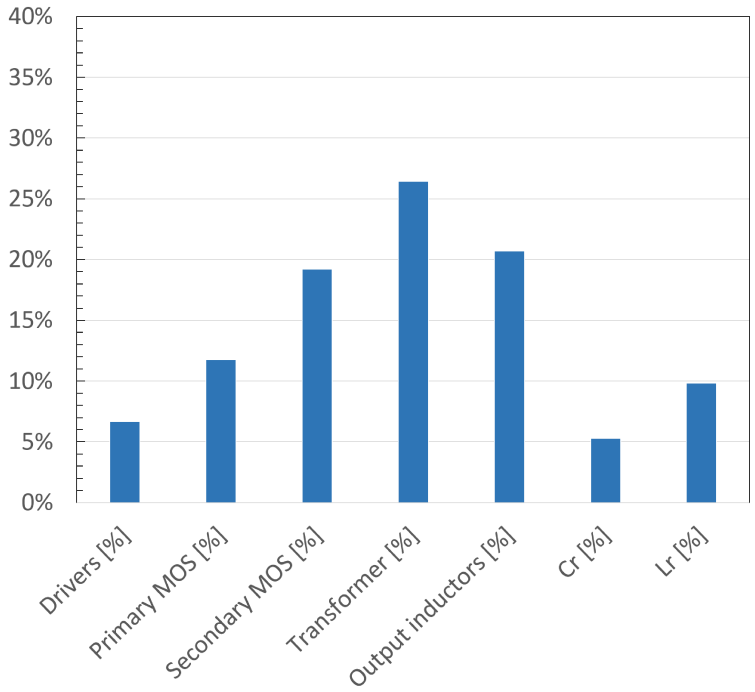
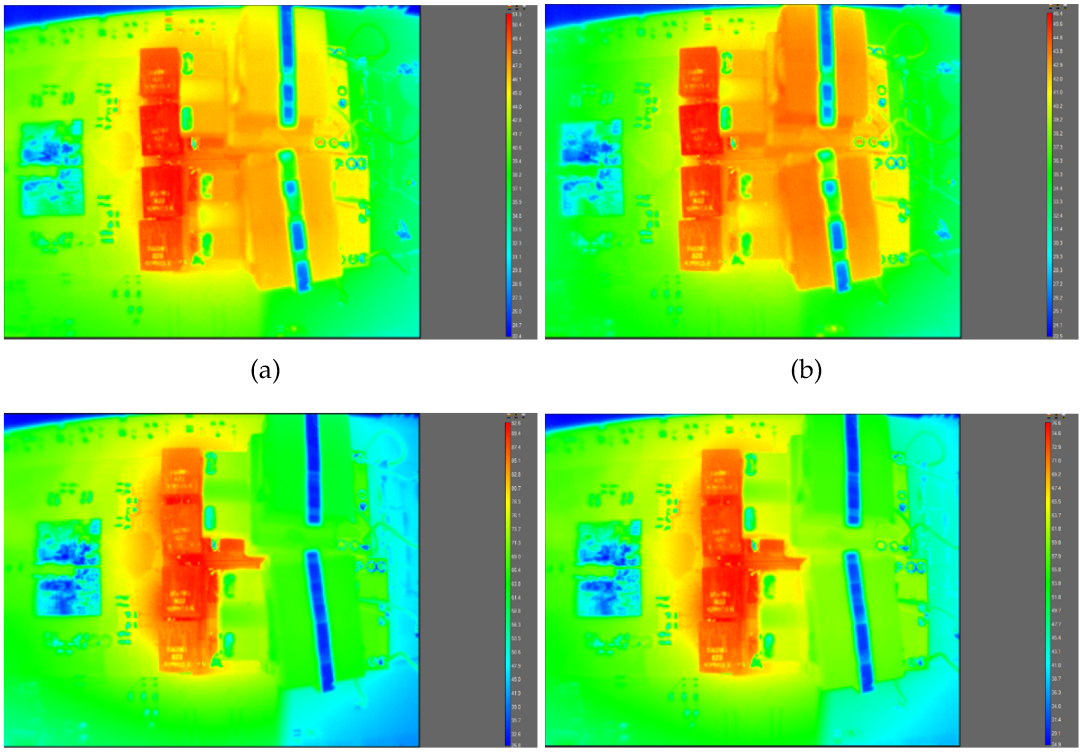


FIGURE 3.24: Loss breakdown of the single cell at the peak efficiency point.

It is also interesting to compare our proposed solutions: 48 V VRM based on FBPS-QR topology presented in section 2.3 and 380 V VRM HBPS-QR; the second one has higher efficiency in light load due to lower copper losses at the primary side. Moreover, the power density achieved with the proposed converter is better than the two-stage solution reported in [23] and [27], where the total occupation area is $2004mm^2$, whilst the proposed solution is $1892mm^2$.

The single-cell loss breakdown at the peak efficiency (i.e. at I_{out} = 30A) is shown in Fig. 3.24. The losses are evaluated analytically and they match the experimental measurements with an error of 20%. As can be seen in Fig. 3.24, the major contribution is coming from the transformer, where the conduction losses are dominant, and from the other magnetic elements. Moreover, the loss contribution of the output synchronous rectifier is relevant. The only significant loss among all the capacitors is the resonant capacitor one but having adopted COG dielectric the ESR value is kept low. The current flowing in the flying capacitor C_f is the recirculating current (i.e. typically $I_{ric} = 500mA$) while in C_1 and C_2 are interested by half of the primary current (i.e. at maximum load the primary RMS current is closed to 1.4 A).

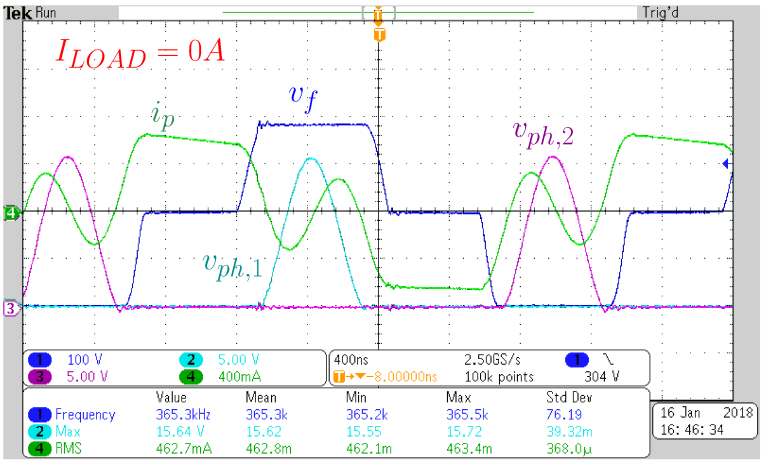
In Fig. 3.25 are reported the thermal images at different load, to validate the thermal performance of the proposed converter. As can be seen the main contribution of the losses comes from the output inductances, whilst the transformer maintains almost the same temperature in all operating load around 50-60°C. Thus, from these thermal images, it is possible to validate the proposed 380 V VRM, since the losses are relevant on the high current side as 12 V VRM solution [23].



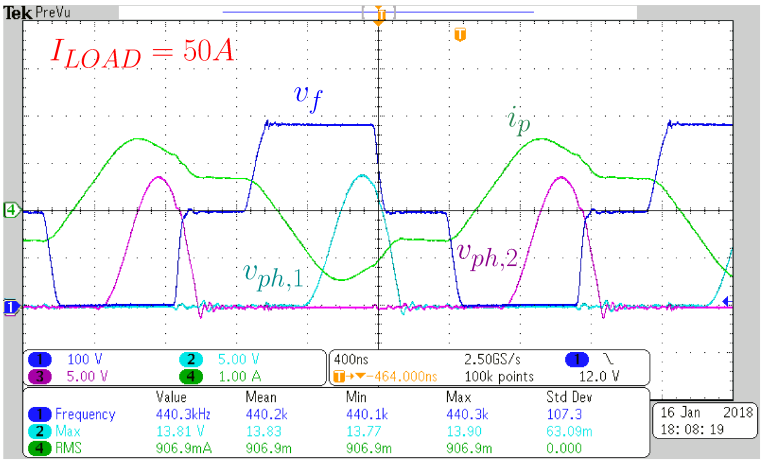
(a) (b)

(c) (d)

FIGURE 3.25: Thermal images at different load conidition for 2 phases prototype: (a) $I_{out} = 0A$, (b) $I_{out} = 30A$, (c) $I_{out} = 80A$ and (d) $I_{out} = 120A$



$a)$



$b)$

FIGURE 3.26: Main experimental converter waveforms: secondary resonant voltages at secondary side v_{ph_1} v_{ph_2}, primary voltage v_f and primary current i_p with a) at 0A of output current and b) at 50A of output current for one single cell.

In Fig. 3.26 the main experimental converter waveforms are reported, corresponding to the proposed HBPS-QR in light load Fig. 3.26(a) and high load Fig. 3.26(b). As it can be seen the primary RMS current is strongly dependent on the primary freewheeling current. It follows that the primary side copper losses are less dependent on the load conditions.

In Fig. 3.27 are reported the primary RMS current for different output currents as it can be noticed the peak RMS current is around 1.2A in high load, thus, the total copper losses at primary side are kept low even in high load. Considering this amount of current in high load it allowed to implement the transformer in a semi-interleaved structure without having an important impact on the efficiency.

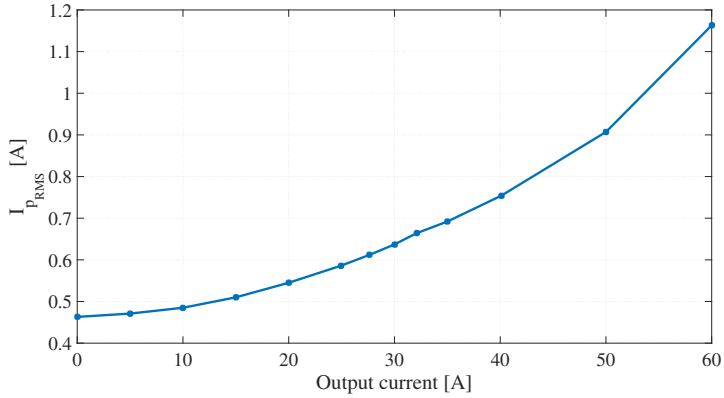


FIGURE 3.27: Primary RMS current varying output current.

To validate the effectiveness of the ZVS strategy at primary side, in Fig. 3.28 are reported the ZVS transitions. From Fig. 3.28(a) and Fig. 3.28(c) it follows how the ZVS transition is ensured by $I_{cir_{HB}}$, whilst, in Fig. 3.28(b) and Fig. 3.28(d) the actual ZVS transition is performed by the current defined in eq. 3.37.

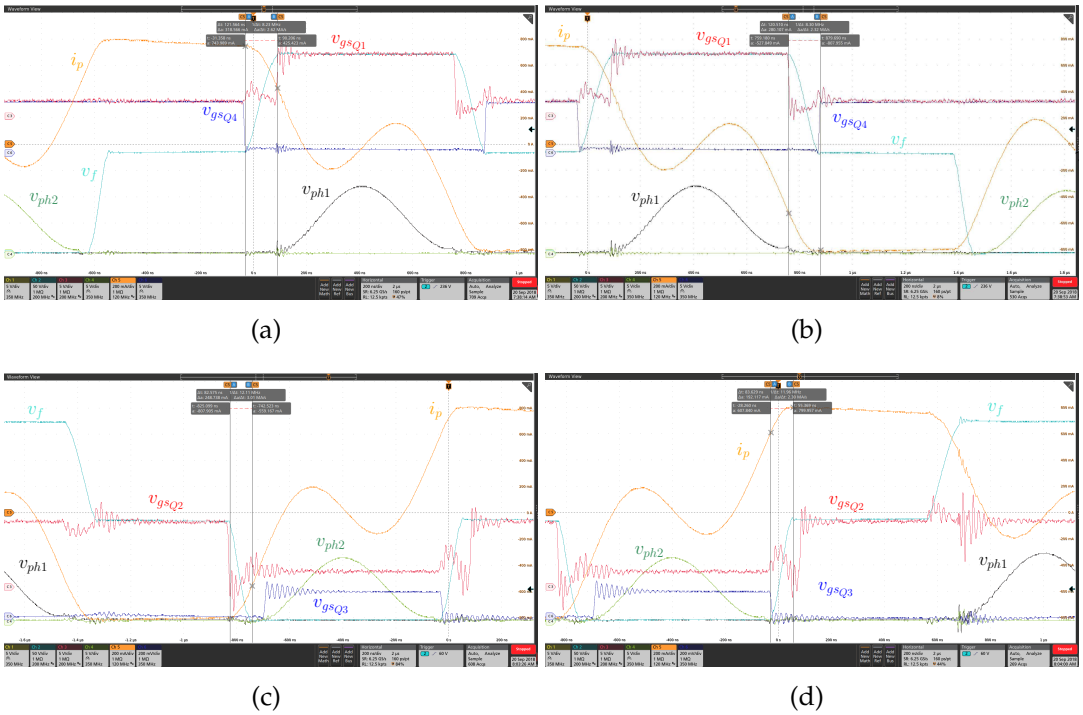


FIGURE 3.28: Waveforms ZVS operations: (a) t_1-t_2, (b) t_5-t_5 (c) t_7-t_8 and (d) t_{11}-t_{12}

Transient-response measurements obtained at $V_{in} = 380V$ and $V_{out} = 1.8V$ are shown in Fig. 3.29 where the output voltage has a resistive behavior, where in this case the control bandwidth is 70KHz. The transient was performed by two Dynamic Load Tools (DLT100AGEVB) in parallel the slew rated is $300A/\mu s$ from 22A to 82A. The proposed converter fully meets the

voltage deviation at VRM output that is compatible with $1m\Omega$ load line requirement.

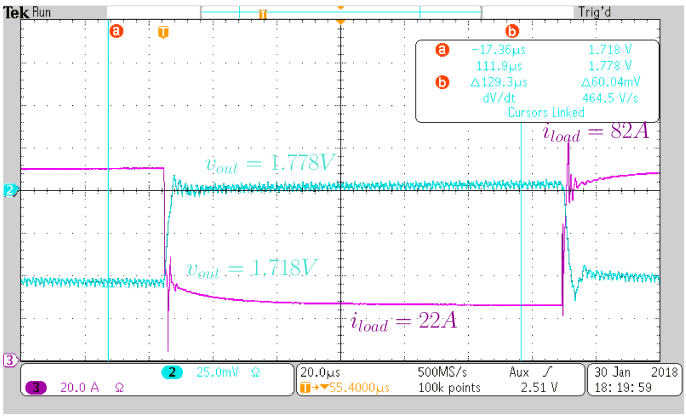
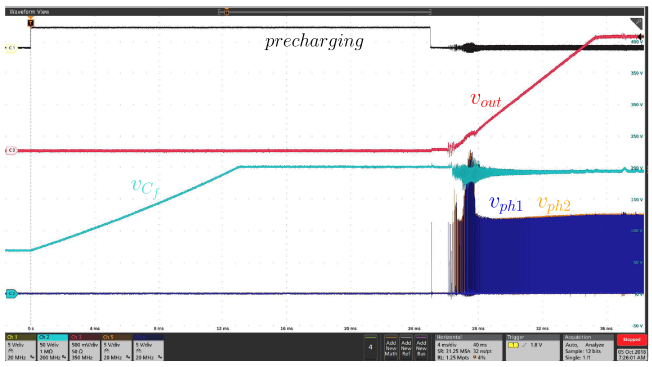
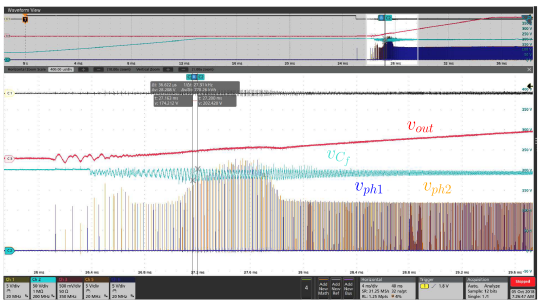


FIGURE 3.29: Transient response from 22A to 82A load step with $300A/\mu s$ as slew rate.

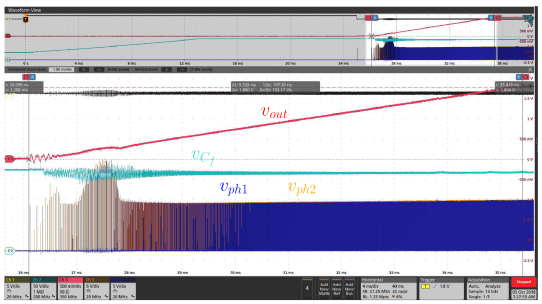
As discussed in Section 3.4 in HBPS-QR the start-up is an important issue for the converter. One of the main concern comes from the multilevel operation at primary side and even the switching frequency at the start-up. In Section 3.4 is proposed a start-up auxiliary circuit which performs the flying capacitor pre-charging. In Fig. 3.30(a) the start-up waveforms are depicted. The start-up procedure is divided in two phases.



(a)



(b)



(c)

FIGURE 3.30: Start up waveforms: (a) all start up procedure, (b) start up bheaviour once converter is enabled (c) converter bheaviour during start up

The first phase is the flying capacitor pre-charging. In cyan is reported the flying capacitor voltage v_{C_f} which is started-up before the VRM enable signal. The flying capacitor is charged with a fixed current coming from the P-MOS, connected to the input voltage. Once the voltage on the flying capacitor reaches the zener voltage of the diode in parallel with the flying capacitor (as reported in Fig. 3.10), the zener starts to conduct to keep the flying capacitor voltage slightly above the half of input voltage. Once the precharging signal falls the pre-charging auxiliary circuit stops to conduct and the first phase finished. The second phase starts when the VRM is enabled, and the converter starts to power-on the load. In this phase the switching frequency is low which can causes high ripple on the flying capacitor as it is possible to get from Fig. 3.30(b). Furthermore, during the start-up procedure the resonant transition is boosted because of the circulating current has not reached the steady state.

3.7.1 HBPS-QR with coupling inductor experimental results

Finally, in Fig. 3.31 is depicted the prototype realized with coupling inductor for the current doubler. The converter implemented with noncoupled (Fig. 3.22) inductor presents slightly the same power density. In Fig. 3.32 reports the efficiency comparison between the coupling current doubler (in blue) implemented with CL1108-2-50TR-R and the noncoupled current doubler (in red) performed by using TDK-VLB7050HT-R09M. The main passive components parameters for the converter implemented with coupled inductance current doubler are as follows: $L_r = 28.8\mu H$, $L_0 = 380nH$ $M = 300nH$ (EATON CL1108-2-50TR-R), $C_r = 209nH$, whereas the elements parameters for the converter implemented with a traditional solution are as follows: $L_r = 28.8\mu H$, $L_{out} = 90nH$ (TDK-VLB7050HT-R09M) and $C_r = 342nH$. The switching frequency in light load are almost the same for both experiments 410kHz.

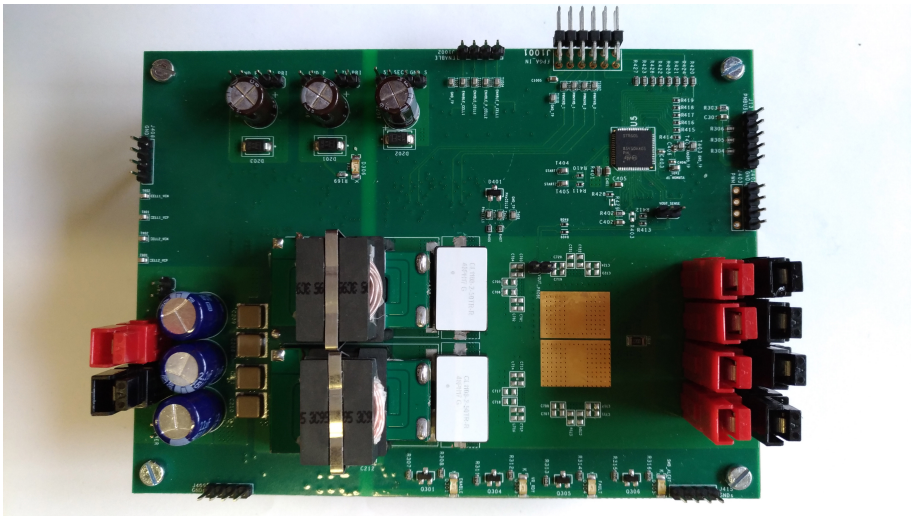


FIGURE 3.31: Test board VRM from 380V to 1V8 with coupled inductor.

Efficiency measurements comparison are depicted in Fig. 3.32, including converter driving losses at nominal output voltage $V_{out} = 1.8V$ and $V_{in} = 380V$. By using inverse coupling inductors the efficiency can be improved by 3.6% at full loads and by 1.4% in light load. Instead, at high load the big difference in efficiency is mainly due to the higher current capability that offers the HBPS-QR with coupling inductor, as reported in section 3.5. In fact, HBPS-QR coupling inductor presents lower frequency variation in the entire load range (i.e. in the experiment proposed in Fig. 3.32 the frequency variation between light load to high load is from 400kHz to 495kHz). On the other hand, noncoupled configuration offers lower current capability, and therefore higher frequency variation from light to high load condition (i.e. in the experiment proposed in Fig. 3.32 the frequency variation between light load to high load is from 400kHz to 630kHz).

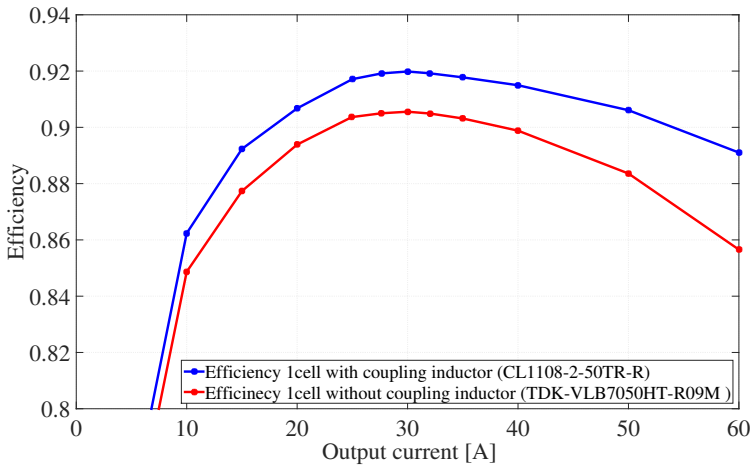


FIGURE 3.32: Efficiency comparison between coupled inductor and noncoupled inductor double current with the same transient inductance obtained at nominal output voltage $V_{out} = 1.8V$ and $V_{in} = 380V$.

In Fig. 3.33 is reported the maximum voltage of the resonant voltage, in all load conditions, for both coupled inductor and noncoupled inductor double current. From Fig. 3.33 it is possible to notice how the coupled inductor configuration presents higher resonant voltage (in blue). This behaviour is analytically described in equations 3.26 and 3.25.

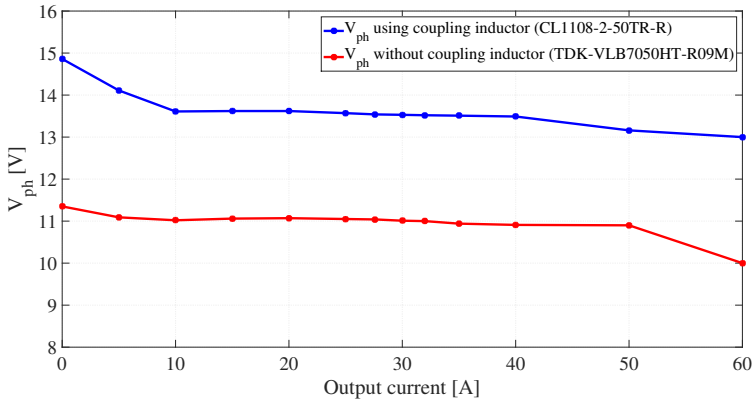


FIGURE 3.33: Maximum voltage on the resonant voltage comparison between coupled inductor and noncoupled inductor double current with the same transient inductance obtained at nominal output voltage $V_{out} = 1.8V$ and $V_{in} = 380V$.

Whilst in 3.34 is experimentally reported and validate the higher *current capability* obtained with coupled inductor configuration. As it is reported in section 3.5, the higher power capability of coupling inductor configuration gives lower frequency variation in all entire load. This is also proven from the efficiency plot where at maximum load the coupled inductor prototype gives 3.6% higher efficiency comparing with noncoupled configuration.

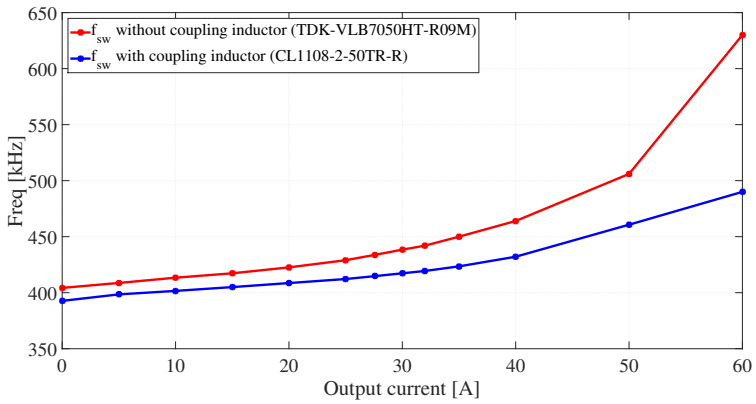
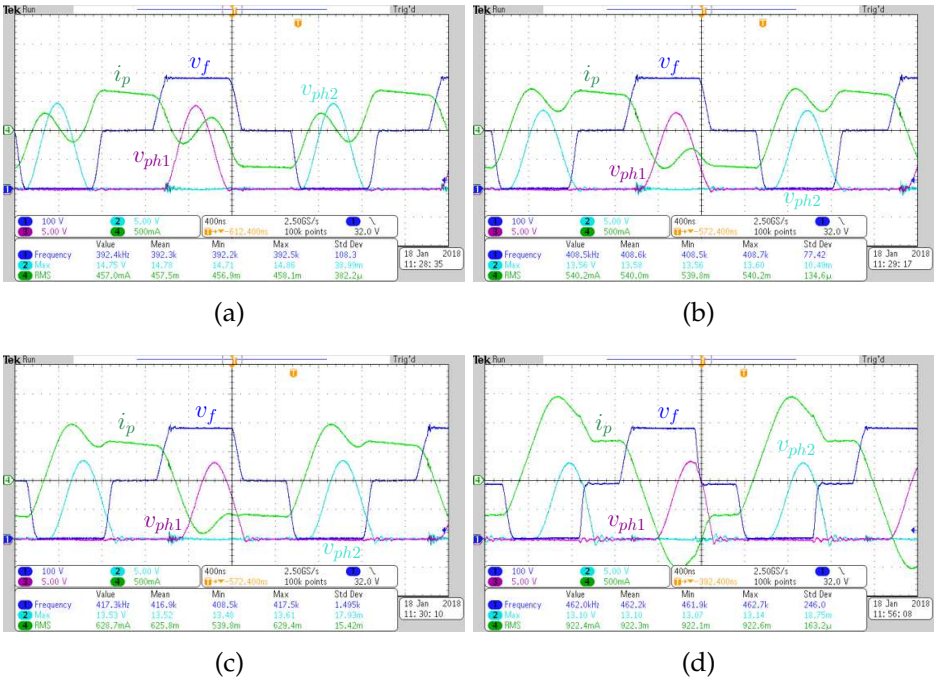


FIGURE 3.34: Switching frequency comparison between coupled inductor and noncoupled inductor double current with the same transient inductance obtained at nominal output voltage $V_{out} = 1.8V$ and $V_{in} = 380V$, at different load condition.

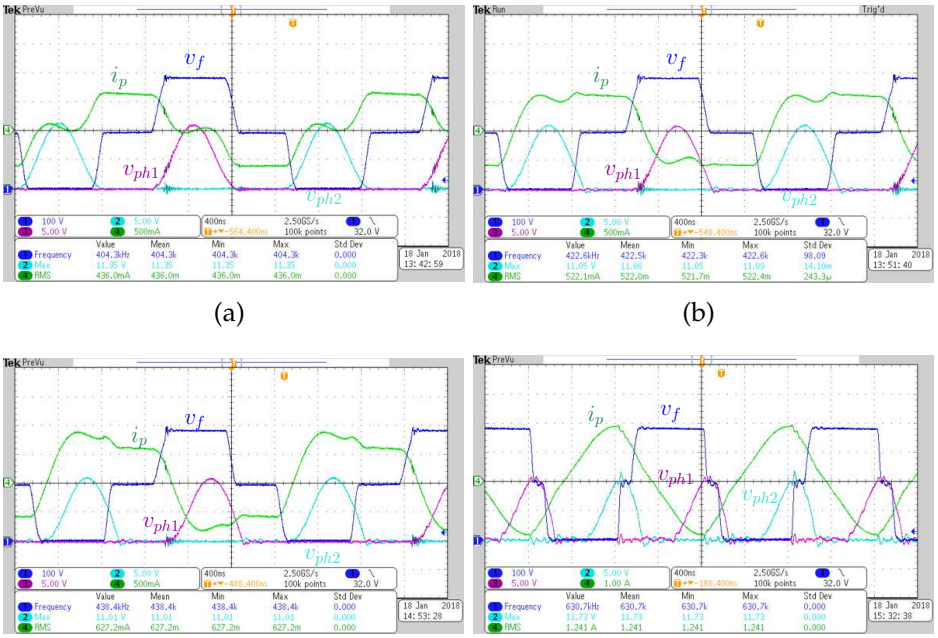
In Fig. 3.35 and 3.36 are reported the main experimental waveforms respectively for coupled and noncoupled HBPS-QR for current-doubler implementation. It is possible to notice how the RMS current at primary side is slightly the same for both configuration, since it is mainly dominated from the freewheeling current at primary side that is the same for both prototype (same on-time at primary side T_{sh}).



(a) (b)

(c) (d)

FIGURE 3.35: Main experimental converter waveforms at different load conidition for 1 phase prototype realized with coupling inductor: (a) $I_{out} = 0A$, (b) $I_{out} = 20A$, (c) $I_{out} = 30A$ and (d) $I_{out} = 50A$



(a) (b)

(c) (d)

FIGURE 3.36: Main experimental converter waveforms at different load conidition for 1 phase prototype realized without coupling inductor (i.e. $L_{out} = L_0 - M$ considering output inductances used in Fig. 3.35): (a) $I_{out} = 0A$, (b) $I_{out} = 20A$, (c) $I_{out} = 30A$ and (d) $I_{out} = 60A$

3.7.2 HBPS-QR comparison between different primary side FETs

In Fig. 3.37 are depicted efficiency measurement with $L_r = 28.8\mu H$, $L_{out} = 150nH$ and $C_r = 200nH$ implemented with semi-interleaved transformer using two different primary side FETs. From Fig. 3.37 it follows that the unique figure of merit for selecting the primary side MOSFETs depends mainly from the output parasitic capacitance C_{oss}. The efficiency obtained with BSZ42DN25NS3 has an higher efficiency in almost all load condition except for the high load, where the impact of the $R_{ds_{on}}$ is important.

This experimental result validate the design procedure reported in section 3.6.2.

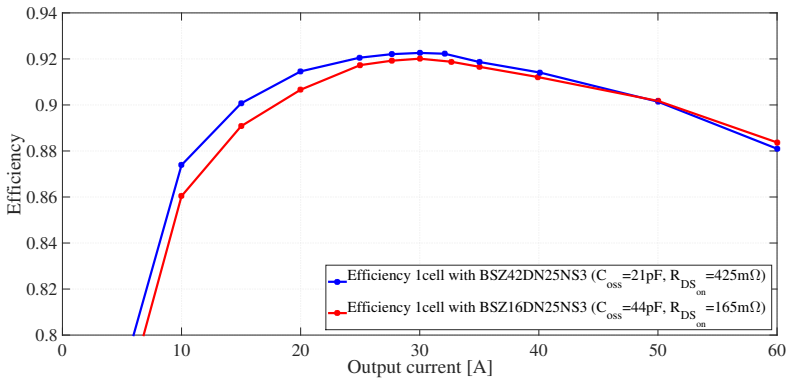


FIGURE 3.37: Efficiency comparison between different primary side MOSFETs: BSZ42DN25NS3 in blue and BSZ16DN25NS3 in red.

Chapter 4

Magnetics for FBPS-QR and HBPS-QR

Resonant or soft switching topologies such as the proposed FBPS-QR and HBPS-QR can provide relief from the high switching loss ensuring high switching operation. One disadvantage of resonant scheme is the increased of size and conduction losses produced by the circulating energy. The goal of this chapter is to present a new improved integrated magnetic solution for the use in FBPS-QR. Moreover two transformers for HV POL converter has been proposed here. The magnetic structures are simulated using 3D FEA verification and verified in hardware design.

4.1 Planar magnetics transformer and Integrated Magnetics

Today, high power density and high efficiency VRM converter are fundamental to the profitable growth of the power. In Chapter 2 and 3 it is highlighted how important is to find out an appropriate topology for such kind of application, but actually high performance inductor and transformer are mandatory to reach high performance. Planar magnetic component using printed circuit board (pcb) windings are attractive due to their good thermal performance, high precision design and high repeatability. These advantages make planar magnetics attractive in VRM application where high switching frequency, high power density and repeatability are needed [92].

Hence, it essential to integrate passive parts of the converter in order to increase the field density and transport more energy from the primary to the secondary side of the converter. Many techniques has been used for integration of passive magnetics using even the parasitic element of the structure, such as leakage inductances and stray capacitance. However, it is important to control the impact of such parasitic to contain the copper losses and EMI issue.

4.2 Integrated Magnetics for FBPS-QR

Power inductors and transformers size are the primary determinants of power density in low voltage application especially in the proposed FBPS-QR which

presents four magnetic components: transformer, resonant inductance and current doubler inductances.

The proposed converter, described in Section 2.3, is a topology with a full bridge at primary side and a current doubler rectifier at the secondary side. The current-doubler rectifier has been proven to be suitable for high current dc-dc converters [93]. Compared with the conventional center-tap rectifier, the current-doubler rectifier has a simple structure of the transformer, and it halves the secondary winding conduction loss. In order to meet the requirements of modern POL converter here are discussed some integrated magnetic solutions. Several integrated structures have been proposed in literature to integrate the current doubler components into a single core [94], [95] and [96]. In this section we will discuss first a different geometrical approach to integrate a current-doubler with a transformer by using a planar technology and the second an innovative integration of transformer, output inductances and the external inductor connected to the primary side required for ZVS operation, using a single magnetic component.

4.2.1 Integrated magnetics current doubler and transformer

The first solution, to reduce the converter size, is based on integration of transformer and the current-doubler inductances into a single core with an external inductance for L_r. The structure uses two PCBs and EE cores (or E with I core) and it is represented in Fig. 4.1(a) with a cross section reported in Fig. 4.1(b). The top PCB implements the transformer windings and the second, on the bottom of the structure, collects the total current of the inductors of the current-doubler. This integration uses a similar approach of a typical integration magnetic techniques [94], [97] in which the flux of the transformer core coincides with the flux of the output inductors. The proposed topology has very small output inductors each of which is realized using a single winding. The main difference of this integration respect other solutions is the shape of the output inductor coil that it is placed on a vertical plane and not on a horizontal plane, where the primary transformer coil is present. The flux of each inductor $\phi_{1,2}$ flows in the lateral legs of the E core, as reported in Fig. 4.1(a). In the two legs there are also two air gaps that determine the values of $L_{out1,2}$. The equivalent electric circuit is reported in Fig. 4.1(c), in which the current flowing in the two terminals OUT_1 and OUT_2 is the sum of the transformer current and the inductor current. Instead, the output current of the pin COM collects the current of the two output inductors.

Considering the magnetic structure of the proposed transformer reported in Fig. 4.1(b) it is useful to study the dependencies of the inductances with the geometry.

Considering now the reluctance $\Re_c$ due to the lateral gap, here the equivalent output inductance $L_{out1,2}$ is derived:

$$L_{out1,2} = \frac{N_s^2}{\Re_c} = \frac{N_s^2 A_e}{2 l_{gap}} \tag{4.1}$$

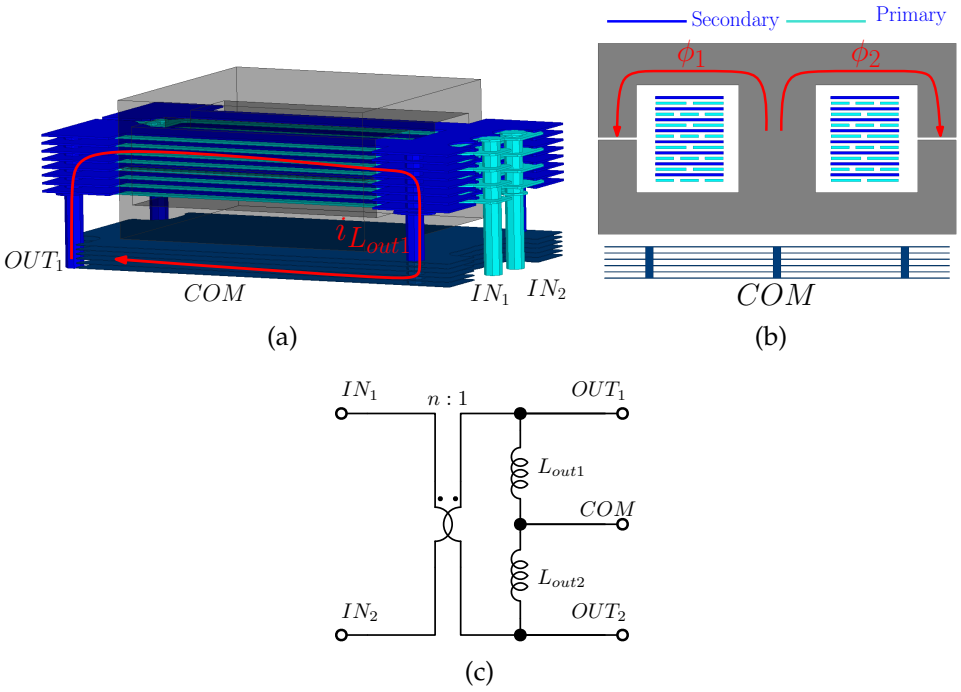


FIGURE 4.1: a) Three dimensional view of the integrated magnetic with $i_{L_{out1}}$ path highlighted b) Cross section with the magnetic flux c) equivalent electrical model

where $N_s = 1$ considering the structure depicted in Fig. 4.1(a), l_{gap} is the gap length and A_e is the equivalent core section area.

Winding losses

Winding losses in the proposed transformer increase dramatically with high frequency due to skin and proximity effect. In the proposed transformer the proximity loss is significantly reduced, since the primary and secondary currents are in phase [98]. However, in the proposed integrated transformer the inductances of the current doubler are implemented with the lateral gaps where are store the energy of L_{out1} and L_{out2} , which actually creates fringing flux inducing eddy currents in the surface of nearby plates conductor, causing an higher ac resistance. In order to minimize the fringing effect, the PCB windings near the air gaps are kept far away. Fig. 4.2 shows the FEA simulation results of the fringing effect on the air gap with different windings locations. In Fig. 4.2 are reported the primary resistance R_{ac} (Fig. 4.2(a)) and the inductance resistance R_{ac} (Fig. 4.2(b)) comparison between classic windings arrangement and graduated windings arrangement around the gap. In Fig. 4.2(c) and Fig. 4.2(d) are depicted respectively the FEA simulation of the distribution ohmic losses in classic windings arrangement and graduated windings arrangement at $1\ MHz$. From Fig. 4.2(c) and Fig. 4.2(d) it follows that the losses around the gap are reduced at high frequency adopting the graduated windings arrangement affecting partially the DC resistance.

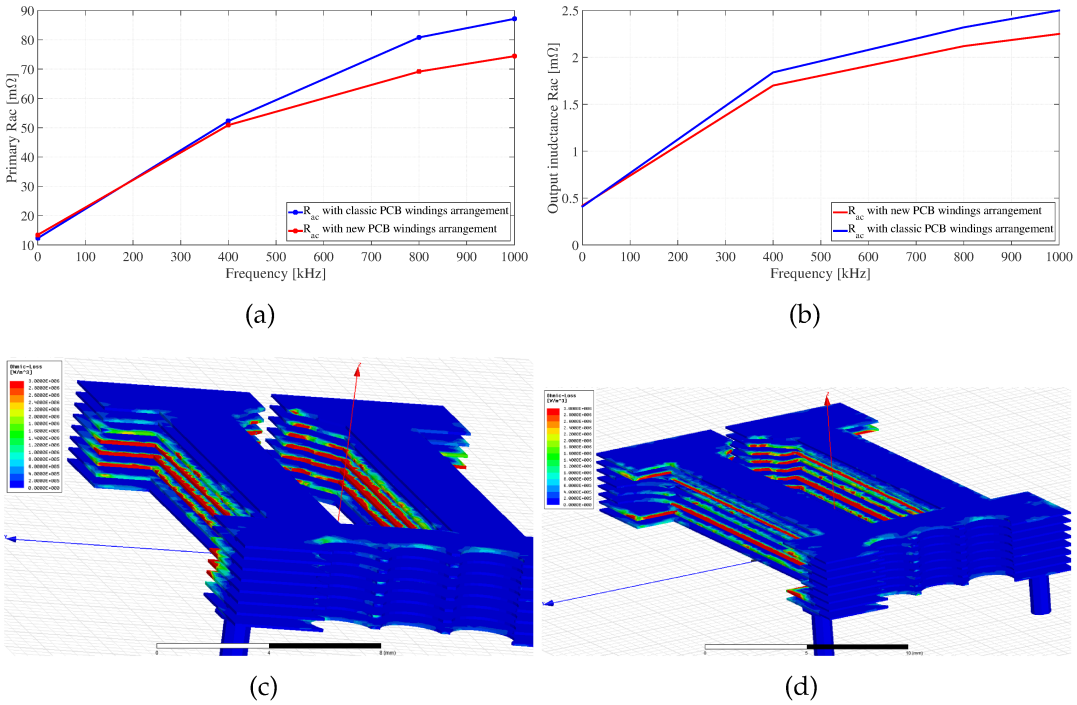


FIGURE 4.2: FEM simulation transformer in Fig. 4.1: a) Primary R_{ac} comparison b) Output inductance R_{ac} comparison c) Ohmic loss distribution classic winding arrangement d) Ohmic loss distribution with graduated windings arrangement.

4.2.2 Integrated magnetics current doubler, transformer and resonant inductance

In order to integrate also the resonance inductor, the structure is changed as reported in Fig. 4.3 (a) (the cross section is in Fig.4.3 (b)). This architecture requires two E cores, one I core and two boards. In this case the current of the output inductors is flowing with similar path of the previous architecture, the main difference is the presence of primary windings on the bottom side board. Considering, for sake of simplicity, only magnetic gap on the external legs of the E core. The flux of each external leg depend on the primary and secondary current that is flowing in the adjacent windings area. This physical consideration can be translated in the equivalent circuit of Fig. 4.3(c).

The electrical circuit can be derived from the 2D structure in Fig. 4.3 (b) and is shown in Fig. 4.3 (c).

In order to understand the operation of the magnetic structure shown in Fig. 4.3 it is essential to find the equivalent electric circuits in all operating modes.

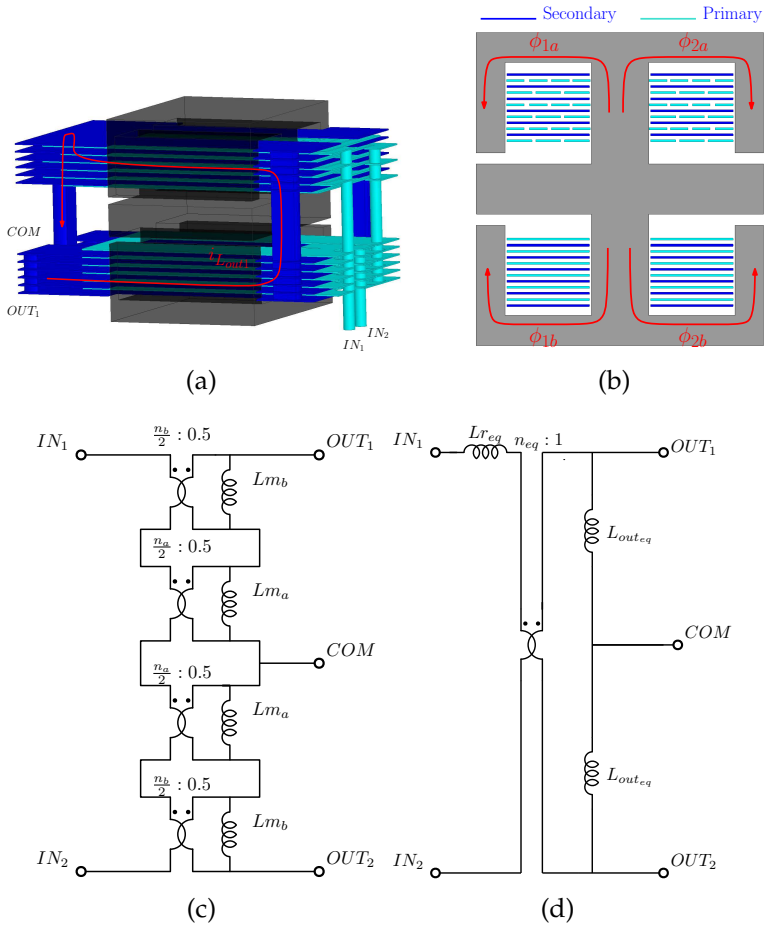


FIGURE 4.3: a) Three dimensional view of the integrated magnetic with $i_{L_{out1}}$ path highlighted; b) cross section with the magnetic flux; c) equivalent electrical model; d) simplified electrical model

ZVS and energization modes

From the circuit in Fig. 4.4 the following equation are derived:

$$V_{in} = (V_1 + V_3)(N_1 - N_2) \tag{4.2}$$

where the current equations are:

$$\begin{cases} N_1 I_{in} + I_{cc1} = I_{L1} \\ N_2 I_{in} + I_{cc1} = I_{L2} \\ N_1 I_{in} + I_{cc2} = I_{L1} \\ N_2 I_{in} + I_{cc2} = I_{L2} \end{cases} \tag{4.3}$$

Considering $L_3 = L_1$ and $L_4 = L_2$, it follows that $I_{cc1} = I_{cc2} = I_{cc}$, so $V_1 = V_3$ and $V_2 = V_4$. In fact, in this phase there is no current that flows from node COM. From equations (4.2) and (4.3) and from aforementioned consideration, it is possible to derive the following equations system:

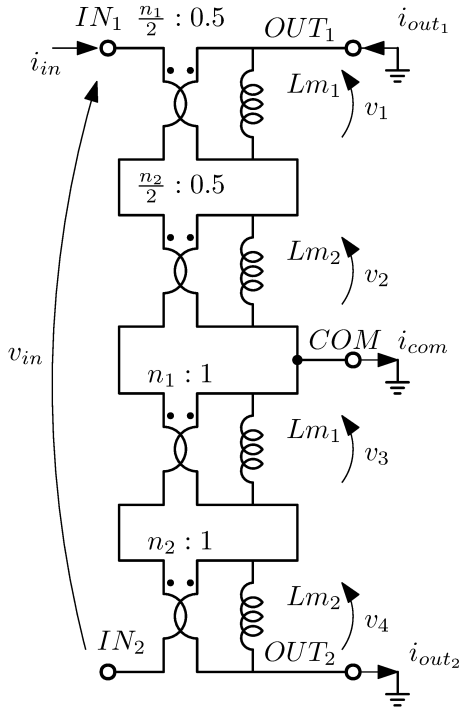


FIGURE 4.4: ZVS and energization modes equaivalent elecgtric circuit

$$\begin{cases} N_1 I_{in} + I_{cc} = I_{L1} \\ N_2 I_{in} + I_{cc} = I_{L2} \\ V_{in} = 2V_1 \cdot (N_1 - N_2) \end{cases} \tag{4.4}$$

the expressions can be rewritten as:

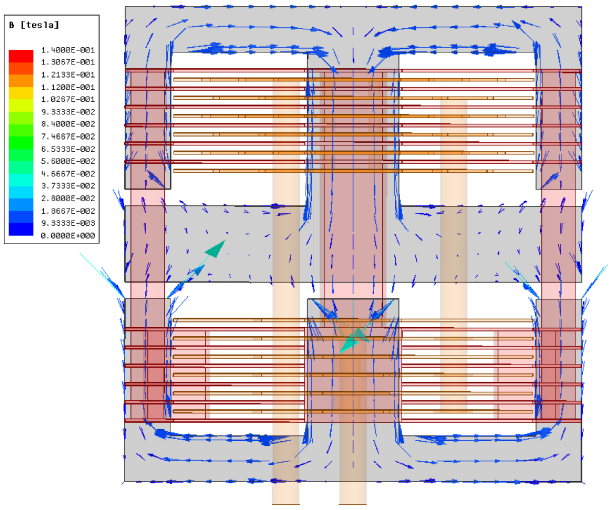


FIGURE 4.5: ZVS and energization modes magnetic flux

$$\begin{cases} I_{in} = \frac{I_{L1} - I_{L2}}{N_1 - N_2} \\ V_{in} = 2V_1 \cdot (N_1 - N_2) \end{cases} \tag{4.5}$$

and considering the following equations:

$$\begin{cases} I_{L1} = \frac{V_1}{sL_1} = \frac{V_{in}}{s2L_1 \cdot (N_1 - N_2)} \\ I_{L2} = \frac{V_2}{sL_2} = -\frac{V_1}{sL_2} = -\frac{V_{in}}{s2L_2 \cdot (N_1 - N_2)} \end{cases} \tag{4.6}$$

the input impedance is given by:

$$Z_{in} = \frac{V_{in}}{I_{in}} = 2 \cdot s \frac{L_1 L_2}{L_1 + L_2} \cdot (N_1 - N_2)^2 = L_{insec,cc} \tag{4.7}$$

Assuming the output transformer shorted, the shorted current I_{cc} is calculated as follows:

$$\begin{aligned} I_{cc} &= I_{L1} - N_1 I_{in} \\ &= V_{in} \cdot \frac{\frac{L_2}{L_1+L_2} \cdot (N_1 - N_2) - N_1}{s2 \cdot \frac{L_1 L_2}{L_1+L_2} \cdot (N_1 - N_2)^2} \\ &= -V_{in} \cdot \frac{N_1 L_1 + N_2 L_2}{s2 \cdot L_1 L_2 \cdot (N_1 - N_2)^2} \end{aligned} \tag{4.8}$$

$$I_{cc} = -\frac{V_{in}}{L_{insec,cc}} \cdot \frac{N_1 L_1 + N_2 L_2}{L_1 + L_2} \tag{4.9}$$

from which it is possible to calculate the ratio of the transformer:

$$N_{4ST} = \frac{N_1 L_1 + N_2 L_2}{L_1 + L_2}, \tag{4.10}$$

In Fig. 4.5 are depicted the magnetic flux during the ZVS energization. From Fig. 4.5 it is interesting to notice that the dc flux in the middle plate is reduced due to magnetic flux cancellation. This is paramount important to consider since the overall volume can be reduced.

Resonance modes

The circuit shows in Fig. 4.6 is described from the following equations:

$$\begin{cases} 0 = N_1 V_1 + N_2 V_2 + N_1 V_3 + N_2 V_4 \\ V_{secx} = V_1 + V_2 \\ V_4 = -V_3 \end{cases} \tag{4.11}$$

from which it follows:

$$V_{secx} = -(V_1 + V_2) \cdot \frac{N_1 - N_2}{N_2} \tag{4.12}$$

whilst the current equations are:

$$\begin{cases} N_1 I_{in} + I_{outx} = I_{L1} \\ N_2 I_{in} + I_{outx} = I_{L2} \\ N_1 I_{in} + I_{outy} = I_{L3} \\ N_2 I_{in} + I_{outy} = I_{L4} \end{cases} \tag{4.13}$$

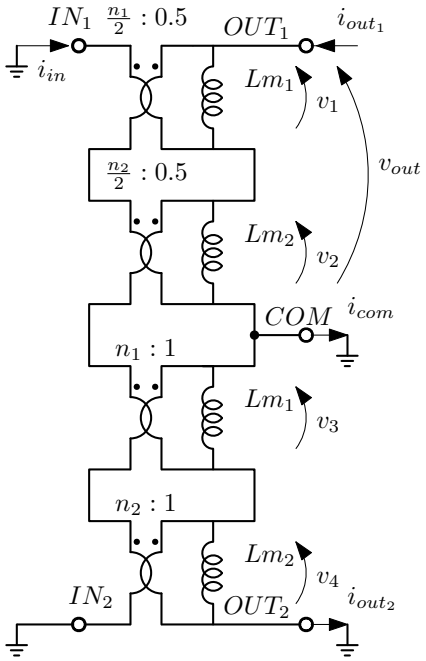


FIGURE 4.6: Resonance modes

from which it derives:

$$\begin{cases} I_{in} \cdot (N_1 - N_2) = I_{L1} - I_{L2} \\ I_{in} \cdot (N_1 - N_2) = I_{L3} - I_{L4} \end{cases} \tag{4.14}$$

the expression can be rewritten as:

$$I_{L1} - I_{L2} = I_{L3} - I_{L4}, \tag{4.15}$$

assuming the following $I_{L1} = \frac{V_1}{sL_1}$, $I_{L2} = \frac{V_2}{sL_2}$, $I_{L3} = \frac{V_3}{sL_1}$ e $I_{L4} = \frac{V_4}{sL_2}$, hence $\frac{V_1}{sL_1} - \frac{V_2}{sL_2} = \frac{V_3}{sL_1} - \frac{V_4}{sL_2}$. Considering the aforementioned equations it follows that:

$$(V_1 - V_3) = \frac{L_1}{L_2} \cdot (V_{secx} - V_1 + V_3), \tag{4.16}$$

the secondary side voltage during resonance mode is given by:

$$V_{secx} = \left(1 + \frac{L_1}{L_2}\right) \cdot (V_1 - V_3), \tag{4.17}$$

and

$$V_3 = V_1 - \frac{L_1}{L_1 + L_2} \cdot V_{secx}, \tag{4.18}$$

from $V_1 + V_3 = -V_{secx} \cdot \frac{N_2}{N_1 - N_2}$ is obtained:

$$V_1 = V_{secx} \cdot \frac{L_{1 \cdot (N_1 - N_2) - N_2 \cdot (L_1 + L_2)}}{2 \cdot (L_1 + L_2) \cdot (N_1 - N_2)} \tag{4.19}$$

it follows that I_{outx} is:

$$\begin{cases} I_{outx} = I_{L1} - N_1 I_{in} \\ I_{outx} = I_{L2} - N_2 I_{in} \end{cases} \tag{4.20}$$

and

$$I_{outx} = I_{L1} \cdot \frac{N_2}{N_2 - N_1} - \frac{N_1}{N_2 - N_1} \cdot I_{L2} \tag{4.21}$$

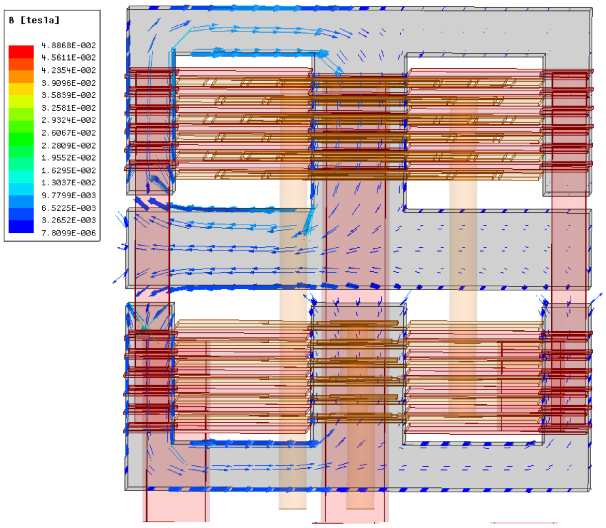


FIGURE 4.7: Resonance modes flux

Thus, it is possible to calculate an inductance from the output, considering the transformer input shorted, using the following equation:

$$L_{res,sec} = \frac{2 \cdot L_1 L_2 \cdot (L_1 + L_2) (N_1 - N_2)^2}{N_1^2 \cdot L_1^2 + N_2^2 \cdot L_2^2 + 2 \cdot L_1 L_2 \cdot (N_1^2 - N_1 \cdot N_2 + N_2^2)} \tag{4.22}$$

From the foregoing analysis all equivalent discrete components of the circuit in Fig. 4.3(d) are derived, where $L_{res} = 2 \cdot \frac{L_1 L_2}{L_1 + L_2} \cdot (N_1 - N_2)^2$, $N_{4ST} = \frac{N_1 L_1 + N_2 L_2}{L_1 + L_2}$ and $L_{out} = L_1 + L_2$

In Fig. 4.7 are depicted the magnetic flux during the resonant transition. In this mode the converter is in powering mode, the power is transferred from the primary side to the secondary side. As can be seen the output inductance are formed by the external legs. The only drawback of using this structure is that an high RMS current, that is the actual current carried by the output inductance, is flowing from the bottom part of the transformer to the top, causing high copper losses.

Finally, it can be seen that the solution in Fig. 4.1(a) reduces the total area of the converter by eliminating the output inductors area. If there are not any low profile requirements, the resonant inductor can be realized on the top of the magnetic structure. In this case, the solution of Fig. 4.3(a) can also reduce

the profile of the magnetic part, because the bottom windings can be realized on the main board.

4.3 Experimental results of Integrated magnetics for 48 V VRM FBPS-QR

To demonstrate the effectiveness of the proposed integrated structures two prototype have been realized for FBPS-QR converter for 48 V VRM application.

Fig. 4.8 shows the integration of the current-doubler described in Fig. 4.1 with an external inductor mounted on the top, the total size is $15.2mm\ X\ 24.7mm$. Instead, Fig. 4.9 shows the proposed architecture of Fig. 4.3 that has a dimension of $15.2mm\ X\ 23.5mm$. The values of the equivalent output inductors L_{out} is 120 nH, the equivalent resonant inductor L_r is $1.7\ \mu H$ and the equivalent turns ratio n is 6. Each magnetic module can supply a current up to 60 A with 1.8 V of output voltage. The switching frequency is about 560 kHz for each phase. The measured efficiency comparison is depicted in Fig. 4.10. The magnetics integrated structures have lower efficiency, but higher power density. In general lower efficiency in the integrated structures, comparing with the discrete structure, is caused by copper losses, as discussed in section 4.2.1. The long paths of output inductances depends from the transformer size which actually depends from the output voltage as reported in eq. (3.12), this can be easily demonstrated by looking at Fig. 4.10. In Fig. 4.10 it is possible to notice how the efficiency in high load is extremely degraded comparing with discrete solution.

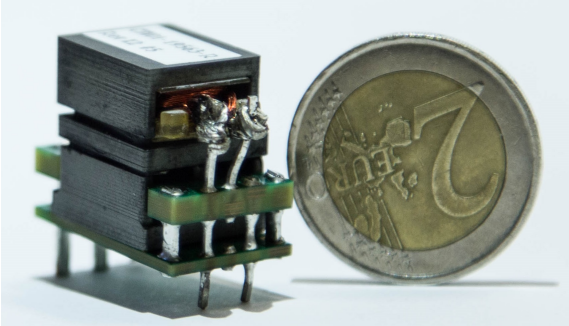


FIGURE 4.8: Prototype of the integrated magnetic of Fig. 4.1 with the resonant inductor on the top.

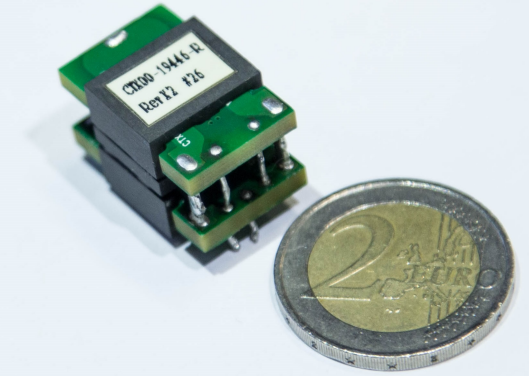


FIGURE 4.9: Prototype of the integrated magnetic of Fig. 4.3.

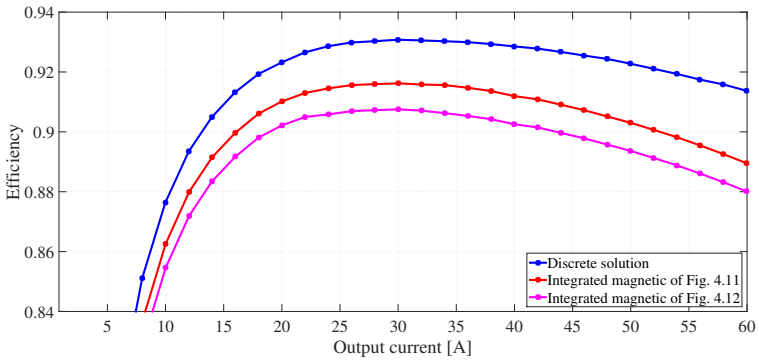


FIGURE 4.10: Efciency comparison between discrete solution, integrated magnetic solution depicted in Fig. 4.1 (in red) and full integrated magneric solution in yellow, for FBPS-QR for 48 V VRM application.

4.4 Transformer realization for HBPS-QR

The converter proposed in chapter 3 is an evolution of the FBPS-QR converter presented in section 2.3. In this dissertation has been widely discussed the power density issue introduced by the FBPS-QR. FBPS-QR needs four magnetic components as HBPS-QR. HBPS-QR would had been realized with center-tapped as rectifier which can reduce the size of the output inductor, as demonstrated in section 2.5.1, however center-tapped rectifier suffers of higher copper losses in the transformer windings. On the contrary, the current doubler rectifier reduces the number of the primary windings turns by half compared to the center-tapped rectifier. This is paramount important to consider because by adopting current doubler rectifier the parasitic stray capacitance between primary side and secondary side are contained.

In section 4.2 are presented two different integrated magnetic topologies suitable for a VRM application, these structures integrate respectively 3 and 4 magnetic components in one core. For HBPS-QR are not proposed magnetic integrated structures but actually they can be realized using the same concept applied for FBPS-QR, presented in section 4.2. Instead, for HBPS-QR is discussed the realization of the transformer for HV POL application.

In section 4.1 has been widely discussed how planar magnetics are very attractive for VRM application. High voltage input using planar magnetic structure introduces some essential difficulties such as the effect of the parasitic components on the converter functionalities at such VRM switching frequency (i.e. 300kHz to 1MHz). As discussed in section 4.1 the parasitic stray capacitance of the transformer is produced by inter-winding capacitances C_w. Moreover, in section 3.2 is discussed the important impact that inter-winding capacitances has on the ZVS performance at primary side of FBPS-QR, that actually does not affect the ZVS capability of HBPS-QR, but influences the resonant tank components. In Fig. 4.11 is reported the proposed HBPS-QR converter considering the parasitic stray capacitance of the actual transformer. To simplify the analysis the leakage inductance L_k is neglected since $L_r >> L_k$.

The purpose of this section is to estimate the actual effect of the non-ideal transformer on the converter functionalities for HBPS-QR working as HV POL. Two different transformers with different cross section here are discussed.

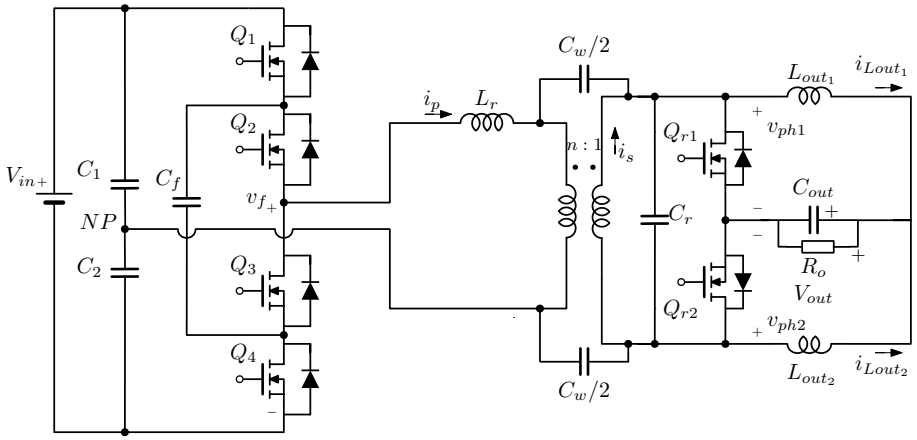


FIGURE 4.11: HBPS-QR converter with the parasitic stray capacitance transformer model.

4.4.1 Transformer fully-interleaved

In general a layer structure arrangement fully-interleaved reduces the ac winding resistance if the powering phase of the secondary is at the same time on the primary side. On the other hand, fully-interleaved structure increases the intrwinding capacitance, which, in high voltage applications, can produce several issues, such as, EMI problem and converter functionality issue. In this subsection will be discussed, through an analytical model, the effect of the stray capacitance on the converter functionalities. Finally experimental results will be presented to underline the effect on the resonant transition caused by stray-capacitance and the EMI issue.

Based on the schematic depicted in Fig. 4.12 it is possible to define the new resonant angular frequency considering the parasitic stray capacitance of the transformer C_w:

$$\omega_{r_{Cw}} = \sqrt{\frac{L_r + n^2 L_{out}}{L_{out} L_r \left(C_r + C_w/2\right)}}, \tag{4.23}$$

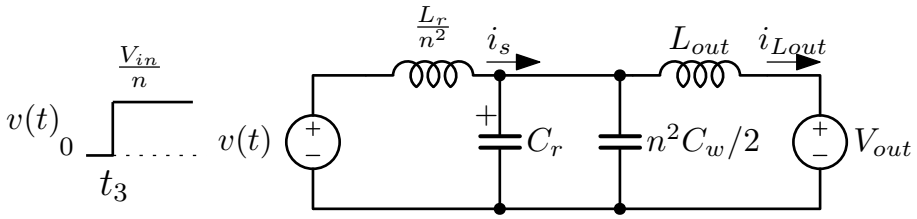


FIGURE 4.12: Equivalent resonant tank during resonant transition considering the interwindings capacitance C_w.

where the parasitic stray capacitance C_w is basically due to the electrical coupling between the primary and secondary windings. In the case of planar transformer, static layer capacitances can easily be estimated, since the windings arrangement can be assimilated as a two parallel conductive plates, thus C_w is given by:

$$C_w = \varepsilon_r \varepsilon_0 \frac{S}{d} n_o, \tag{4.24}$$

where ε_r is the relative permittivity of the dielectric material between two layers (i.e for FR4 $\varepsilon_r = 4.4$), ε_0 is the permittivity of air, S represents the overlapping area of the two plates, d is the distance between two layers and n_o are the primary side layers exposed to secondary side layers.

From equation 4.23 it follows that the resonant on-time depends on the transformer geometry. Thus, the design of the transformer yields in a balance between the effect on the resonant capacitance and the ac resistance.

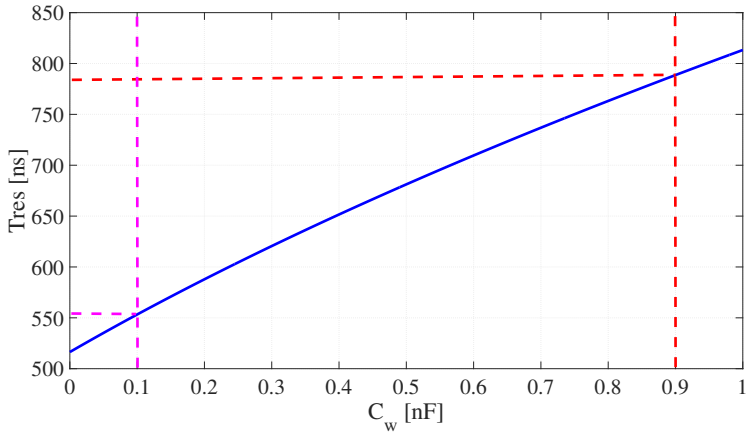


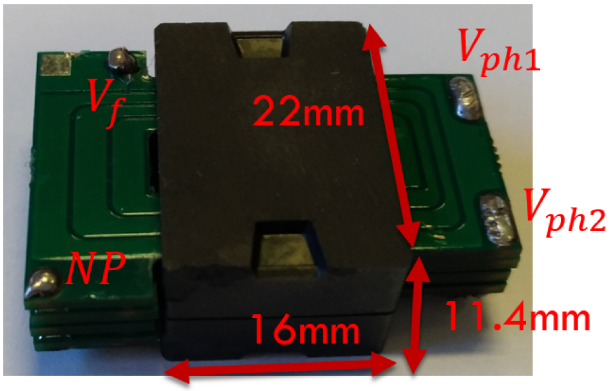
FIGURE 4.13: Variation of T_{res} in function of parasitic stray capacitance with $L_p = 30\mu H$, $L_{out} = 150nH$, $C_{res} = 135nF$ and $n = 20$, considering the converter in $Mode\ A$.

An important advantages of fully-interleaved structure is that the current is almost equally distributed in the paralleled windings layers, reducing the overall copper losses, but the transformer works also as resonant component [99] as it is possible to get from Fig. 4.13. In fact, the resonant transition it is almost dominated by parasitic stray-capacitance once C_w is around 1nF.

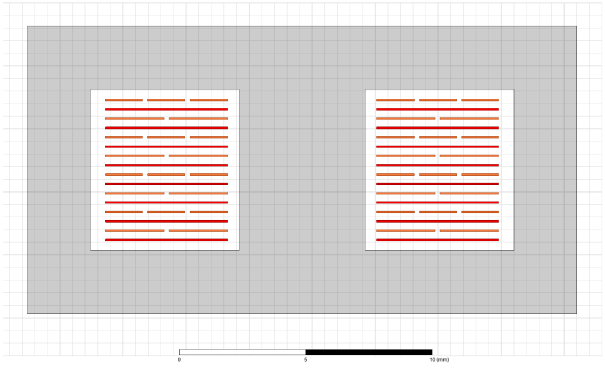
4.4.2 Experimental results Transformer fully-interleaved

In attempt to decrease the ac winding resistance and verify the impact on the current waveform on the excitation side and on the overall efficiency here is proposed a fully-interleaved transformer reported in Fig. 4.14(a). The aim of this experiment is to verify the actual low AC resistance transformer and even the current injected on the primary side during the resonant transition.

The transformer prototype depicted Fig. 4.19(a) is realized with 16 layers exploiting the entire winding area to reduce the parasitic stray capacitance. The transformer is realized with a planar E core E22/6/16 (equivalent area $78.3\ mm^2$) with 3F3 material. The turns ratio of the transformer is 20:1. The realized prototype has $750\ pF$ as stray capacitance between primary side and secondary side. Considering the discrete equivalent model of the transformer in Fig. 4.11, it is possible to calculate the capacitance reported at secondary side which is around $142\ nF$. The resonant time increments by 31% using the geometry proposed in Fig. 4.14(b) and the converter parameters of table 3.2.



(a)



(b)

FIGURE 4.14: Transformer prototype 20:1 realized in fully-interleaved structure in (a) and cross-section (b) (orange is primary side red is secondary side)

In Fig. 4.15 is reported the AC resistance of the prototype transformer.

Comparing with semi-interleaved transformer the AC resistance at the switching frequency is 3 times less, moreover at high frequency the overall performance is very good. Thus, the proposed solution can provide higher efficiency maintaining the same ZVS capability, as in semi-interleaved prototype, at primary side.

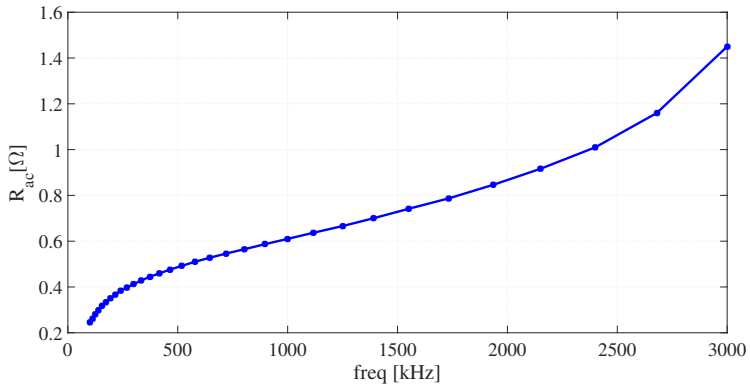


FIGURE 4.15: R_{ac} of transformer prototype 20:1 realized in fully-interleaved structure.

In Fig. 4.16 is reported the experimental leakage inductance of the proposed fully-interleaved transformer. As a fully interleaved structure the value of the leakage inductance is contained, reducing EMI issue and proximity effects.

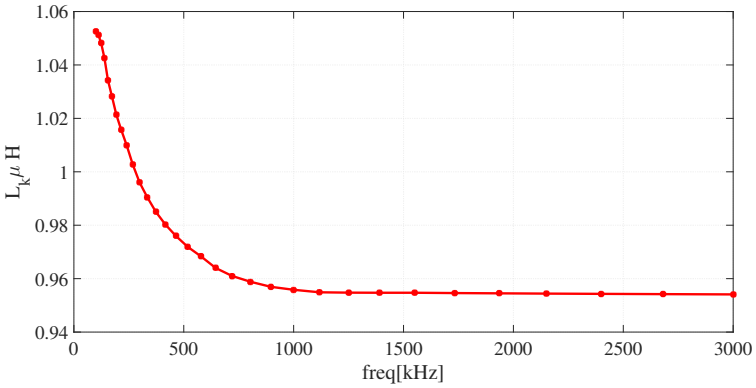


FIGURE 4.16: L_k of transformer prototype 20:1 realized in fully-interleaved structure.

Considering the actual model of the converter with non-ideal transformer depicted in Fig. 4.17. The capacitance C_w is responsible of unwanted resonances and oscillations of the primary and secondary side currents, reducing the system's efficiency and functionalities. Using the prototype in a fully-interleaved arrangement it is possible to investigate on CM noise considering a voltage with a certain dv/dt generated during the powering phase of HBPS-QR.

In Fig. 4.18 are reported in green the CM noise effect on the primary current. Considering the schematic in Fig. 4.17, the current $i_{p_{CMnoise}}$ reported in

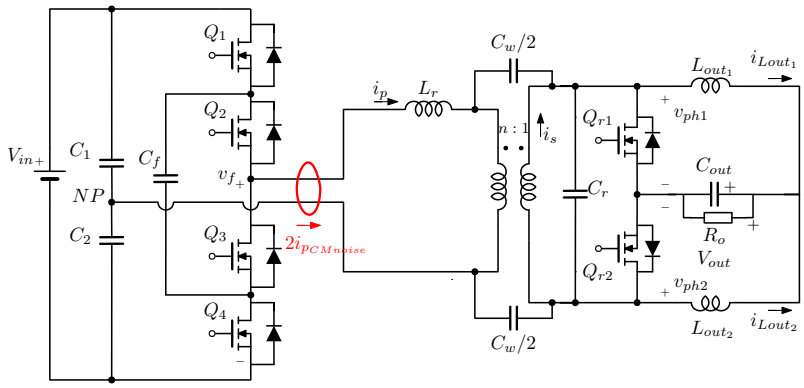


FIGURE 4.17: HBPS-QR converter schematic with the effect of commom mode noise at primary side.

Fig. 4.18 presents a peak of 100 mA during the resonant transition. The experiment was done with a switching frequency of $350kHz$ and input voltage of $V_{in} = 200V$ because the functionality at full input was not stable due to CM noise issue. From this experiment it is possible to understand how the parasitic capacitance of the transformer can heavily affect the performance of the converter, since the proposed topology uses a resonant parallel tank to make the resonant voltage transition at secondary side.

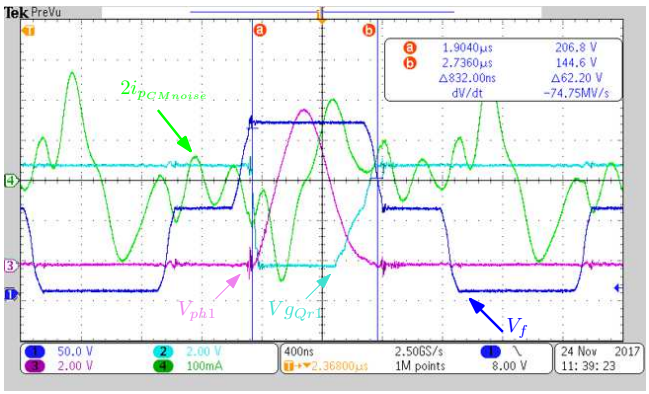


FIGURE 4.18: Main experimental waveforms of HBPS-QR converter schematic with the effect of commom mode noise at primary side.

Thus, the resonant transition is affected by the actual parasitic capacitance, as reported in equation (4.23). The main issue comes from the rectification of the resonant voltage. In fact the total Q factor of the resonance is deteriorated due to the injected current at primary side. The reduction of the Q factor results in a non ideal resonant voltage which could not reach the voltage threshold for enabling the ZVS predictor circuit.

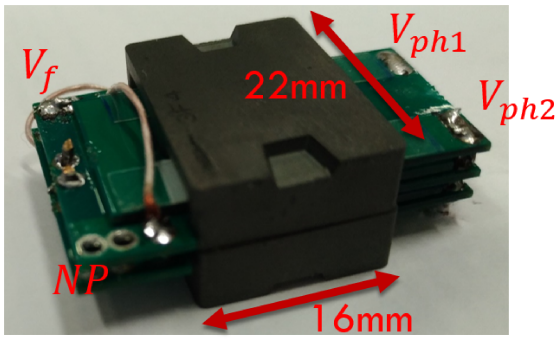
4.4.3 Transformer semi-interleaved

The concept of interleaving windings arrangement is proposed to reduce the ac resistance of the converter. The fully-interleaved transformer is implemented with 16-layers PCB causing large distributed interwinding capacitance creating large CM noise current for the proposed HV POL converter. The propagation path of CM noise is the parasitic capacitance C_w, depicted in Fig. 4.12, which produces EMI issue [100]. An alternative solution over the 16-layers full-interleaved solution is to use a semi-interleaved arrangement finding the balanced between the ac resistance of the transformer and the impact of the CM noise on the losses and converter functionality.

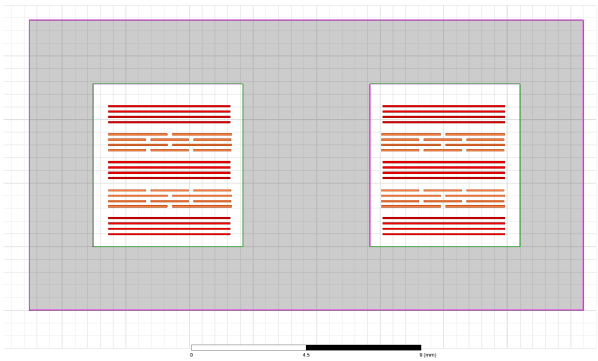
4.4.4 Experimental results Transformer semi-interleaved

In attempt to overcome the problem introduced by the fully-interleaved structure here is proposed a transformer with a semi-interleaved windings arrangement.

In Fig. 4.19(a) is depicted the transformer structure realized with 20 layers, with a planar E core E22/6/16 (equivalent area $78.3mm^2$) and 3F3 material.



(a)



(b)

FIGURE 4.19: Transformer prototype 20:1 realized in semi-interleaved structure in (a) and cross-section (b) (orange is primary side red is secondary side)

The turns ratio of the transformer is 20:1. As can be noticed in Fig. 4.19(b) the winding area of the transformer is not fully filled, to contain the parasitic transformer stray capacitance C_w. The realized prototype has $100pF$ as stray capacitance between primary side and secondary side. When the parasitic stray capacitance is reported at secondary side it can be modelled by a discrete capacitance equal to $20nF$ as demonstrated in section 4.4.1. With the semi-interleaved structure, exposing only 4 faces between primary and secondary side, the resonant ot time increments by 7% considering the converter parameters in table 3.2.

In Fig. 4.20 is reported the experimental AC resistance of the transformer prototype depicted in Fig. 4.19(a). Considering the ratio between the ac resistance R_{ac} (i.e. at switching frequency) and the dc resistance R_{dc} it follows that by adopting a non-interleaved winding arrangement the impact on the ac resistance is important [97]. It is also possible to decrease C_w by reducing the copper area, however the dc resistance increased. In this scenario it is essential to calculate the optimal solution considering all effects, finding the optimal winding structure and copper area for the transformer.

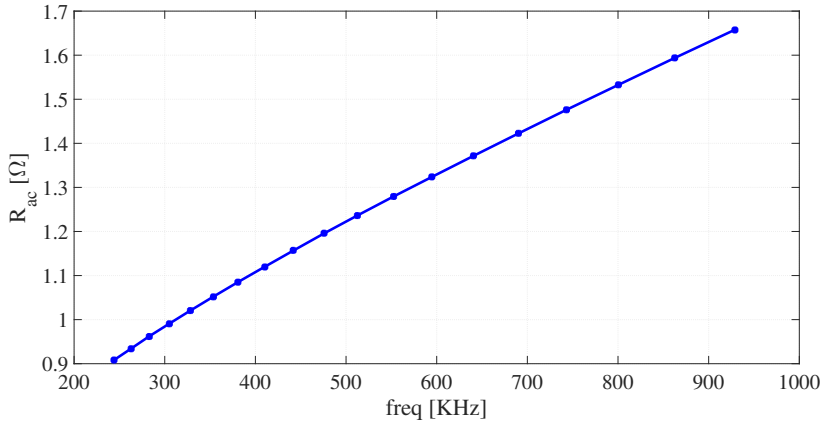


FIGURE 4.20: R_{ac} of transformer prototype 20:1 realized in semi-interleaved structure.

By adopting a non-fully interleaved structure, the leakage inductance for the proposed transformer is high, as reported in Fig. 4.21. An high value of leakage inductance my appear as a benefit for this topology, since the primary inductance needs to be integrated with an external inductance, but actually large value of leakage inductance affects the efficiency of the converter, causing proximity effect on the transformer windings, increasing the ac resistance.

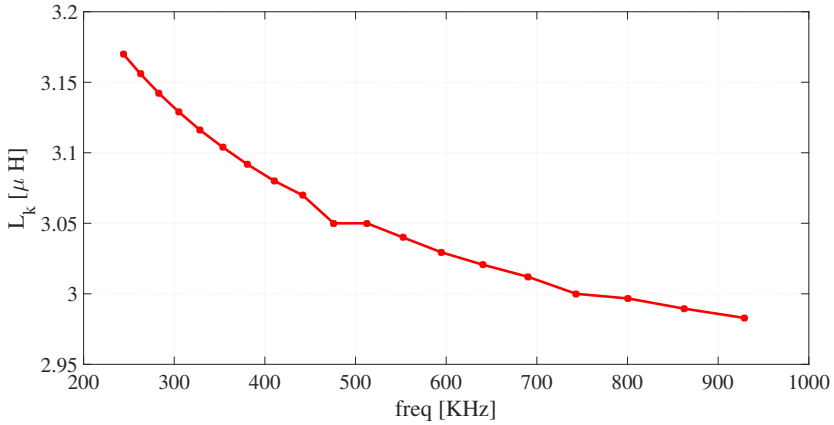


FIGURE 4.21: L_k of transformer prototype 20:1 realized in semi-interleaved structure.

The strategy proposed in section 4.4.3 is confirmed to be the best solution for the proposed HBPS-QR. Semi-interleaved structure is the optimal trade off between ac resistance and EMI issue. The optimal solution is reached by reducing the number of layers at primary side exposed directly to the secondary side, which reduced the static layer capacitance by enhancing the distance. In general the windings arrangement should results in the minimal energy associated with the electric field.

Chapter 5

Conclusion

5.1 Summary

Today, every digital load such as CPU, GPU, ASIC, etc., are powered by a Voltage Regulator Module (VRM), called also Point-of-Load converter (POL). These circuits are placed closed to the digital load to contain copper losses dissipation down to the digital load and ensuring all dynamic requirements. The problem is exacerbated with the current trend: reducing the size of all forms, increasing the efficiency of the system and increasing the power density. Investing of alternative power conversion topology is one of the approaches to increase the power conversion efficiency but actually the limitation imposed by the power distribution system architecture can not be overcome by the single dc dc converter. For this reason in the last few years the transition from 12 V to 48 V bus at rack level has been demonstrated to increase the overall rack efficiency resulting in optimized conversion system, if a single stage VRM is adopted from 48 V. Because of the rapid growth of cloud computing, energy consumption is still increasing and the 48 V bus will not carry the high current required. In this scenario a new power distribution architecture at rack level is proposed replacing the 48 V bus with 380 V bus. It is clear that boosting the overall data center power efficiency can be easier if less conversion stages are used. One possible solution is to adopt a single stage conversion from 380 V working as HV POL.

In the beginning, a general analysis of the constrains for HV POL converter is proposed to clarify the challenges of the converter. Different topologies are presented allowing us to compare the advantages and disadvantages between all topologies. Chapter 1 proposes an HV POL based on FBPS in ISOP configuration which simplified the transformer design by allowing a lower turns ratio yielding the dynamic requirement, but actually can not ensure phase shedding operation. Chapter 2 focuses on a new high step down isolated converter based on quasi resonant converter. The proposed solution is suitable to guide optimal design in different applications, for example 48 V VRM for the single stage 48 V approach, ensuring fast phase shedding and flat high efficiency curves even at light load condition. The proposed topology have been tested for VRM and DDR applications from 48 V.

Next a IBC converter is presented based on FBPS-QR with center tapped rectifier designed as first stage from 380 V to 12 V. The proposed converter can be regulated ensuring a stable 12 V for the VRM input voltage, with

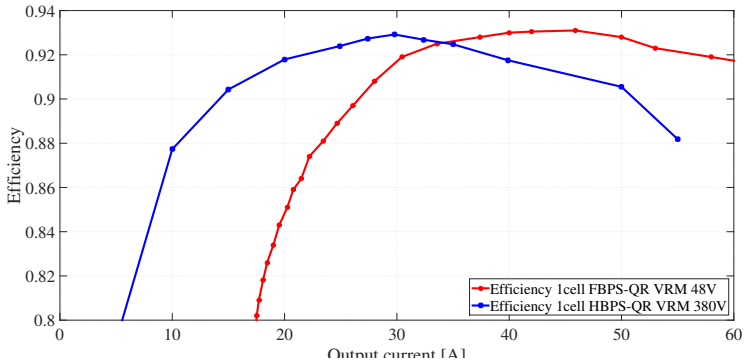


FIGURE 5.1: Efficiency comparison between 48 V VRM bases on FBPS-QR (in red) and 380 V VRM HBPS-QR (in blue).

high power density for a 600 W application. From the experimental results it follows that the only limitation comes from the primary side MOSFETs. Then an evaluation for FBPS-QR as HV POL is performed highlighting that the main limitation comes from the high voltage rating at primary side and the high transformer turns ratio. In attempt to improve the performance for primary side switches, improving the power capability and reducing the required transformer turns ratio, a multilevel HV POL based on double half bridge is studied. The proposed topology ensure higher voltage capability but actually the two powering modes create problem in light load condition increasing the voltage of the resonant transition.

In chapter 3 is presented an HV POL based on multilevel topology and resonant operation, ensuring ZVS both at primary and secondary side. Comparing with FBPS-QR the voltage stress on primary MOSFETS is half the voltage input, allowing to use lower voltage MOSFETs which are less affected from the C_{oss} nonlinear behavior. Moreover, half of turns ratio of the planar transformer is required comparing with FBPS-QR. The secondary side is implemented in a current-doubler topology where both the noncoupled and a coupled-inductor versions are proposed. Then, to demonstrate the wherewithal of the proposed solution experimental results are presented showing the high performance and the effectiveness of the proposed HV POL.

It is also interesting to compare the 380 V VRM based on HBPS-QR with 48 V VRM based on FBPS-QR. Both of them present the same dynamic performance. Both prototypes have slightly the same power density as reported in Fig. 2.20 and Fig. 3.22. The main difference comes from the efficiency comparison. As depicted in Fig. 5.1, 380 V VRM based on HBPS-QR has higher efficiency in light load due to lower copper losses at the primary side, the peak efficiency is slightly the same while in high load the secondary side losses are dominated in 380 V VRM because of different secondary side MOSFETs between the solutions. In general from the efficiency comparison it follows that by increasing the step down of the quasi-resonant converter, here proposed, the efficiency increases. In fact, overcoming the limitation regarding the ZVS at primary side, by using a multilevel topology, it is possible to step down from 380 V to 1.8 V with higher overall efficiency.

In chapter 4 are presented two different integrated magnetic solutions for

48 V VRM based on FBPS-QR proposed in chapter 2. The first integrated structure has a transformer and the current doubler inductances realized using a single core whilst the second integrates even the primary inductance in one core. Both integrated magnetic structures have been tested showing good efficiency performance with a very high power density. Chapter 4 also cover the modelling design and realization of the transformer for HV POL based on HBPS-QR converter. Experimental results confirm the equivalent electric structure of the transformer.

In conclusion, this research has proposed a quasi-resonant multilevel dc-dc converter, which performs a VRM function and provides a microprocessor core voltage rail directly from the 380 V bus. The proposed converter reaches high efficiency and power density. HBPS-QR presents higher ZVS capability at primary side, comparing with FBPS-QR, due to the independance from parasitic stray capacitance. Moreover, by using ZVS at secondary side HBPS-QR is able to achieve high efficiency with high dynamic performance, offering high power density, comparable with 48 V VRM converter. This is also obtained by using a multiphase approach that implements a novel current sharing technique. Moreover, a double current coupling inductor is proposed showing higher efficiency comparing with noncoupled configuration at the same transient responses. The proposed dc-dc quasi-resonant converter fully meets the goals of providing a direct conversion from 380 V to main computing low voltage rails with high current consumption reaching 93% peak efficiency.

Appendix A

Demonstrations

A.1 V_{out} in function of T_ϕ

Considering the equation of the resonant transition V_{ph1} depicted in Fig. 2.8, under hypothesis that: $V_{out}L_r << nV_{in}L_{out}$, $t_4 = 0$ and $t_5 - t_4 = T_\phi$:

$$v_{ph1}(t) = \frac{nV_{in}L_{out}}{L_r + n^2L_{out}} \left((1 - cos(\omega_r t)) - H\left(t - T_\phi\right)\left(1 - cos\left(\omega_r(t - T_\phi)\right)\right)\right). \quad \text{(A.1)}$$

from eq. A.1 it follows that the resonant time in $Mode\ B$ is $T_{rB} = \frac{T_\phi + T_r}{2}$ as demonstrated in Section 2.3.2.

By averaging eq. (2.12) over T_{rB} is possible to get the output voltage V_{out}:

$$\begin{aligned}
V_{out} &= f_{sw}\int_0^{T_{rB}} v_{ph1}(t)dt \\
&= f_{sw}\alpha\int_0^{T_{rB}} \left(1 - cos\left(\omega_r t\right)\right)dt - f_{sw}\alpha\int_{T_\phi}^{T_{rB}} \left(1 - cos\left(\omega_r(t - T_\phi)\right)\right)dt \\
&= f_{sw}\alpha\omega_r\left[T_\phi \right. \\
&\qquad \left. - sen\left(\omega_r\left(\frac{T_r}{2} + \frac{T_\phi}{2}\right)\right)/\omega_r + sen\left(\omega_r\left(\frac{T_r}{2} - \frac{T_\phi}{2}\right)\right)/\omega_r\right] \\
&= f_{sw}\alpha\left[T_\phi + sen\left(\omega_r\frac{T_\phi}{2}\right)/\omega_r + sen\left(\omega_r\frac{T_\phi}{2}\right)/\omega_r\right] \\
&= \left(\frac{\omega_r T_\phi + 2\sin\left(\omega_r\frac{T_\phi}{2}\right)}{2\pi}\right)\frac{nL_{out}V_{in}}{L_r + n^2L_{out}}\frac{f_{sw}}{f_r}
\end{aligned} \quad \text{(A.2)}$$

where $\alpha = \frac{nV_{in}L_{out} + V_{out}L_p}{L_p + n^2L_{out}}$ and is used the relations: $sen\left(\pi + x\right) = -sen(x)$ and $sen\left(\pi - x\right) = sen(x)$.

A.2 R_{eq} for small signal model of FBPS-QR

Here the demonstration of R_{eq} parameter for the small signal depicted in Fig. 2.14 analysis is carried out.

Considering the average value of v_{ph} in eq. (2.12) averaging its value over T_{rB} reported in eq. (2.13) is possible to derive:

$$
\begin{aligned}
V_{ph} &= \frac{f_{sw}}{f_r}\left(T_\phi f_{cc} + \frac{sin\left(\omega_{cc}\frac{T_\phi}{2}\right)}{\pi}\right)\frac{V_{out}L_r + nL_{out}V_{in}}{L_r + n^2L_{out}} \\
&\simeq \frac{f_{sw}}{f_r}\left(T_\phi f_{cc} + \frac{sin\left(\omega_{cc}\frac{T_\phi}{2}\right)}{\pi}\right)\frac{nL_{out}V_{in}}{L_r + n^2L_{out}}\frac{f_{sw}}{f_r},
\end{aligned}
\tag{A.3}
$$

where T_ϕ is given by eq. (2.10).

Now under hypothesis that I_{cir} and the inductance ripple ΔI_{Lout} do not depend from the variation of the output current is possible to calculate the equivalent resistance due to output current variation:

$$
\begin{aligned}
R_{eq} &= \frac{\partial V_{ph}}{\partial I_{out}} \\
&= \frac{f_{sw}}{f_r}\frac{nL_{out}V_{in}}{L_r + n^2L_{out}}\left(\frac{L_r f_{cc}}{2nV_{in}} + \frac{L_p}{2nV_{in}}\frac{2\pi f_{cc}}{2\pi}cos\left(\omega_{cc}\frac{T_\phi}{2}\right)\right) \\
&= \frac{f_{sw}}{f_r}\frac{nL_{out}V_{in}}{L_r + n^2L_{out}}\left(\frac{L_r f_{cc}}{2nV_{in}}\right)\left(1 + cos\left(\omega_{cc}\frac{T_\phi}{2}\right)\right) \\
&= f_{sw}\frac{L_{out}\cdot L_r}{2\left(L_r + n^2L_{out}\right)}\left(1 + cos\left(\frac{\omega_r T_\phi}{2}\right)\right).
\end{aligned}
\tag{A.4}
$$

A.3 V_{out} in function of ΔT_{start}

Rewriting the equation 2.20 as:

$$
V_{out} = \frac{f_{sw}}{f_{cc}}\frac{V_{out}L_r + nV_{in}L_{out}}{L_r + n^2L_{out}}\left(2\pi - cos^{-1}\left(\frac{1-\alpha^2}{1+\alpha^2}\right) - 2\alpha\right), \tag{A.5}
$$

where $\alpha = \frac{L_pL_{out}\Delta I\omega_{cc}}{V_{out}L_p + nV_{in}L_{out}}$ and using the following simplification $cos^{-1}(x) \simeq \frac{\pi}{2} - x$ is possible to derive:

$$
V_{out} = \frac{f_{sw}}{f_{cc}}\frac{V_{out}L_r + nV_{in}L_{out}}{L_r + n^2L_{out}}\left(2\pi - \frac{\pi}{2} + \left(\frac{1-\alpha^2}{1+\alpha_2}\right) - 2\alpha\right), \tag{A.6}
$$

applying the following simplification:

$$
\alpha \simeq \frac{L_pL_{out}\frac{nV_{in}}{L_p}\Delta T_{start}\omega_{cc}}{nV_{in}L_{out}} = \Delta T_{start}\omega_{cc}, \tag{A.7}
$$

and rewriting it in the following form:

$$
\frac{1-\alpha^2}{1+\alpha^2} \simeq \frac{1-\left(\Delta T_{start}\omega_{cc}\right)^2}{1+\left(\Delta T_{start}\omega_{cc}\right)^2} \tag{A.8}
$$

now is possible to rewrite the equation A.6.

$$V_{out} = \frac{f_{sw}}{f_{cc}} \frac{V_{out}L_r + nV_{in}L_{out}}{L_r + n^2 L_{out}} - f_{sw} \frac{2(V_{out}L_r + nV_{in}L_{out})}{4f_{cc}(L_r + n^2 L_{out})} + f_{sw} \frac{V_{out}L_r + nV_{in}L_{out}}{(L_r + n^2 L_{out})\omega_{cc}} - f_{sw} \frac{2(V_{out}L_r + nV_{in}L_{out})\Delta T_{start}}{L_r + n^2 L_{out}}, \tag{A.9}$$

deriving equation A.9 in T_{start} it easy to get the following equation:

$$\frac{\partial V_{ph1,2}}{\partial \Delta T_{SR}} = f_{sw} \frac{2\left(nV_{in}L_{out} + V_{out}L_r\right)}{L_r + n^2 L_{out}} \cdot \left(\frac{\omega_r^2 \Delta T_{SR}^2}{\omega_r^2 \Delta T_{SR}^2 + 1}\right). \tag{A.10}$$

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