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Ph.D. degree in electronic engeneering

Ph.D. Thesis

Ionizing radiation effects in nanoscale CMOS technologies exposed to ultra-high doses

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Abstract

This thesis studies the effects of radiation in nanoscale CMOS technologies exposed to ultra-high total ionizing doses (TID), up to 1 Grad(SiO_2). These extreme radiation levels are orders of magnitude higher that those typically experienced by space applications (where radiation effects in electronic are of concern). However, they can be found in some specific applications like the large-hadron-collider (LHC) of CERN, and, in particular, in its future upgrade, the high-luminosity LHC (HL-LHC). The study at such high doses has both revealed new phenomena, and has contributed to a better understanding of some of the already known radiation-induced effects.

The radiation response of four different CMOS technology nodes, *i.e.*, 130, 65, 40 and 28 nm, coming from different manufacturers, has been investigated in different conditions of temperature, bias, dose-rate and for different transistor's sizes, providing an unique and comprehensive set of data about the ultra-high TID-induced phenomena in modern CMOS technologies.

This study has confirmed that the thin gate oxide of nanoscale technologies is extremely robust to radiation, even at ultra-high doses. The main cause of performance degradation has been identified in the presence of auxiliary oxides such as shallow trench insulation oxides (STI) and spacers.

Both radiation-induced drain-to-source leakage current increase and radiation-induced narrow channel effect (RINCE) are caused by positive charge trapped in the STI. In this work, thanks to exposures to very high TID levels and to measurements performed in different conditions of temperature and bias, we show that the two effects are provoked by charge trapped in different locations along the trench oxide. Moreover, a new unexpected ultra-high-dose drain current increase (UCLI) effect, affecting narrow and long nMOS transistors, has been observed.

In-depth studies of the radiation-induced short channel effect (RISCE), related to the presence of the spacers, have shown that, at ultra-high doses, the degradation mechanism consists of two phases. A first increase of the series resistance, caused by the radiation-induced charge trapping in the spacers, is followed by a threshold voltage shift provoked by the transport of hydrogen ions from the spacers to the gate oxide. This model has been validated by several static measurements, TCAD simulations and charge pumping measurements. The dependencies of these effects on bias, temperature and size of the transistors have also been studied in detail.

Moreover, an unexpected true dose-rate sensitivity has been measured in both nMOS and pMOS transistors in 65 and 130 nm technologies, although the radiation response of MOS devices is considered insensitive to true dose-rate effects. The current degradation in samples irradiated at a dose-rate comparable to that expected in the HL-LHC is larger by a factor of ~ 2 than that measured in the typical qualification test, usually carried out with a much higher dose-rate. This is clearly of serious concern for the qualification of circuits designed for the particle detectors of the HL-LHC.

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Chapter 1

Introduction

Over the years, radiation-induced effects have been identified as a possible serious threat to electronic components, capable of temporarily or permanently compromising the normal operation of circuits, applications and systems [1–7]. A famous example of how radiation can strongly affect electronics is the failure of the communications satellite Telstar 1 in 1962. The cause of the failure was a malfunction of the control system caused by degradation in the performance of some BJT transistors after an increase in the radiation level in Van Allen's belt due to high altitude nuclear tests from both the USA and the USSR [8–10]. More recent examples are the robots that, over a period of more than six years, have failed in their attempt to locate and verify the condition of the melted fuel in the Fukushima power plant, due to the very high radiation levels reached after the accident in 2011 [11–13].

Radiation effects in electronics can be defined as any interaction between a particle and an electronic device that can perceptibly influence the expected behaviour of the device itself. These radiation-induced effects can be more or less relevant depending on both the type of the device (*e.g.* MOSFETs, BJTs, diodes, etc.) and the energy and type of the incident particle (*e.g.* electrons, protons, neutrons, photons, heavy ions, etc.) [14, 15]. However, for the purpose of this thesis, we are interested in those interactions that lead to an ionization of the material constituting the electronic component, in particular MOS transistors[1]. The ionization process generates electron-hole (e-h) pairs and when this occurs in parts of the device capable of retaining the generated charge (*e.g.* isolation material such as SiO_2), the effects produced by multiple interactions can accumulate over time. Therefore, although the impact of the charge generated by the interaction with a single particle may be completely negligible[2], it is important to assess the effect of prolonged exposure of the device to a particle stream. In fact,

[1]Non-ionizing processes can lead to the displacement of atoms from their position in the lattice, an effect called *displacement damage* (DD) [16–35], which however is generally of little concern for MOS transistors.

[2]When, however, the quantity of charge induced by a single radiation event, i.e. a single particle strike, is high enough to, for instance, corrupt the data stored in a register, we talk about *single event effects* (SEEs) [36–43]. It is important to notice that SEEs happen when e-h pairs are generated in the silicon rather than in the oxides.

as we will see, electronic devices operating in radiation environments are subject to numerous interactions with particles.

The number of the generated *e-h* pairs depends on the amount of energy per unit of mass released during the interaction between the particle and the material which is called *total-ionizing-dose* (TID). The TID-induced effects in CMOS technologies are the main topic of this thesis. Contributions to the deposited dose can come from both charged (heavy ions, protons, electrons, etc.) and neutral (neutrons, photons, etc.) particles. Although the unit of measure in the SI for the absorbed total dose is the **gray** (Gy) where $1\,\mathrm{Gy} = 1\,\mathrm{J\,kg^{-1}}$, it is still widely used the **rad** where $1\,\mathrm{rad} = 100\,\mathrm{ergs/g} = 0.01\,\mathrm{Gy}$. The value of the total dose deposited in a material depends on the material itself, therefore for both Gy and rad it should be referenced (*e.g.* Gy(GaAs), rad(SiO_2), etc.). Due to the presence of the gate oxide and other isolation oxides, CMOS technology is intrinsically sensitive to TID effects and this has led, over the years, to a large number of publications in the form of journal articles [see *e.g.*, 44–47, and references therein], short courses (*e.g.*, [48, 49]) and books (*e.g.*, [50, 51]). Since the silicon dioxide SiO_2 is still widely used as main isolation material in CMOS technology,the TID levels in this thesis will be referred to this material. In fact, despite more advanced technology, as the 28 nm, have a gate oxide made in *high-K* material, the parasitic oxides, that are the main cause of degradation in modern MOS transistors, are still produced using SiO_2.

Among all the environments in which radiation is a major threat to complex electronic systems, the large hadron collider (LHC) running at CERN [52], and in particular its future upgrade, the High Luminosity-LHC (HL-LHC) that should be operational in 2025 [53], is by far the one where the highest levels of TID are expected to be reached. Figure 1.1 shows a comparison of the estimated total dose levels for different applications while Table 1.1, summarizes the dose-rate, *i.e.*, the amount of TID per unit of time, for different environments [3, 6, 41, 54–64]. These comparisons, although approximate, clearly show that the HL-LHC is undoubtedly the harsher environment in terms of ionizing dose.

With its circumference of 27 km, the LHC is the largest and most powerful particle accelerator in the world. This machine is mainly used to accelerate two beams of protons in opposite directions to a energy of 7 TeV each and make them collide in 4 specific points along the ring. The set of electronic sensors and particle detectors placed in the collision points is called *experiment* and the main experiments along the ring are ATLAS (A Toroidal LHC ApparatuS), CMS (Compact Muon Solenoid), LHCb (Large Hadron Collider beauty) and ALICE (A Large Ion Collider Experiment). ATLAS and CMS, which measured the Higgs boson in 2012, have to withstand the highest radiation level.

Table 1.1: Order of magnitude of the maximum dose rates in different environments (approximately).

	Ground level	Low Orbit	LHC	HL-LHC
rads/day	$\leq 10^{-3}$	$\sim 10^{-3}$–10^{0}	$\sim 10^{3}$	$\sim 10^{5}$

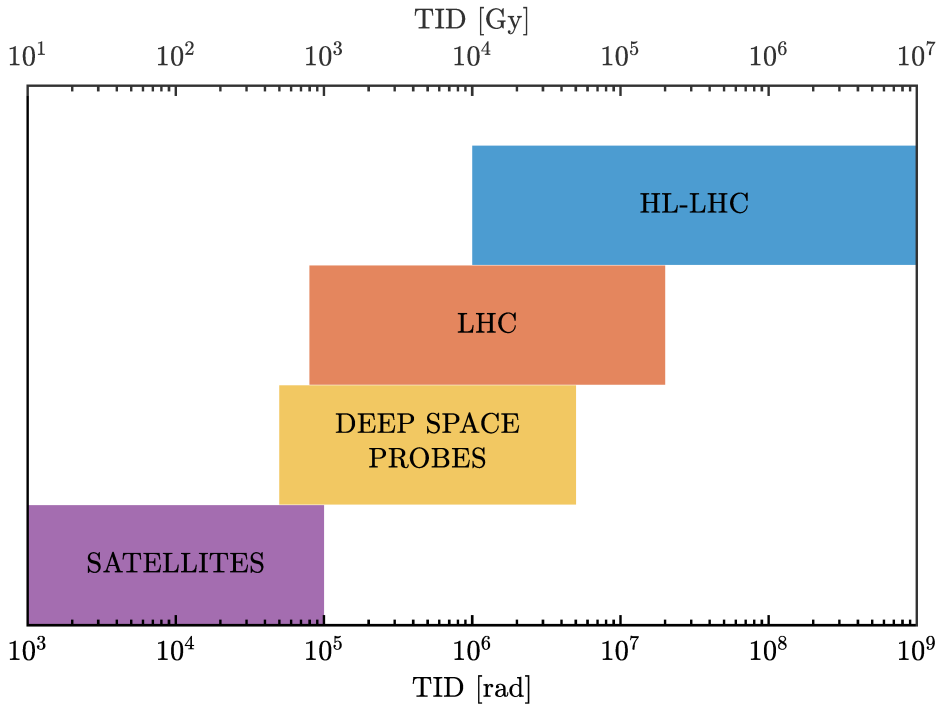
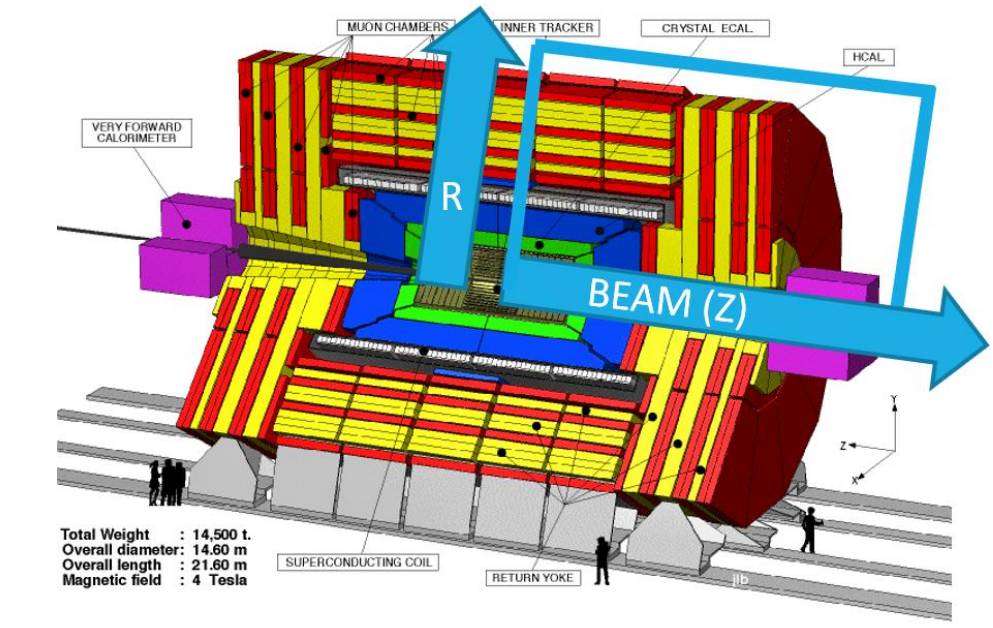


Figure 1.1: Approximate radiation levels in different applications. The maximum level of TID expected in the HL-LHC is more than one order of magnitude higher than that reached in the LHC and more than two orders of magnitude higher than that experienced by deep-space probes.

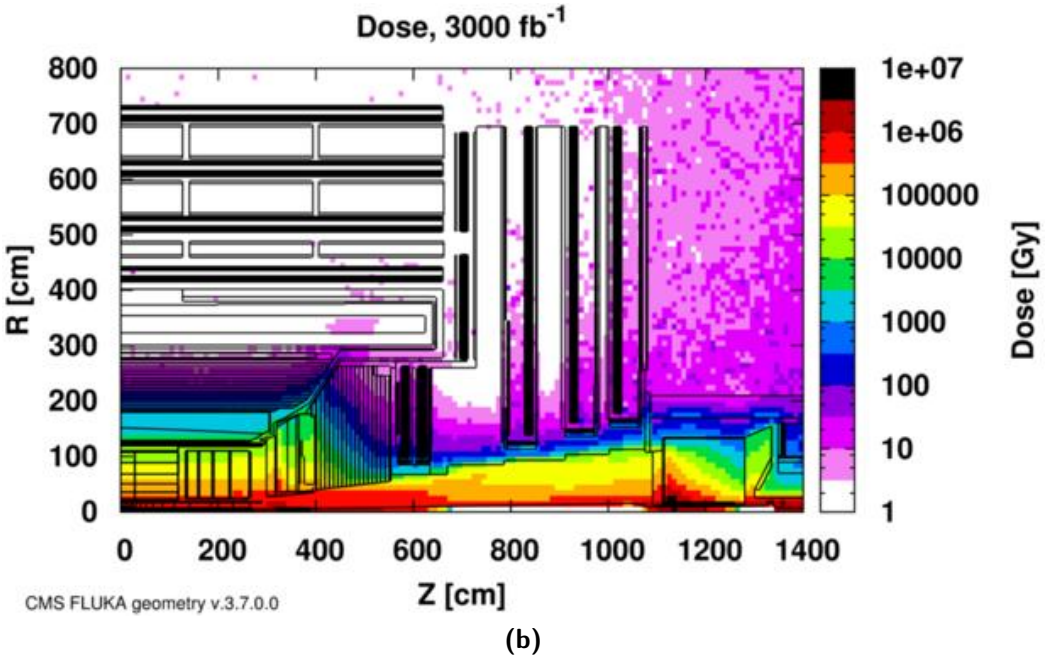
Since the LHC radiation environment is produced by the proton-proton inelastic interactions, an important parameter related to the TID is the number of interaction per unit of time, *i.e.*, the luminosity $\mathcal{L}$ [65]. The HL-LHC will reach a luminosity up to 5×10^{34} cm^{-2}s^{-1}, against the peak of 2.06×10^{34} cm^{-2}s^{-1} reached in the LHC in 2017 [66], and an integrated luminosity of $\sim$3000 fb^{-1} after 10 years of operations [67] where 1 barn $= 10^{-43}$ m^2. During this time the accumulation of ionizing dose will reach unprecedented levels, with peaks of 1 Grad(SiO$_2$) in the inner layer of particle detectors and an average dose rate of $\sim$ 0.3 Mrad(SiO$_2$)/day [68, 69], as shown, for CMS, in Figure 1.2. In particular, Figure 1.2a reproduce the internal part of CMS while Figure 1.2b reports the simulated dose after 10 years of operation, where it can be noticed that the inner layer of detectors is expected to be exposed to a TID ranging from 100 Mrad(SiO$_2$) to 1 Grad(SiO$_2$) [70]. For the purpose of this thesis we define TID levels from 10 Mrad(SiO$_2$) as *ultra-high* doses.

It is important to know that the devices installed in the areas of the experiments where the highest levels of radiation are reached (*i.e.*, those closest to the collision point), are kept at a temperature between ~ -30 and ~ -20 °C. As we will see, this has some important consequences in the study of their radiation response.

As in all modern digital and analog electronics, the use of CMOS technology is pervasive also in devices designed for high-energy physics. Because the development of a radiation-hard state-of-the-art semiconductor technology requires an



(a)



(b)

Figure 1.2: Simulation of the TID levels expected in CMS [53].

investment in multi-billion-dollar range, CERN relies on the use of commercial CMOS technologies for the design of the application-specific-integrated-circuits (ASICs) for particle detectors. However, since the market is largely dominated by applications where the radiation levels are low and the devices are expected to quickly become obsolete and often replaced, the semiconductor manufacturer companies give little or no importance to the radiation effects and, in general, they do not provide any information about the maximum total dose that a technology can withstand, leaving the task of qualifying the technology to the end user.

The present LHC detectors use the 250 nm CMOS technology, while the next generation of ASICs for the HL-LHC will be designed in 130 and 65 nm technologies. It was decided to move to more advanced nodes both because this allows greater computational power and increased functionality and because the technology scaling goes in the direction of improving the radiation hardness of MOS transistors. However, as it will be detailed throughout this thesis, MOS transistors exposed at the extreme HL-LHC TID levels show a severe reduction in their performance, due to various degradation phenomena, some of which only evident at ultra-high doses. The chips designed for the particle detectors have therefore to be made radiation-hard in the design phase. Hence, it is essential to understand the fundamental mechanisms of radiation-induced degradation in CMOS technology, in order to find some strategies to be adopted by the chip designers to prevent or reduce TID-induced failures in the detectors. This task is complicated by the extremely elaborate production process of modern CMOS technologies, the technical details of which are often confidential and therefore little known. Moreover, since the uniquely high TID levels in the LHC brought to light new degradation phenomena, qualification processes for electronic components designed to work in environments with lower levels of radiation, such as space missions, may not be suitable for assessing the real long-term degradation of components intended to be installed inside the particle accelerator. It is therefore necessary to define a dedicated qualification procedure to ensure that the produced devices can actually withstand the levels of TID expected in the HL-LHC.

This thesis studies the radiation response of nanoscale CMOS technologies exposed to ultra-high TID, as those that will be reached in the HL-LHC, focusing on both the understanding of the basic radiation-induced phenomena and how to ensure the radiation hardness of the integrated circuits designed for the particle detectors. This is in an attempt to present in an organic way the results of measurements made over several years at the CERN X-ray irradiation facility, which have produced a large amount of data in different technologies and for different irradiation conditions.

In particular, in Chapter 2 we will describe the basic of the TID-induced degradation mechanisms in MOS transistors, focusing on the generation and transport of the generated charge in SiO_2. This chapter summarizes the current understanding of the basic phenomena and is essential to introduce several concept that will be used throughout the thesis.

Chapter 3 details the experimental setup that has been used to obtain most of the results reported in this thesis and it describes some general aspects of the radiation response of modern CMOS technologies.

Chapter 4 introduces the effects related to the presence of the shallow-trench-isolation oxides. In particular, we will study the radiation-induced drain-to-source leakage current and the radiation-induced narrow channel effects, investigating the influence of size, bias and temperature for 4 different technology nodes, *i.e.*, 130, 65, 40 and 28 nm.

In Chapter 5 we analyse the impact of the spacers in transistor exposed to ultra-high doses. Particular emphasis will be placed on the description of a model capable of explaining both the behaviour of the MOS transistor during exposure and its post-irradiation evolution. This model will also be useful for explaining the radiation-induced short channels effects. As for the STI, the study will be conducted on four different technological nodes and for different condition of bias and temperature.

In Chapter 5 we show an unexpected dose-rate dependence of the radiation response in 65 and 130 nm CMOS technology. As we shall see, this phenomenon is a serious concern for the designers of the HL-LHC particle detectors.

In Chapter 7 we directly compare the radiation response of 3 different manufacturer in 65 nm CMOS technology and 4 different technology nodes. This comparison is extremely useful for assessing which CMOS process can be used in the design of the detectors and which could be a good candidate to replace the 65 nm technology.

Finally, Chapter 8 summarises the results obtained.

Chapter 2

Basic TID-Induced Mechanisms in MOS Devices

MOS transistors exposed to ionizing dose can show a strong variation in their nominal behaviour and, under certain conditions, a severe reduction of their performance. As far as TID effects are concerned, the main issues are caused by radiation-induced charge trapped both in the oxides present in the MOSFET structure and at the interface between these oxides and the silicon. This section will show in detail the current understanding in the formation and evolution of radiation-induced defects and trapped charge in MOS transistors. It is worth to be noted that the vast majority of articles published on the subject focus mainly on the study of radiation effects in the gate oxide. Although, as we will see, the radiation response of this oxide has become less critical in modern technologies, the basic principles set out in the continuation of this chapter remain valid for all the oxides in the MOS transistor. These basic effects have been extensively studied and several excellent books (*e.g.* [50, 51]), articles (*e.g.* [44, 46, 47]) and short courses summarize the main results obtained over the years.

2.1 How Photons Interact With Solid Materials

Photons interact with matter in essentially three ways, namely the Compton effect, the photoelectric effect, and pair production [48, 71, 72]. The probability of either of these effects to occur depends on the incident photon energy and on the target material. At 10 keV, which is the energy where the spectrum of the X-ray source used in the majority of the experiments reported in this thesis reaches its maximum intensity, photons interact with silicon ($Z_{Si} = 14$) and silicon dioxide ($Z_O = 8$) mainly through photoelectric effect, as shown in Figure 2.1.

In the photoelectric effect the incident photon is completely absorbed by the target atom, which in turn releases an electron. If the incident photons have enough energy to excite an electron in the K-shell, i.e. the closest shell to the nucleus, then 80% circa of the interactions will occur with electrons from the K-shell [48, 72, 73]. For Si, the energy of the K-Shell is 1838.9 eV [74]. Once the electron is released, an other electron coming from an external orbit (L-orbit if the electron belonged the K-shell) will drop in the vacated state, causing a

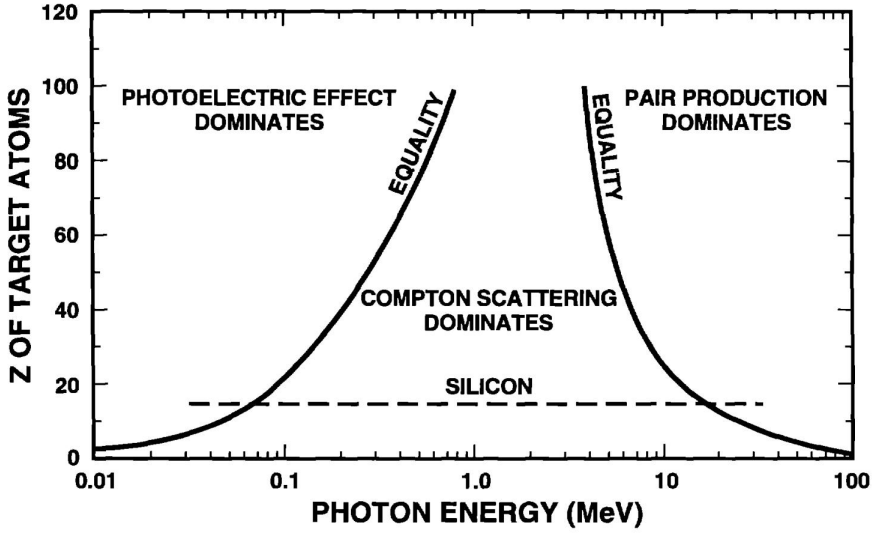


Figure 2.1: Relative weight of the main three photon-matter interaction processes at different energies and for several materials. At 10 keV photons interact with silicon (Z = 14) mainly through photoelectric effect (After [71]).

low-energy photon to be emitted. The process therefore ends with the formation of an electron-hole pair. Figure 2.2 shows a schematic representation of the photoelectric effect.

The electron emitted in the photoelectric process can in turn directly ionize many other atoms along its path. Therefore, the largest part of the ionization is due to electrons generated by the interaction between photons and atoms rather than the photon itself.

2.2 Trapping and Transport of Charge in Oxides

As we saw in the previous section, the ionizing radiation generates electron-hole pairs (*e*-*h* pairs) in the oxides present in the MOS structures. This charge can move through the oxide, where it can react with H atoms realising H^+ ions (protons), and be trapped in oxide traps. If this charge does not get trapped, it will eventually reach the oxide-silicon interface where it can be swept away from the oxide. When the released protons reach the interface, they react with Si – H,

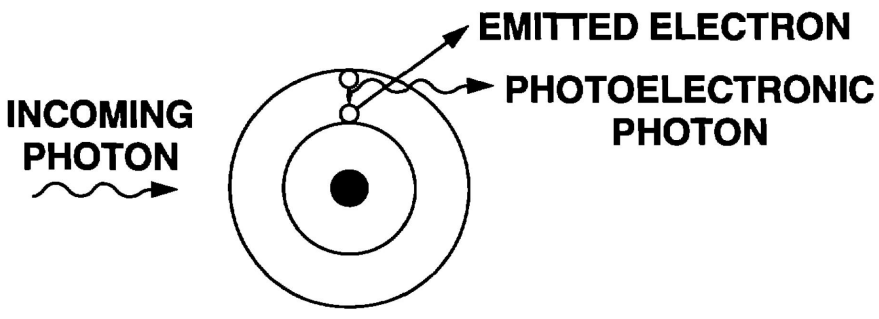


Figure 2.2: Schematic representation of the photoelectric effect.

forming interface traps.

Figure 2.3 shows a schematic representation of the band digram of a nMOS with *positive* voltage applied at the gate where the main phenomena that occur after the radiation-induced generation of *e*-*h* pairs in the gate oxide [46] are highlighted. Those phenomena are:

a) Radiation-induced electron-hole pairs creation

b) Recombination of a fraction of *e*-*h* pairs

c) Transport of holes in the oxide

d) Release of hydrogen ions (H^+)

e) Trapping of holes *close* to the Si/SiO_2 interface

f) Transport of H^+ and formation of interface traps

In the continuation of this chapter we will analyse in detail each of these points, providing a vision of the current understanding of the various phenomena.

2.2.1 Radiation-Induced Electron-Hole Pairs Creation

As reported in section 2.1, the electron emitted from an atom after the interaction between a photon and the material can, in turn, ionize other atoms, generating electron-hole pairs. In SiO_2 the pair density generated per rad is equal to $8.1 \times 10^{12}\,\text{pairs/cm}^3$ [48], with an *e*-*h* pair creation energy of 17 eV [75]. Part of this charge is however promptly recombined, as explained in the next subsection.

2.2.2 Electron-Hole Pairs Recombination

As soon as the electron-hole pairs are produced, a fraction of them will recombine. The fraction of holes that *escape* this recombination is called *charge yield*. Recombination occurs only in the very first moments after the generation of the *e*-*h* pairs, due to the relatively high mobility of electrons in silicon dioxide and hence their tendency to quickly move away from the pair generation point. The mobility of electrons in the SiO_2 is approximately $20\,\text{cm}^2\text{V}^{-1}\text{s}^{-1}$ at room temperature and $40\,\text{cm}^2\text{V}^{-1}\text{s}^{-1}$ at temperatures lower than $-100\,^\circ\text{C}$, with a saturation level of velocity around $1 \times 10^7\,\text{cm s}^{-1}$ for electric fields higher than $5 \times 10^5\,\text{V cm}^{-1}$ [76–79]. Therefore, even in an oxide with a thickness of 100 nm, electrons will exit from the SiO_2 in picoseconds, if the polarization voltage is high enough ($> 5\,\text{V}$ in this example) to let them reach the saturation velocity. Holes mobility significantly varies with temperature and the electric field in the oxide, E_{OX}, but it is in any case several orders of magnitude lower than the electron mobility [80–82] and therefore, with respect to electrons, they can be considered immobile, at least in the very first instants after the pairs' generation. For these reasons, after the initial recombination, the effects due to electrons are definitely negligible compared to those caused by holes.

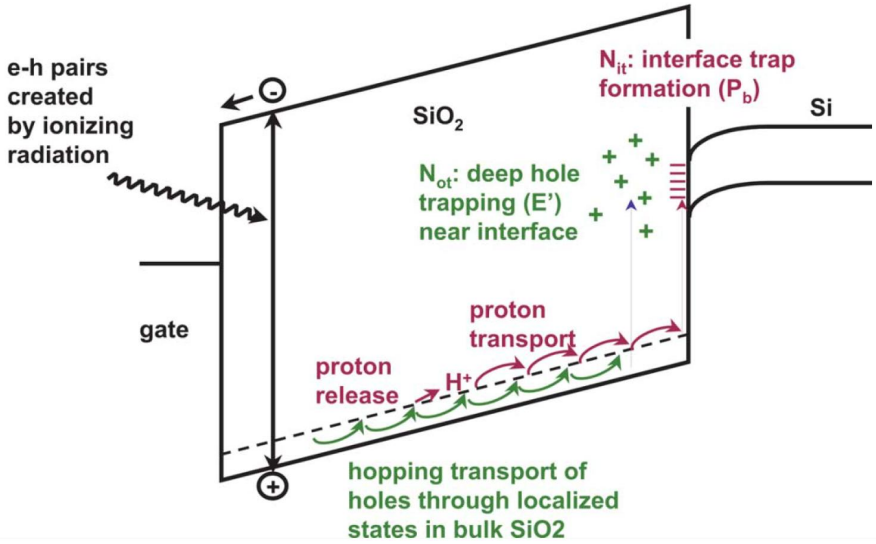


Figure 2.3: Schematic representation of the main TID-induced processes in the gate oxide of a nMOS transistors polarized with a positive gate bias, where the phenomena related to the formation of oxide-traps are reported in red while those related to the formation of traps at the interface are shown in green. (after [46]).

The charge yield is also affected by the average distance between the generated pairs, which is dependent on both the incident particle and the material, with an higher recombination probability for neighbouring pairs [44]. Two models of recombination have been analytically solved: the *geminate* recombination model, where the distance between different *e-h* pairs is supposed to be much larger than the distance between the electron and the hole of the same pair [44] and the *columnar* model, where the electron-hole pairs are generated in a dense column [83]. Since in the columnar model the *e-h* pairs are closer to each other than in the geminate model, the recombination rate is higher. Obviously, the actual recombination process for most of the materials and particles of interest is a combination of both the geminate and columnar model [44].

In Figure 2.4 the charge yield for different incident particles versus the electric field is reported. Note that for sufficiently large electric fields ($E >\sim 3\,\mathrm{MV\,cm^{-1}}$) the charge yield values of ^{60}Co and 10 keV X-rayare very close. Therefore, if the electric field in the oxide is high enough, this two sources are definitely comparable.

2.2.3 Transport of Holes in the Oxide

In the presence of an electric field, the holes having escaped the initial recombination move from the generation point to the negative electrode, i.e, toward the Si/SiO_2 interface in the case of a MOS transistor polarized with a positive gate voltage or toward the Si/gate interface if the gate is biases with a negative voltage. Holes transport in the SiO_2 through "polaron hopping", a rather complex phenomenon strongly dispersive [84] in time. A polaron is a quasi-particle that describes the interaction between the carrier and the surrounding atoms, leading

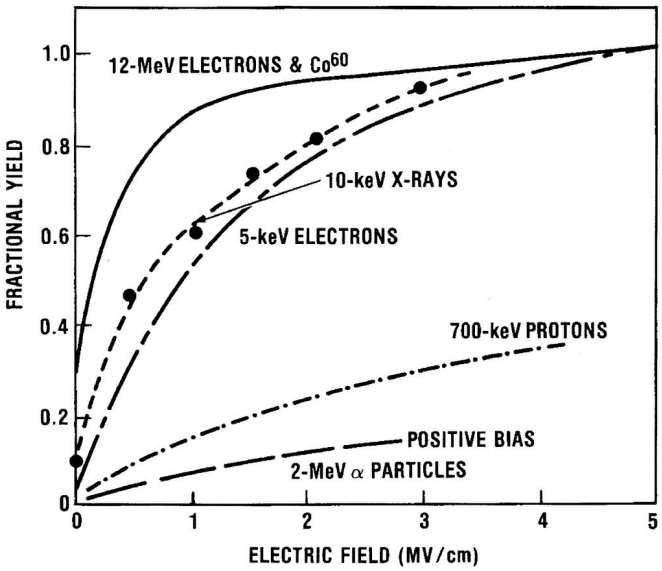


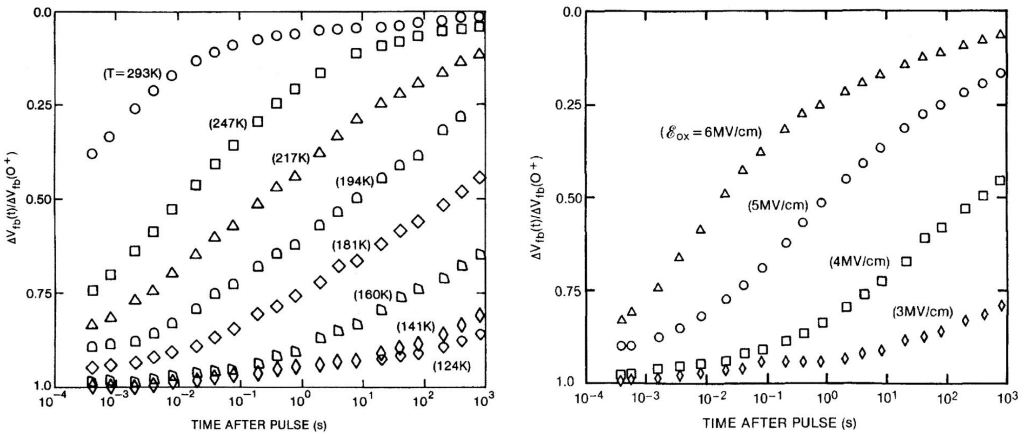
Figure 2.4: Charge yield for different incident particles (after [44]).

to a localized distortion of the structure of the material. Polarons move into the oxide "hopping" through localized shallow (i.e. close to the oxide valence band) states, randomly distributed but with an average distance of 1 nm [44]. Those states can be identified with the E'_δ centers [46, 85, 86] (see subsection 2.2.5).

It has been shown that the hole transport is strongly dependent on temperature [87] (Figure 2.5a), electric field [88] (Figure 2.5b) and oxide thickness [89]. Figures 2.5a and 2.5b report in fact the time needed to remove the effect of the radiation-induced trapped charge after an irradiation pulse, in different conditions of temperature and bias. In this kind of experiments, the gate oxide is irradiated with a relatively fast (4 µs) 12 MeV electron pulse [82], in order to minimize the time between the end of the generation/recombination process and the measurements. Note how, in Figure 2.5a and 2.5b, the flat band voltage is almost completely recovered to its pre-irradiation value for high temperature and/or high electric fields ($\Delta V_{fb}(t = 10^3 \text{ s})/\Delta V_{fb}(0^+) \sim 0$). This means that, in these oxides, little amount of holes are trapped in trapping centers (see Subsection 2.2.5). Moreover, it has been shown that the hole transit time varies as $\sim t_{OX}^4$ [44]. This means that in modern technologies, with a gate oxide thickness of few nanometers ($t_{OX} \ll 10\,\text{nm}$) and electric field $E_{OX} \geq 2\,\text{MeV}$, all the not-trapped holes can, at room temperature, be swept out from the gate oxide few instances after the *e-h* pairs generation.

Despite the dependence of the hole transport on temperature, electric field and oxide thickness, these parameters only change the time scale of the process and not its behaviour, that is therefore universal in nature [44, 90]. This can be seen in Figure 2.6, where the evolution in time of the flatband voltage shift $\Delta V_{\text{fb}}(t)$ is almost identical for different temperatures once plotted in the same scaled time $t/t_{1/2}$, where $t_{1/2}$ is the time at which $\Delta V_{fb}(t)/\Delta V_{fb}(0^+) = 0.5$ [82].

Several works (see [44] and the references within its III.C paragraph) have proved that the hole transport can be well described with the continuous time random walk (CTRW) formalism, useful to model hopping transport processes,



(a) Normalized flat band voltage recovery at different temperatures ($t_{OX} = 86.5\,\text{nm}$, $E = 1\,\text{MV cm}^{-1}$) [87].

(b) Normalized flat band voltage recovery at different electric fields ($t_{OX} = 86.5\,\text{nm}$, $T = 79\,\text{K}$) [88].

Figure 2.5: Normalize flat band voltage post-irradiation evolution at different temperatures and electric fields.

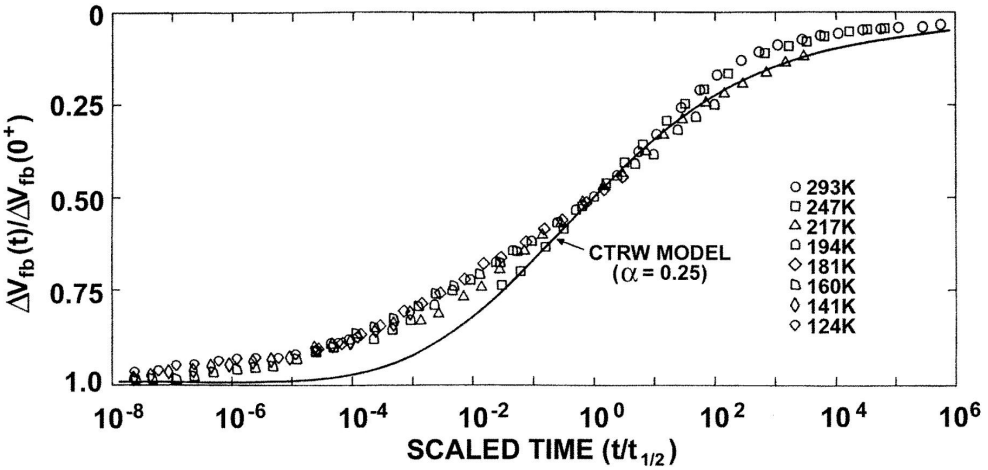


Figure 2.6: Normalized flatband voltage shift at different temperature and same scaled time. The behaviours are almost identical, proving the universality of the response. The solid line shows the fitting obtained with the CTRW model (after [90]).

as shown by the solid line in Figure 2.6. This model leads to describe the hole transport in the functional form $F(\alpha; t/t_s)$ [82], where only the time scale factor t_s is dependent on temperature, electric field and gate oxide, while α is independent on these parameters, as expected from the universality of the behaviour. For the gate oxide reported in Figure 2.6, $\alpha = 0.25$.

2.2.4 Release of Hydrogen Ions

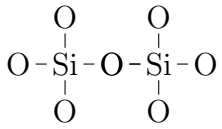
Since hydrogen is heavily used in the fabrication process of CMOS technology (see *e.g.* [91]), the holes moving into the oxide can react with the H present in the oxide, releasing hydrogen ions (H^+) [92]:

$$h^+ + H \text{ (in oxide)} \rightarrow H^+$$

Where h^+ is the hole. As we will see soon, the protons released in this process have a key role in the formation of interface traps.

2.2.5 Trapping of Holes Close to the Interface

Along their path from the bulk oxide to the interface, holes can be trapped in oxide traps, which can be mostly identified with oxygen vacancies in the SiO_2 structure. In amorphous silicon dioxide the Si atom is bound with four O atoms. Each of this four atoms is shared between two Si atoms, so the final structure can be described with this diagram:



or, in a more compact way:

$$\equiv \text{Si} - \text{O} - \text{Si} \equiv$$

where $\equiv$Si indicates the silicon atom bounded with three oxygen atoms. When an oxygen atom is missing, the two silicon atoms are weakly bonded together and a hole can easily break the bond and recombine with one of the two electrons of the Si – Si bond, a structure generally called E′ center. When the remaining electron of the Si – Si bond is shared between the two silicon atoms, we refer to it as an E'_δ center, with an energy level between 0.5 and 1 eV above the valence band [85]. As said in subsection 2.2.3, these traps have an important role in the hole transport. On the other hand, when the remaining electron is mainly associated with one of the two silicon, we obtain an asymmetrical positively charged structures [93]: a configuration called E'_γ center[1], with an energy level $\geq\sim 3$ eV [85]. This last process is depicted in Figure 2.7(a) and (b), where are respectively reported the Si – Si bond and the subsequent hole trapping [94].

[1]Since the E'_γ center, studied in amorphous SiO_2, have properties completely similar to those of the E'_1, studied instead in α-quartz, the two nomenclatures are sometimes used interchangeably. However, when referring to the oxides present in the MOS transistor, the first is the correct one.

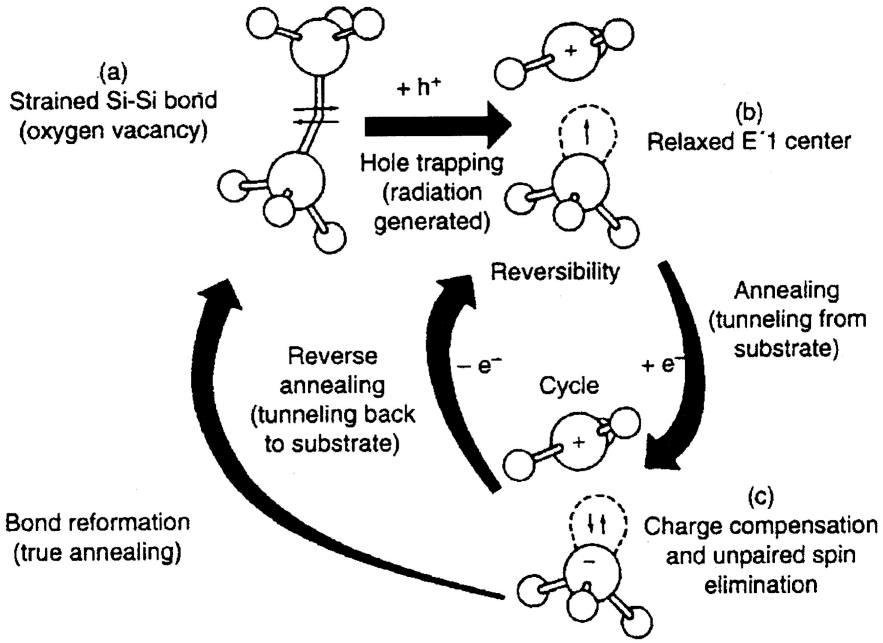


Figure 2.7: Generation and annealing of oxide trapped charge (after [94]).

Figure 2.7 also shows the annealing processes, reversible or permanent, that can neutralize the positive trapped charge. When an electron tunnelling from the silicon substrate recombines with the positively charged silicon atom in the oxide, the Si - Si bond is reformed and the annealing is permanent (Figure 2.7(c)→(a)). On the other hand, an electron can also tunnel to the neutral silicon atom [94], a process that can be reversed applying a negative bias (Figure 2.7(b)) to the gate.

The probability that a charge trapped in the oxide can be neutralized by an electron coming from the silicon bulk is clearly dependent on the distance between the oxide trap and the interface. Oxide traps relatively far from the interface have a very small probability to be reached by an electron coming from the Si and therefore the charge trapped in these defects is annealed only in relatively long times. On the other hand, if an oxide trap is close to the interface, it can easily exchange electrons with the silicon substrate, so it can quickly react to any change of bias, switching back and forth from the positive charged to the neutral configuration. This kind of oxide traps are called border traps [95, 96], as formalized by Fleetwood in [97], where, as a rule of thumb, all the E′ centers within 3 nm from the Si/SiO_2 interface are considered as border traps.

The main effect related to the presence of charge trapped in the oxide is a negative threshold voltage shift, both for nMOS, where positive charges attract electrons from the silicon bulk to the Si/SiO_2 interface and therefore to the channel, and pMOS transistors, where the holes in the channel are repelled by the holes trapped in the oxide. The same effect can also be seen as a variation of the flat band voltage V_{FB}, i.e. the voltage needed to be applied to the gate in order to flat the energy band diagram of the semiconductor. The variation of the flat band voltage can be expressed as [50, 75, 98–102]:

$$\Delta V_{FB} = -\frac{1}{C_{OX}} \int_0^{t_{OX}} \frac{x}{t_{ox}} \rho_{OX}(x)\, dx = -\frac{1}{\epsilon_{OX}} \int_0^{t_{OX}} x \rho_{OX}(x)\, dx \qquad (2.1)$$

where t_{OX} is the oxide thickness, $C_{OX} = \epsilon_{OX}/t_{OX}$ is the oxide capacitance per unit area, ρ_{OX} is the density of the charge trapped in the oxide and the reference point ($x = 0$) is taken at the gate/SiO_2 interface. An increase in the amount of charge trapped in the gate oxide produces a decrease in the flat band voltage and, hence, a decrease in the threshold voltage since (see e.g. [103]):

$$V_T = V_{FB} + 2\phi_f + \frac{\sqrt{2qN_A\epsilon_{Si}}}{C_{OX}}\sqrt{2\phi_f} \tag{2.2}$$

where

$$\phi_f = V_{th} \ln\left(\frac{N_A}{n_i}\right) \tag{2.3}$$

and N_A is the doping density in the semiconductor, n_i is the intrinsic carrier concentration and $V_{th} = kT/q$ is the thermal voltage, where k is the Boltzmann's constant and T is the temperature in kelvin.

If we consider a constant concentration $\rho_{OX}(x) = \bar{\rho}_{OX}$, Eq. 2.1, can be expressed as:

$$\Delta V_{FB} = -\frac{\bar{\rho}_{OX}}{\epsilon_{OX}} \int_0^{t_{OX}} x(x)\, dx = -\frac{\bar{\rho}_{OX}}{2\epsilon_{OX}} t_{OX}^2 \tag{2.4}$$

From Eq. 2.4 we can see how the shift in flat band voltage, and in the threshold voltage, is quadratically dependent on the oxide thickness t_{OX}. The extreme scaling of CMOS technology goes therefore in the direction of a constant increase in the radiation hardness of the gate oxide, at least for the effects related to the charge trapped in the oxide. This behaviour has been confirmed for gate oxides thicker than 20 nm, while for thinner gate oxides the dependence becomes even steeper, as reported in Figure 2.8, where the flat band voltage shift in MOS capacitors [104] and the threshold voltage shift in MOSFETs [105] have been measured at $T \simeq 80$ K. In fact, as reported in [106], at very low temperatures holes are "frozen" in the generation point, preventing the formation of interface traps (see subsection 2.2.6). In this condition the only contribution to the radiation-induced flat band and threshold voltage shift comes from the charge trapped in the oxide.

In [104] and [105] the further reduction in the flat band and voltage shift is explained by the increasing probability of neutralization of holes trapped in the oxides by electrons tunnelling from both the silicon substrate and the gate[2].

2.2.6 Transport of Hydrogen Ions and Formation of Interface Traps

As said in subsection 2.2.4, holes moving into the SiO_2 can react with Si – H bonds in the bulk of the oxide, releasing hydrogen ions H^+. Under a positive electric field, these ions will eventually reach the Si/SiO_2 interface[3] where they react with Si – H bonds, forming a H^2 and leaving a silicon dangling bond, i.e. a

[2]Note that the tunnelling of electrons from the gate or the silicon substrate to the gate oxide is equivalent to the tunnelling of holes from the gate oxide to the the gate or to the silicon substrate.

[3]Under negative bias the H^+ions will reach the Si/gate interface, where they are less critical. This is the reason way pMOS were, in old technologies, much more robust than nMOS.

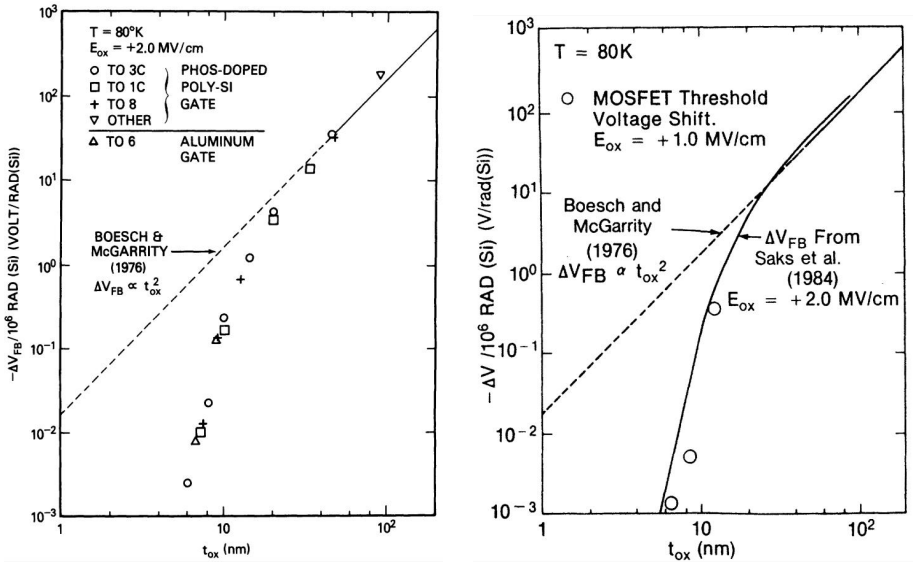


Figure 2.8: Flat band voltage shift per Mrad(SiO_2) in MOS capacitors (a) [104] and threshold voltage shift per Mrad(SiO_2) in MOSFETs (b) [105] measured for several gate oxide thickness and with $T = 80\,\mathrm{K}$. For gate oxide thicker than $\sim 20\,\mathrm{nm}$ the behaviour is well described by Eq.2.4, while for thinner oxides the voltage shift is significantly smaller than the one expected from the t_{OX}^2 dependency.

silicon atom bonded with three silicon atoms and with an unparied electron at the Si/SiO_2 interface, as reported in Figure 2.9. This defect is called P_b center [107–112].

The transport and the formation of interface traps is strongly dependent on both temperature and electric field, as can be seen in Figure 2.10a and 2.10b, respectively, where the density of interface states D_{it} in states/cm^{2}eV and N_{it} in states/cm^2 is reported. These figures clearly show that the formation of interface traps takes much more time than the trapping/annealing of oxide-trapped charge. At room temperature the process needs more than $\sim 1000\,\mathrm{s}$ to reach a saturation value. Moreover, the annealing of interface traps can be extremely slow, and evident only at relatively high temperatures [113, 114].

As for the oxide-trapped charge, the density of interface traps is strongly dependent on the oxide thickness, with thin oxides having a better response in terms of radiation hardness [116, 117].

P_b centers can either accept or donate an electron depending on their position with respect to both the midgap E_M and the Fermi E_F level. As schematically reported in Figure 2.11, the defects in the bottom part of the band are mostly donor-like, i.e. they tend to give an electron when above the Fermi level, becoming positive, while are neutral below E_F. On the other hand the P_b centers above the midgap are acceptor-like, going from negative to neutral respectively below and above the Fermi level [111, 112]. Therefore, while the charge trapped in the oxide is always positive, the sign of the charge trapped at the interface is dependent on the bias applied at the gate (and at the other terminals). This means that in

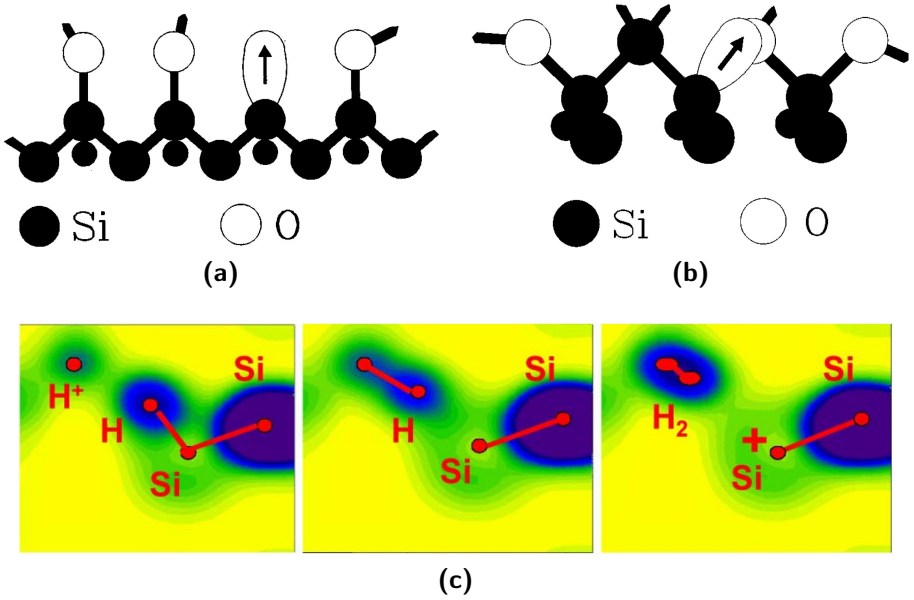
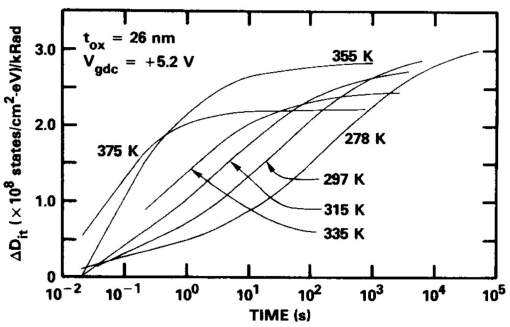
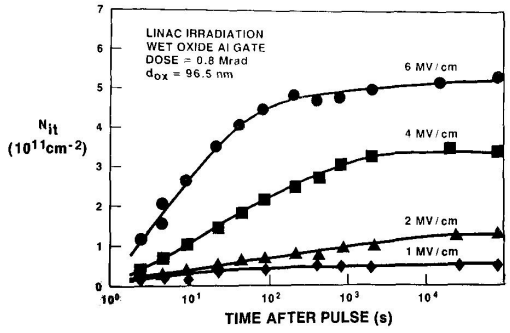


Figure 2.9: Schematic representation of P_b centers at the (111) (a) and (100) (b) Si/SiO_2 interface [107] and their formation (c) [47, 108]. In (c) it is also reported the electron density, where darker regions correspond to an higher electron density.

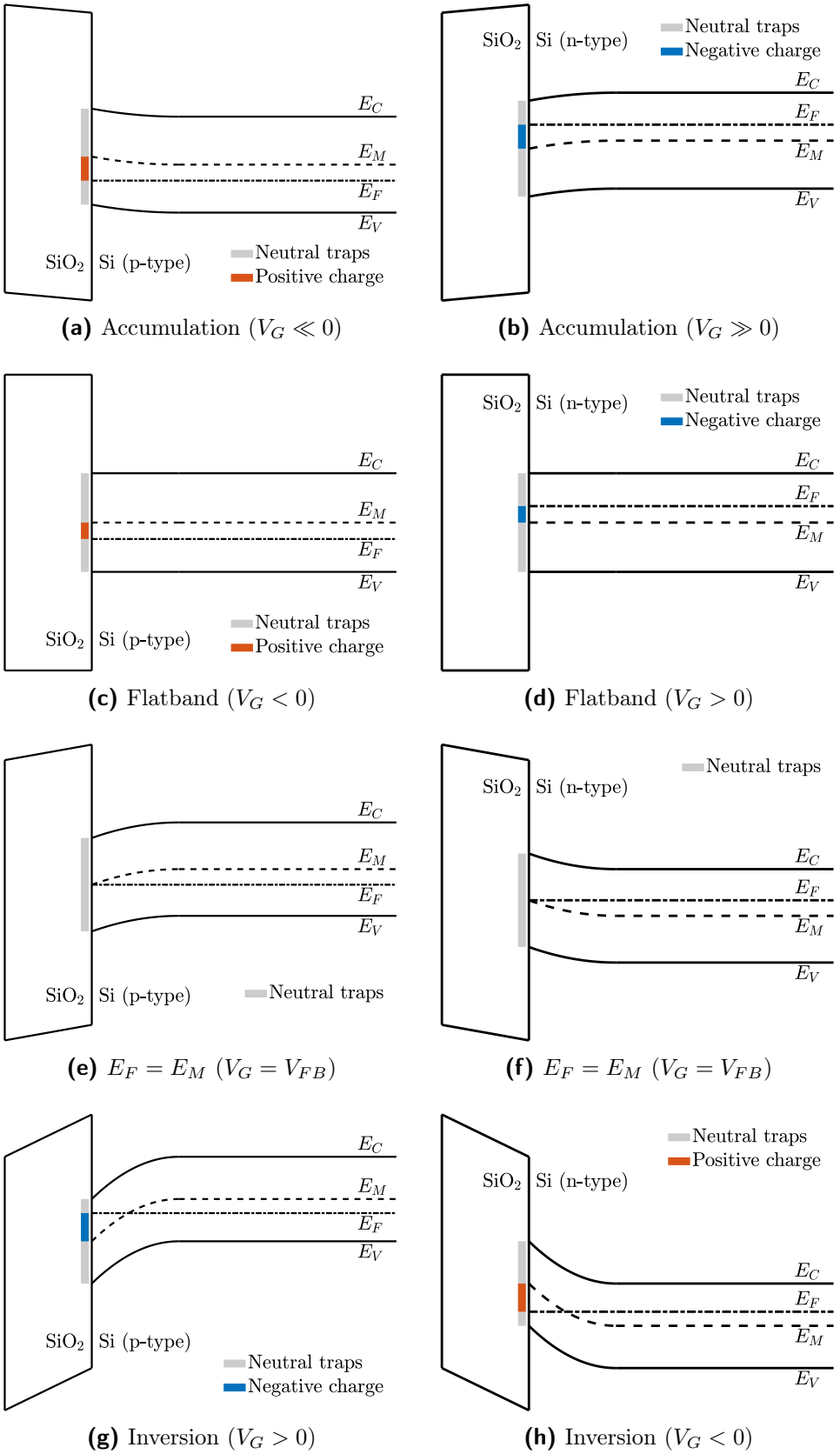


(a) Evolution on of the interface traps density at different temperatures on MOSFETs irradiated with six 1.5 µs 40 MeV electron pulses, providing 50 krad(SiO_2) each [115].



(b) Buildup of interface traps at room temperature (295 K) in Al-gate MOS capacitors with $t_{OX} = 96.5$ nm. The samples were irradiated to 800 krad(SiO_2) with a 4 µs 13 MeV pulse [112].

Figure 2.10: Interface traps buildup at different temperatures and electric fields.



(a) Accumulation ($V_G \ll 0$)

(b) Accumulation ($V_G \gg 0$)

(c) Flatband ($V_G < 0$)

(d) Flatband ($V_G > 0$)

(e) $E_F = E_M$ ($V_G = V_{FB}$)

(f) $E_F = E_M$ ($V_G = V_{FB}$)

(g) Inversion ($V_G > 0$)

(h) Inversion ($V_G < 0$)

Figure 2.11: Schematic representation of the interface traps sign at different voltages for p-type (left) and n-type (right) silicon substrates.

nMOS transistors, which typically have a gate voltage ≥ 0, the interface traps are mostly negatively charged, while in pMOS they are predominantly positive. The different sign in the trapped charge provokes a substantial difference in the overall radiation response of nMOS and pMOS transistors, with the latter usually more damaged by the TID. In fact, in pMOS transistors both the oxide- and the interface-trapped charge are positive and therefore their effects accumulate. On the other hand, in nMOS the charge trapped in the oxide and at the interface at least partially compensate.

Chapter 3

General Elements

In this chapter we will introduce some general elements that will help us to better understand the results shown in the following chapters. In particular, we will detail the setup used to perform most of the experiments reported in this thesis, we will introduce the main parameters that describe the radiation response of MOS transistors and we will highlight what are the elements that make modern CMOS technologies sensitive to ionizing radiation.

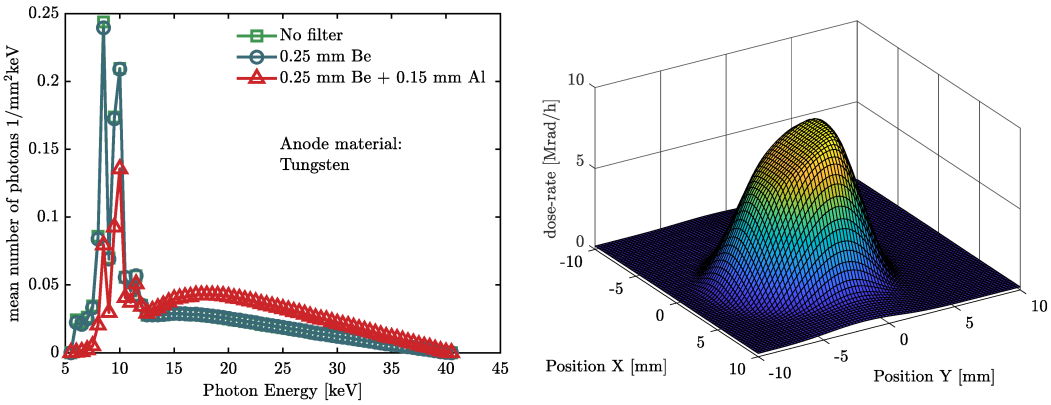
3.1 Experimental Setup

The extremely high levels of TID required for HL-LHC applications combined with the need to maintain the duration of irradiation test within a reasonable time span require the use of a radiation source capable of providing very high dose-rates. Despite radiation sources based on ^{60}Co are still a reference and some of the experiments reported in this thesis were performed with a ^{60}Co source, the maximum dose-rate reached is, in general, too low for our purposes. Therefore, the irradiation facility of the Electronics Systems for Experiments (ESE) group at CERN uses two Seifert RP149 systems with a 10-keV X-ray irradiation source, that allows to reach very high dose-rates (in our case up to 10 Mrad(SiO_2)/h) [118]. This irradiation system has very similar characteristic to that developed in 1982 by Palkuti and LePage [119].

Each of the two systems hosted in the X-ray CERN facility consists of:

- an X-ray tube using a Tungsten target with a Beryllium window of 250 µm to seal the tube and an Aluminium filter of 150 µm, generating an X-rays spectrum with a peak at 10 keV, as reported in Figure 3.1a [120]. Details on the tube operation can be found in [119].
- a cabinet to shield the external environment from the scattered X-rays.

Changing the tube-target distance and the power at which the tube is supplied, regulated by both the input voltage V_{tube} and the current I_{tube}, it is possible to select the dose-rate at which to irradiate the device-under-test DUT. The dose-rate DR is defined as $DR = \text{TID}/\text{time}$ and, for our purposes, is often measured in Mrad(SiO_2)/h.



(a) X-ray spectrum generated by irradiation system with and without the Beryllium and Aluminum filters. The applied voltage to source the tube is 40 kV [120].

(b) Map of the dose-rate produced by the X-ray tube at 2 cm form the target with V_{tube} = 40 kV and I_{tube} = 50 mA. In this case the diode was maintained in a fixed position and the beam was moved in steps of 0.1 mm.

Figure 3.1: Spectrum and dose rate of the X-ray irradiation system.

In order to measure the dose-rate of the beam, a pre-calibrated positive intrinsic negative (PIN) photo-diode is used [119, 121]. Its current, when reversely biased, depends on the electron-hole pairs generated in the depletion region and, in turn, on the energy of the incident photons. The dose-rate DR is obtained subtracting from the measured current I_{exposed} the background value $I_{\text{dark current}}$, measured when the PIN diode is not exposed and multiplying the results by a provided coefficient β, as shown in Equation 3.1.

$$DR = \beta \cdot (I_{\text{exposed}} - I_{\text{dark current}}) = \beta \cdot I_{\text{photo-current}} \tag{3.1}$$

Changing the relative position between the tube and the calibration diode it is possible to obtain a map of the spatial distribution of the dose-rate inside the cabinet. Figure 3.1b shows the dose-rate map obtained with a distance between the beam and the photo-diode of 2 cm and an input voltage and current respectively equal to 40 kV and 50 mA. Note that the peak of the dose-rate used to irradiate the transistors is ∼10 Mrad(SiO_2)/h, a value that allows to reach 1 Grad(SiO_2) in just ∼ 4 days. The dose-rate provided by the X-ray tube is 3 orders of magnitude higher than the 0.01 Mrad(SiO_2)/h expected in the HL-LHC (see Chapter 1). Despite the radiation response of CMOS technology is known to be independent of dose-rate [122, 123], in Section 6 we will show recent and surprising results suggesting a dose-rate sensitivity in MOS transistors exposed at ultra-high doses.

This irradiation system is used to expose electronic devices, in our case mainly MOS transistors, to total ionizing dose. The transistors to be measured are on a silicon die fabricated as an ASIC and are usually arranged in arrays properly designed to study a particular aspect of the radiation response. Figures 3.2a shows the 3 arrays belonging to one of these ASICs. Each array consists in two columns of pads and each pad is connected to one of the terminals of the device,

as described in the captions on the sides of the arrays. To maximize the number of MOSFETs contained in an array, several devices belonging on the same array often share the source, gate and bulk terminal. Custom electrostatic-discharge (ESD) protection circuits have been designed and implemented to protect the devices, except in the case of arrays designed to perform specific measure (*e.g.*charge pumping), that can be done only in structures without ESD protections.

In order to measure these ASICs, a probe card provided with needles of few µm of diameter is used. The contact between the needles and the ASIC is made manually, thanks to a microscope and CCD camera connected to a screen placed outside the cabinet. Figure 3.2b reports a picture of the screen showing the needles approaching the ASIC, where 6 columns of pads can be observed, corresponding to the 3 arrays of Figure 3.2a. When the needles touch the surface of the pads, they remove the thin layer of oxide placed on top of the pads and reach the underlying metal, providing the electrical contact, as shown in Figures 3.2c.

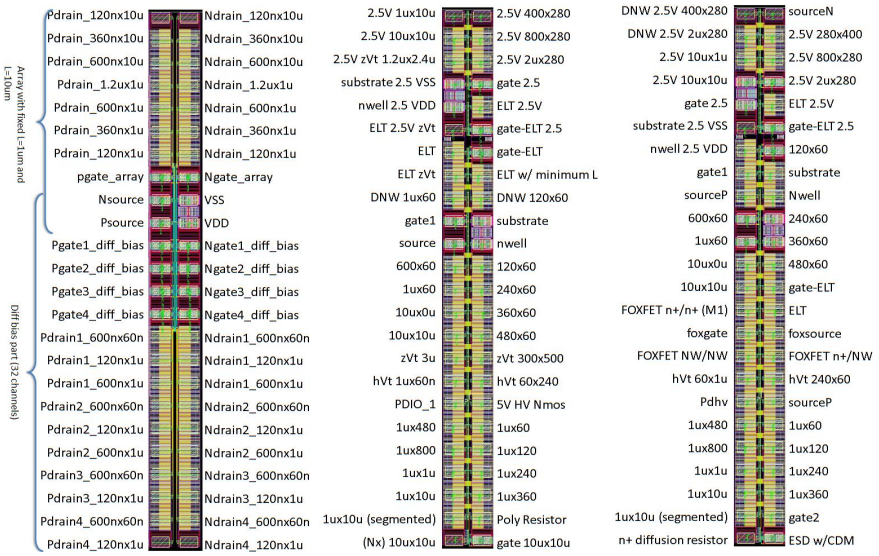
In order to contact the pad with the needles, the ASIC is placed on a copper block which is in turn placed on a thermal chuck whose position is manually adjusted in the three directions thanks to an external controller. Good thermal exchange and electrical isolation between the chip/block and block/thermal chuck surfaces is ensured by a thermal pad, *i.e.*, a layer of a material that ensures both good thermal conductivity and electric isolation. As said before, the position of the DUT with respect to the position of the needles is verified with a microscope connected to a CCD camera. The thermal chuck can also regulate the temperature of the DUT, ranging from $-50\,^{\circ}\mathrm{C}$ to $200\,^{\circ}\mathrm{C}$. To perform measurements at $T \ll 0\,^{\circ}\mathrm{C}$ the cabinet is saturated of dry air, decreasing the dew point and therefore avoiding the formation of ice.

Figure 3.3a shows a picture taken inside the cabinet of the X-ray irradiation system, where the main elements are highlighted.

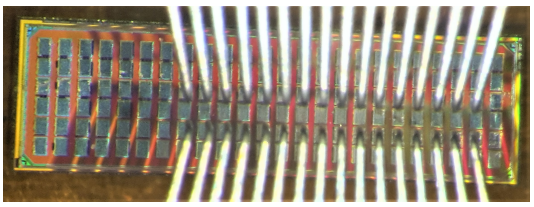
The needles are connected inside the probe card to triaxial Lemo connectors, which are in turn connected through triaxial Lemo cables to a switching matrix Keithley 707A hosting 3 7072 Matrix cards with 12 outputs each, providing a total of 36 outputs (see Figure 3.3b). The switching matrix has the essential role to route the signals coming from the devices to the 6 source-measure units (SMU) of the Keithley 4200A-SCS semiconductor analyzer, a powerful instrument for the characterization of electronic devices. Each of these SMUs allows to both sourcing and measuring at the same time a device. In our case they are used to sweep a voltage and to measure the relative current (for instance to perform $I_D\,(V_G)$ and $I_D\,(V_D)$ measurements). Figure 3.4a schematically displays the connection between the SMUs and the DUT obtained through the switching matrix. In this case 3 SMUs are used to measure the second device, as indicated by the coloured dots.

As shown in Figure 3.4b, in addition to the 6 inputs used to connect the SMUs, the switching matrix has 2 more input channels, sometimes used to perform CV measurements thanks to the capacitance-voltage unit (CVU) of the 4200A but more often connected to a voltage generator in order to bias the DUT between measurements, *i.e.*,during the irradiation or annealing steps.

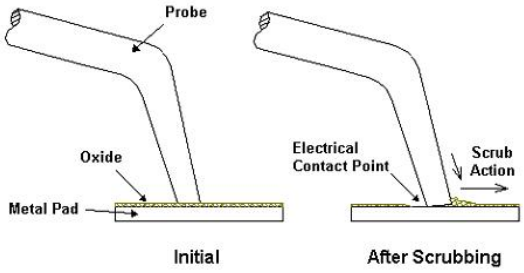
The typical irradiation stress test consists in a series of subsequent steps of



(a) A test chip can contain several devices with different characteristics, which is essential for studying the dependence of the radiation response on the various parameters of the MOS transistor.

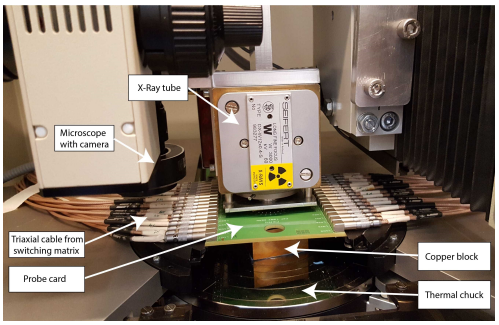


(b) A picture of the chip described in Figure 3.2a contacted by the needles.

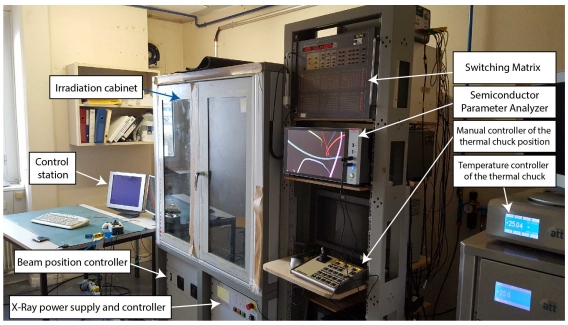


(c) When the needles touch the surface of the pad they remove the surface oxide layer thus reaching the metal and providing an electrical contact point.

Figure 3.2: Example of test chip and probe card.

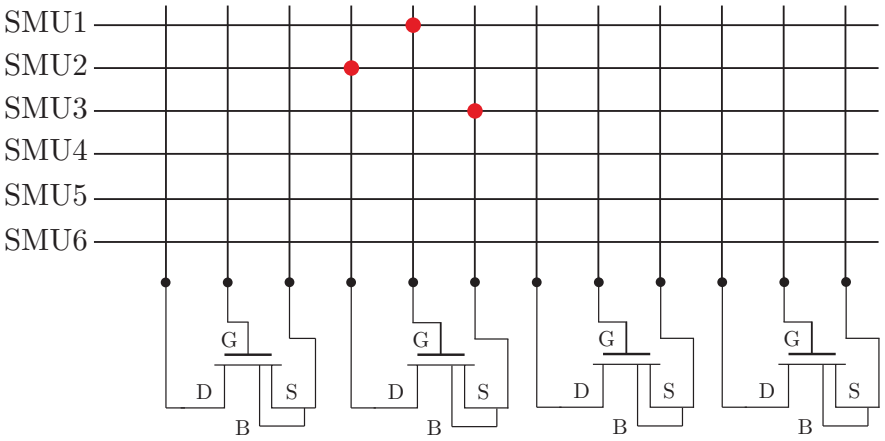


(a) Inside the irradiation cabinet

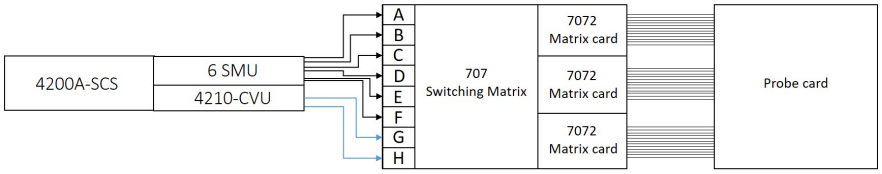


(b) Irradiation cabinet and insrtuments used to measure the DUT.

Figure 3.3: CERN X-ray irradiation setup



(a) Schematic representation of the connections between the SMU and the DUT through the switching matrix, whose role here is represented by the coloured dots.



(b) Overview of the experimental setup.

Figure 3.4: Switching matrix and its connection between the probe card and the semiconductor analyzer.

irradiation and measurements, as illustrated in Figure 3.5. At the end of each measurement step, in which all the devices of interest are characterized, the desired polarization is applied to the DUT and the chip is irradiated up to a certain total dose and then measured again. The TID steps are defined before starting the test, which is carried out in a completely automated manner thanks to a custom LabVIEW software developed in the EP-ESE-ME section of CERN.

In order to measure the post-exposure evolution of the DUT, at the end of all the irradiation/measurement steps the ASIC is removed from the probe card inside the X-ray machine and connected to an external setup, very similar to the one depicted in Figure 3.4b but with a HP-4155B semiconductor analyzer.

The experimental setups described in this chapter have been exploited to study the details of the radiation response of CMOS technologies in different conditions of bias, temperature and dose rate, providing a unique set of results in several CMOS technologies produced by different manufacturers.

3.2 Main Parameters and Extraction Methods

To describe the radiation response of MOS transistors we will use a series of parameters extracted from $I_D\,(V_G)$ measurements performed on the devices under test. Since for some of these parameters there are different extraction methods, it is important to describe how they are obtained.

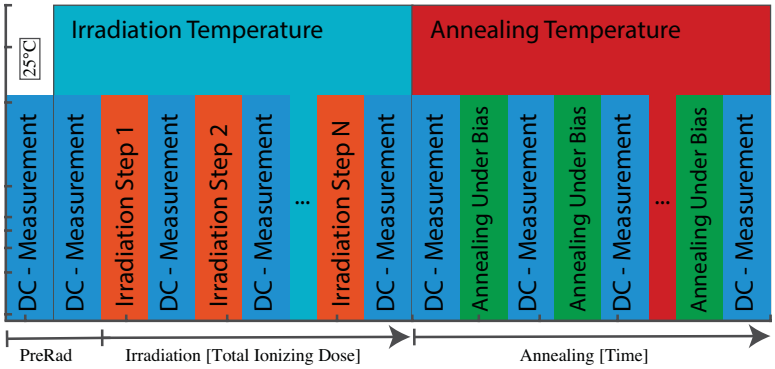


Figure 3.5: Typical measurement procedure. Pre-exposure measurements are performed at 25 °C and at the temperature at witch the irradiation will be performed.

Figure 3.6a shows the drain current I_{DS} (solid line) of an nMOS transistor in 65 nm CMOS technology, measured in linear region ($V_{DS} = 20\,\text{mV}$) sweeping the gate voltage V_G from -0.2 to $1.2\,\text{V}$ while $V_S = V_B = 0\,\text{V}$. The maximum level of current, reached at $V_G = V_{DD} = 1.2\,\text{V}$, is called I_{ON}^{lin}, as indicated in the figure. Another important parameter is the threshold voltage, which ideally defines the transition point between the OFF and ON regions of the $I_D\,(V_G)$ characteristic. To extract the threshold voltage in linear region, indicated as V_{TH}^{lin}, we use the *linear extrapolation* method [see *e.g.*, 124, 125, and references therein] that relies on the simple description of the drain current in the ON region:

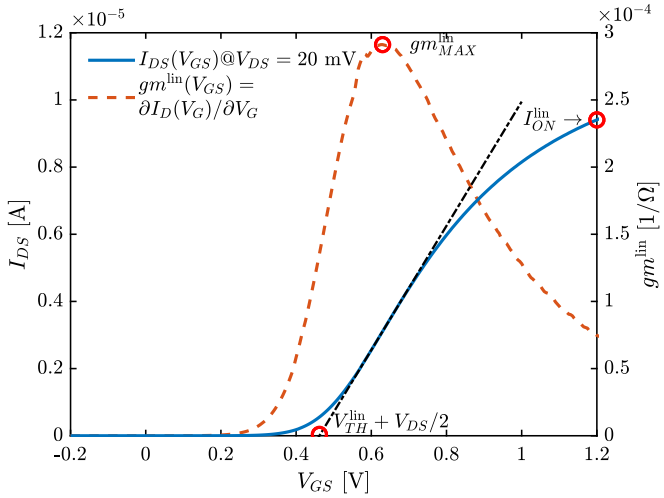
$$I_{DS}^{\text{lin}} = \frac{W}{L}\mu C_{OX}\left[\left(V_{GS} - V_{TH}^{\text{lin}}\right)V_{DS} - \frac{V_{DS}^2}{2}\right] \tag{3.2}$$

where W and L are, respectively, the channel width and the length of the transistor, μ is the mobility measured in m^2/Vs and C_{OX} is the intrinsic capacity (F/m^2). According to this equation, $I_{DS}^{\text{lin}} = 0$ when $V_{GS} = V_{TH}^{\text{lin}} + V_{DS}/2$. The peak of the transconductance $gm^{\text{lin}}(V_{GS}) = \partial I_{DS}^{\text{lin}}/\partial V_{GS}$, reported as a dashed line in Figure 3.6a, is used to find the region of the $I_D\,(V_G)$ characteristic that is better described by the linear relation reported in Equation 3.2. The intersection between the linear fit (dash-dot line) of the characteristic and the $I_{DS} = 0\,\text{A}$ axis minus $V_{DS}/2$ defines the threshold voltage V_{TH}^{lin}.

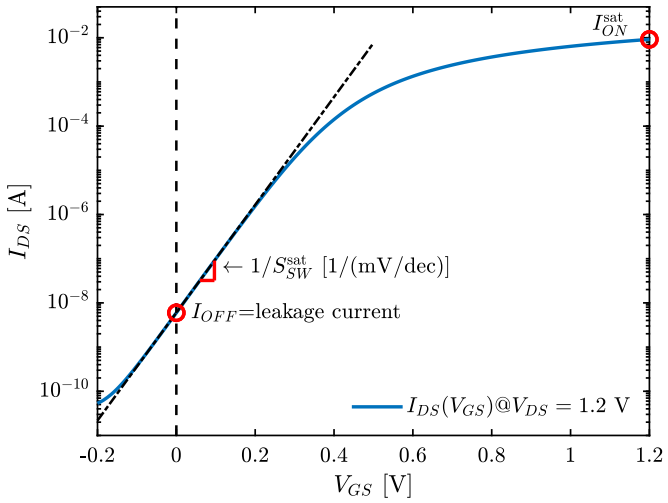
The maximum value of the transconductance gm_{MAX}^{lin} is an important parameter itself and will be used throughout this thesis to evaluate the radiation response. As can be infer form Equation 3.2, it is related to the mobility μ, a parameter strongly affected by radiation. Moreover, as we will see, a variation in the transconductance can indicate a change in the source-drain series resistance.

Figure 3.6b shows an $I_D\,(V_G)$ in saturation region, reported in logarithmic scale. As for the linear region, we define I_{ON}^{sat} the maximum level of the current, reached at $V_G = V_{DD} = 1.2\,\text{V}$, while the I_D measured at $V_{GS} = 0\,\text{V}$ (leakage current) is called I_{OFF}.

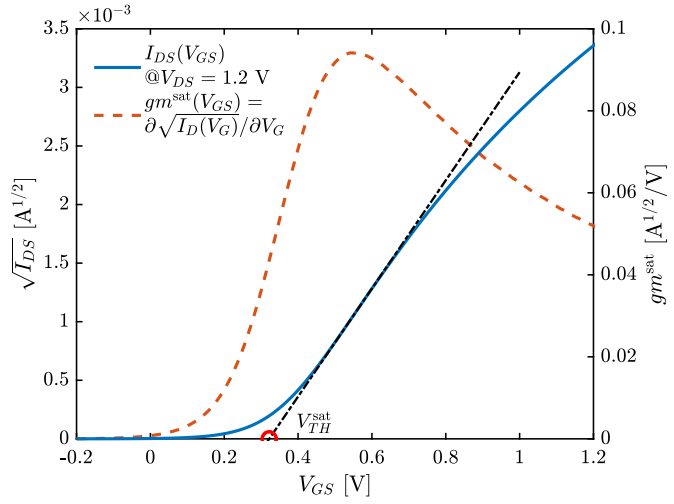
The subthreshold swing S_{SW}^{sat} is the inverse of the slope, in logarithmic scale, of the $I_D\,(V_G)$ characteristic in the OFF region, *i.e.*, below the threshold voltage, and it is measured in mV/dec.



(a) Example of $I_D\,(V_G)$ and $gm(V_G)$ in linear region.



(b) $I_D\,(V_G)$ characteristic in saturation region plotted in logarithmic scale.



(c) Square root of an $I_D\,(V_G)$ in saturation region.

Figure 3.6: Definition and extraction methods of the main parameters used to study the radiation response of MOS transistor.

The threshold voltage in saturation region V_{TH}^{sat} is extracted using the *liner extrapolation method in saturation region* [124, 126, 127], that uses, as reported in Figure 3.6c, the intersection between the linear fit of the square root of equation

$$I_{DS}^{\text{sat}} = \frac{W}{2L}\mu C_{OX}\left(V_{GS} - V_{TH}^{\text{sat}}\right)^2 \tag{3.3}$$

and the $\sqrt{I_{DS}} = 0\,\text{A}^{1/2}$ axis to extract the threshold voltage. The solid line shows the square root of the current and the dashed line its derivative that is used, similarly to what was done for the current in linear region, to find the point where to perform the linear fit (dash-dot line).

As we will see, all these parameters can be strongly affected by radiation, and will be extremely useful to understand the physicals mechanisms underling the radiation response of MOS transistors.

3.3 Overview of TID effects in Modern Technologies

As said in Chapter 1, 130 nm and 65 nm CMOS technologies have been chosen for the design of ASICs to be used in the detectors of the HL-LHC's experiments. The gate oxide thickness of the CMOS technologies studied in this thesis is $\ll 4\,\text{nm}$ [128–131], and therefore extremely robust to TID-related effects (see Chapter 2 and, in particular, Figure 2.8). However, as depicted in Figure 3.7, the radiation-induced transistor's performance degradation can still be large, especially at very high doses. Figure 3.7 shows in fact the percentage variation of the I_{ON}^{sat}

$$\%I_{ON}^{\text{sat}}(\text{TID}) = 100 \times \frac{I_{ON}^{\text{sat}}(\text{TID}) - I_{ON}^{\text{sat}}(\text{Pre-rad})}{I_{ON}^{\text{sat}}(\text{Pre-rad})} \tag{3.4}$$

measured at different total dose levels up to $1\,\text{Grad}(SiO_2)$, the maximum dose expected to be reached in the HL-LHC detectors. Each measure is indicated in figure with a circle. Both nMOS and pMOS transistors in this 65 nm CMOS technology show an extreme current degradation at the end of exposure, to levels that make the devices no longer usable for any practical application. Note that the same measurement performed without irradiation (triangles) does not affect the performance of the devices, proving that the I_{ON}^{sat} degradation is actually provoked by the exposure to X-ray and not to other phenomena such as, *e.g.*, negative bias temperature instability [132] or hot carrier effects [133].

The significant reduction in performance of MOS transistors, which cannot be explained by charge being trapped in gate oxide, is caused by the presence of other oxides, in particular the *shallow trench isolation* STI oxides and the *spacers*, which are, in general, much thicker and richer in defects than the gate oxide and therefore prone to trap a relatively large amount of charge. Figure 3.8 shows a schematic representation of a nMOS transistor with both these oxides included. In the next chapters we will describe the main STI- and spacers-related effects in nanoscale CMOS technology, whit a special focus on the 65 nm technology. We will also report results in 130, 40 and 28 nm technologies, giving therefore a

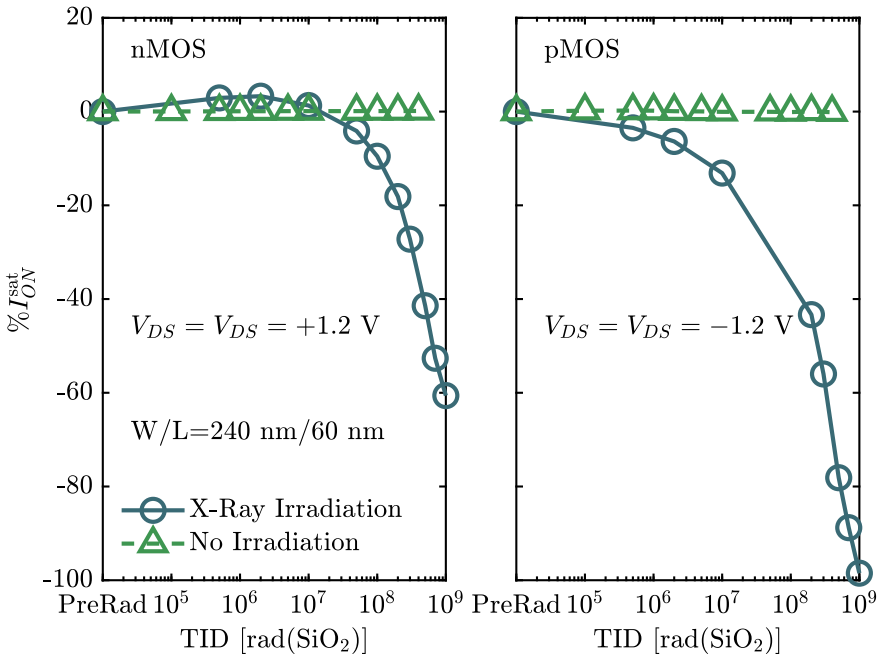


Figure 3.7: Percentage variation of the I_{ON}^{sat} current for nMOS (left) and pMOS (right) transistors with channel width $W = 240\,\text{nm}$ and length $L = 60\,\text{nm}$ irradiated up to $1\,\text{Grad(SiO}_2\text{)}$ at T=25 °C and kept under bias with $V_{GS} = V_{DS} = \pm 1.2\,\text{V}$ during the exposure. The dashed lines report the results of a measure performed in the same condition but without irradiation.

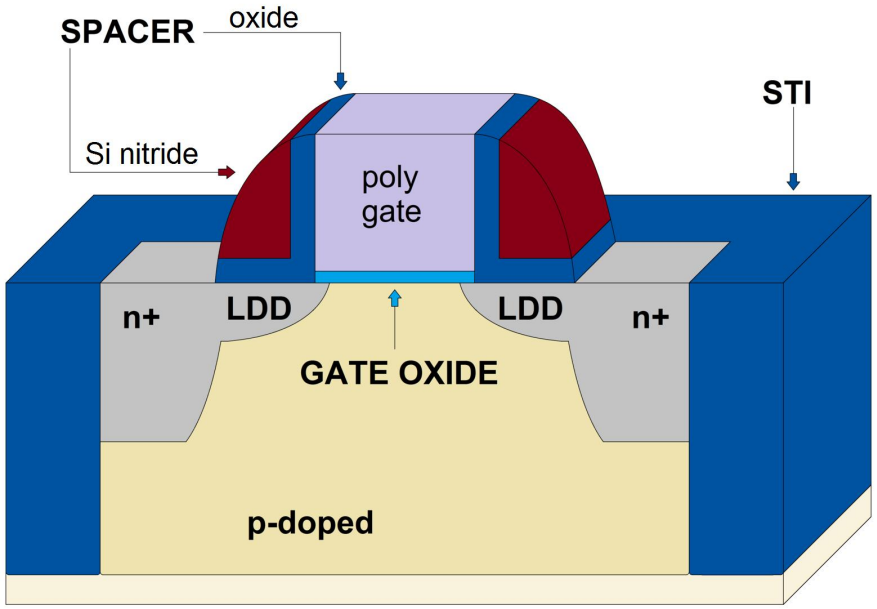


Figure 3.8: Schematic representation of a nMOS transistor. In addition to gate oxide, isolating oxides such as STIs and spacers are also reported. These oxides are much thicker and richer in defects than the gate oxide.

comprehensive picture of the radiation response in nanoscale devices exposed to high and ultra-high doses (to 1 Grad(SiO_2)). We will try to both focus on the physical mechanisms underlying the radiation response of nanoscale devices and to provide some indication for the qualification of the ASICs for the ultra-high level of TID expected to be reached in inner layers of particle detectors of the HL-LHC.

Before proceeding, it is important to know that radiation significantly increases the device-to-device variability [134]. Therefore, rather than focusing on the specific value reached by a certain parameter after irradiation, we are interested in evaluating the general trend of its radiation response as the TID varies.

Chapter 4

STI-Related Effects

Ionizing radiation effects related to the presence of STI oxides (introduced at the 250 nm technology to replace their predecessors LOCOS) are a well know problem for the radiation hardness of CMOS technology. In fact, while the gate oxide is extremely thin and robust to TID [45, 123], the STI can have a thickness of several hundreds of nanometers [135, 136], making this oxide prone to trap radiation-induced charge.

Although the effects of the presence of STI have been studied for more than 20 years, exposure to very high doses has provided further information on the physical mechanisms underlying some of these effects. In particular, we will describe in details two phenomena that can significantly affect the radiation hardness of a nano-scale CMOS technology: the radiation-induced drain-to-source leakage current[1] and the radiation-induced narrow channel effects (RINCE).

4.1 Radiation-Induced Drain to Source Leakage Current

The radiation-induced drain to source leakage current increase is a well known phenomenon (see *e.g.* [140, 141]), and it is one of the major problems in CMOS technology exposed to ionizing radiation as it can cause a considerable increase in static power dissipation [142]. We will begin this section studying the 130 nm CMOS technology, which shows several features already widely known in the literature but will nevertheless help us to introduce the phenomenon and to show how it depends on various parameters such as bias and temperature. Later in this section, results will also be shown in 65, 40 and 28 nm CMOS technologies. As explained below, the parasitic leakage current is only of concern in nMOS transistors.

[1] During this thesis we will often shorten the term "drainage leakage current at the radiation-induced source" to the simpler "radiation-induced leakage current". However, this should not be confused with RILC [137–139], which instead identifies the dependence of the gate current on radiation. Since in the technologies studied in this thesis we have not measured significant increases in gate current, this phenomenon will not be discussed and therefore the term "leakage current" will be used exclusively for the I_{OFF} current.

4.1.1 Leakage Current in 130 nm CMOS Technology

Figure 4.1 show the evolution of the leakage current (I_{OFF}) measured at different TID levels for two nMOS transistors in 130 nm technology with $W = 150\,\text{nm}$ and $L = 130\,\text{nm}$. The solid lines report the response of transistors biased, during irradiation, with $V_{GS} = 1.2\,\text{V}$ and $V_{DS} = 0\,\text{V}$. All transistors are produced by the same manufacturer and present the same pre-rad electric performance but they came from two different fabs, namely "Fab. A" and "Fab. B". We will come back later on the results depicted by the dashed line.

While the transistor from Fab. A shows, at TID = 2 Mrad (SiO_2), an increase in the leakage current of more than 4 orders of magnitude, the I_{OFF} of the nMOS from Fab. B has an almost negligible evolution. This figure clearly illustrates the extreme process-dependency of the radiation-induced effects in the isolation oxides, which makes it very difficult to develop a model capable to predict the radiation response without knowing the details, often confidential, of a given technology. This variability is in fact most likely caused by small differences in the STI fabrication process, as also reported by Brady and co-workers in [143]. In [144] the within-wafer variability of the radiation response is studied, with a detailed review of the possible sources of this variability in the fabrication process of the STI. Note that the pre-exposure value shown in Figure 4.1 is almost the same for both fabs, proving that these process variations do not change the performance of a not-irradiated transistor.

Figure 4.2 shows the $I_D\,(V_G)$ characteristics of the nMOS transistor from the Fab. A reported in Figure 4.1, measured before irradiation, after a total dose of 2 Mrad(SiO_2) and at the end of exposure, when the sample reached a TID of 200 Mrad(SiO_2). The increase in the drain-to-source leakage current can be clearly noticed in the curve plotted in logarithmic scale (dashed line, left axis) at 2 Mrad(SiO_2) while at 200 Mrad(SiO_2) the characteristic is close to the pre-irradiation value, with a slight increase in the subthreshold swing, *i.e.*, the inverse of the slope of the linear portion, in logarithmic scale, of the $I_D\,(V_G)$ below the threshold voltage (see Figure 3.6b).

The main cause of the increase in the leakage current is the activation of parasitic transistors along the STI, as schematically reported in Figure 4.3. The positive charge trapped in the STI can in fact attract enough electrons from the silicon bulk to invert the parasitic lateral drain-to-source channels. It is clear that this does not happen in pMOS transistors because both the charge trapped in the oxide and the charge trapped at the interface are positive, and therefore tend to repel the holes of the doped silicon, with a consequent increase in the threshold voltage of the parasitic transistors.

Note that the $I_D\,(V_G)$ characteristic shown in Figure 4.2 is almost flat in the range $-0.2\,\text{V} \leq V_{GS} \leq 0.1\,\text{V}$ at TID = 2 Mrad (SiO_2), therefore the current flowing in these parasitic transistors is beyond the control of the gate voltage. This suggests that the charge responsible for the inversion of the parasitic channels is trapped relatively far from the STI-gate corner (also called trench corner) [146, 147, 150, 151]. When, on the other hand, the leakage current is due to charge trapped closer to the channel, it changes significantly with the gate voltage and is strongly dependent on the STI topology, and in particular on the corner between

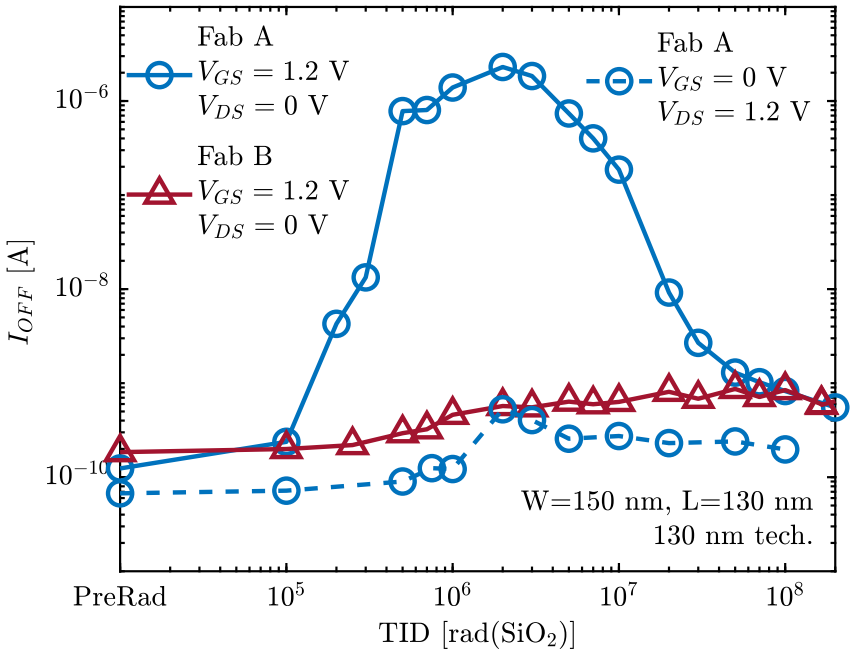


Figure 4.1: *Solid lines*: Leakage current versus total dose for two nMOS transistors in 130 nm technology irradiated up to TID $\geq$ 100 Mrad(SiO$_2$) with V_{GS} = 1.2 V and V_{DS} = 0 V. Small variations in the manufacturing process can result in a completely different radiation response. *Dashed lines*: Applying a V_{GS} = 0 V during irradiation strongly reduces the I_{OFF} increase.

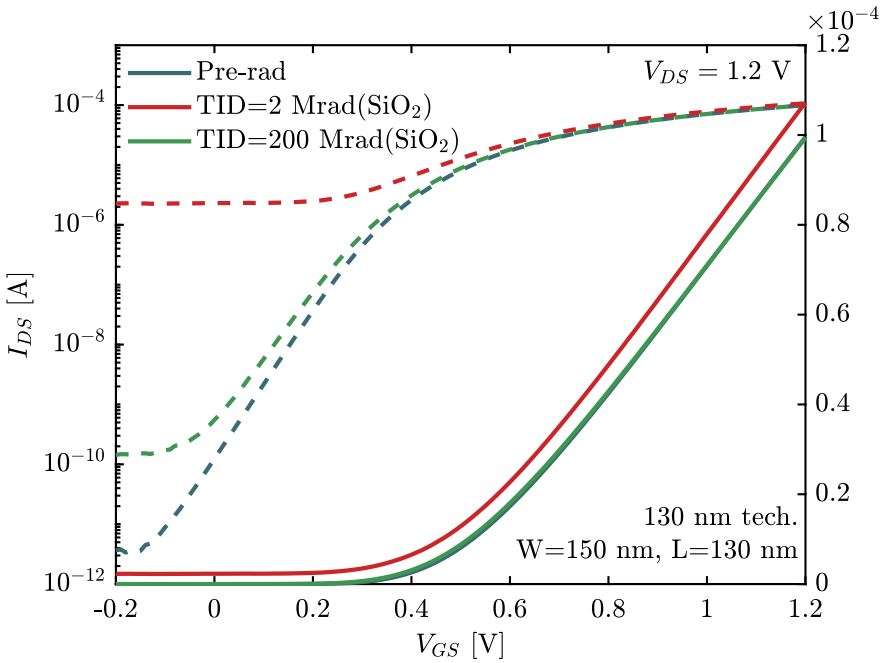
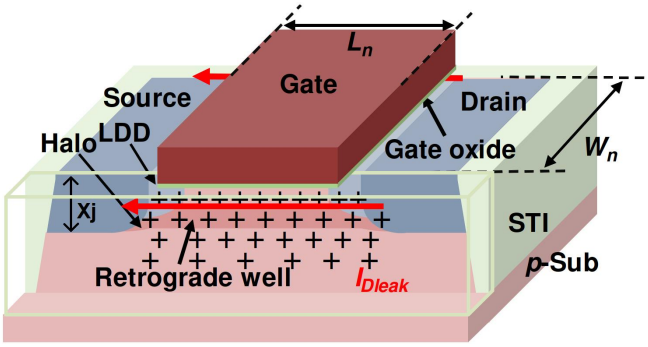
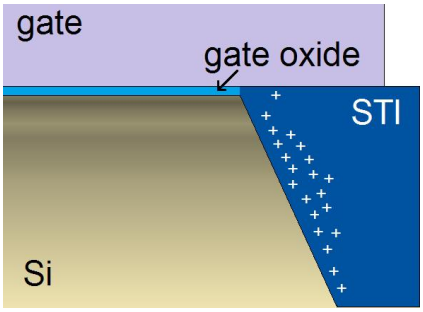


Figure 4.2: $I_D\,(V_G)$ characteristics in saturation region (V_{DS} = 1.2 V) of the nMOS transistor from Fab. A reported in Figure 4.1 before irradiation, after TID = 2 Mrad(SiO$_2$) and after TID = 200 Mrad(SiO$_2$). The dashed lines show the curves in logarithmic scale (left axis) while the solid lines refer to the characteristics in linear scale (right axis).



(a) Parasitic paths due the charge trapped in the STI. LDD and Halo implants, as well as the retrograde well are depicted [145]. Note that the channel length of the parasitic transistor is roughly equal to that of the main MOS.



(b) Cross section an MOS transistor in the source-drain direction. The doping profile changes with detpth, as indicated by the different coulours in the Si bulk.

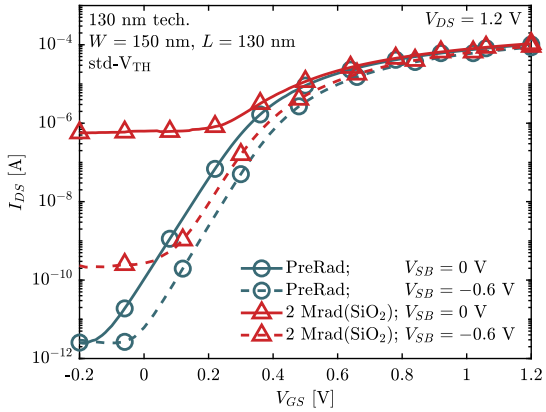
Figure 4.3: Schematic representation of the leakage path opened by the positive charge trapped in the STI. Doping density of the channel and the silicon substrate is highly engineered, and the distribution of charge in the STI is not uniform [146–151]. Note also that the gate overlaps the STI.

the STI and the channel [135, 146, 152].

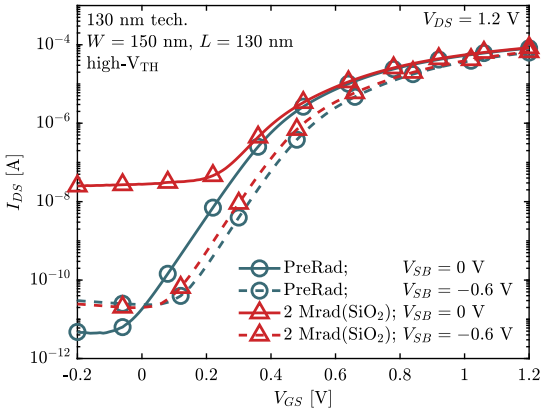
To further confirm our hypothesis on the location of the charge responsible for the increase of the leakage current, we show in Figure 4.1 the I_{OFF} of a nMOS transistor irradiated with $V_{GS} = 0\,\text{V}$ and $V_{DS} = 1.2\,\text{V}$ (dashed line). In this case, the leakage current peak is almost completely removed. Since, as clarified later and as also reported in [145], the V_{DS} has a small impact in the evolution of the I_{OFF}, this experiment proves the strong dependence of the leakage current from the gate bias. The removal of the I_{OFF} when $V_{GS} = 0\,\text{V}$ is an important indication that the leakage current is flowing far from the trench corner. In fact, as reported in [147, 151], when a $V_{GS} > 0\,\text{V}$ is applied during irradiation, the positive charge is "pushed" in the lower portion of the STI by the electric field generated by the part of the polysilicon gate that exceeds the width of the transistor and surmounts the STI oxides (see Figure 4.3b). Thus, the absence of a gate voltage prevents the radiation-generated charge from reaching the location where it can invert the parasitic channel, inhibiting the creation of leakage paths.

Figure 4.4 provides some further details about the radiation-induced leakage current. Figures 4.4a to 4.4c reports the $I_D\,(V_G)$ characteristics before and after a TID $= 2\,\text{Mrad}\,(\text{SiO}_2)$ of, respectively, standard-, high- and low-V_{TH} nMOS transistors from the 130 nm technology with a $W/L = 150\,\text{nm}/130\,\text{nm}$, measured with two different source-to-substrate voltages ($V_{SB} = 0\,\text{V}, -0.6\,\text{V}$), while Figure 4.4d shows the evolution of their I_{OFF} with TID. All the transistors have been irradiated at the same time with $V_{GS} = V_{DS} = 1.2\,\text{V}$ and $V_{SB} = 0\,\text{V}$. From the reported results we can infer:

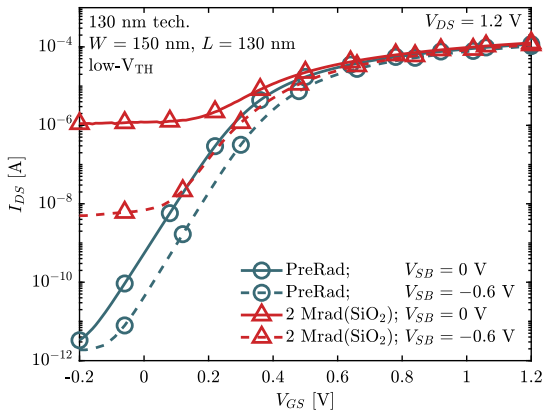
- In the measurement performed with $V_{SB} = -0.6\,\text{V}$ the leakage current is strongly reduced.
- High-V_{TH} transistors have a significantly lower radiation-induced leakage



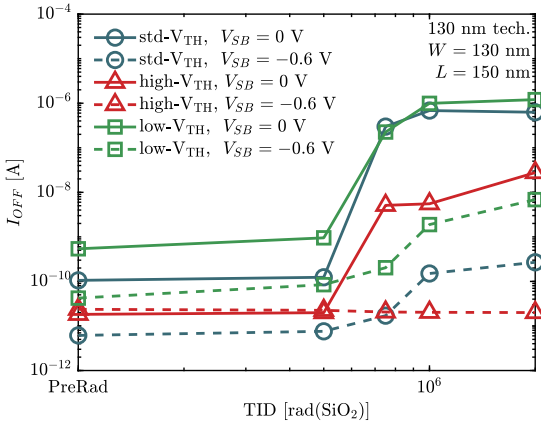
(a) std-V_{TH} nMOS measured at $V_{SB} = 0$ and -0.6 V before and after irradiation.



(b) high-V_{TH} nMOS measured at $V_{SB} = 0$ and -0.6 V before and after irradiation.



(c) low-V_{TH} nMOS measured at $V_{SB} = 0$ and -0.6 V before and after irradiation.



(d) I_{OFF} vs TID for std-, high- and low-V_{TH} nMOS at $V_{SB} = 0, -0.6$ V.

Figure 4.4: Radiation-induced leakage current for different V_{SB} for std-, high- and low-V_{TH} nMOS transistors in 130 nm technology.

current.

The first effect has been already reported by Niu and co-workers in [146] and is due to an increase of the width of the depletion region below the channel and consequent reduction of free carriers available for the parasitic transistors. The second effect can be explained by a difference in the doping levels of the substrate used to modulate the V_{TH}, where higher doping density leads to a smaller radiation-induced leakage current [151, 152].

The I_{OFF}(TID) characteristic depicted in Figure 4.1 is clearly non-monotonic, as also pointed out by the $I_D\,(V_G)$ curves reported in Figure 4.2. To try to understand this behaviour it is useful to describe the parasitic transistors as MOSFETs whose gate voltage, and therefore drain current, is controlled by the amount of charge trapped in the STI. Hence, knowing the density of positive charge N_{OT} in the trench oxide, it could be possible to plot the $I_{OFF}(N_{OT})$ characteristic. This has be done by Esqueda and co-workers in [148] and McLain and co-workers in [149], showing that the N_{OT} expected to be trapped at $1 \sim 2$ Mrad(SiO_2) is sufficient to bring in strong inversion the parasitic transistors of the devices used in their work. Once in strong inversion, a large amount of charge is needed to increase the current further and therefore the derivative of $\log_{10}(I_{OFF}\,(TID))$ tends to decrease as TID increases. This explains why the I_{OFF} reported in Figure 4.1 reaches a sort of saturation value from TID $= 50\,\mathrm{krad}\,(SiO_2)$ to TID $= 5\,\mathrm{Mrad}\,(SiO_2)$ with a peak of $2.3\,\mu\mathrm{A}$ at TID $= 2\,\mathrm{Mrad}\,(SiO_2)$. Moreover, Faccio and co-workers [153, 154] proposed an explanation of the saturation in the I_{OFF} based on the concurrent effects of oxide- and interface-trapped charge, that are opposite in sign and have different build-up times (see Chapter 2). This model can also be used to explain the decrease, also reported in Figure 4.1, in leakage current after TID $= 5\,\mathrm{Mrad}\,(SiO_2)$.

In the 130 nm technology form Fab. A, both effects have an impact when transistors are irradiated at ultra-high doses. Figure 4.5 shows the $I_D\,(V_G)$ characteristics in saturation region for a nMOS transistor subject to 4 cycles of irradiation up to 1 Mrad(SiO_2) and subsequent annealing at $T = 25\,^{\circ}\mathrm{C}$. All the irradiation steps have been performed with $V_{GS} = V_{DS} = 1.2\,\mathrm{V}$ (diode) while in the annealing steps the device was either polarized in diode configuration or not biased. Note that the level of the I_{OFF} after irradiation is very comparable to that reached in Figure 4.1, proving that the V_{DS} voltage does not have a strong impact in the radiation-induced leakage current. The first irradiation step of $\sim$1 Mrad(SiO_2) provokes an increase in the I_{OFF} up to its saturation value ($\sim 1\,\mu\mathrm{A}$). However, after the room temperature annealing the leakage current due to the parasitic transistors drops below the level of the drain-source current flowing in the main channel. This fast annealing is an indication that the leakage current is caused by positive charge trapped in energetically shallow defects in the STI. Every additional irradiation to 1 Mrad(SiO_2) tends to restore the parasitic leakage current, which however is always at a lower level than that reached in the previous irradiation step. This behaviour can be explained as follow:

1. Irradiation provokes a build-up of positive oxide-trapped charge that turn on the parasitic transistors.

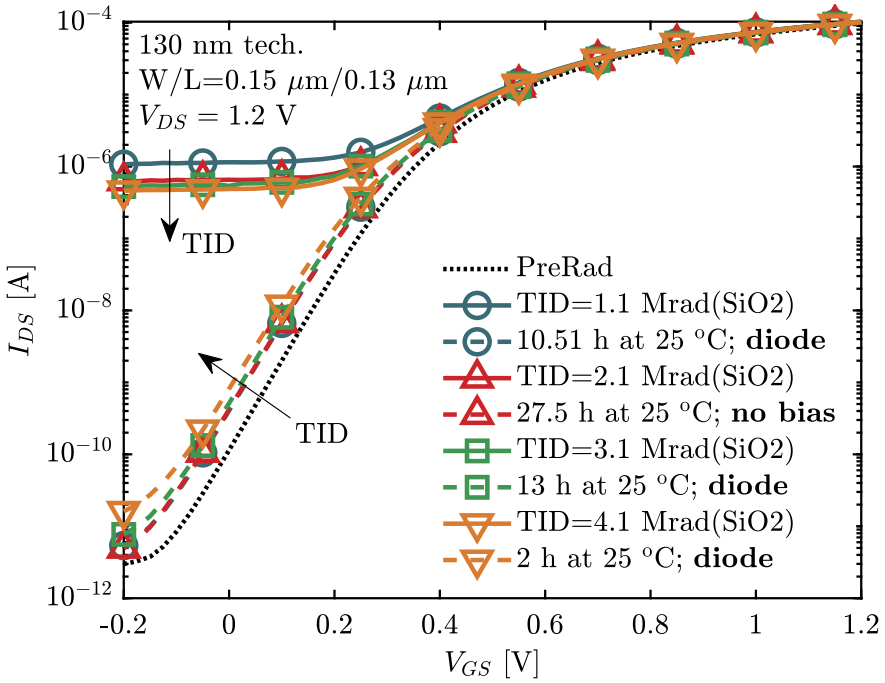


Figure 4.5: Cycles of subsequent irradiation and room temperature annealing. After the first irradiation step the leakage current is constantly decreasing while the negative shift of the post-annealing curves is always increasing. This behaviour is independent on the bias applied during annealing.

2. As seen in Section 2.2, the hole transport induces the release of H^+ ions, responsible for the formation of interface traps.

3. The room temperature annealing removes enough charge to bring the current of the parasitic transistor below the I_{OFF} flowing in the main channel.

4. A new irradiation step restores the leakage paths. Since the charge produced by a TID = 1 Mrad (SiO_2) is sufficient to bring the parasitic transistors in saturation, the level of I_{OFF} reached is always comparable to those obtained after the previous irradiation step.

5. However, the formation of negative charge trapped at the interface makes it more difficult for the new positive charge generated after a further irradiation step to reverse the parasitic channels, lowering the maximum leakage current.

It is therefore clear that the formation of the leakage current is a complex phenomenon that involves both oxide- and interface-trapped charge, making the task of predicting its impact in real circuits quite difficult.

Form the post-annealing steps in Figure 4.5 (dashed lines), we can also observe that the negative shift of the $I_D\,(V_G)$ characteristic is constantly increasing, independently from the bias applied during annealing. The negative shift is an indication of the lowering of the threshold voltage of the main transistor provoked by positive-trapped charge [155]. It is evident that the charge inducing this shift does not anneal at the same rate as that causing the leakage current.

Moreover, the negative shift increases monotonically with the dose, at least in the measured TID range. As we will se later, the decrease in the threshold voltage is provoked by radiation-induced narrow channel effects, which are also related to the presence of the STI oxide. This experiment is the first indication that, despite they are both caused by charge trapped in the STI, the radiation-induced drain-to-source leakage current and the radiation-induced narrow channel effects are regulated by different mechanisms.

We now move to study the temperature dependence of the radiation-induced leakage current. It is important to study this aspect both because it provides us with further details on the physical mechanisms underlying the radiation response of the I_{OFF}, and because, when operational, some particle detectors in the HL-LHC, and especially those close to the interaction points, will be kept at temperatures in a range between -30 and $-20\,°C$ (see Chapter 1).

The solid line in Figure 4.6 shows the leakage current vs TID of a nMOS transistors in 130 nm technology irradiated at $T = -30\,°C$, while the dashed line reports, to facilitate the comparison, the response at 25 °C already shown in Figure 4.1.

At low temperature the leakage current reaches a higher maximum peak and drops much slowly than at $T = 25\,°C$. This suggests that the accumulation of interface traps is significantly slowed at low temperature, thus making the effect of positive charges trapped in the oxide more evident. From the point of view of the qualification procedure it means that high dose-rate, low-temperature test is certainly the worst-case scenario for the evolution of the radiation-induced leakage current in the studied 130 nm CMOS technology from Fab. A.

4.1.2 Leakage Current in Other CMOS Technologies

In analogy with the results shown above for the 130 nm process, also more scaled technologies can be subject to TID-induced leakage currents.

We start by evaluating the evolution of the leakage current in the 65 nm CMOS technology. Figure 4.7 reports the I_{OFF} variation of three nMOS transistors of the same size ($W = 240\,\text{nm}, L = 60\,\text{nm}$) from three different manufacturing companies (Man. A, Man. B and Man. C) irradiated at room temperature up to 1 Grad(SiO_2), with $V_{GS} = V_{DS} = 1.2\,V$.

Transistors from Man. A and Man. C show a difference in the pre-irradiation I_{OFF} of more that one order of magnitude, but a relatively small variation of the leakage current even at very high doses. The leakage current increase of nMOS A is almost perfectly monotonic with TID, going from $I_{OFF} =\sim 28\,\text{pA}$ before irradiation to $I_{OFF} =\sim 448\,\text{pA}$ at TID = 1 Grad (SiO_2). On the other hand, nMOS C shows a small bump around TID = 5/10 Mrad (SiO_2) followed by a decrease and a subsequent further increase up to 1 Grad(SiO_2). A similar but much more pronounced trend can be seen in nMOS B, where the peak reached at TID = 3 Mrad (SiO_2) is almost 4 orders of magnitude higher than the pre-irradiation value. It has to be noticed that the I_{OFF} of nMOS B decreases during the first irradiation steps up to TID = 200 krad (SiO_2). An analogous behaviour was reported also in [146], and was explained by a reduc-

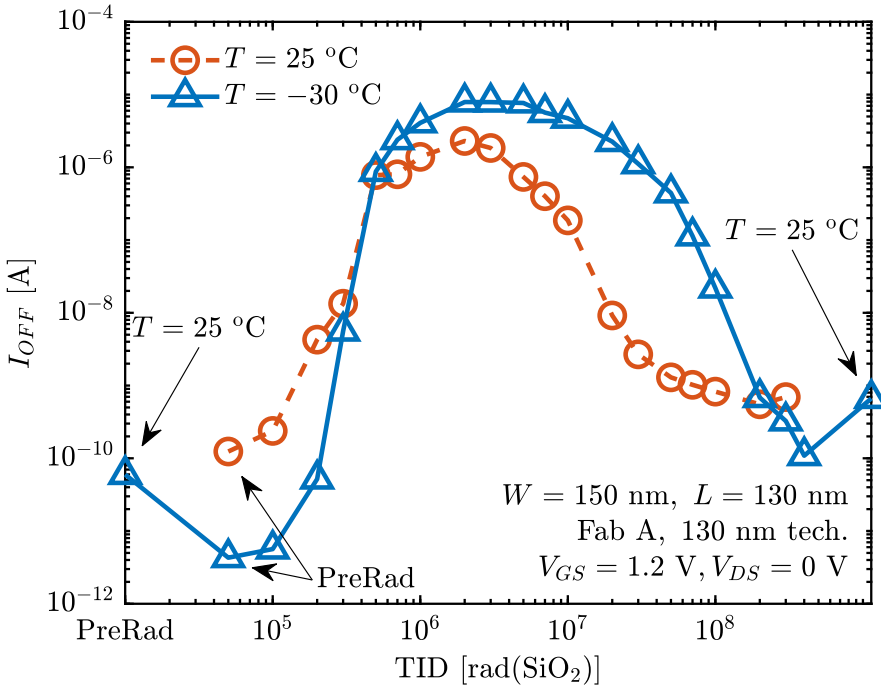


Figure 4.6: $I_{OFF}(TID)$ for nMOS transistor in 130 nm technology exposed at 25 (dashed line) and −30 °C (solid line). The first and the last point of the sample irradiated at low temperature have been measured at $T = 25$ °C.

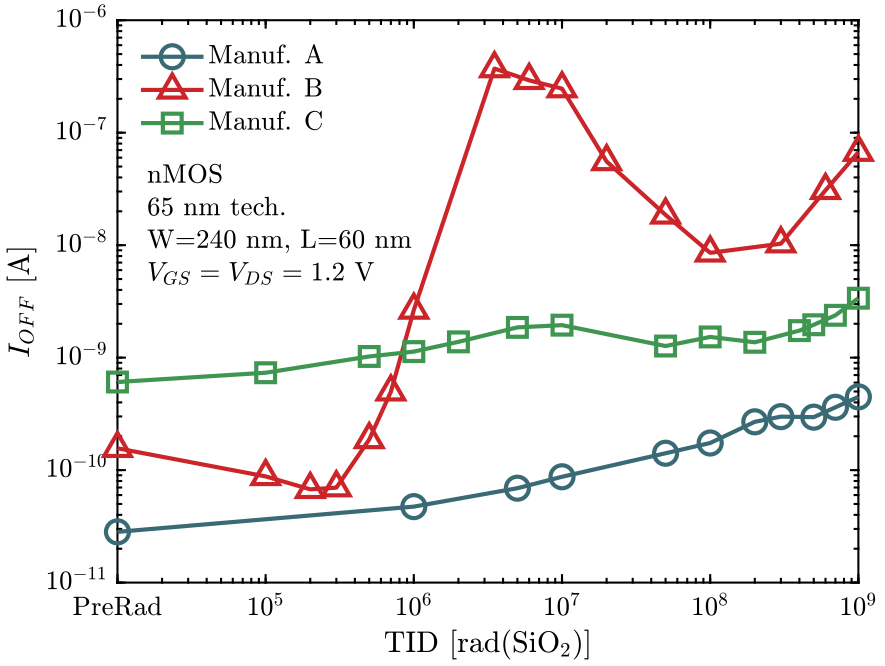


Figure 4.7: Leakage current vs TID for three different manufacturer in 65 nm CMOS technology exposed up to 1 Grad(SiO_2). The I_{OFF} variation is extremely process-dependent, showing in samples from some manufacturers a first peak around 5/10 Mrad(SiO_2) and a late increase after 100 Mrad(SiO_2).

tion in the band-to-band tunnelling current due to the decrease of the drain-to-channel fringing field induced by the positive-trapped charge in the STI. After the first peak, the leakage current decreases by almost two orders of magnitude up to TID = 100 Mrad (SiO_2) and then increases again reaching 67.1 nA at TID = 1 Grad (SiO_2). This further leakage current increase has never been seen before and could be explained by a creation of leakage paths due to trapped-charge located in a different position in the STI with respect to the one causing the first peak. In fact, we can describe the leakage current as the sum of the currents of several parasitic transistors connected in parallel, whose threshold voltage depends on the concentration of doping in the silicon and the thickness of the oxide (see Figure 4.3). Since in modern technologies the doping profile in the Si bulk is not uniform but varies with the depth, and, in general, also the thickness of the oxide varies, these parasitic transistors will have different threshold voltages and therefore will contribute differently to the leakage current [146–151]. Moreover, even the charge distribution in the STI is not uniform and depends on both the electric field and the charge already trapped. Therefore, it is reasonable to assume that some parasitic transistors begin to conduct a relevant current only at high doses or that the charge previously trapped in the oxide and at the interface changes the electric field in the STI, pushing the new radiation-induced charges to different locations in the trench oxide. This interesting hypothesis has to be confirmed by further study.

As already reported for the 130 nm technology, the radiation-induced leakage current variation is extremely process-dependent and even transistors with slight differences in the manufacturing process can have very different radiation-response. Therefore, the technologies chosen to be used in the detectors have to be constantly monitored in order to know if their radiation response changed as a consequence of variations in the production process. It is worth mentioning here that the manufacturer currently used for the design of particle detectors is the Man. A, that shows the smallest leakage current both before and after irradiation.

Figure 4.8 reports the I_{OFF} variation and $I_D(V_G)$ characteristics for nMOS transistors with similar size in 40 nm and 28 nm technologies from Man. A exposed up to 500 Mrad(SiO_2) ans 1 Grad(SiO_2) respectively. Compared to the radiation response of Fab. A in 130 nm and manufactures B and C in 65 nm reported in Figure 4.2 and 4.7, neither 40 nm nor 28 nm technology show a non-monotonic behaviour in the radiation-induced leakage current. In 40 nm technology the I_{OFF} increases by more than 5 orders of magnitude after 500 Mrad(SiO_2) and the current flowing in the parasitic transistors is only slightly dependent on the gate voltage, as can be seen from the $I_D(V_G)$ characteristics around $V_{GS} = 0$ V. Therefore, as in 130 nm and 65 nm technologies, the charge is trapped far from the trench corner. The situation is different for the nMOS in 28 nm technology. The transistors have a relatively low threshold voltage already before irradiation, and the current in the parasitic leakage paths is, at $V_{GS} = 0$ V, comparable to the current flowing in the main channel. Hence, the increase in the I_{OFF} observed in the figure on the left is, in this 28 nm technology, provoked both by the creation of parasitic paths and by a negative shift of the threshold voltage, caused, as we

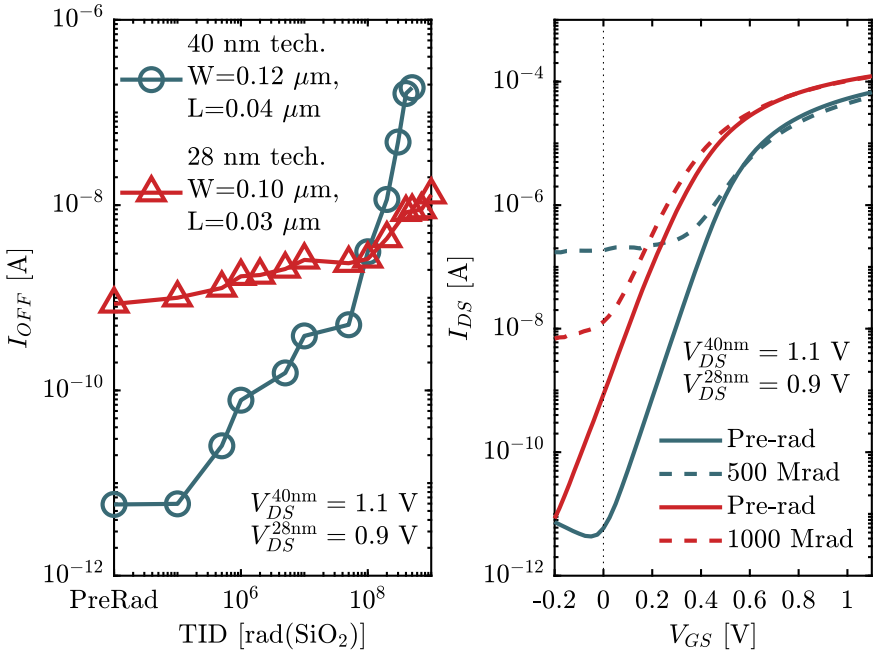


Figure 4.8: Left: leakage current vs TID for nMOS in 40 nm (in blue) and 28 nm (in red) technology. Right: $I_D\,(V_G)$ characteristic before and after irradiation for the same nMOSFETs. For both technologies the leakage current increases monotonically with TID, and is caused by charge trapped deep in the STI.

will see later, by a combination of radiation induced narrow- and short- channel effects.

However, Zhang and co-workers showed in [145] that a 28 nm technology of the same Man. A studied in this thesis but with a different fabrication process, suffers a severe leakage current increase ($I_{OFF} \sim 100$ nA at TID = 1 Grad (SiO_2)) mainly caused by the creation of parasitic paths. Also in that case, the drain-to-source leakage current was independent on the V_{GS}, indicating that the positive-trapped charge is located far from the trench corner.

Moreover, in [145] the monotonic increase in the $I_{OFF}$is also modelled. The following equation:

$$I_{OFF} = I_{OFF}^{\text{PreRad}} \left[1 + \left(\frac{TID}{TID_{\text{crit}}} \right)^{k} \right] \tag{4.1}$$

has been used to describe with a simplified charge-based EKV MOSFET model the current increase in the parasitic transistors. TID_{crit} is the dose at which the current in the parasitic transistor is equal to the current in the main channel and k is the slope of the measured $I_{OFF}(TID)$ curve in log-log scale. Thanks to this model it was possible to prove that the parasitic channels in the studied 28 nm technology are in weak inversion even at very high doses. This is coherent with the monotonic behaviour reported in Figure 4.8, where increasing levels of TID provoke a substantial increase in the leakage current. On the other hand, as previously said, the I_{OFF} saturation level reached in the 130 nm technology and reported in Figure 4.1 could indicate that the parasitic transistors are in strong inversion, where a large amount of charge is needed to change the current.

Figure 4.9 shows the I_{OFF} versus the transistor's size for the 40 nm technology exposed to a TID of 500 Mrad(SiO_2). While, on one hand, the leakage current is practically independent on the channel width (figure on the left), on the other hand it follows a $1/L$ line (figure to the right). This is a strong indication that the leakage current is actually flowing in parasitic channels from source to drain, with a channel width dependent only on the amount and distribution of the positive charge trapped in the STI. A similar dependence for the 28 nm technology was reported by Zhang and co-workers in [145].

Summarizing, despite the differences in the studied CMOS technologies, all of them can be prone to radiation-induced leakage current, that is mainly due to charge trapped in the STI well below the gate level. Small variations in the fabrication process can provoke large changes in the radiation response, which has therefore to be monitored each time a new technology is proposed to be used in harsh environments and also during the development and production phases of the ASICs, since the foundry may change some details in the process, leading to a possible substantial variation in the radiation response.

It is worth to mention that the radiation-induced drain-to-source leakage current increase can be completely avoided with *hardness by design* techniques and, in particular, enclosed-layout transistors (ELT) [156–158], where the STI oxides do not face the channel and, therefore, the charge trapped in the STI does not create leakage paths, as schematically represented in Figure 4.10a. This layout completely remove any radiation-induced leakage current increase, as can be seen in Figure 4.10b, where the I_{OFF} evolution of ELTs is reported for three different technologies nodes, *i.e.*, 130, 65 and 40 nm.

These transistors are clearly extremely useful for the design of electronic devices operating in radiation environments. However, there are some drawbacks that limit their use. For example, the aspect ratio of an ELT is always higher than that of a standard transistor with the same L. In other words, while the channel length of an ELT may be as short as for a standard transistor, the minimum channel width is defined by the size of the ring between the source and the drain and is therefore significantly larger than the minimum W that can be obtained in a normal device. This certainly limits the possibility of using ELTs when very high performance is required in terms of both speed and density, as ELTs occupy, for the same W/L, a larger surface area than standard transistors. In addition, the limited use of these devices in commercial products results in a poor availability of libraries in digital design tools and is therefore complex to accurately simulate their behaviour. In addition, enclosed transistors are inherently asymmetric, meaning that the roles of source and drain are not exclusively defined by the voltage applied to the terminals because, as shown in Figure 4.10a, the two terminals are geometrically different [159]. Therefore, although these transistors may be essential to ensure greater radiation hardness at critical points of the circuit, their use entails unpractical consequences and performance penalties. For this reason, after the systematical use of ELTs for all circuits developed in 250 nm CMOS for the LHC experiments, this design is only punctually adopted ai 130 and 65 nm technologies for the HL-HLC.

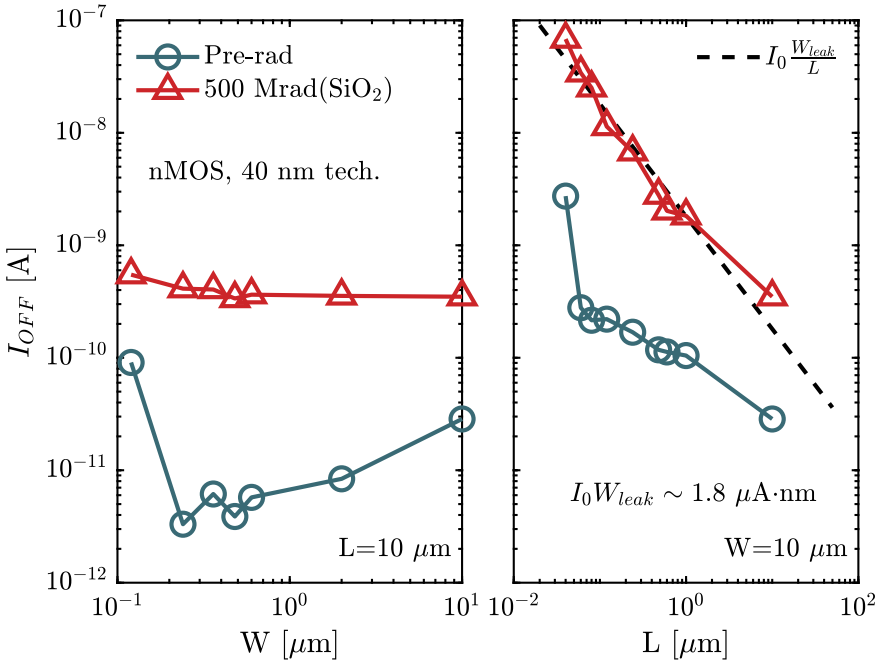
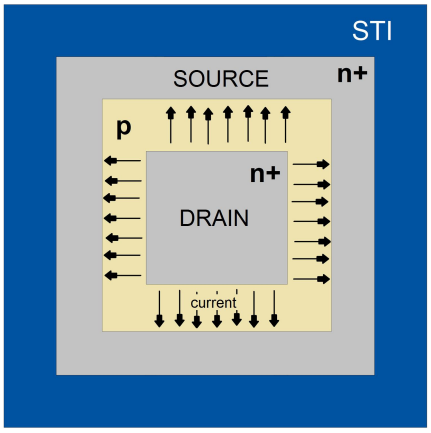
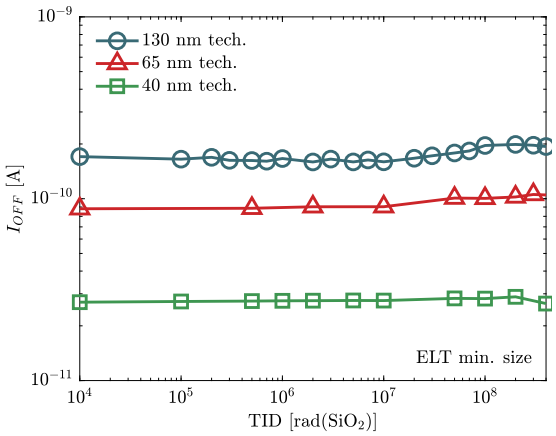


Figure 4.9: I_{OFF} vs transistor's size for nMOS in 40 nm technology exposed to 500 Mrad(SiO_2). The leakage current is almost independent on the channel width but decreases with L, as reported by the dashed line.



(a) Schematic representation of an enclosed layout transistor. The STI oxides do not face the channel and the trapped charge does not affect the current.



(b) Leakage current of ELTs in different technologies. The I_{OFF} is almost indipendent from radiation.

Figure 4.10: Enclosed layout transistor

4.2 Radiation-Induced Narrow Channel Effects

The term RINCE (radiation-induced narrow channel effects) has be introduce by Faccio and co-workers in [153] to describe the unexpected channel-width dependence of the radiation response of MOS transistors. Although the intensity of the phenomenon may vary between technologies, RINCE is present in all the measured CMOS processes and, as we will see, has common characteristics in all the devices studied. This is an important difference with respect to the leakage current, which, as we have seen, in some cases is practically negligible (see *e.g.* Figure 4.1). RINCEs can significantly deteriorate the performance of MOS devices and it is therefore appropriate to evaluate their behaviour at increasing TID and their impact on the devices.

4.2.1 RINCE in 65 nm CMOS Technology

Under this heading we discuss the particularly rich phenomenology of narrow channel effects induced by radiation. We will report results in the 65 nm CMOS technology of manufacturer "A" (see Figure 4.7), which is currently used in the design of the HL-LHC particle detectors.

In the first section we will introduce the RINCEs, showing their dependence on the size of the transistor and highlighting both the similarities and differences with the radiation-induced leakage current.

In the second section we will show the bias dependence of the radiation response in narrow channels MOSFETs. This will lead us to introduce a new phenomenon measured in nMOS transistors and we will therefore dedicate the subsequent section to the study of this effect.

Before concluding, we will investigate how temperature influences the radiation response of narrow devices and then we will finish by showing how RINCE is present in all the 65 nm CMOS processes analyzed. The phenomena introduced here will then be examined also in all the other technologies studied in this thesis.

Dependence on size. The graphs in the top row of Figure 4.11 present the percentage variation of I_{ON}^{sat} in nMOS (left) and pMOS (right) transistors exposed to a total dose of 500 Mrad(SiO_2). These transistors have a channel length $L = 10\,\mu\text{m}$ and different channel widths ranging from $W = 120\,\text{nm}$ to $W = 1\,\mu\text{m}$. As we will see in Section 5, a channel length of 10 µm strongly mitigates the spacer-related effects and therefore the evolution of these transistors is almost entirely due to the presence of the STI [160]. During irradiation, the temperature was kept at 25 °C and the devices were polarized with $V_{GS} = V_{DS} = \pm 1.2\,\text{V}$.

The radiation response of both nMOS and pMOS is strongly dependent on the channel width, with narrower transistors showing a more evident variation. Note that, for both nMOS and pMOSFETs, the transistors with $W/L = 1\,\mu\text{m}/10\,\mu\text{m}$ have a relatively small degradation even at very high doses, proving that the gate oxide in modern technologies is extremely radiation-hard.

As for the leakage current, nMOS transistors present a non-monotonic behaviour due to the different time-scale of the build-up of charge trapped in the

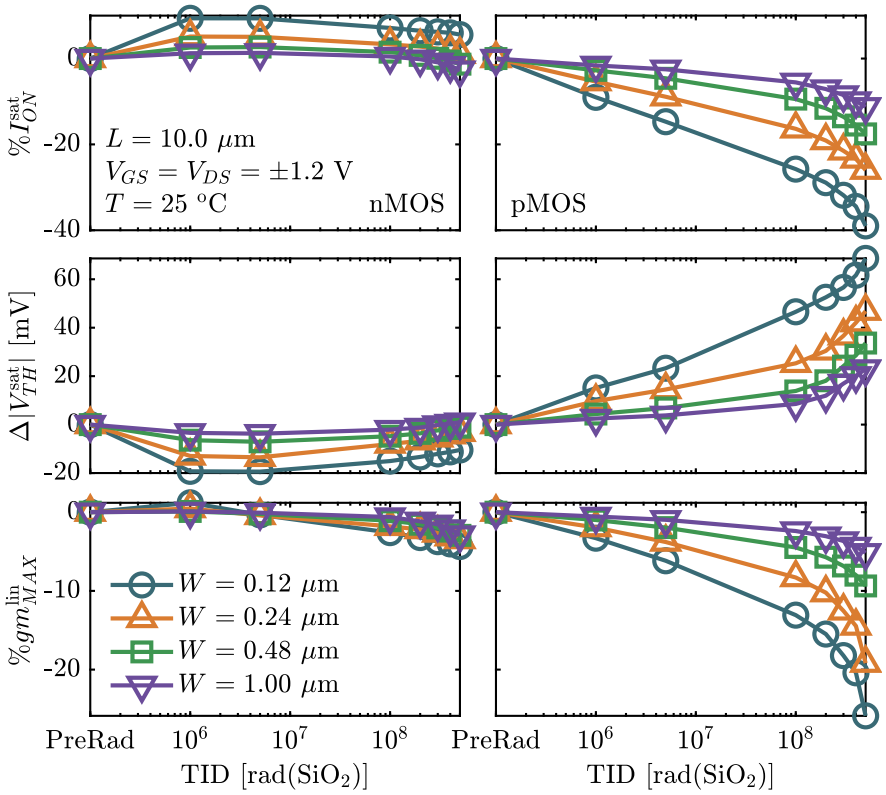


Figure 4.11: Radiation response of the maximum current I_{ON}^{sat} (top row), the threshold voltage V_{TH}^{sat} (middle row) and the peak of transconductance gm_{MAX}^{lin} (bottom row) for nMOS (left column) and pMOS (right column) transistors with different channel width and a channel length of 10 µm. For both pMOS and nMOS the effect of radiation is more evident in narrow transistors.

oxide (faster and positive) and charge trapped at the interface (slower and negative) [160]. The increase in the I_{ON}^{sat} around 1 Mrad(SiO_2) in nMOS transistors is mainly due to a decrease in the threshold voltage as illustrated in the middle row of Figure 4.11, where the variation of the absolute value of the V_{TH} extracted in saturation region is reported. The current degradation after 5 Mrad(SiO_2) is traceable to both an increase in the threshold voltage and a decrease in the transconductance, shown in the last row of the figure.

pMOS transistors, on the other hand, show a monotonic degradation of the I_{ON}^{sat}, due to both an increase in the absolute value of the threshold voltage[2] and a decrease in the transconductance. The narrowest pMOS undergoes a considerable current degradation at the end of the exposure, with a decrease in the I_{ON}^{sat} of almost 40 % at 500 Mrad(SiO_2).

The higher degradation in performance of pMOS compared to nMOS is a common feature of modern CMOS technologies, as shown repeatedly in this thesis, and is due to the sign of the charge trapped in the oxides and at the interface: while in pMOS both the oxide-trapped charge and the interface-trapped charge are positive, in nMOS they have opposite sign (positive in the oxide and negative at the interface) and therefore their effects tend to somehow compensate.

The channel width dependence, or RINCE, can be understood looking at Figure 4.12, that shows a top view of a wide and long transistor (top row) and a narrow and long transistors (bottom row), before (left column) and after (right column) irradiation. Since, in a first approximation, the thickness and quality of the STI do not change with the size of the transistor, the amount of charge trapped at the end of the exposure is more or less the same for both the narrow and the wide MOSFET. As a result, the parasitic electric field generated by the charge trapped in the STI region facing the channel is similar for the two transistors. However, the narrow transistor is proportionally much more affected by radiation, since the percentage of channel influenced by the electric field is higher [154, 160, 161]. From this figure it is also clear that the use of ELT transistor completely removes RINCEs, since the charge trapped in the STI does not face the channel (see Figure 4.10a).

It is important to notice how, in nMOS transistors, the threshold voltage decrease around 1 Mrad(SiO_2) does not lead to an increase in the leakage current, as can be seen in Figure 4.13, where the I_D (V_G) characteristic of the nMOS measured at 1 Mrad(SiO_2) does not show any substantial variation in the drain current at $V_{GS} = 0$ V (bottom-left plot). On the other hand, at TID = 500 Mrad (SiO_2), the I_{OFF} increases of more than one order of magnitude (form $\sim$ 1 pA to $\sim$ 10 pA), while the threshold voltage is increasing with respect to its value reached at TID = 1 Mrad (SiO_2). This observation leads us to conclude that the causes of the negative threshold voltage shift in narrow-channel nMOS transistors are

[2] To facilitate comparison with nMOS transistors, in this thesis we will mainly show the variation of the absolute value of the threshold voltage rather than the variation of the threshold voltage itself. Although this may generate some ambiguity with respect to the sign of the variation, it should be noted that in pMOS the trapped charge is positive both in the oxide and at the interface, which tends to always decrease (*i.e.*, make more negative) the threshold of the transistor.

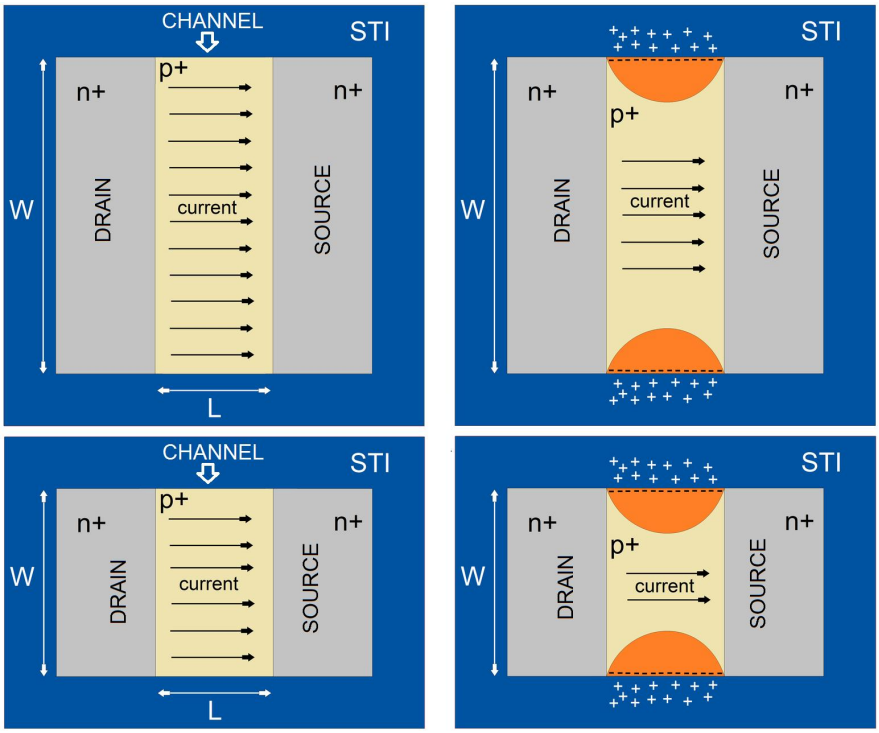


Figure 4.12: Schematic representation of the radiation induced narrow channel effects (RINCE). In narrow transistors the electric field generated by the charge trapped in the STI influences a larger percentage of the channel.

somewhat different from the causes of the radiation-induced drain-to-source leakage current, although both effects are certainly due to the positive charge trapped in the STI oxides. As further support for this claim, we show in Figure 4.14 the bias-dependence of this phenomenon. The radiation-induced threshold voltage shift is independent on both V_{GS} and V_{DS}, while the leakage current increase is basically suppressed if a $V_{GS} = 0\,\mathrm{V}$ is applied during exposure (see Figure 4.1). The independence from the bias suggests that this effect is either not related to a transport of charge in the STI or the time scale of this transport is much larger (or smaller) than the one that can be distinguished from these measures. Moreover, unlike the leakage current, the radiation-induced V_{TH}^{sat} shift does not significantly anneal with time, as shown by the right side of Figure 4.14.

The independence of the threshold voltage shift in narrow transistors was also reported by Gaillardin and co-workers in [161] for I/O pMOS transistors in 180 nm CMOS technology and was explained by the strong contribution to the electric field of the positive charge trapped in the STI after few krad(SiO_2), that reduces the effect of the applied bias on the subsequent oxide- and interface-charge trapping.

Since both RINCE and radiation-induced leakage current are obviously related to the presence of positive oxide trap in the STI, our hypothesis is that this charge is trapped in different locations: while the leakage current is caused by charge trapped in the lower part of the STI (see Subsection 4.1), the negative V_{TH} shift in nMOS is due to charge trapped in the STI-gate oxide corner. As suggested in [161], the formation of leakage paths in the trench corner is prevented by the

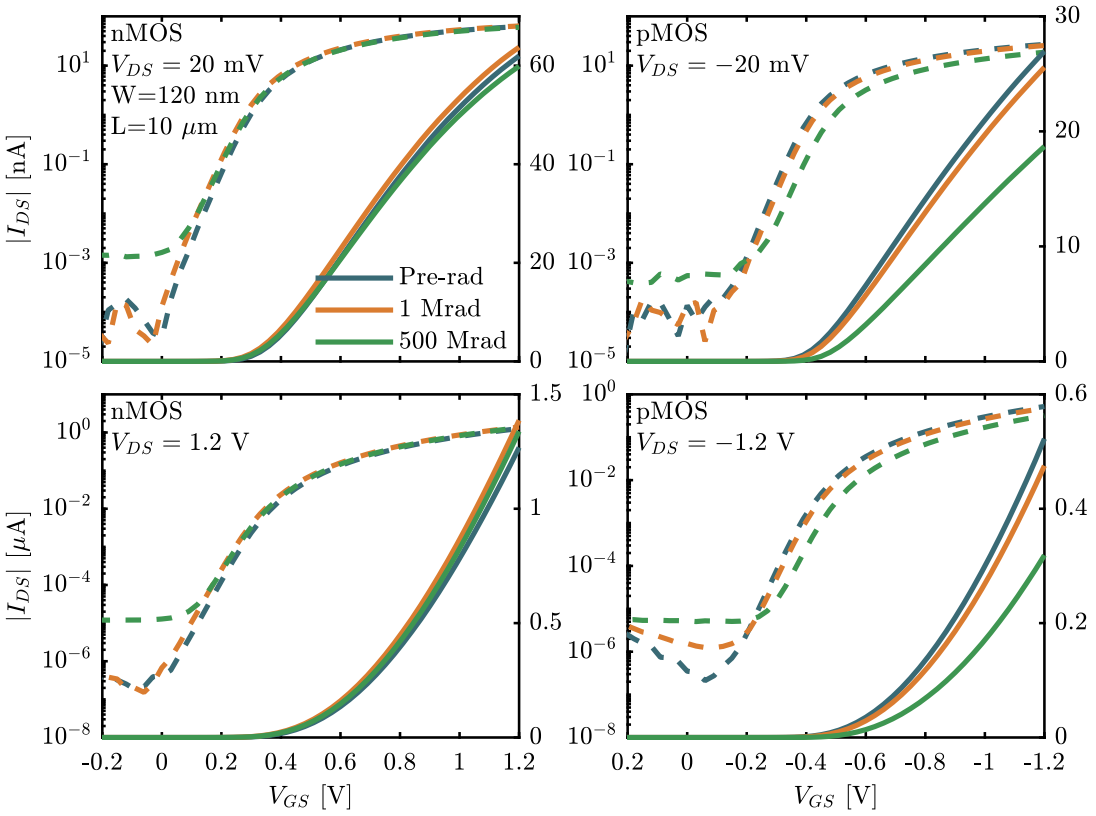


Figure 4.13: $I_D\,(V_G)$ characteristics for nMOS (left column) and pMOS (right column) transistors with a $W/L = 120\,\text{nm}/10\,\mu\text{m}$, measured in linear (top row) and saturation (bottom row) region. The degradation is clearly more important in pMOS.

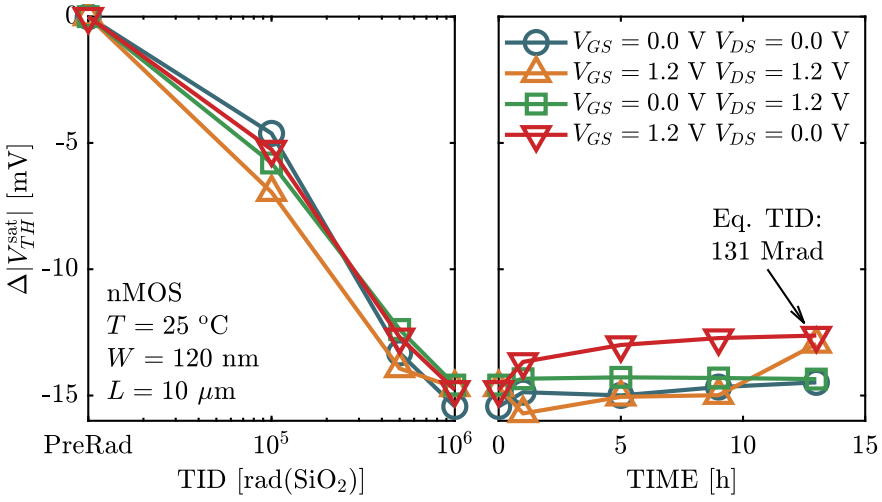


Figure 4.14: Threshold voltage shift of narrow transistors with different bias applied during irradiation. Unlike the radiation-induced leakage current, the threshold voltage shift in nMOS transistors is independent on the applied bias and does not significantly anneal with time.

gate, which has more efficient control over the parasitic transistors that tend to form in that area of the device and thus prevents it from being switched on.

Despite this being a promising first step towards developing a comprehensive model of radiation-induced effects caused by the presence of the STI, it does not clearly explain some important details, *e.g.* the different bias-dependency between the radiation response of the I_{OFF} and the threshold voltage during irradiation or why the RINCE is present in all the studied technologies while the behaviour of the radiation-induced leakage current is extremely variable. Further studies are therefore needed to investigate the STI-related effects, which, moreover, become even more peculiar when ultra-high doses are reached.

Dependence on bias. Although the influence of bias on V_{TH} variation is, in all measured technologies and for both nMOS and pMOS, negligible for TID $\leq$ 10 Mrad (SiO_2), at ultra-high doses its effect becomes apparent. Figure 4.15 shows the radiation response of 4 narrow/long channel ($W/L = 120\,\text{nm}/10\,\mu\text{m}$) nMOS (top row) and pMOS (bottom row) transistors in 65 nm CMOS technology exposed to a TID = 400 Mrad (SiO_2) and briefly annealed at $T = 25\,^\circ\text{C}$ (second column) before the high temperature annealing, performed at $T = 100\,^\circ\text{C}$ (last column). Both during irradiation and annealing, the transistors were biased with different configurations, as reported in the legend.

For pMOSFETs, a $V_{GS} < 0\,\text{V}$ provokes a large degradation in the I_{ON}^{sat} that becomes even larger when also a $V_{DS} = -1.2\,\text{V}$ is applied. This is therefore the worst case for pMOS transistors, and it is the reason why a large part of the experiments shown in this section have been performed with the devices biased in this configuration. Both the room- and high-temperature annealing do not provoke a substantial change in the I_{ON}^{sat}, that can actually recover with respect its value at the end of the exposure. However, since narrow pMOS transistors suffer a significant degradation in their performance under all the bias conditions, their use in the ASICs for the HL-LHC has to be carefully evaluated.

nMOS transistors have a more complex bias dependence. As we already noticed, the I_{ON}^{sat} increase happening around 1 Mrad(SiO_2) is the same regardless the bias. Increasing doses provoke a current reduction in transistors with $V_{GS} = 1.2\,\text{V}$, as saw in Figure 4.11 for the case $V_{GS} = V_{DS} = 1.2\,\text{V}$. This decrease seems only slightly dependent on V_{DS}. However, when $V_{GS} = V_{DS} = 0\,\text{V}$ this degradation is strongly reduced and the I_{ON}^{sat} actually further increases if $V_{DS} > 0\,\text{V}$. To summarize the observations in the nMOS:

- For TID $< \sim 10$ Mrad(SiO_2)
  - The increase in I_{ON}^{sat} is independent on the bias
- For TID $> \sim 10$ Mrad(SiO_2)
  - A $V_{GS} = 1.2\,\text{V}$ causes a degradation of the current regardless the V_{DS}
  - If $V_{GS} = 0\,\text{V}$, higher V_{DS} voltages tend to further increase the I_{ON}^{sat}

To the best of our knowledge, the "second" increase in the drain current has been described for the first time by Koch and co-workers in [162], where it is

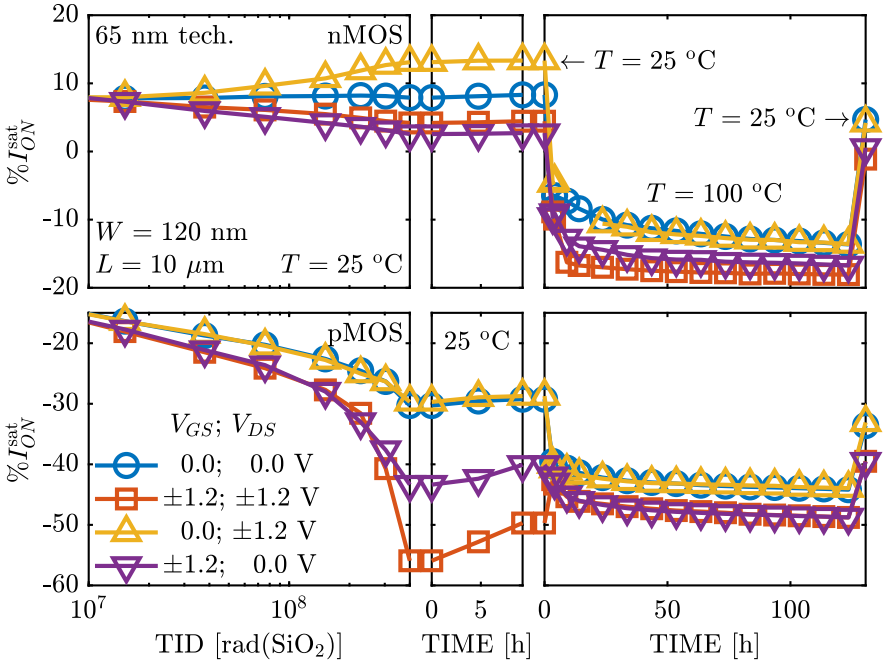


Figure 4.15: I_{ON}^{sat} evolution for nMOS (top row) and pMOS (bottom row) transistors in 65 nm technology with a $W/L = 120\,\text{nm}/10\,\mu\text{m}$, and polarized with 4 different bias configuration both during exposure (TID = 400 Mrad (SiO_2)) and during annealing at $T = 25\,°C$ (second column) and $T = 100\,°C$ (last column). The first and the last point in the high temperature annealing plot have been measured at $T = 25\,°C$.

observed in the 65 nm CMOS technology. However, we have measured it *in every technology and for every manufacturer* we tested: as already said, while the behaviour and the intensity of the radiation-induced leakage current is extremely variable, RINCEs seem to be an intrinsic feature of nanoscale CMOS technology. We will now detail how this phenomenon, called here, Ultra-high-dose Drain Current Increase (UDCI), depends on the applied bias and on the transistor size.

Ultra-high-dose Drain Current Increase effect. Figure 4.16 shows the V_{DS}-, W- and L-dependency of this effect. Because these results were obtained using chips from different wafers (and because radiation greatly increases the device-to-device variability [134]), it is not surprising that small discrepancies exist between the results of nominally equal transistors irradiated under the same conditions. However, the trends shown in the figure contribute to substantially improve our understanding of this phenomenon.

The first column depicts the I_{ON}^{sat} of 4 transistors with a $W/L = 120\,\text{nm}/10\,\mu\text{m}$, exposed to a TID = 700 Mrad (SiO_2) and biased with $V_{GS} = 0$ V and $V_{DS} = 0$, 0.6, 1.2 and 1.5 V. While at TID = 1 Mrad (SiO_2) the I_{ON}^{sat} is only slightly dependent on the bias (triangles), increasing V_{DS} voltages lead to higher drain current at ultra-high doses (squares). Moreover, although this is not clear from this figure, this effect does not saturate even at extremely high TID. This means that the contribution of the negative interface-trapped charges is somehow overwhelmed by the positive charge even at these very high doses.

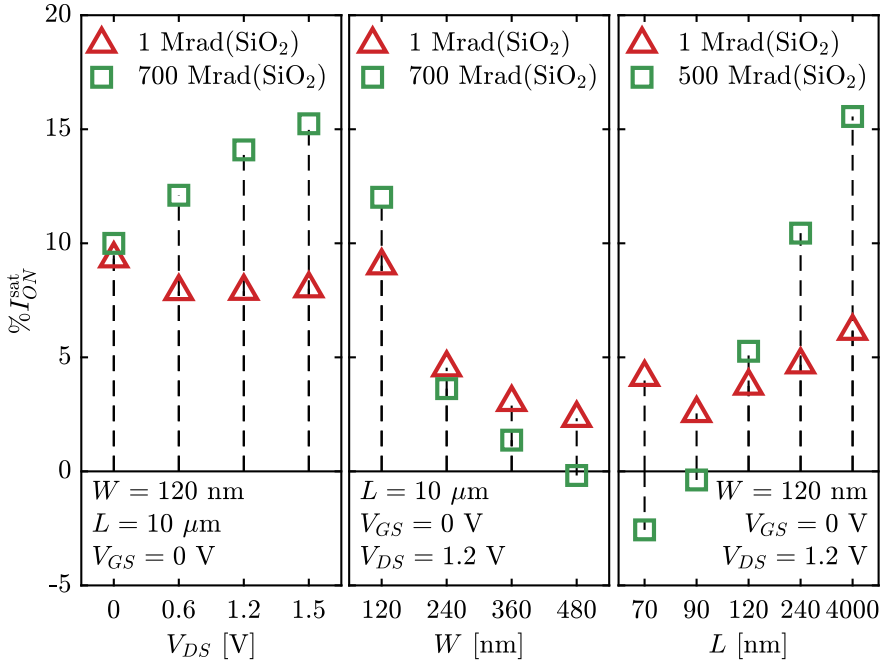
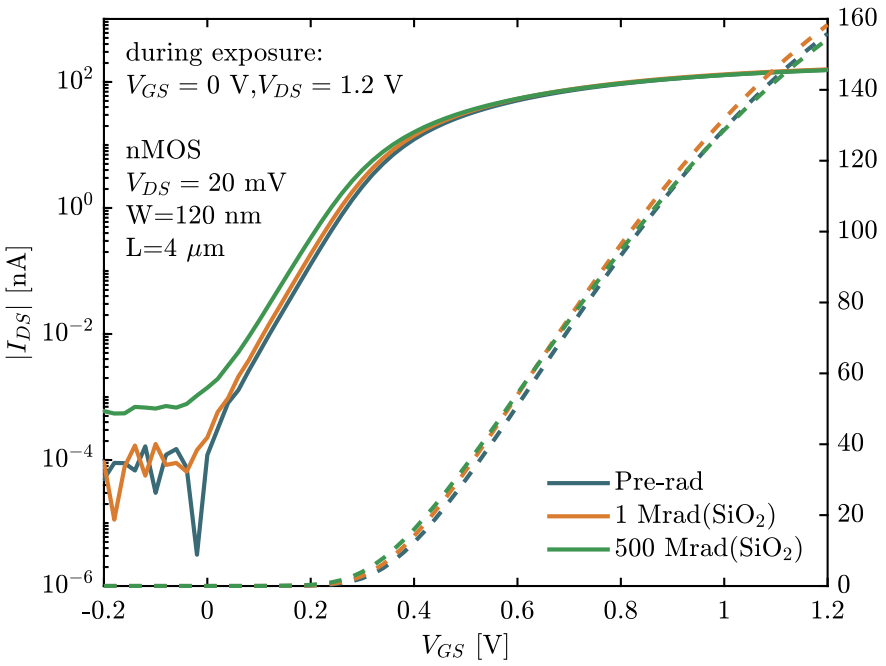


Figure 4.16: V_{DS}-, W- and L-dependency of the I_{ON}^{sat} evolution in nMOS transistors irradiated with $V_{GS} = 0\,V$ to 1 Mrad(SiO_2) (triangles) and ultra-high doses (squares). These results were obtained using chips from different wafers.

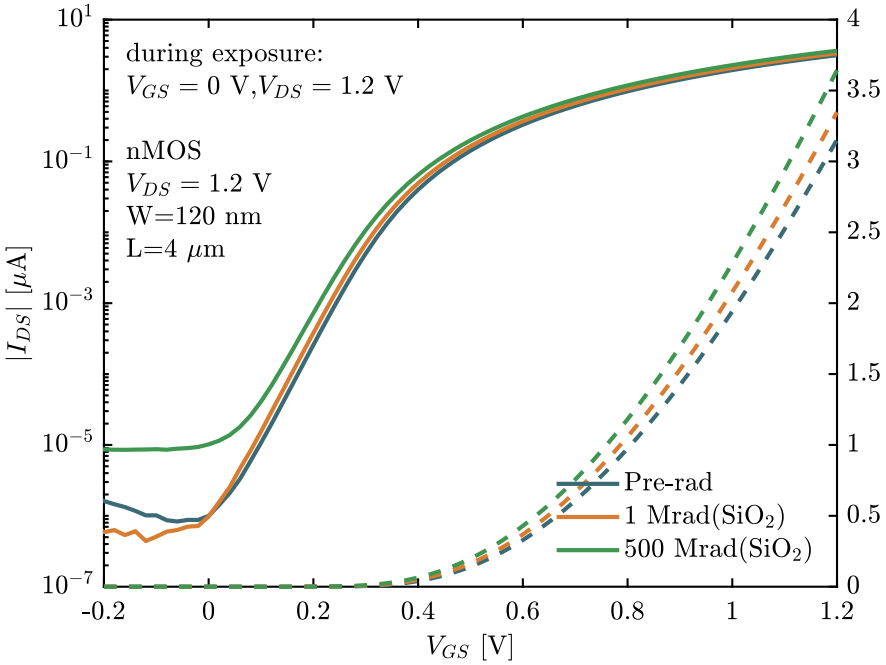
The second column shows the W-dependence of this phenomenon. Four nMOS transistors with the same channel length ($L = 10\,\mu m$) and different channel widths, have been irradiated to 400 Mrad(SiO_2) with $V_{GS} = 0\,V$ and $V_{DS} = 1.2\,V$. In this case the variation of the I_{ON}^{sat} at the end of the exposure decreases with increasing W, proving that this is a RINC-effect related to the presence of the STI. Note that the I_{ON}^{sat} at 700 Mrad(SiO_2) is lower than the I_{ON}^{sat} at 1 Mrad(SiO_2) already for the transistor with a $W = 240\,\mu m$.

Interestingly, this effect is strongly dependent on the channel length, as reported in the last column, where MOS devices with a $W = 120\,nm$ and different L have been exposed to a TID = 500 Mrad (SiO_2). In this case, the UDCI is completely removed in short channel transistors. This could be caused by concurrent radiation-induced short channel effects that, as we will see in Section 5, tend to degrade short transistors more. Another possible interpretation is that LDD and halo implants influence the doping profile in short-channel transistors, similarly to what Bonaldo and co-authors proposed in [163] to explain the dependence of the radiation response on the channel length in 28 nm technology [164–167].

To further investigate this phenomenon, we report in Figure 4.17 the $I_D\,(V_G)$ characteristics in linear (Figure 4.17a) and saturation (Figure 4.17b) region of the nMOS transistor with $W/L = 120\,nm/4\,\mu m$ of Figure 4.16, measured before irradiation, after 1 Mrad(SiO_2) and at the end of the exposure (TID = 500 Mrad (SiO_2)). We chose this transistor because it shows both the largest increase in the I_{ON}^{sat} at the end of the irradiation and the largest difference between the drain current measured at 1 and at 500 Mrad(SiO_2). Comparing the curves plotted in linear scale (dashed line, right axis), it can be noticed that,



(a) Linear region ($V_{DS} = 20\,\text{mV}$)



(b) Saturation region ($V_{DS} = 1.2\,\text{V}$)

Figure 4.17: Plot of the $I_D\,(V_G)$ characteristics in linear (Figure 4.17a) and saturation (Figure 4.17b) region of an nMOS transistor in 65 nm technology with $W/L = 120\,\text{nm}/4\,\mu\text{m}$, measured before irradiation, after 1 Mrad(SiO_2) and at the end of the exposure (TID = 500 Mrad (SiO_2)). During irradiation the device was biased with $V_{GS} = 0\,\text{V}$ and $V_{DS} = 1.2\,\text{V}$.

while in saturation region the drain current at $V_{GS} = 1.2\,\mathrm{V}$ always increases with TID, in linear region it reaches its maximum at TID $= 1\,\mathrm{Mrad}\,(SiO_2)$ while at $500\,\mathrm{Mrad}(SiO_2)$ it is lower that the pre-rad value. Therefore, in this technology, the UDCI appears only when the transistor is measured in saturation region. In addition, this effect seems to be related to the behaviour of the current in strong inversion. The radiation-induced variations in the subthreshold region of the current measured in linear mode are in fact very similar to those measured in saturation. Note also that the S_{SW} increases in both linear and saturation region, therefore the bias applied during irradiation does not seem to preclude the formation of interface traps.

The UDCI is a new and interesting effect, that, as already said, occurs in every technology we tested. From the qualification point of view, its impact in the real application has to be evaluated. Although Figure 4.15 shows that high temperature annealing removes this effect, it is not easy to understand how much time the mechanism that provokes the post-irradiation current reduction will take at 25 or $-30\,^{\circ}\mathrm{C}$ to completely remove the excess of drain current. Therefore, before we can reasonably estimate the change in performance due to this phenomenon, it is necessary to carry out further tests to understand the fundamental mechanisms underlying this effect and the respective time constants as the temperature changes.

Dependence on temperature. Moving to the study of the temperature dependence of RINCEs, we report in Figure 4.18 the maximum level of variation of the I_{ON}^{sat} (top row) and the V_{TH}^{sat} (bottom row) for narrow nMOS (left column) and pMOS (right column) transistors in 65 nm technology from Man. A irradiated at different temperatures, *i.e.*, -30, 0, 25 and $100\,^{\circ}\mathrm{C}$. All the samples have been exposed to $500\,\mathrm{Mrad}(SiO_2)$, except the device at $100\,^{\circ}\mathrm{C}$ that have been irradiated up to $400\,\mathrm{Mrad}(SiO_2)$. The bias applied during irradiation was $V_{GS} = V_{DS} = \pm 1.2\,\mathrm{V}$. Above or below each column in the figure are also indicated the TID levels, in $\mathrm{Mrad}(SiO_2)$, at which the reported value has been measured.

From this figure it is easy to understand that the nMOS transistors have a variation in their performance almost independent of the temperature and, in any case, much lower than that shown by the pMOS, which are instead very sensitive to temperature increases. Moreover, as expected, while in nMOS the maximum variation is obtained in the range between 1 and $10\,\mathrm{Mrad}(SiO_2)$, in pMOS the peak of degradation is always reached at the end of exposure, i.e. at the maximum level of TID.

The extremely large degradation of the $100\,^{\circ}\mathrm{C}$ pMOS transistors must be carefully evaluated. It is in fact important to understand if the large V_{TH} shift measured at $100\,^{\circ}\mathrm{C}$ can appear even at lower temperatures but after a longer period of time. In order to do that we performed an irradiation to $400\,\mathrm{Mrad}(SiO_2)$ at room temperature followed by $\sim 70\,\mathrm{h}$ of annealing at $T = 100\,^{\circ}\mathrm{C}$. Thanks to this experiment we are able to evaluate if the performance decrease measured in the chip irradiated at $100\,^{\circ}\mathrm{C}$ takes place only when the chip is simultaneously exposed to both TID and high temperatures (a condition that should not occur in HL-LHC) or if the increase in temperature after irradiation can cause the same

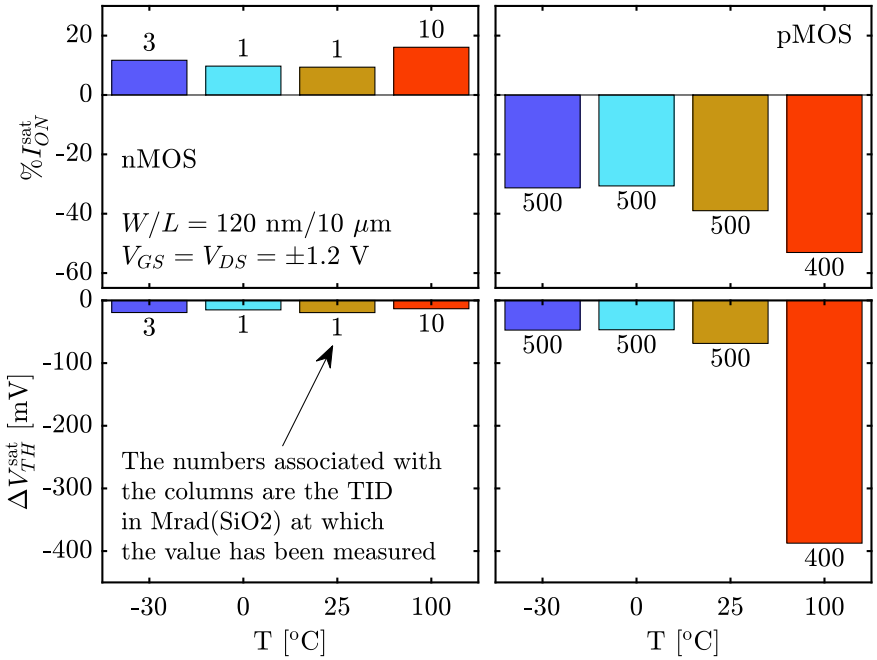


Figure 4.18: Maximum level of variation of the I_{ON}^{sat} (top row) and the V_{TH}^{sat} (bottom row) for narrow nMOS (left column) and pMOS (right column) transistors irradiated at different temperatures, *i.e.*, −30, 0, 25 and 100 °C. All the samples have been exposed to 500 Mrad(SiO_2), except the device at 100 °C that have been irradiated up to 400 Mrad(SiO_2).

degradation. Since the dose-rate of all this experiment is ∼10 Mrad(SiO_2)/h, a total dose of 400 Mrad(SiO_2) is reached in ∼ 40 h. Therefore, with an annealing of ∼ 70 h we are able to assess with certainty whether the degradation measured after high-temperature irradiation can also occur after the exposure at room temperature.

Figure 4.19 shows the variation of 4 parameters, *i.e.*, I_{ON}^{sat}, gm_{MAX}^{lin}, S_{SW}^{sat} and V_{TH}^{sat}, after the room-temperature exposure (circles) and at the end of the annealing (triangles), for transistors with different channel widths. All the reported values have been measured at room temperature. It can be noticed that the I_{ON}^{sat} of the narrowest transistor ($W = 120$ µm) recovers after the high temperature annealing. This is clearly in contrast to what seen in Figure 4.18 for the irradiation performed at 100 °C. However, the absolute value of threshold voltage increases (*i.e.*, V_{TH} decreases) even if to a significantly lower level than that reached at the end of the 100 °C irradiation. The recovery in the current is actually due to the post-irradiation increase in the transconductance, that could be an indication of annealing of interface traps, as also suggested by the decrease in the subthreshold swing. Therefore, the performance degradation of the narrow device irradiated at 100 °C cannot be reproduced by a room temperature exposure followed by high temperature annealing. This means that, from the point of view of the qualification, it is important to perform the test at the same temperature of the real application. Note also that, as expected, the variation of all the extracted parameters is smaller in wider transistors, proving once again the importance of RINCEs.

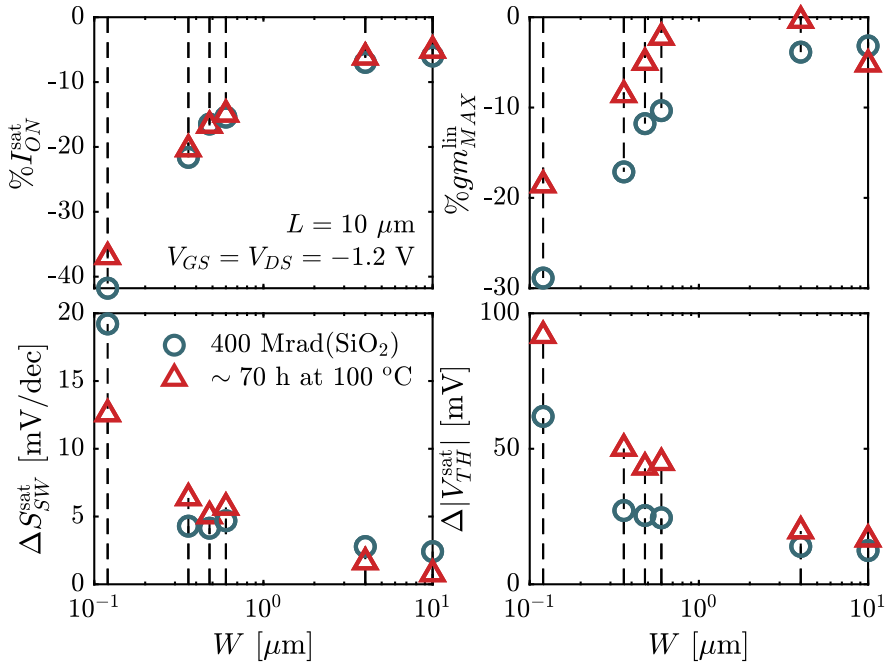


Figure 4.19: Variation of I_{ON}^{sat} (top left), gm_{MAX}^{lin} (top right), S_{SW}^{sat} (bottom left) and V_{TH}^{sat} (bottom right) for pMOS transistors with different channel widths and the same channel length (L10 µm), exposed at room temperature to a TID = 400 Mrad (SiO_2) and then annealed for $\sim$ 70 h at $T = 100$ °C.

RINCE in other 65 nm technologies. Before moving to study the RINC-effects in smaller technology nodes, we show some results on 65 nm CMOS technology from the Man. B and Man. C already introduced in Section 4.1 (see Figure 4.7).

The study of RINCE in devices from Man. B is complicated by the absence of long channel devices in the test structure. All measurements are therefore also influenced by radiation-induced short channel effects, which, as we will see in Section 5, can strongly degrade the transistor performance. Figure 4.20 depicts the radiation responses of nMOS and pMOS transistors in 65 nm CMOS technology from Man. B with minimum channel length (L = 60 nm) and two different channel widths, *i.e.*, 0.12 and 2 µm. In order to obtain some indications of the impact of the channel length, we also reported the evolution of a transistor with a W/L = 2 µm/2 µm. The irradiation has been performed to a TID = 1 Grad (SiO_2), keeping the samples at 25 °C and with $V_{GS} = V_{DS} = 1.2$ V. The effect of the presence of the STI can be noticed in the increase of the I_{ON}^{sat} in the narrow nMOS transistor at $\sim$ 5 Mrad (SiO_2), while the wide channel does not show any radiation-induced current increment. However, the difference between the two transistors is relatively small and the radiation response at high doses is dominated by the I_{ON}^{sat} degradation caused by the short channel effects, as can be deduced looking at the much smaller current decrease of the long/wide transistors. Also pMOSFETs are dominated by short channel effects and they are subjected to a significant degradation at ultra-high doses. Unfortunately, the lack of long-channel devices does not allow us to further study the RINCE in this CMOS process. However, the large decrease in performance together with

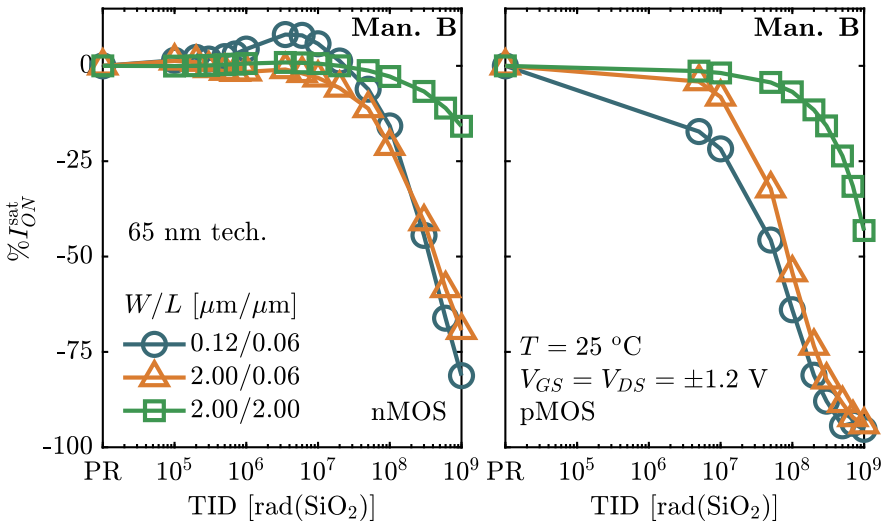


Figure 4.20: Evolution of the I_{ON}^{sat} for nMOS (left) and pMOS (right) transistors in 65 nm CMOS technology from Man. B (top row) and Man. C (bottom row). The blue dotted lines indicate the radiation response of a narrow/long (W/L = 0.12 µm/10 µm) transistor kept at −30 °C during irradiation. The "PR" label on the x-axis indicates the PreRad point.

the radiation-induced leakage current increase reported in Figure 4.7, make the devices form Man. B unsuitable for use in the design of the electronics for the particle detectors of the HL-LHC.

Also samples from manufacturer C present a severe radiation-induce reduction of their performance. In this case we can properly study the impact of RINCEs as an array of transistors with a long channel (L = 10 µm) and different W is available. Figure 4.21 shows the effect of a TID = 1 Grad (SiO_2) on nMOS and pMOS transistors with 2 different channel widths (0.12 and 1 µm). We also evaluated the impact of the temperature on the radiation response, exposing the devices at 2 different temperatures, *i.e.*, 25 and −30 °C. The left column of the figure reports the results obtained for the nMOSFETs. The variation in performance is relatively small and, as with Man. A transistors, is further reduced by keeping the devices at low temperature during exposure. Notice also that the wide transistor has an overall smaller degradation, a clear evidence of RINCE. The situation is somehow different for pMOSFETs (right column) that, at T = 25 °C, undergo a dramatic drain-current degradation regardless the width of the channel. On the other hand, when the irradiation is performed at −30 °C, the decrease in the performance is substantially reduced, and the sample presents the expected channel-width dependence. This significant temperature dependence of the radiation response is similar to that seen in manufacturer A's pMOS transistors. In that case, however, the variation was particularly evident between exposure at 100 °C and those at temperatures below 25 °C (see Figure 4.18). Therefore, it seems likely that similar phenomena occur in the two technologies, with a different temperature dependence caused by differences in the STI oxides fabrication process.

The results reported for devices from manufacturers Man. B and Man. C in-

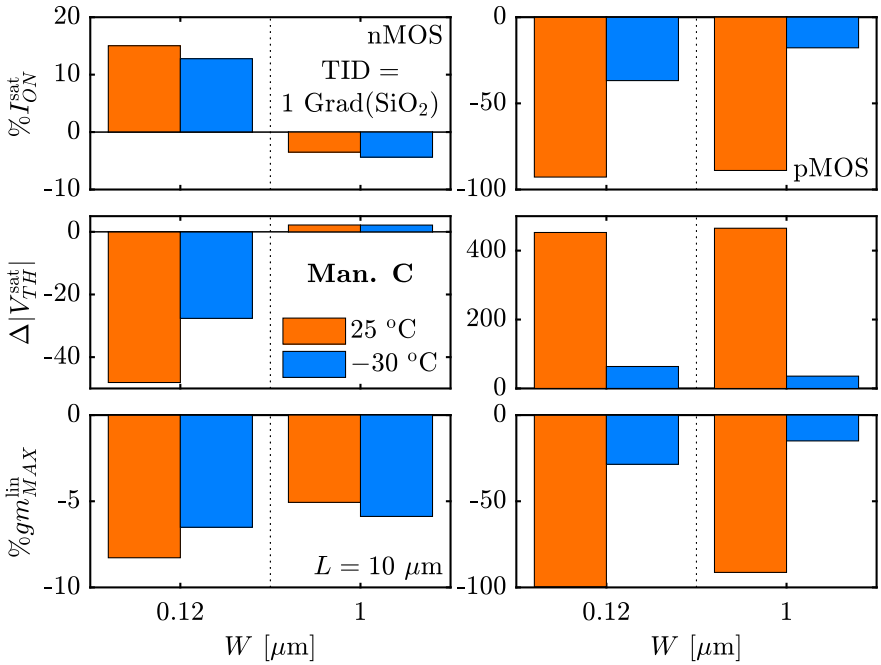


Figure 4.21: Variation of I_{ON}^{sat}, V_{TH}^{sat} and gm_{MAX}^{lin} for long channel nMOS and pMOS transistors in 65 nm CMOS technology from Man. C. The results have been reported for two different channel widths (0.12 and 10 µm) and for two different temperatures (25 and −30 °C).

dicate that RINCEs are a common feature in the 65 nm technology node and radiation-induced charge trapping in the STI oxides can strongly affect the nominal behaviour and performance of MOS transistors. However, similarly to what already seen for the radiation-induced leakage current, the magnitude of RINCE is strongly process-dependent, requiring therefore a careful analysis of the radiation response whenever a new technology is proposed to be used in a radiation environment.

4.2.2 RINCE in Other CMOS Technologies

This section demonstrates that radiation-induced narrow channel effects are a common feature of other and more advanced technology nodes as well.

Figure 4.22 shows the radiation response of an array of nMOS and pMOS transistors in 40 nm CMOS technology form Man. A, with the same $L = 10\,\mu\text{m}$ and different channel widths, exposed to 500 Mrad(SiO_2). The supply voltage of this technology is 1.1 V, therefore the I_{ON} is measured at $V_{GS} = V_{DS} = \pm 1.1\,\text{V}$ for nMOS and pMOS respectively. The irradiation has been performed at room temperature ($T = 25\,°\text{C}$).

The RINC-effect is apparent in both nMOS and pMOS transistors, with narrow devices showing a larger radiation-induced evolution. Note, however, that even the transistor with a $W/L = 10\,\mu\text{m}/10\,\mu\text{m}$ presents significant degradation at the end of the exposure. This is evident in the pMOS device, where the I_{ON}^{sat} decreases by 33.44 % at 500 Mrad(SiO_2). Since the size of the transistor is suffi-

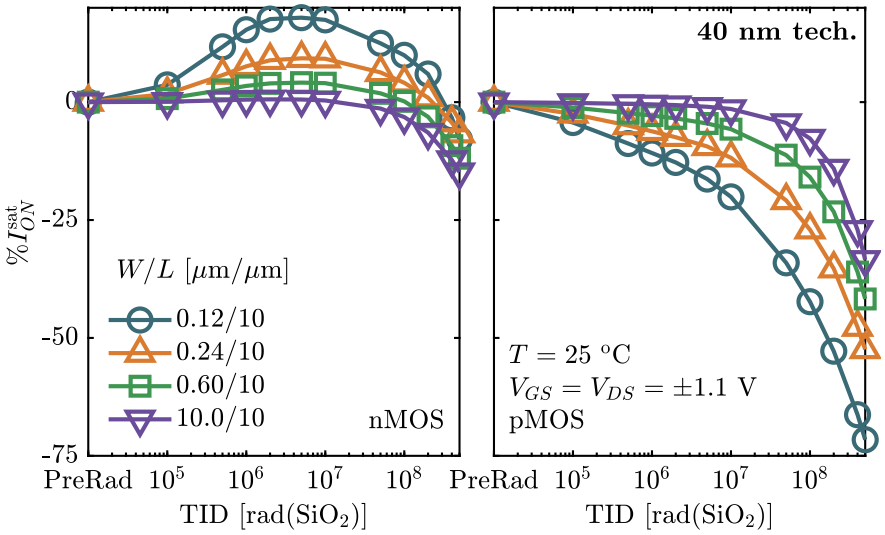


Figure 4.22: Percentage evolution of the I_{ON}^{sat} ($V_{GS} = V_{DS} = \pm 1.1$ V) of nMOS (left column) and pMOS (right column) transistors in 40 nm CMOS technology from Man. A, with the same $L = 10\,\mu$m and different channel widths, exposed to 500 Mrad(SiO_2).

ciently large to drastically reduce the impact of both radiation-induced narrow- and short-channel effects, this severe reduction in drain current could indicate a particularly radiation-sensitive gate oxide. Together with the increase in leakage current seen in Section 4.1, this makes the tested 40 nm CMOS technology unsuitable for use in environments with high radiation levels. Moreover, as indicated in Table 4.1, low temperature irradiations do not significantly improve the radiation-response. In nMOS transistors with a $W/L = 0.12\,\mu$m/$10\,\mu$m, the percentage variation of the I_{ON}^{sat} reaches its maximum at TID = 5 Mrad (SiO_2), going from 17.91 % at 25 °C to 21.98 % at −30 °C. As expected, the I_{ON}^{sat} degradation in pMOS transistors is larger at higher dose. For a TID = 400 Mrad (SiO_2), the percentage variation is −66.28 % and −52.16 % at, respectively, 25 °C and −30 °C. This is a relatively high degradation if compared to the −31.3 % reached by a transistor of the same size in 65 nm technology, exposed at TID = 500 Mrad (SiO_2) while kept at −30 °C (see Figure 4.18).

To evaluate the bias dependence of RINCE effects in 40 nm CMOS technology, we show in Figure 4.23 the radiation response of narrow/long nMOS and pMOS

Table 4.1: Percentage variation of the I_{ON}^{sat} for for a nMOS and a pMOS transistor in 40 nm technology with $W/L = 0.12\,\mu$m/$10\,\mu$m exposed to a TID of 5 Mrad(SiO_2) and 400 Mrad(SiO_2) at different temperature.

T	Mrad(SiO_2)	I_{ON}^{sat} nMOS	I_{ON}^{sat} pMOS
25 °C	5	17.91%	−16.31%
	400	−3.32%	−66.28%
−30 °C	5	21.98%	−14.29%
	400	−0.72%	−52.16%

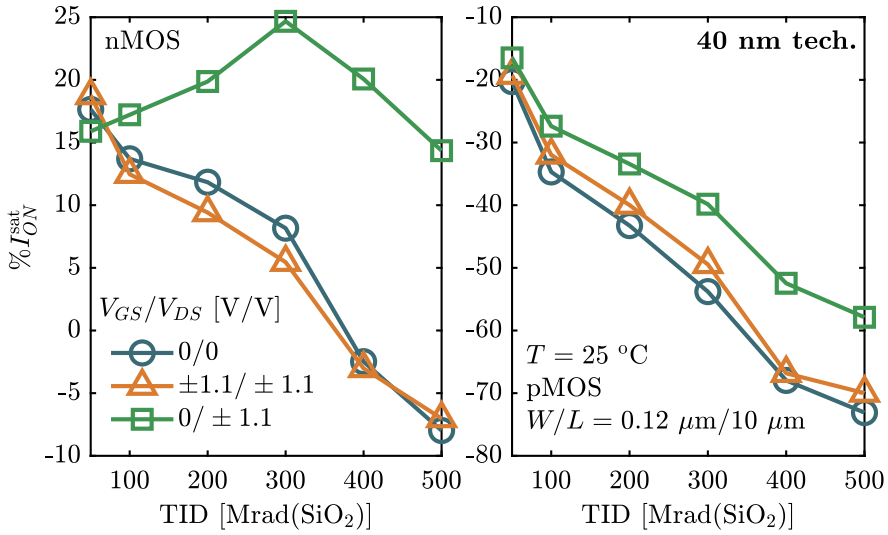


Figure 4.23: Bias dependence of the percentage evolution of the I_{ON}^{sat} ($V_{GS} = V_{DS} = \pm 1.1\,V$) for narrow channel nMOS and pMOS transistors in 40 nm CMOS technology from Man. A. Note that the y-axis scale is not the same in the two charts and the x-axis starts at 50 Mrad(SiO$_2$).

transistors ($W/L = 0.12\,\mu m/10\,\mu m$) polarized with different biases and irradiated, at room temperature, to a TID = 500 Mrad (SiO$_2$). The application of different biases only slightly affects the radiation response, except for the nMOS polarized with $V_{GS} = 0\,V$ and $V_{DS} = 1.1\,V$, were the UDCI effect can be noticed. However, unlike 65 nm, the current tends to decrease when very high doses are reached (in this case TID > 300 Mrad (SiO$_2$)).

The radiation response of narrow channel transistors in the studied 40 nm CMOS technology is therefore very similar to what seen in the 65 nm, with, however, an overall larger degradation at ultra-high TID, maybe caused by a softer gate oxide.

We now move to study the 28 nm CMOS technology that, as we will see, seems very promising from the point of view of the high energy physic applications.

Figure 4.24 shows the evolution of the I_{ON}^{sat} (measured at $V_{GS} = V_{DS} = V_{DD} = 0.9\,V$) for nMOS (left) and pMOS (right) transistors in 28 nm CMOS technology from Man. A. All the transistors have the same L of 1 µm and different channel widths, ranging from 0.1 to 3 µm. The samples have been exposed to 1 Grad(SiO$_2$) while kept at $T = 25\,°C$ and biased with $V_{GS} = V_{DS} = \pm 0.9\,V$. As already seen for all the other technologies studied in this thesis, narrower transistors show a larger evolution (RINCE). A similar behaviour was reported in [165–167] for a different process of the same 28 nm technology form Man. A. Note that the current degradation of the wide/long transistor is relatively small even at the end of the exposure (TID = 1 Grad (SiO$_2$)). In particular, I_{ON}^{sat} decreases by $-6.62\,\%$ for the nMOS transistor while the pMOS undergoes a variation of $-12.5\,\%$. These values clearly demonstrate that, in this technology, the gate oxide is extremely robust to radiation. This is a remarkable result since the gate oxide in this 28 nm CMOS process is fabricated with an High-k Metal Gate (HKMG) gate-

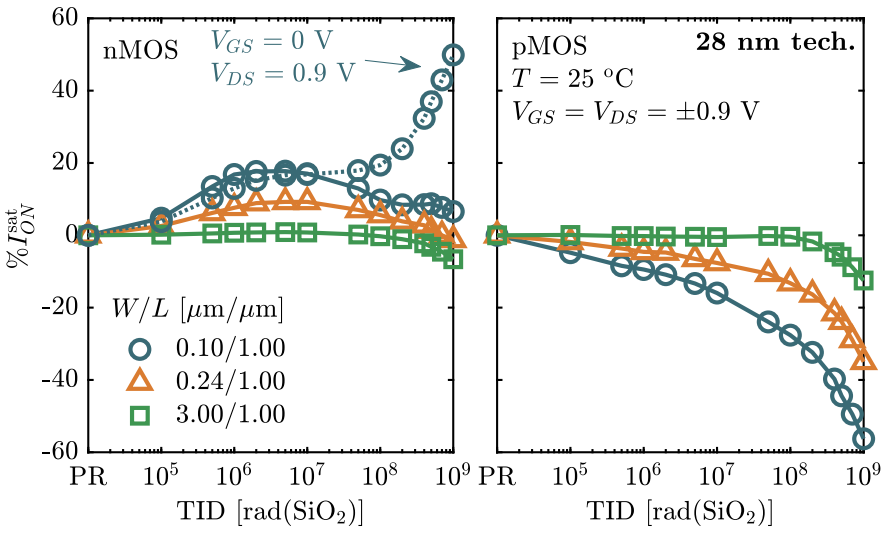
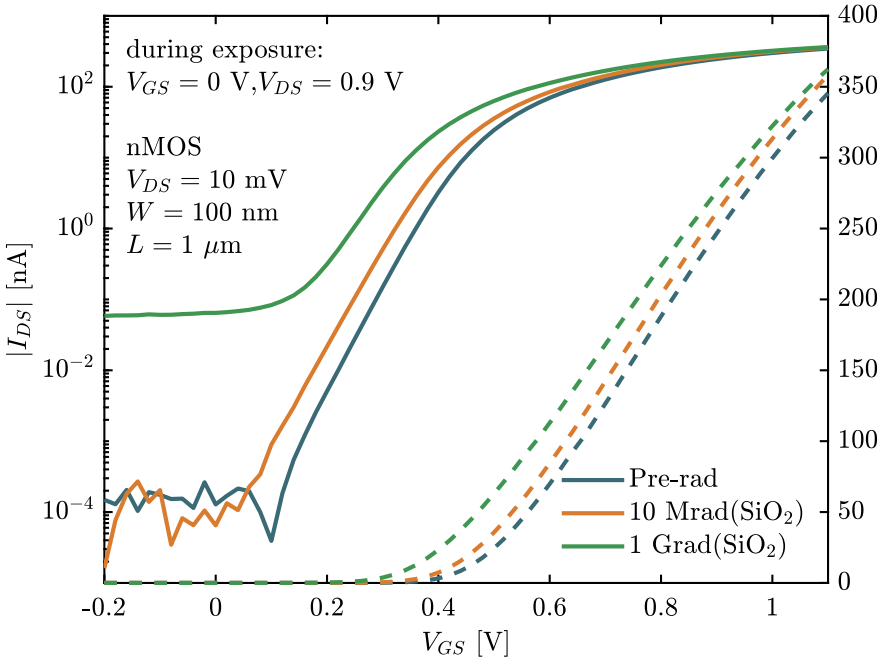


Figure 4.24: Percentage evolution of the I_{ON}^{sat} of nMOS (left column) and pMOS (right column) transistors in 28 nm CMOS technology from Man. A, with the same $L = 1\,\mu m$ and different channel widths, exposed to 1 Grad(SiO$_2$). The dotted line reports the evolution of a narrow nMOS transistor irradiated with $V_{GS} = 0\,V$ and $V_{DS} = 0.9\,V$.

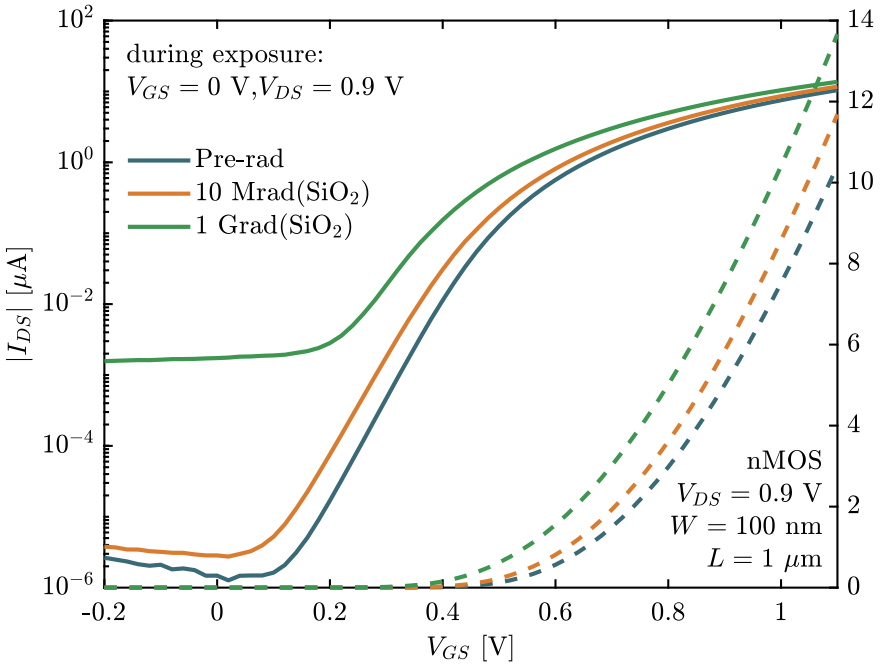
last technology, composed by a stack of hafnium oxide (HfO_2) surmounting a thin layer of SiO_2 [168, 169]. Therefore, although gate oxide in 28 nm technology is physically thicker than in 65 nm CMOS process, its degradation is certainly comparable or even lower. In fact, in an experiment not shown in this thesis, we measured in a pMOS transistor in 65 nm technology with a $W/L = 10\,\mu m/10\,\mu m$ a $\sim 15\,\%$ degradation of the maximum current after a TID = 1 Grad (SiO_2).

Figure 4.24 also shows, indicated by the dotted line, the evolution of the I_{ON}^{sat} for a narrow nMOS transistor irradiated with $V_{GS} = 0\,V$ and $V_{DS} = 0.9\,V$. Similar to what happens in both 65 and 40 nm technologies, the drain current increases at ultra-high doses, reaching a variation of $\sim 50\,\%$ at 1 Grad(SiO_2). Figure 4.25 reports the $I_D\,(V_G)$ characteristics, measured before irradiation, at 1 Mrad(SiO_2) and at 1 Grad(SiO_2), in linear (Figure 4.17a) and saturation (Figure 4.17b) region, where the UDCI effect is clearly more evident. The physical mechanisms that determine this effect have to be studied and their actual impact on the real application has to be evaluated. Therefore, this interesting phenomenon related to the presence of STI will be at the centre of our future research.

Let us now assess the temperature dependence of the radiation response of the 28 nm CMOS technology. Figure 4.26 shows the percentage variation of the I_{ON}^{sat} for two narrow nMOS and pMOS transistors ($W/L = 0.10\,\mu m/1\,\mu m$) after a TID of 1 Grad($SiO_2$). The irradiation was performed at $T = -30\,°C$ and the two transistors were polarized with different biases, as reported in the figure. To facilitate the comparison with the room temperature irradiation, we also report in Table 4.2 the I_{ON}^{sat} degradation at 25 and $-30\,°C$ after 1 Grad(SiO_2). Similar to what happens in the 65 nm technology (see Figure 4.18), the response to radiation of narrow transistor polarized with $V_{GS} = V_{DS} = \pm 0.9\,V$ is only slightly influenced by temperature in the range $-30\,°C \leq T \leq 25\,°C$. However, the UDCI effect is



(a) Linear region ($V_{DS} = 10\,\mathrm{mV}$)



(b) Saturation region ($V_{DS} = 0.9\,\mathrm{V}$)

Figure 4.25: $I_D\,(V_G)$ characteristics in linear (Figure 4.17a) and saturation (Figure 4.17b) region of an nMOS transistor in 28 nm technology with $W/L = 100\,\mathrm{nm}/1\,\mu\mathrm{m}$, measured before irradiation, after 10 Mrad(SiO_2) and at the end of the exposure (TID = 1 Grad (SiO_2)). During the irradiation the device was biased with $V_{GS} = 0\,\mathrm{V}$ and $V_{DS} = 0.9\,\mathrm{V}$ while the temperature was kept at 25 °C.

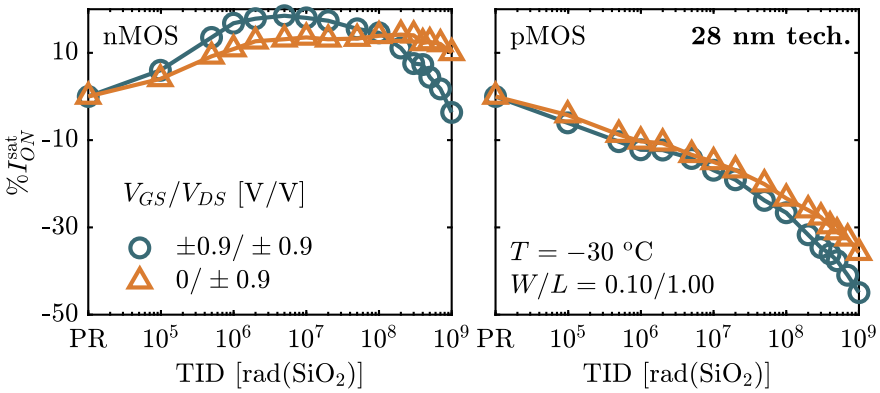


Figure 4.26: I_{ON}^{sat} vs TID for nMOS (left) and pMOS (right) transistors with a $W/L = 0.10\,\mu m/1\,\mu m$. The irradiation was performed at $T = -30\,°C$ with two different biases to a TID of 1 Grad(SiO_2).

Table 4.2: Percentage variation of the I_{ON}^{sat} for transistors in 28 nm technology exposed to a TID of 1 Grad(SiO_2) at different temperatures and biases.

T	TID	V_{GS}/V_{DS}	I_{ON}^{sat} nMOS	I_{ON}^{sat} pMOS
25 °C	1 Grad(SiO_2)	± 0.9 V/± 0.9 V	6.58%	−56.28%
		0 V/± 0.9 V	49.89%	−34.82%
−30 °C	1 Grad(SiO_2)	± 0.9 V/± 0.9 V	−3.65%	−44.94%
		0 V/± 0.9 V	9.99%	−35.8%

significantly reduced. This is a clear indication that also for the 28 nm technology temperature can play a major role and more studies are therefore needed. It is also worth to be noted that, to the best of our knowledge, this is the first time that a study of the temperature dependence of the radiation response in the 28 nm CMOS technology node is reported.

4.2.3 Conclusions on STI-Related Effects

In this long section we have described the main radiation-induced STI-related effects, *i.e.*, the leakage current increase and the RINCE, in 130, 65, 40 and 28 nm CMOS technologies. Both these effects can be a serious threat for the reliability of ASICs operating in radiation environments, provoking an increase in the power consumption and a strong variation from the nominal performance. While the radiation response of the leakage current is extremely sensitive to variation in the process, RINCE is common to all the studied technologies, with some distinguishing features such as a larger degradation in pMOS transistors, a relatively small dependence on temperature and an increase in the I_{ON}^{sat} in narrow nMOS transistors biased with $V_{GS} = 0\,V$ and $V_{DS} > 0\,V$. Both RINCE and the leakage current increase can be avoided using enclosed layout transistors, which prevent the charge trapped in the STI from affecting the electric field in the channel. It is however important to note that ELTs have a minimum equivalent channel width significantly larger than the minimum W of a standard transistor in the

same technology (*e.g.*, in 65 nm technology $W_{\text{min}}^{\text{ELT}}/W_{\text{min}}^{\text{STD}} = 1320\,\text{nm}/120\,\text{nm}$), therefore, since RINCEs become less important at larger W, the use of an ELT has to be carefully evaluated by comparing its radiation response with that of a standard transistor of the same size. In fact, in the absence of leakage, a standard transistor could have a radiation response similar to that of an ELT of the same dimensions without introducing the problems related to the use of enclosed transistors that we have described at the end of Subsection 4.1.

Chapter 5

Spacers-Related Effects

In addition to STI, other oxides used during the manufacturing process of advanced CMOS technologies can severely degrade the radiation hardness of MOS transistors. This is the case for the spacer oxides located along the sides of the polysilicon gate and employed in order to allow the implantation of LDD extensions. They usually consist of a layer of SiO_2 surmounted by silicon nitride Si_3N_4 [170, 171]. Figure 5.1 shows a transmission electron microscopy (TEM) image of a 65 nm CMOS transistor [172] where the two spacers, the silicon oxide and silicon nitride layers, have been highlighted. Note that the thickness of these insulators is significantly higher than that of the gate oxide, thus making them more sensitive to damage caused by ionizing radiation.

Unlike the STI, the spacers-related effects on the radiation response of MOS transistors have only been studied recently, as their impact is evident only at very high doses (TID $\gg 1\,\mathrm{Mrad}\,(SiO_2)$), much higher than those of interest for space application. Large part of the following description of spacers-related phenomena in 65 nm CMOS technology is reported in [172].

The first indication of a possible impact of spacers on the radiation response was the discovery of a channel length dependence in the evolution of the drain current in irradiated devices, as shown in Figure 5.2. The percentage degradation of the maximum drain current I_{ON} is shown for transistors of different lengths irradiated up to $400\,\mathrm{Mrad}(SiO_2)$ and then kept at $T = 100\,^{\circ}\mathrm{C}$ for 100 h after exposure. Since the W of these transistors is equal to 20 µm, the effects related

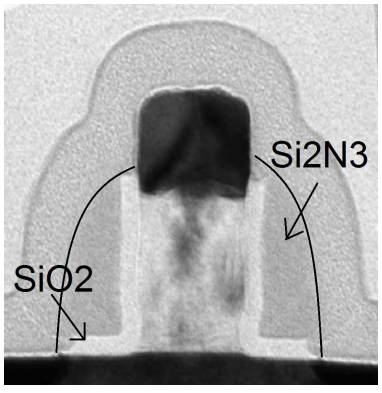


Figure 5.1: TEM image of a 65 nm CMOS technology [172].

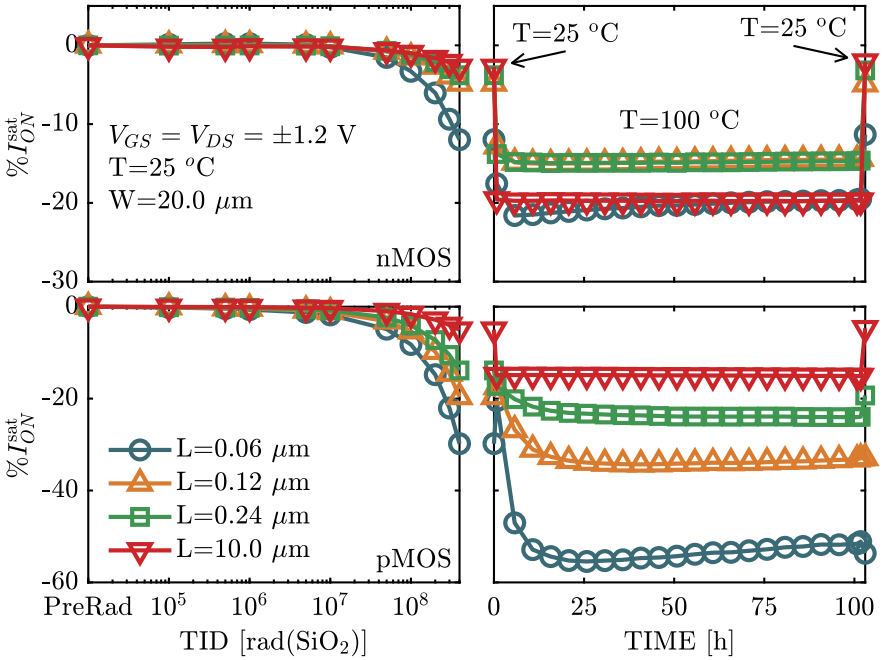


Figure 5.2: Percentage variation of the I_{ON} for nMOS (top row) and pMOS (bottom row) transistors with different channel length and a $W = 20\,\mu m$ measured during irradiation up to 400 Mrad(SiO_2) (left column) and for 100 h with $T = 100\,°C$. Note the that the first and the last point of the post-irradiation evolution have been measured at $T = 25\,°C$.

to the presence of STI can be completely neglected, as detailed in Chapter 4. Moreover, very similar results have been obtained also in enclosed transistors, where the influence of the STI on the radiation response is avoided by design.

Shorter transistors are clearly more affected by the ionizing dose, with a larger degradation in pMOSFETs, which also show a further dramatic deterioration as the temperature rises (right column). The first and the last point of the reported annealing have been measured at $T = 25\,°C$ while all the other measurements have been performed at $T = 100\,°C$. Note that the longest transistor ($W/L = 20\,\mu m/10\,\mu m$) has a very small degradation during irradiation and a negligible evolution during high-temperature annealing, proving once again the extreme robustness of the gate oxide. Note also that the current degradation is almost negligible for both nMOS and pMOS up to at least a TID = 10 Mrad (SiO_2), which is a quite high total dose for space applications, but is two orders of magnitude lower than the highest level of TID expected to be reached in HL-LHC.

The phenomena that cause the dependence of the radiation response on the channel length have been described by Faccio ad co-authors in [160] as radiation-induced short channel effects or RISCE.

5.1 RISCE in 65 nm CMOS Technology

Since RISC-effects are easier to study in pMOS transistors, the first part of this subsection will focus on the radiation response of p-channel MOSFETs.

Figure 5.3 shows the evolution of the transconductance gm^{lin}_{MAX} and the threshold voltage shift during irradiation and annealing. During exposure, the current degradation reported in Figure 5.2 is almost entirely caused by a decrease in the transconductance while the absolute value of the threshold voltage only marginally increases. On the other hand, high temperature annealing leads to both a slightly recovery of the transconductance and an increase in the absolute value of the threshold voltage of almost 250 mV with respect to the value reached at the end of irradiation. The V_{TH} of these pMOS transistors becomes therefore more negative.

The degradation of the transconductance during irradiation is related to an increase in the series resistance R_{SD}. The $gm = \frac{\partial I_{DS}}{\partial V_{GS}}$ curves of an ELT with $W/L = 10\,\mu\text{m}/60\,\text{nm}$ measured at different irradiation levels and reported in Figure 5.4a show in fact a "vertical translation" of the gm characteristics, a behaviour commonly related to an increase in the series resistance [173]. Figure 5.4b shows the extracted ΔR_{SD} for the array of different channel lengths and $W = 20\,\mu\text{m}$ reported in Figure 5.2. The method used to extract the series resistance is the one proposed by Fleury and co-workers in [174], but qualitatively similar results have been obtained using also other extraction methods (*i.e.*, [175, 176]). For this array the series resistance increases of $400\,\Omega \cdot \mu\text{m}$ after a TID = 400 Mrad (SiO_2). Note that a single value of R_{SD} is extracted for all the different channel lengths in the array because the series resistance should be independent on the channel length[1]. However, as the channel length decreases, the source-drain current increases and consequently the voltage drop caused by the series resistance increases. This explains the channel length dependence of the radiation response displayed in Figure 5.2. Figure 5.4b also reports the ΔR_{SD} for an array of pMOS transistors irradiated at T=−30 °C. In this case the degradation is clearly lower, in analogy with what already reported for the STI-related effects.

We have seen that during high temperature annealing the transconductance recovers but, on the other hand, pMOS transistors undergo a severe threshold voltage shift (see Figure 5.3). Moreover, post-irradiation annealing makes the transistor highly asymmetric. Figure 5.5a reports the $I_D\,(V_G)$ characteristics in saturation region of an enclosed transistor exposed to a TID = 400 Mrad (SiO_2) and then annealed at 100 °C for 21 h. The dashed lines show the drain current measured with the roles of the drain and source electrodes reversed with respect to the configuration used during irradiation, here called "nominal", as also indicated in Figure 5.5c. Before irradiation the transistors is, as expected, symmetric, *i.e.*, with the role of source and drain only determined by the applied bias[2]. Even after a TID = 400 Mrad (SiO_2) the $I_D\,(V_G)$ in nominal and reverse configuration are almost identical. However, after high temperature annealing the transistor gets strongly asymmetric, with a large threshold voltage shift of the drain current measured in nominal configuration. This asymmetry is noticeable only in saturation region ($V_{DS} = -1.2\,\text{V}$) while, as reported in Figure 5.5b, in linear re-

[1] Recently, a possible L-dependence of the series resistance has been proposed in [177].

[2] Enclose transistors are actually physically asymmetric, in the sense that source and drain electrodes have different dimensions (see Figure 4.10a). However this does not affect the symmetry of the $I_D\,(V_G)$ characteristics before irradiation.

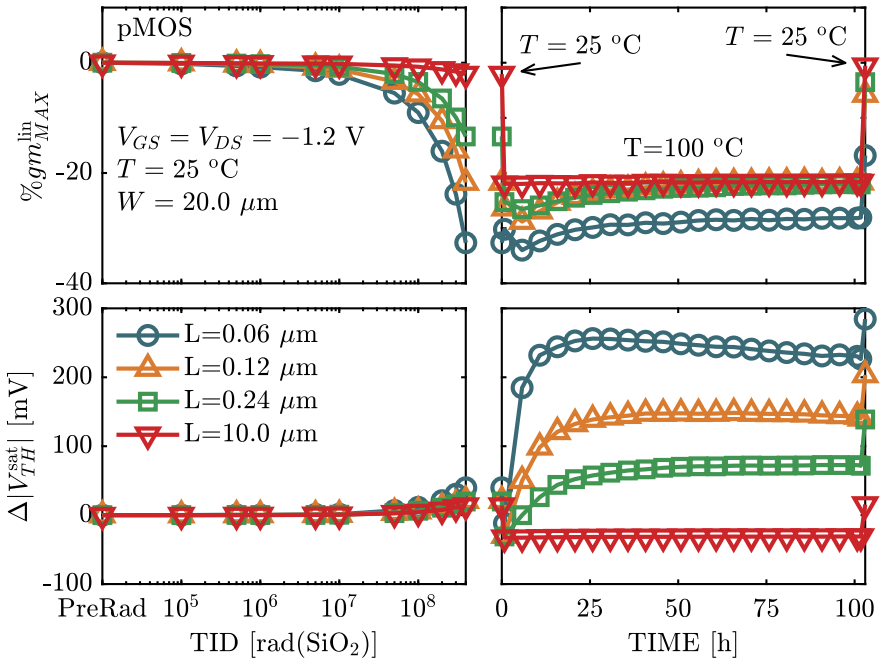
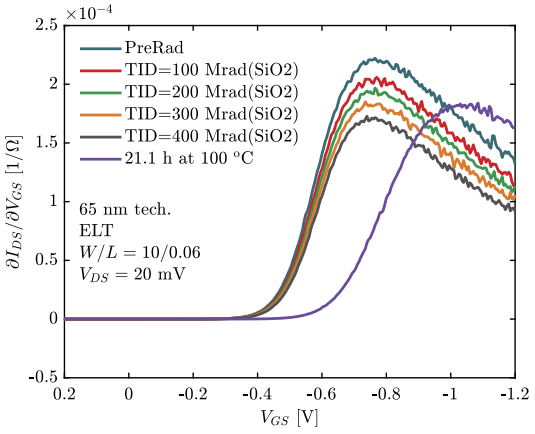
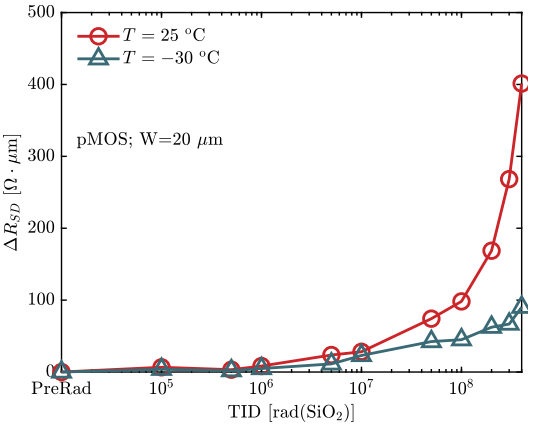


Figure 5.3: Percentage variation of the gm^{lin}_{MAX} (top row) and threshold voltage shift (bottom row) for pMOS transistors with different channel length and a $W = 20\,\mu\text{m}$ measured during irradiation up to 400 Mrad(SiO$_2$) (left column) and for 100 h with $T = 100\,^{\circ}\text{C}$.

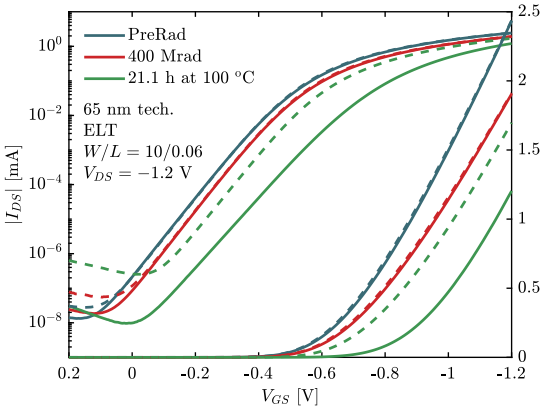


(a) gm vs V_{GS} for a short channel ELT pMOS transistor irradiated to 400 Mrad(SiO$_2$) and then annealed at $T = 100\,^{\circ}\text{C}$. The degradation is comparable for all values of V_{GS}, suggesting that mobility degradation is not the dominant mechanism (after [172]).

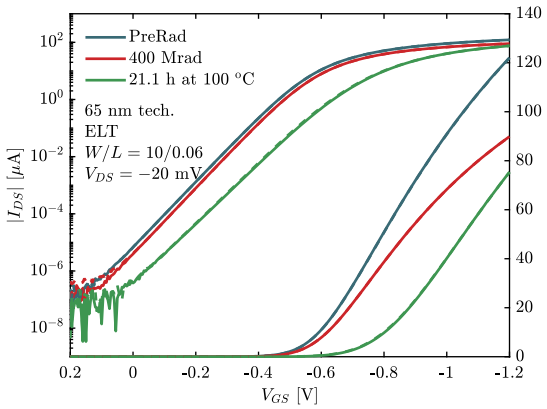


(b) Radiation-induced increase in the series resistance for pMOS transistors exposed to a TID = 400 Mrad (SiO$_2$) at 25 and $T = -30\,^{\circ}\text{C}$. Low tempertaures strongly reduce the radiation-induced increase in the series resistance.

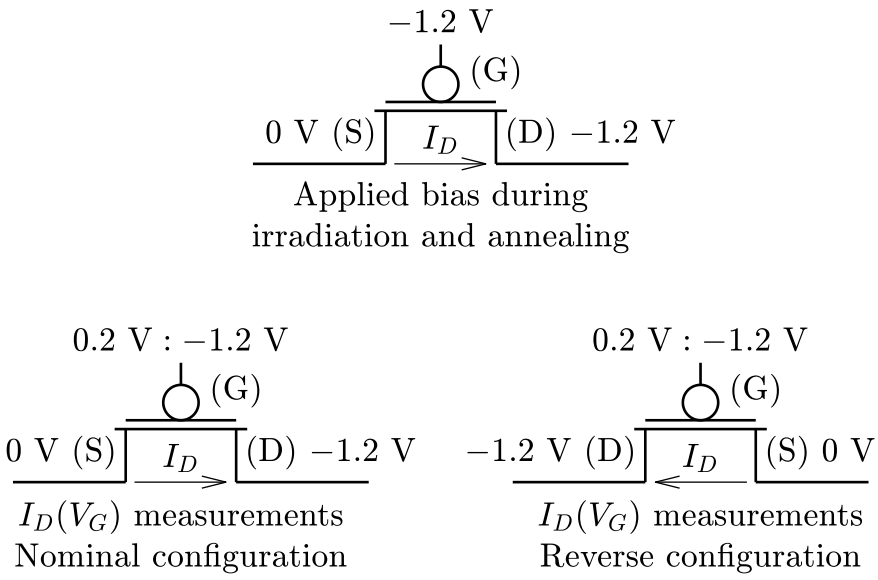
Figure 5.4: Transconductance variation and series resistance increase in 65 nm technology.



(a) $I_D\,(V_G)$ in saturation region for a short-channel ELT pMOS transistor measured in nominal (solid lines) and reverse (dashed lines) configuration before exposure, after irradiation and at the end of 21 hours of annealing at $T = 100\,°C$. The transistor becomes asymmetric only after annealing, with the nominal configuration suffering a larger V_{TH} shift (after [172]).



(b) $I_D\,(V_G)$ in linear region for a short-channel ELT pMOS transistor measured in nominal (solid lines) and reverse configuration before exposure, after irradiation and at the end of 21 hours of anenaling at $T = 100\,°C$. The transistor does not show any asymmetry, and the V_{TH} shift is comparabale to that measured in saturation for the nominal configuration.



(c) Schematic representation of the nominal and reverse configuration. The top illustration depicts the transistor with the bias applied during irradiation and annealing, while the two images in the bottom report the voltages applied during measuremenets in nominal (left) and reverse (right) configurations. In the reverse configuration (bottom right), the roles of source and drain are reversed with respect to those used during irradiation and annealing (top).

Figure 5.5: Radiation-induced asymmetry in short channel pMOS transistors.

gion there is no sign of any asymmetry, even if the voltage-current characteristic experiences a threshold voltage shift comparable to that measured in saturation.

Both radiation-induced threshold voltage shift and asymmetry are strongly dependent on temperature and bias, as respectively report in Figure 5.6a and 5.6b. If the temperature is sufficiently high, the threshold voltage shift can appear already during irradiation (Figure 5.6a). While transistors irradiated at -30 and 25 °C show a relatively small ΔV_{TH} and negligible asymmetry, samples irradiated at high temperatures undergo a large threshold voltage shift and become all the more asymmetrical the higher the temperature during irradiation.

Figure 5.6b shows the evolution of ELT polarized with different combination of V_{GS} and V_{DS} exposed up to a TID = 400 Mrad (SiO_2) at 25 °C and then annealed for 100 h at 100 °C. As already mentioned, the use of enclosed transistors removes any influence of the STIs, therefore the radiation response is dominated by the presence of the spacers. Only a $V_{GS} < 0$ V provokes a large V_{TH} shift, that becomes even larger and asymmetric if a $V_{DS} < 0$ V is applied.

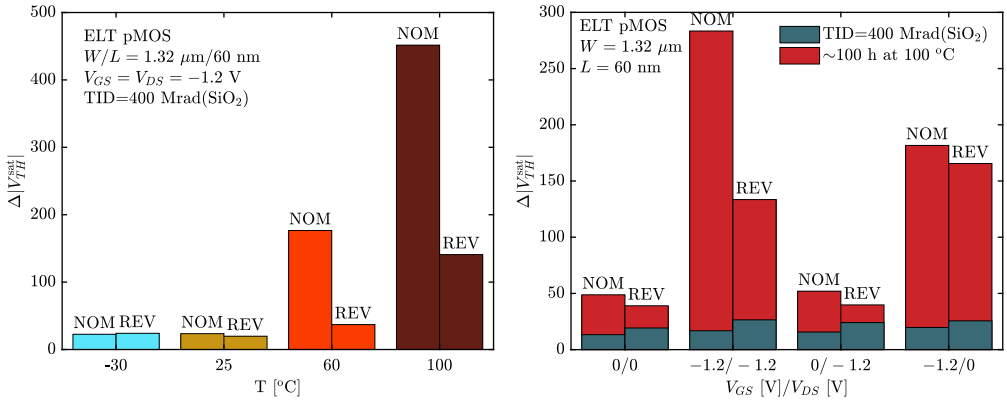
All the evidences reported so far can be summarized as follow:

- Irradiation causes an increase in the series resistance, substantially independent on bias (see Figure 5.6b and [178])
- High temperature can provoke, either during or after irradiation, a large threshold voltage shift if a $V_{GS} < 0$ is applied
- If also a $V_{DS} < 0$ is applied the transistor becomes asymmetric, however only in the saturation regime

This complex radiation response has been explained with the following model, detailed by Faccio and co-workers in [172]:

1. Figure 5.7a. Irradiation causes an accumulation of charge and releases hydrogen ions in the spacers, resulting in an increase in the series resistance and a consequent decrease in the transconductance. In particular, the electric field generated by the charge trapped in the spacers affects the underlying low-doped LDD extensions. A similar hypothesis can also be found in [173, 179].
2. Figure 5.7b. Under high temperature and bias, the hydrogen ions H^+ released during irradiation drift from the spacers into the gate oxide. If a $V_{DS} < 0$ is applied, this charge transport is inhibited on the drain side but promoted on the source side (in pMOS).
3. Figure 5.7c. Once in the gate oxide, the hydrogen ions de-passivate Si-H bonds creating Si/SiO_2 interface traps as described in subsection 2.2.6 and provoking the measured large threshold voltage shift.

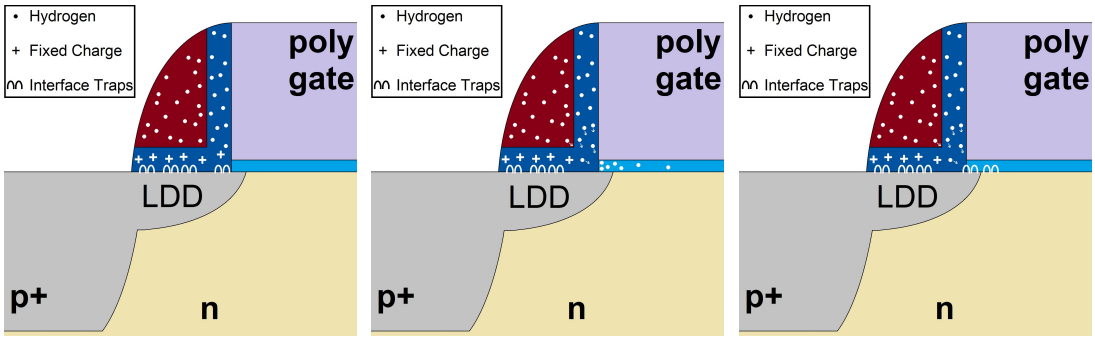
In the following we will validate this model both through numerous experimental tests, such as static and charge pumping measurements, and thanks to TCAD simulations. We will also extract the activation energy of the threshold



(a) V_{TH} shift measured in nominal (NOM) and reverse (REV) configuration for short-channel pMOS irradiated up to 400 Mrad(SiO_2) at different temperatures (no annealing). Higher temperatures result in larger V_{TH} shift and an evident asymmetry already during exposure.

(b) V_{TH} shift measured in nominal (NOM) and reverse (REV) configuration for short-channel pMOS transistors irradiated up to 400 Mrad(SiO_2) with different V_{GS} and V_{DS}. Only a $V_{GS} < 0$ V provokes a large V_{TH} shift, that becomes even larger and asymmetric if a $V_{DS} < 0$ V is applied.

Figure 5.6: Temperature and bias dependence of RISCEs in pMOS transistors in 65 nm CMOS technology.



(a) Radiation-induced charge trapped in the spacers. Its presence affecs the LDD extensions, increasing the series resistance.

(b) H^+ drift from the spacers in the thin gate oxide. This transport is strongly dependent on temperature and electric field.

(c) Hydrogen ions react at the interface causing the formation of interface traps.

Figure 5.7: Schematic representation of the spacer-related effects.

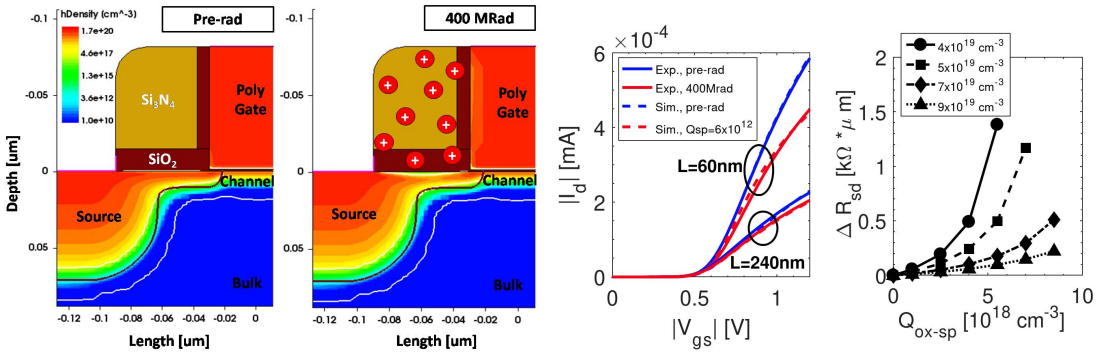
voltage shifting process, showing that low temperatures can significantly slow down its evolution.

The increase of series resistance induced by charge trapped in the spacers has been studied in [178] with TCAD simulations. Figure 5.8a shows the carriers' density in a cross section of a simulated pMOS transistor. The effect of irradiation has been emulated by placing positive charge in the spacers, as reported on the right side of the figure. The electric field generated by the trapped charge strongly reduces the hole-density in the LDD extension, increasing therefore the series resistance. The left side of Figure 5.8b depicts the measured vs simulated $I_D\,(V_G)$ characteristics for two pMOS transistors with two different channel lengths. To emulate the measured degradation, it has been introduced in the spacers a charge $Q_{sp} = 6 \times 10^{18}\text{cm}^{-3}$ (independently on the channel length) [178]. The right side of Figure 5.8b shows the simulated increase in series resistance for different doping levels in the LDD extensions, as charge density in spacers $Q_{\text{ox}-\text{sp}}$ varies [178]. Higher doping levels reduce the impact of trapped charge, a behaviour similar to what seen for the leakage current (see Figure 4.4).

The role and transport of hydrogen ions H^+ has been confirmed by the value of the activation energy extracted for the post-irradiation process. In particular, pMOS transistors have been exposed to 100 Mrad(SiO_2) at 25 °C and then annealed at 4 different temperatures, *i.e.*, 100, 80, 60 and 40 °C, measuring the I_{ON}^{sat} every 2 minutes.

Because the time needed to complete one of this test can be of several weeks and the X-ray machine at the CERN facility is continuously used, it was not possible to use the measurement setup described in Chapter 3.1. We developed therefore a system, similar to that described in [180], where 3 pMOS with identical dimensions, $W/L = 600\,\text{nm}/60\,\text{nm}$ have been bonded to a board connected to 3 Keithley 2000 digital multimeters to measure the drain current. The choice to use 3 transistors of the same size was made both for statistical purposes and because previous experiments had revealed a certain fragility of these transistors. We have therefore tried to make the system redundant, also considering the significant duration of these experiments, which would have made their repetition almost impossible if they had not been successfully completed. The 3 transistors share the same source terminal at the chip level, while, for reasons of system simplicity and robustness, the gate and drain terminals have been shorted within the board. With a single voltage generator it is therefore possible to polarize the three MOSFETs with $V_{GS} = V_{DS} = -1.2\,\text{V}$, the configuration that causes the greatest degradation in performance, and measure the current in saturation. This type of connection makes it impossible to carry out $I_D\,(V_G)$ measurements, and therefore to extract the threshold voltage, as the drain voltage also varies with the variation of the gate voltage[3]. However, from all the experiments carried out

[3]We have made measurements varying the voltage supplied by the generator and measuring the drain current, from which we have seen how, after annealing, the entire characteristic moves towards higher threshold voltage values (in absolute value). However, we decided not to report these measurements because they are not easy to interpret and do not provide information about the temporal evolution of the phenomenon, as it is not possible to carry them out with the same frequency at which the drain current was measured.



(a) TCAD simulation of the effects of the charge trapped in the spacers [178]. This TCAD simulation shows how the charge trapped in the spacers affcts the carrier concetration in the LDD extension, increasing the series resistance.

(b) Left: measured vs simulated $I_D\,(V_G)$ for ELT pMOS with different channel lengths. The TID effects have been simulated with a $Q_{sp} = 6 \times 10^{18}\text{cm}^{-3}$ in the spacers. Right: ΔR_{SD} vs $Q_{\text{ox-sp}}$ for different doping concentrations.

Figure 5.8: Results of TCAD simulations for the radiation-induced series resistance increase [178].

on short channel transistors in 65 nm, the only phenomenon of degradation of the drain current after irradiation is related to an increase in the absolute value of the threshold voltage. We can therefore use the I_{ON}^{sat} as an indicator of the evolution of the V_{TH}.

As depicted in Figure 5.2, the post-irradiation evolution reaches an almost stable point after the further degradation caused by the V_{TH}-shift. Taking this settling level as the final value of the process and using the approach proposed by Schwank and co-workers in [181], we estimated, as reported in Figure 5.9, an activation energy $E_A \simeq 0.92\,\text{eV}$, a value close to the one found for H^+ transport in SiO_2 films [110, 182, 183]. This value, together with the strong dependence of the process on the electric field, provides a strong indication of the importance of hydrogen ions in the radiation response.

The last step of the proposed model is the formation of interface traps in the gate oxide and in particular in the region close to the LDD extensions. $1/f$ noise measurements on irradiated and annealed devices confirmed the presence of interface traps in the gate oxide [172]. In fact, as previously said in this subsection, the transport of H^+ is strongly dependent on the V_{DS}, and, in pMOS, is inhibited on the drain side and promoted on the source side if $V_{DS} < 0$. In this case, the interface traps are formed only on one side of the channel, making the transistor asymmetric.

The effect of the applied electric field on the hydrogen ions is depicted in Figure 5.10. for a pMOS transistor. When the device is polarized in DIODE configuration (*i.e.*, $V_{GS} = V_{DS} = -1.2\,\text{V}$), the transport of positive charge is oriented from source to drain (top of the figure). If the charge trapped in the gate is not removed, the transistor become physically asymmetric. On the other hand, a $V_{DS} = 0\,\text{V}$ and a $V_{GS} = -1.2\,\text{V}$ (ON configuration) tends to promote the transport of H^+ in the gate oxide from both source and drain [178], leaving the device symmetric. Note that the situation is the opposite for the nMOS, with

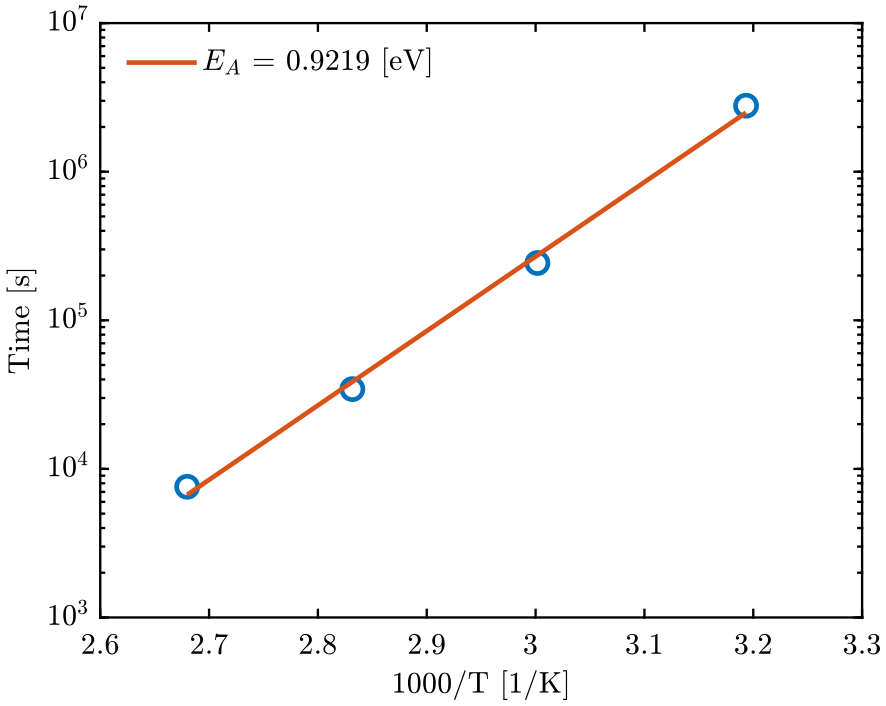


Figure 5.9: Arrhenius plot of the post-irradiation process in 65 nm technology for short channel MOS. The activation energy is comparable to that measured for H^+ transport in SiO_2 (after [172]).

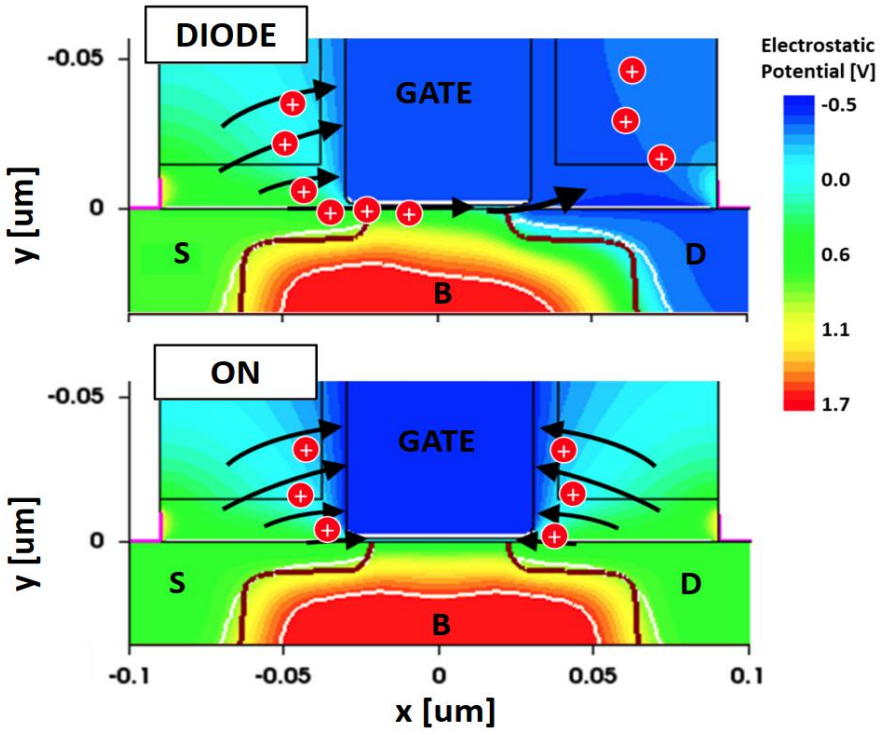


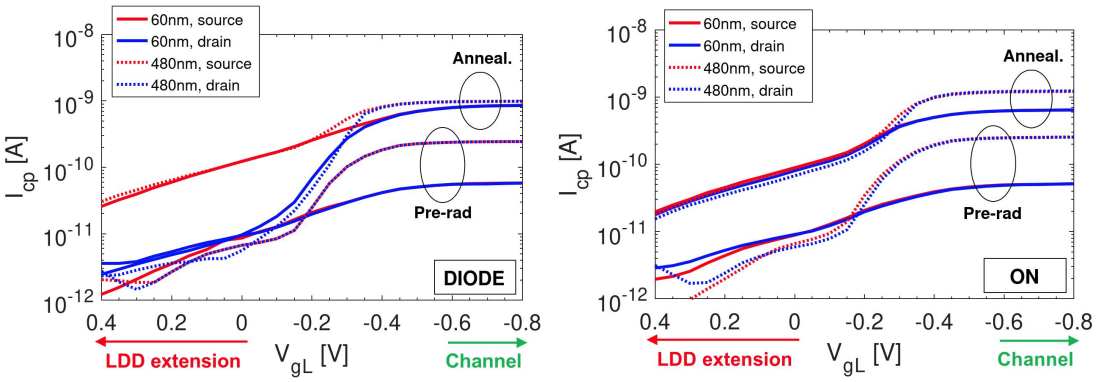
Figure 5.10: TCAD simulation of the electrostatic potential in the spacers for a pMOS transistor biased in two different configurations (DIODE and ON) [178].

the positive charge transported at the drain side in DIODE configuration (*i.e.*, $V_{GS} = V_{DS} = 1.2\,\mathrm{V}$ for the nMOS).

Charge pumping measurements provided further details on the location of the interface traps, confirming that they form near the LDD extensions and propagate to the centre of the channel at a distance dependent on the intensity of the electric field [172, 178]. Figure 5.11 shows the results of charge pumping measurements performed by Bonaldo and co-workers in [178] on enclosed pMOS transistors with a channel length of 60 and 480 nm. These pMOS transistors have been irradiated to 400 Mrad(SiO_2) at room temperature and annealed for 24 h at $T = 100\,^{\circ}\mathrm{C}$ with $V_{GS} = V_{DS} = -1.2\,\mathrm{V}$ (*i.e.*, DIODE configuration, Figure 5.11a) and $V_{GS} = -1.2\,\mathrm{V}$, $V_{DS} = 0\,\mathrm{V}$ (*i.e.*, ON configuration, Figure 5.11b). Thanks to the technique described in [184, 185], it was possible to study separately the impact of interface traps on the source side and on the drain side. In fact, the measured charge-pumping current I_{cp} is dependent on the number of interface traps and, by varying the V_{gL} voltage, it is possible to selectively take into account only the interface traps located in a specific portion of the channel. In particular, for $V_{\mathrm{gL}} \geq -0.18\,\mathrm{V}$ only the interface traps under the spacers and in the extension implants contribute to I_{cp} [178]. On the other hand, at lower V_{gL} also the interface in the channel contribute to the current. Since in this plots the I_{cp} current is not normalized to the gate size, longer transistors have a higher I_{cp} in the channel, as it can be clearly seen for $V_{\mathrm{gL}} <\sim -0.4\,\mathrm{V}$. Note that the large pre-irradiation difference between the I_{cp} currents of the two transistors significantly decreases after the annealing, meaning that in the short-channel device a larger built-in of interface traps occurred.

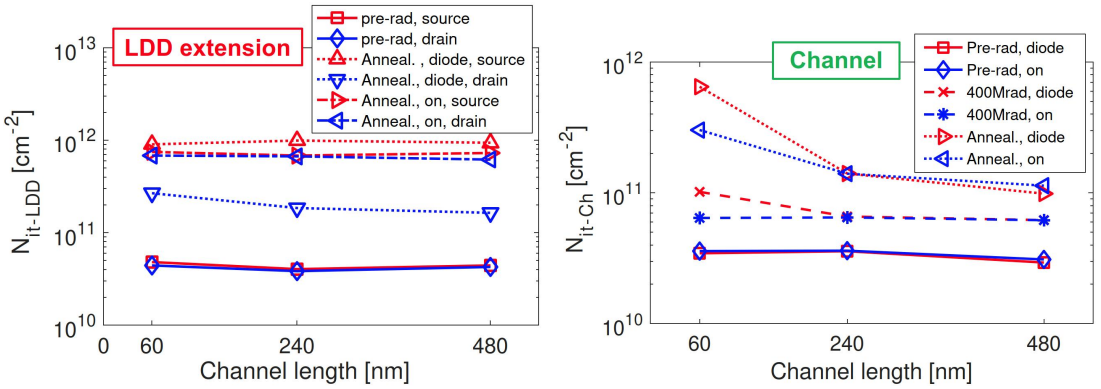
From this figures we can clearly see that the transistor become significantly asymmetric after annealing only in the DIODE configuration, proving once again the impact of the V_{DS} on the H^+ transport. In this case, as expected, the I_{cp} current increases more at the source side (in pMOSFETs). Note that the I_{cp} does not depend on the channel length under the LDD extensions, as the fabrication process of the LDD does not significantly change with the channel length. On the other hand, short channel transistors have both a larger increase in the current after annealing and a more evident asymmetry. When the transistors are polarized in ON configuration, the I_{cp} increases comparably in both source and drain side.

Thanks to the technique developed in [186], it is has been possible to estimate the interface trap density from the charge pumping measurements. Figure 5.12a shows the trap density under the LDD extensions ($N_{\mathrm{it-LDD}}$) for transistors with different channel length and different biases applied during irradiation and annealing [178]. As expected, the density is essentially independent on the gate length while is depended on the polarization, with the pMOS transistors biases in diode configuration showing a clear asymmetry after the high temperature annealing (dashed blue line vs dotted blue line). On the other hand, the interface traps density in the channel ($N_{\mathrm{it-Ch}}$, Figure 5.12b) starts to be more evident in short transistors after high temperature annealing, with the pMOS polarized in diode configuration showing the largest increase. As explained in [178], the slight channel length dependence visible, after annealing, in the $N_{\mathrm{it-Ch}}$ of pMOS polarized with ON configuration, could be an artefact of the charge pumping



(a) DIODE configutration: $V_{GS} = -1.2\,\mathrm{V}$, $V_{DS} = -1.2\,\mathrm{V}$ **(b)** ON configutration: $V_{GS} = -1.2\,\mathrm{V}$, $V_{DS} = 0\,\mathrm{V}$

Figure 5.11: Results of charge pumping measurements performed on enclosed pMOS transistor exposed to 400 Mrad(SiO_2) at room temperature and annealed at 100 °C [178].



(a) Interface traps density under the LDD for transistors of different channel lenghts, biased in different configuration and measured at the souce and drain side.

(b) Interface traps density in the channel for transistors of different channel lenghts and biased in different configuration.

Figure 5.12: Interface trap density under the spacers and in the channel. The transistors have exposed to a TID = 400 Mrad (SiO_2) and then annealed for 24 h at 100 °C.

measurements, related to a contribution from the interface traps in the LDD extensions, that leads to an overestimation of $N_{\mathrm{it-Ch}}$ for short channel devices.

Another way to understand the impact of interface traps is looking at the drain induced barrier lowering (DIBL) of irradiated transistors. DIBL is a short channel effect [187] appearing as a modulation of the threshold voltage by the applied V_{DS}. We define:

$$V_{DIBL} = -\frac{V_{TH}^{\mathrm{sat}} - V_{TH}^{\mathrm{lin}}}{V_{\mathrm{sat}} - V_{\mathrm{lin}}} \tag{5.1}$$

where $V_{\mathrm{sat}} = -1.2\,\mathrm{V}$ and $V_{\mathrm{lin}} = -20\,\mathrm{mV}$. Here V_{TH}^{sat} and V_{TH}^{lin} have been extracted selecting an arbitrary drain current level in the weak-inversion range on the transistor and taking the respective V_{GS} values. Figure 5.13 shows the DIBL of 3 ELT with different channel lengths and the same channel width, measured before irradiation, after a TID = 400 Mrad (SiO_2) and at the end of high temperature annealing.

As expected, the pre-irradiation value of the DIBL is much higher in shorter transistors and practically identical in nominal and reverse configuration. After 400 Mrad(SiO_2), V_{DIBL} slightly decreases, but the transistor is, as expected, still symmetric. However, at the end of high temperature annealing the short channel transistor becomes strongly asymmetric, with a large increase of V_{DIBL} in reverse configuration and a decrease in the nominal one. This behaviour can be understood looking at Figure 5.14, where the surface potential in weak inversion after irradiation (b) and at the end of annealing measured in nominal (c) and reverse (d) configuration is schematically reported. At the end of the irradiation the hydrogen ions are not yet drifted inside the gate oxide and therefore no interface traps have been formed. V_{DIBL} is similar to its pre-irradiation value, and is determined by the difference of the heights of the potential barrier in linear (solid lines) and saturation (dashed lines) region. As temperature increases the ions transport is accelerated and if a negative V_{DS} is applied, the H^+ions tend to move from the spacers to the gate oxide only from the source side, thus making the transistor asymmetric. The positive charge trapped at the interface causes an increase in threshold voltage, as described by the potential bump in (c). In nominal configuration this bump now defines the maximum height of the potential barrier (and therefore the V_{TH}), and it is only slightly influenced by the voltage applied at the drain. Therefore V_{DIBL} strongly decreases while threshold voltage increases in both linear and saturation region (see Figure 5.5). When the transistor is measured in reverse configuration, the bump at the "physical" source side (which in this case is the electrical drain) still dominates in linear region, but when a large negative voltage is applied to the physical source, the bump is lowered and the threshold voltage is determined by the height of the potential barrier on the physical drain side, which is significantly lower that the value in linear region. As a result, the threshold voltage in saturation is much lower than in linear region and therefore V_{DIBL} increases enormously.

Before moving on to see the behaviour of nMOS transistors and the radiation-response from other manufacturers and on other technology nodes, we try to

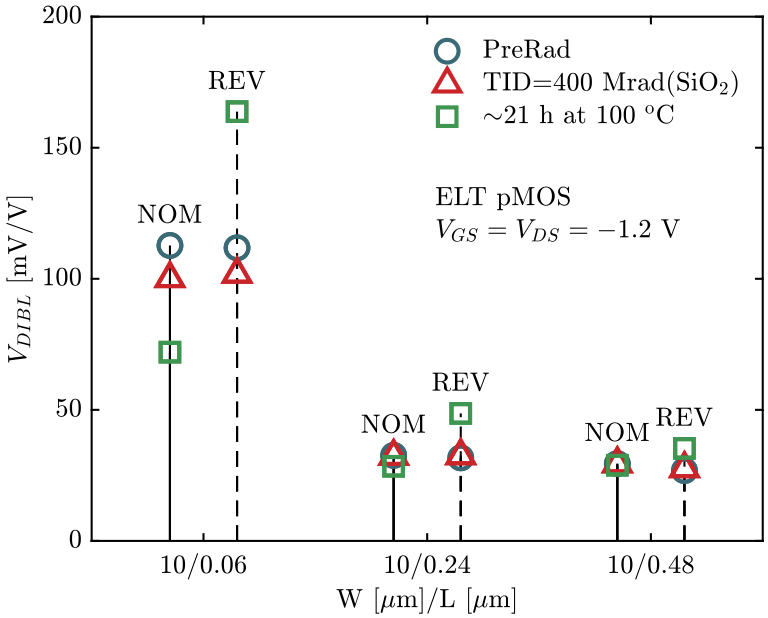


Figure 5.13: V_{DIBL} for ELT pMOSFETs with different channel lengths measured in nominal (NOM) and reverse (REV) configuration before exposure, after irradiation and at the end of 21 h of annealing at $T = 100\,°C$. The V_{DIBL} behaviour suggests that the interface traps are located at the source side.

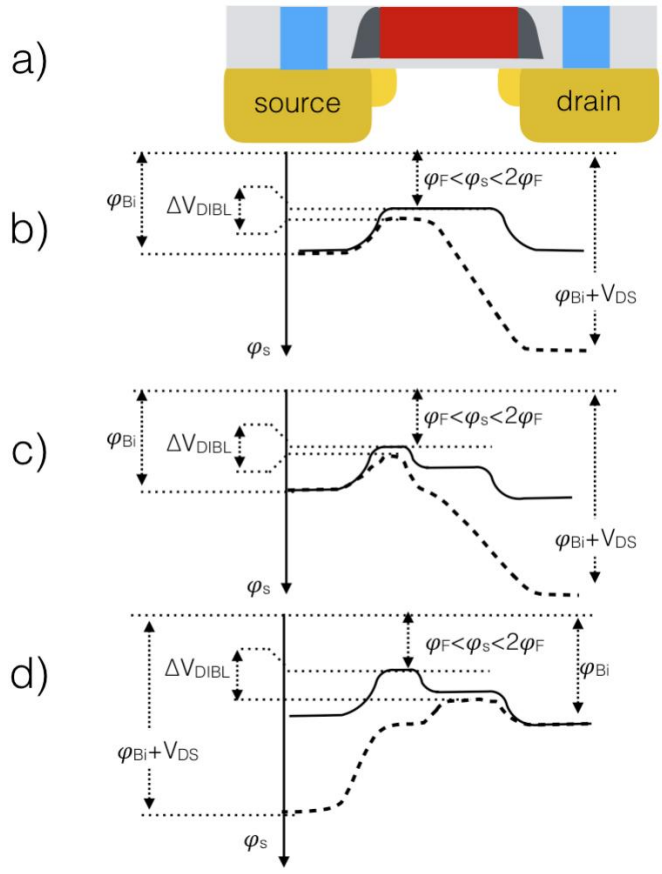


Figure 5.14: Schematic representation of the potential barrier in an irradiated transistor before and after high temperature annealing (after [172]).

estimate the impact of the spacer-related threshold voltage shift in the context of defining a qualification process for particle detectors.

The same data used for the extraction of the activation energy shown in Figure 5.9 have been used to estimate the time needed by this process to complete its evolution when the transistor is operating at different temperatures. This estimation is of fundamental importance, because chips in the particle detectors are usually kept at −20 °C, as described in Chapter 1.

The solid lines in Figure 5.15 show the normalized I_{ON}^{sat} measured at different temperatures after an irradiation up to 100 Mrad(SiO_2). The data at 100, 80, 60 and 40 °C have been used to extract the activation energy and to elaborate the model shown by the dashed lines, which very well matches the evolution of the I_{ON}^{sat} measured at 25 °C (not used to define the model). The initial increase in the drain current visible in the curves measured at 25 and 80 °C is most likely due to a recovery of the transconductance, similar to what reported in Figures 5.3 and 5.4a. However, the lack of $I_D\,(V_G)$ measurements does not allow to confirm this hypothesis with certainty.

Thanks to this model we can predict that the H^+ transport and the subsequent formation of interface traps will take more than 400 years to complete only half of the entire process at −20 °C. This result has a direct and very important implication on the qualification procedure for electronics operating in the particle detectors of the HL-LHC. In fact, standard qualification procedures for space application (see *i.e.*, [188]) include high temperature annealing after irradiation. In the case of chips exposed to ultra-high total doses, this phase of the qualification procedure can lead to a strong overestimation of the performance degradation, accelerating a process whose impact is completely negligible in the scale of operating times and working temperatures of particle detectors.

In this long discussion on radiation-induced spacers-related effects we have shown mainly results obtained on pMOS transistors. The main reason for this choice is that although the same phenomena seen for pMOS occur in nMOS, they are complicated by two factors:

- Interface- and oxide-trapped charge are different in sign
- The transport of H^+ and the consequent creation of interface traps appears to happen already at room temperature

The partial compensation between the effects produced by the interface- and oxide-trapped charge strongly reduces the radiation-induced increase in the series resistance, which is 10 times lower than that measured in pMOS, as reported in Figure 5.16a. As for pMOS transistors, lower temperatures lead to a smaller degradation and the radiation-induced increase in the series resistance is so small that a proper evaluation of the ΔR_{SD} becomes extremely difficult. Figure 5.16b shows the V_{TH}^{sat} (top) and the V_{DIBL} (bottom) for enclosed nMOS transistors measured at room temperature in four different bias configuration and exposed to a TID of 400 Mrad(SiO_2), then annealed fo 21 h at $T = 100$ °C. Contrary to what happens in pMOS, the transistor polarized at $V_{GS} = V_{DS} = 1.2$ V becomes asymmetrical already at the end of the irradiation. Note that the reverse configuration

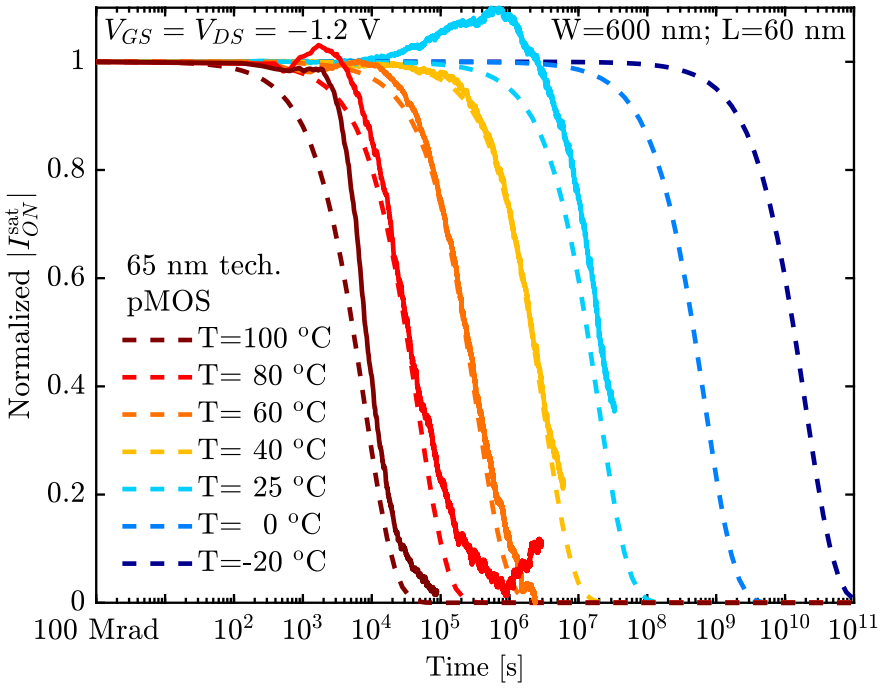
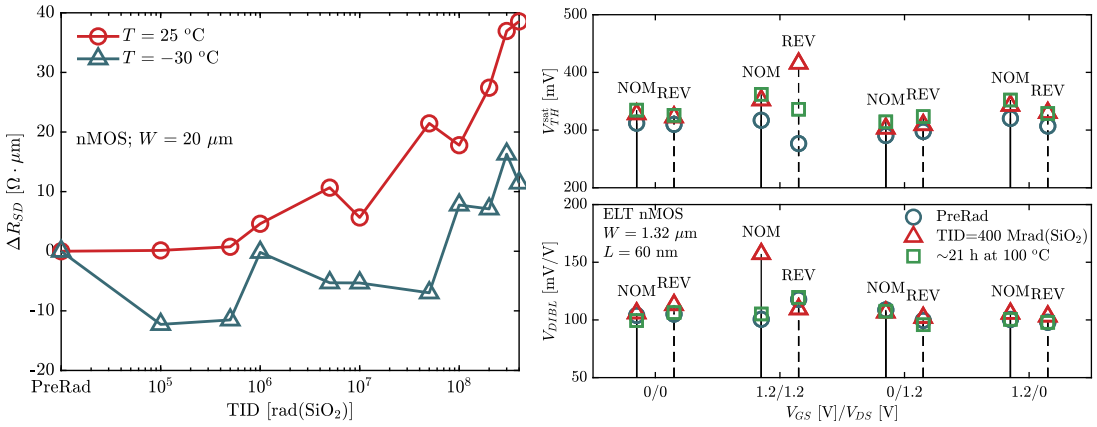


Figure 5.15: Prediction of the post-irradiation I_{ON}^{sat} evolution. At $T = -20\,°\text{C}$ it takes 400 years to complete only half of the entire process.



(a) Radiation-induced increase in the series resistance for nMOS transistors exposed to a TID $= 400\,\text{Mrad}\,(\text{SiO}_2)$ at 25 and $T = -30\,°\text{C}$. In nMOS transistors the radiation-induce series resistance increase is much smaller than in pMOS (repored in Figure 5.4b).

(b) V_{TH}^{lin} and V_{DIBL} for short-channel nMOS polarized with four different biases and measured in nominal (NOM) and reverse (REV) configuration before exposure, after irradiation and at the end of 21 hours of annealing at $T = 100\,°\text{C}$. nMOS transistors become asymmetric already during irradiation, with the NOM and REV configuration behaviour being the opposite of that measured in pMOS.

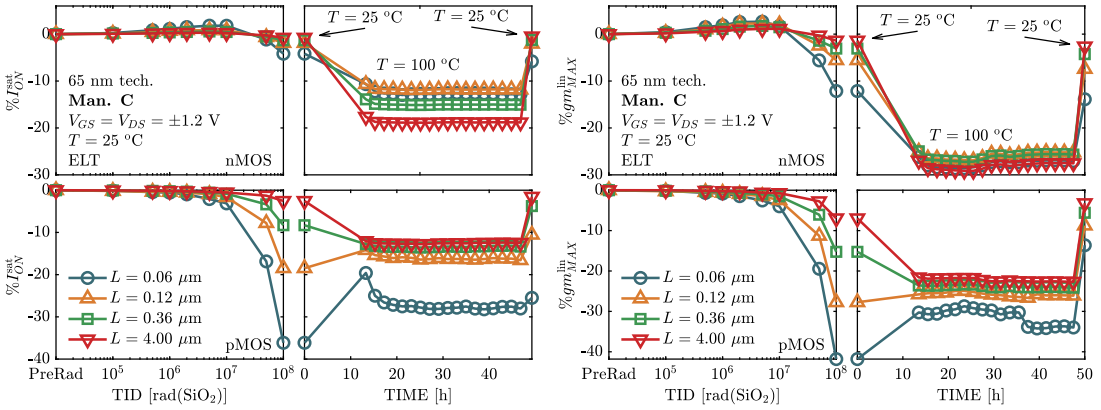
Figure 5.16: Radiation response for short channel nMOS transistors in 65 nm CMOS technology.

is the one that suffers the greatest variation of the threshold voltage, which is recovered at the end of the annealing. Also the DIBL has opposite trend compared to what seen in the pMOS, with the nominal configuration that, already at the end of the irradiation, shows an increase of V_{DIBL} bigger than the one measured in reverse configuration. The behaviour of the DIBL suggests that in nMOS the interface traps formed by the reaction of H^+ are located near the drain side. This is not surprising as the source-drain electric field in nMOS has opposite direction to that of pMOS, as also already mentioned in the discussion about Figure 5.10. From a practical point of view it is important to notice that, in general, short channel nMOS transistors are less affected by the spacer-related effects, both because the charges trapped in the oxide and at the interface are opposite in sign, and because the greatest degradation occurs in the reverse configuration that is very rarely used in actual chips.

The proposed model for the radiation-induced spacers-related effects has been extensively studied for the 65 nm CMOS technology used at CERN in the design of ASICs for particle detectors, produced by a manufacturer that we will henceforth identify as manufacturer "A". However, similar results have been obtained also in samples from other manufacturers. This was never reported before and it is a strong indication that spacers might represent a point of vulnerability for the radiation-hardness of the whole 65 nm CMOS technology node. In the following we therefore report the results obtained by irradiating samples from manufacturers B and C, indicating the similarities with what already saw for the devices from Man. A. We will start by studying producer Man. C, for whom we have more complete data.

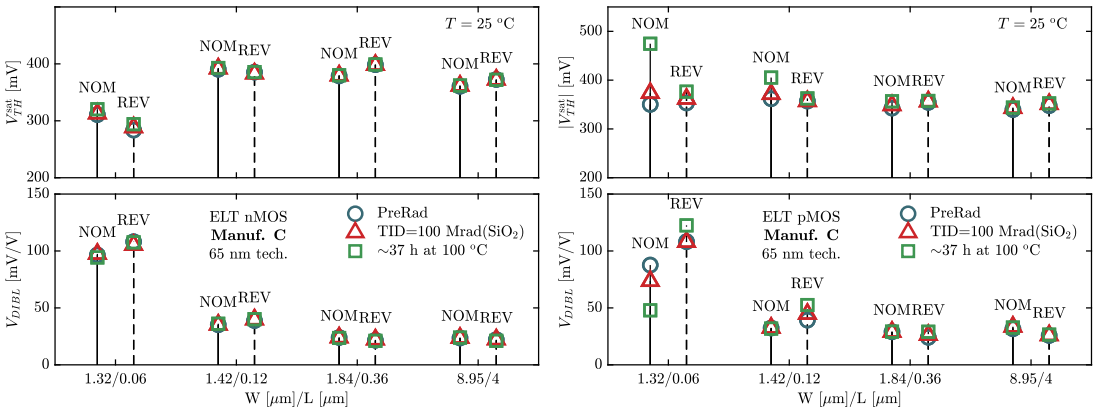
Figure 5.17 reports the results obtained for an array of enclosed transistors form the manufacturer "C" exposed to a TID = 100 Mrad (SiO_2) and the subsequent high temperature annealing ($T = 100\,°C$). Also in this case the I_{ON}^{sat} degradation is strongly dependent on the channel length and much more evident in pMOS transistors (Figure 5.17a), a clear evidence of RISCEs. During irradiation the drain current decreases mainly due to a reduction in the peak of the transconductance (Figure 5.17b) while pMOSFETs show a large threshold voltage shift after high temperature annealing due to charge trapped at the source side, as can be understood looking at the DIBL evolution reported in Figure 5.17d. On the other hand nMOS transistors have a small evolution at high temperature, as evidenced in Figure 5.17c. Therefore, despite the difference in the magnitude of the radiation-induced variation in the performance and the likely differences in the production process, the mechanisms causing the current degradation are the same as those identified in the transistors produced by Man. A.

A similar behaviour can also be found in devices from Man. B. Figure 5.18 reports the $I_D\,(V_G)$ characteristics in linear (Figure 5.18a) and saturation (Figure 5.18b) region for a pMOS transistor with $W/L = 1\,\mu m/60\,nm$ exposed to a TID = 100 Mrad (SiO_2) and then annealed for 145 h at $T = 100\,°C$. Also for this technology the asymmetry appears only after the high-temperature annealing while the degradation during exposure is caused by a decrease in the transconductance. Note also that the transconductance significantly recovers after the high temperature annealing, another similarity to what seen in the pMOS transistors



(a) I_{ON} percentage variation for ELTs with different channel lengths from Man. C.

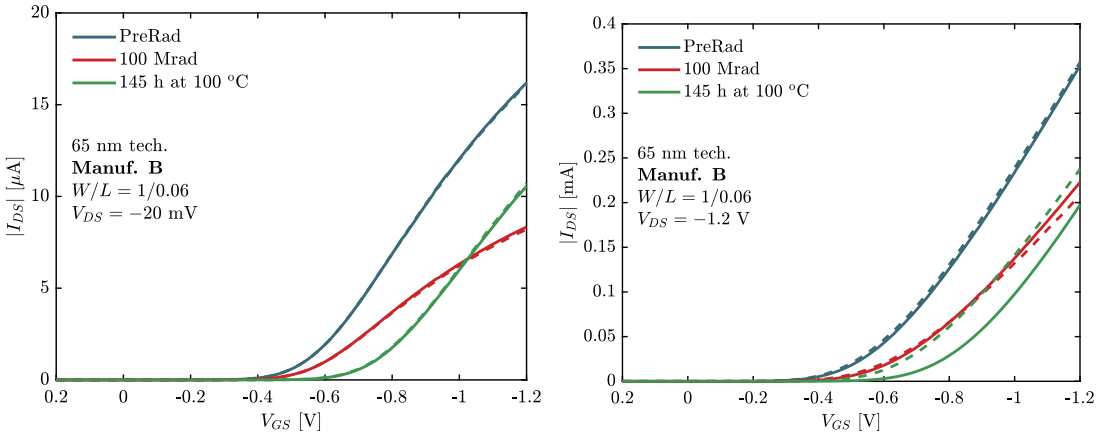
(b) gm_{MAX}^{lin} evolution for ELTs with different channel lengths from Man. C.



(c) V_{TH}^{lin} (top) and V_{DIBL} (bottom) for nMOS ELTs from manufacturer Man. C.

(d) V_{TH}^{lin} (top) and V_{DIBL} (bottom) for pMOS ELTs from manufacturer Man. C.

Figure 5.17: RISCE in 65 nm technology from Man. C.



(a) Linear region.

(b) Saturation region.

Figure 5.18: $I_D\,(V_G)$ in linear and saturation region for a short channel pMOS transistor from manufacturer Man. B measured in normal (solid lines) and reverse (dashed lines) configuration.

from the other manufactures.

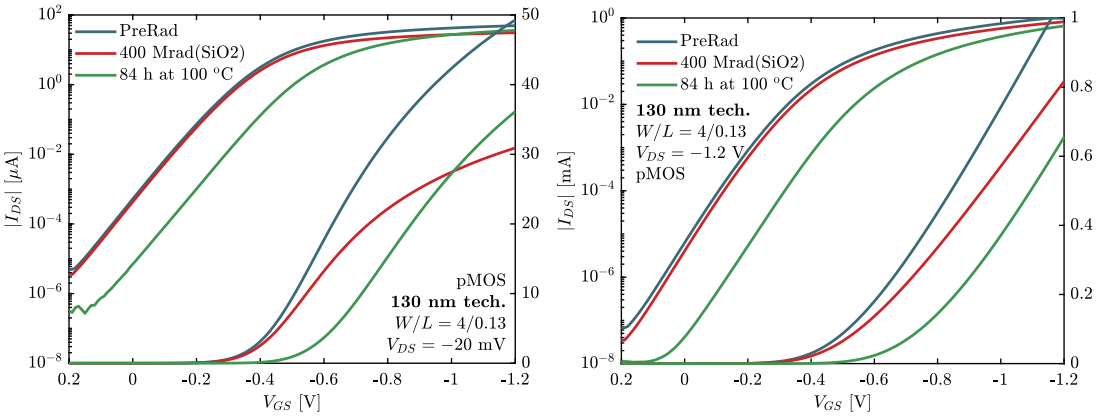
5.2 RISCE in Other CMOS Technologies

In this subsection we will briefly describe RISCEs in 130 nm and 28 nm CMOS technology, already introduced in Section 4.

Figure 5.19 shows the $I_D\,(V_G)$ characteristics of a short and wide channel pMOS transistor in 130 nm technology measured in linear (figure 5.19a) and saturation (Figure 5.19b) region before irradiation, after exposure to 400 Mrad(SiO_2) and at the end of post-irradiation evolution. Despite no reverse-configuration measurements are available, the degradation mechanisms are clearly the same as seen for 65 nm technology, with the evolution during irradiation dominated by the transconductance degradation and a large threshold shift as a result of an increase in temperature.

Although the proposed mechanism for describing the radiation-induced short channel effects can be applied to all the 65 nm and 130 nm technologies studied, this is no longer the case when moving to the 28 nm CMOS technology.

Figure 5.20 shows the evolution of the I_{ON} for transistors with different channel length and a $W = 3\,\mu m$ in 28 nm CMOS technology exposed to 1 Grad(SiO_2) and then annealed fo 4 h at $T = 100\,°C$. The radiation response of this technology has a completely different channel length dependence compared to 65 nm, with the longest transistors showing the greatest degradation in both n- and p-MOSFETs. In addition, this technology proves to be extremely robust to radiation with a current degradation of less than 10 % after a total dose of 1 Grad(SiO_2), with negligible variation even after high-temperature annealing. It can therefore be said that in this technology the presence of spacers is no longer of concern. Indeed, very similar results have also been obtained in a 28 nm CMOS technology from the same manufacturer but with a slightly different process [145, 164–167]. However, to generalize this result to the whole 28 nm technology node, samples from other manufacturers should be measured. This will be done in the near future, as a test chip designed using the 28 nm CMOS technology from another manufacturer will soon be available.



(a) Linear region. **(b)** Saturation region.

Figure 5.19: $I_D\,(V_G)$ in linear and saturation region for a short channel pMOS transistor in 130 nm CMOS technology.

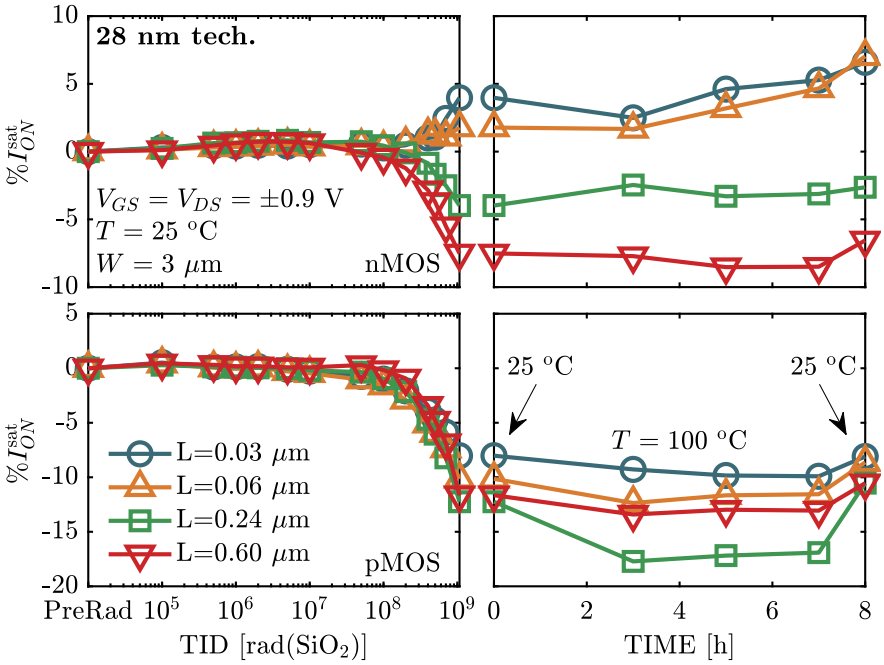


Figure 5.20: Percentage variation of the I_{ON} for nMOS (top row) and pMOS (bottom row) transistors in 28 nm CMOS technology with different channel length and a $W = 3\,\mu$m measured during irradiation up to 1 Grad(SiO_2) (left column) and for 4 h with $T = 100\,°C$. Note the that the first and the last point of the post-irradiation evolution have been measured $T = 25\,°C$.

Chapter 6

Dose-Rate Effects

CMOS technology is usually considered insensitive to true dose-rate effects, *i.e.*, differences in the radiation response of transistors exposed at the same TID but at different dose-rates and not caused by time-dependent effects [47, 188, 189]. However, Witczak and co-workers recently reported an enhanced dose-rate sensitivity of the TID-induced leakage current in nMOS transistors in 180, 250 and 350 nm CMOS technologies that could not be attributed to "normal" time-dependent charge trapping and annealing processes [190].

In this section we report some results about an unexpected true dose-rate sensitivity in the radiation response of the I_{ON}^{sat} measured in transistors in 65 and 130 nm and described in detail in [180]. All the experiments showed in this section on the 65 nm technology have been performed using a setup identical to that described in Subsection 5.1, constituted by 3 nMOS and 3 pMOS transistor with a $W/L = 600\,\text{nm}/60\,\text{nm}$. For the 130 nm technology, the study was made using 3 ring oscillators, called "standard lib", "clock buffer", and "high density", designed with different stages, different W/L ratio, and different nominal frequency, as reported in Table 6.1.

The dose-rate used in most of the tests performed with the X-ray machine at the CERN facility is around $10\,\text{Mrad}(SiO_2)/\text{h}$, 3 orders of magnitude higher than the one expected in the HL-LHC (see Chapter 1). To verify if this difference has an impact in the radiation response, we performed a series of experiments

Table 6.1: Characteristics of tested ring oscillators.

		standard lib	clock buffer	high density
W/L (nm/nm)	nMOS	430/130	450/130	130/130
	pMOS	635/130	1270/130	650/130
Nominal Frequency (MHz)		2.475	3.095	2.097
Nominal Average Current (µA)		165	109	70
Number of Stages +1 NAND for Reset		7168	7168	8000

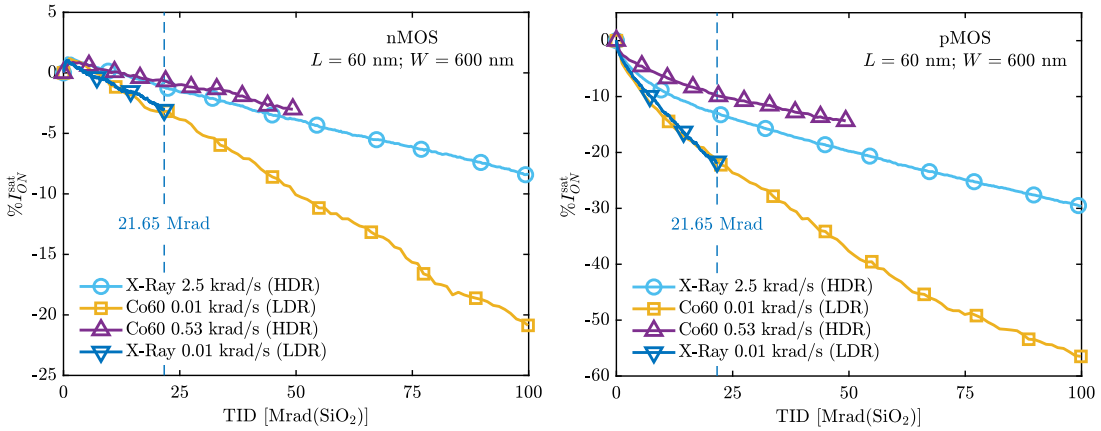
at much lower dose-rates than those normally used in the X-ray facility. Obviously, to perform tests at low-dose-rate the sample has to be exposed for a longer time in order to reach the same TID of a device irradiated at high-dose-rate. Because of the limited availability of the CERN facility, it was possible to reach only a TID of 21.6 Mrad(SiO_2) with a dose-rate of 0.01 krad(SiO_2)/s, equal to 0.036 Mrad(SiO_2)/h and similar to that expected in the HL-LHC (see Chapter 1). To have results at higher TID, we exposed the samples for 4 months at the CC60 CERN-EN ^{60}Co facility, reaching 100 Mrad(SiO_2) with a dose-rate of $\sim$0.01 krad(SiO_2)/s. Finally, we performed another HDR experiment at the ^{60}Co facility "Pagure" of the LABRA laboratory of CEA, Saclay, France, reaching a TID of 50 Mrad(SiO_2) with a dose-rate of 0.528 krad(SiO_2)/s, the maximum achievable. In Table 6.2 the dose-rates and the experiments performed at the different facilities are summarised.

Figures 6.1a and 6.1b report the results of these measurements in nMOS and pMOS transistors respectively. For both nMOS and pMOS, the degradation induced at low-dose-rate is significantly larger. Moreover, the damage at similar dose-rate is comparable between X-ray and ^{60}Co. Note also that, as seen in the previous sections, the degradation is larger in pMOS than in nMOS.

This results is a strong indication of a dose-rate dependence of the radiation response. However, the difference in the time scale of the experiments does not allow us to draw a definitive conclusion. To ensure that the increased current degradation is not due to time-dependent phenomena (*e.g.*bias-temperature instability, hot-carrier stress, and/or post-irradiation build-up of interface traps [47, 96, 172, 189, 191]), it is necessary to compare a low-dose-rate irradiated device with a high-dose-rate device exposed to the same TID and then kept at the same temperature and bias conditions for a time equal to that required to complete the low-dose-rate experiment. This comparison, for pMOS transistor, is shown in Figure 6.2, where the I_{ON}^{sat} degradation in the low-dose-rate experiment performed with the X-ray source is reported on the same time scale as for a sample exposed at high-dose-rate. At the end of the experiment the pMOS exposed at low-dose-rate show a larger degradation (by a factor of 2). Hence, the difference between the two sets of data cannot be explained by time-dependent effects. Despite a comparison on the same time scale would be needed, the results reported in Figure 6.3 strongly suggest that also the 130 nm CMOS technology

Table 6.2: Summary of the parameters for the different radiation tests.

Facility	Dose-rate krad(SiO_2)/s	TID Mrad(SiO_2)	Duration	Type
CERN X-ray	2.5	100	11.1 h	HDR
	0.528	100	53 h	HDR
	2	21.6	3 h	HDR
	0.01	21.6	25 days	LDR
Pagure ^{60}Co	0.528	50	24 h	HDR
CERN ^{60}Co	0.01	100	$\sim$ 120 days	LDR



(a) nMOS **(b)** pMOS

Figure 6.1: Comparison of the I_{ON}^{sat} percentage degradation of nMOS (Figure 6.1a) and pMOS (Figure 6.1b) transistors for exposure with X-ray and ^{60}Co sources at high- and low-dose-rate (after [180]).

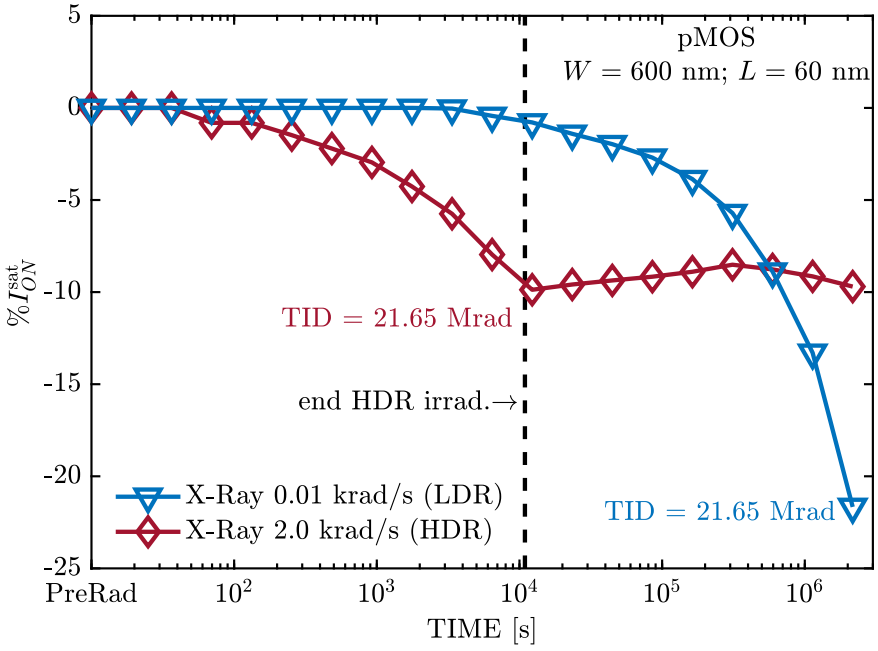


Figure 6.2: The I_{ON}^{sat} percentage degradation for pMOS transistors irradiated to 21.6 Mrad(SiO$_2$) at HDR and LDR shown on the same time scale. The post-irradiation time of the HDR sample is $\sim$ 200 time longer than its exposure time. If purely time-dependent effects introduced further significant degradation, this would be noticed in the second part of the HDR experiment, after irradiation. But none is seen (after [180]).

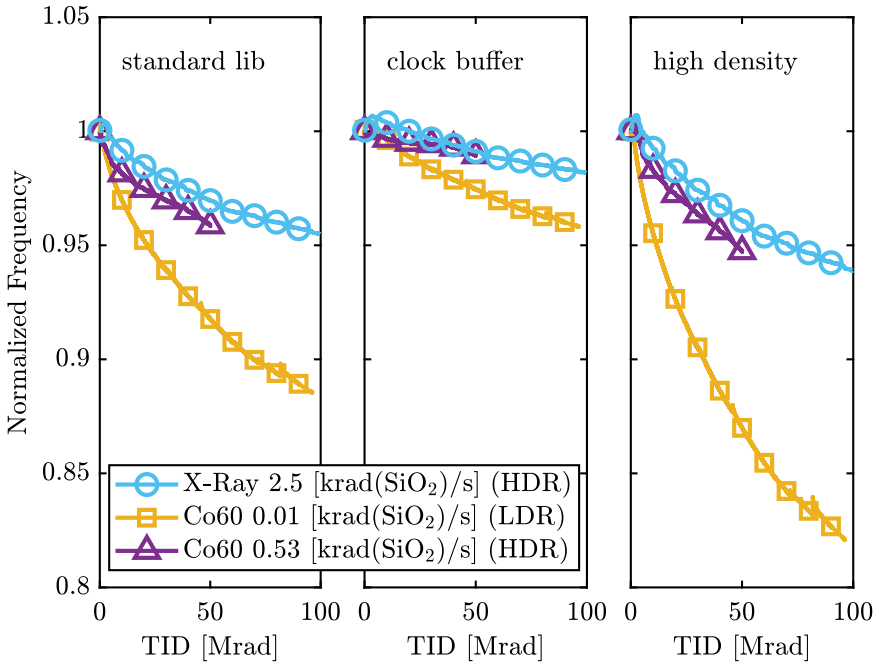


Figure 6.3: Radiation response of the normalized frequency of ring oscillators in the 130 nm technology during irradiation at HDR and LDR with X-ray and ^{60}Co. The difference in the total amount of degradation between the 3 oscillators can be explained by the difference in the channel width of both nMOS and pMOS transistors used for the inverters, as shown in Table 6.1 (after [180]).

is sensitive to dose-rate effects.

The dose-rate effect measured in CMOS transistors is of serious concern for the qualification of circuits designed for the particle detectors of the HL-LHC. The standard tests performed at the CERN X-ray facility at high rate could in fact underestimate by a factor of 2 the actual degradation in the hadron collider. Moreover, irradiations at high-dose-rate and high-temperature usually performed to simulate the ELDRS in the qualification of bipolar transistors [192, 193] are not suitable for verify the long-term reliability of ASICs designed for the inner part of the detectors in the LHC. High temperature will in fact accelerate the spacers-related effects, that, as described in Figure 5.15, are actually negligible in chips kept at −20 °C.

True dose-rate phenomena are not common in CMOS technologies but the enhanced low-dose-rate sensitivity (ELDRS) of bipolar transistors is a well known effect [47, 194–200]. It has been shown that the ELDRS is more evident in thick and defect-rich oxides irradiated at a low electric field [47, 194, 197]. This, of course, is not the case with gate oxides and explains why MOS transistors are insensitive to true dose-rate effects. However, as detailed throughout this chapter, the radiation response of modern CMOS technologies is driven by isolation oxides (STI and spacers), which are thicker and have a higher defect density than gate oxides and are generally subject to small electric fields. Therefore, all the radiation-induced effects caused by the presence of these oxides could be enhanced

when the samples are irradiated at low-dose-rate, but understand which oxide is more affected is almost impossible from the measurements we performed so far. In fact, the size of the measured transistors ($W/L = 600\,\text{nm}/60\,\text{nm}$) does not allow us to completely rule out the effects caused by the STI nor, obviously, those due to the spacers. Moreover, the lack of voltage-current measurements severely limits our possibilities to figure out the cause of this enhanced degradation.

For these reasons and for the strong impact that this effect can have on the qualification procedure, we plan to carry out a long and accurate campaign of measurements at different dose-rates, with transistors of various sizes and with a new setup capable of performing $I_D\,(V_G)$ measurements.

Chapter 7

Technology Comparison and Qualification Procedure

In this chapter we compare the general trend of the radiation-response of the studied CMOS technologies and we give some indication regarding the best practices to qualify an ASIC for the ultra-high radiation levels expected to be reached in the HL-LHC. We will also present the work carried out to include the radiation effects at ultra-high TIDin the PDK model of manufacturer A's 65 nm CMOS technology.

7.1 Technology Comparison

During this work we studied the radiation response of 4 different CMOS technology nodes (*i.e.*, 130, 65, 40 and 28 nm), showing that all of them are prone to radiation-induced performance degradation. Now we try to compare these technologies directly in order to guide the designers' choice in view of ASICs developments for particle detectors.

Figure 7.1 shows the I_{ON}^{sat} of nMOS and pMOS transistors in 65 nm CMOS technology from three manufacturers (*i.e.*, Man. A, Man. B and Man. C). Since the W/L is 240 nm/60 nm for all the measured samples, therefore quite close to the minimum available size of this technology ($W/L = 120\,\text{nm}/60\,\text{nm}$), the devices suffer from both RINCE and RISCE effects. To facilitate the comparison between the three manufacturers we report here (Figure 7.2) the radiation-induced drain-to-source leakage current that has been already shown in Figure 4.7. Moreover, Table 7.1 reports the I_{ON}^{sat} degradation for pMOS ELTs from Man. A and C with a $L = 4\,\mu\text{m}$ and an equivalent $W = 9.95\,\mu\text{m}$.

Looking at both Figure 7.1 and 7.2 it is apparent that the transistors from Man. B undergo the largest radiation-induced damage, making them unsuitable for high-energy physic applications. The small-size Man. C nMOS transistors of Figure 7.2 have the smallest I_{ON}^{sat} degradation at both 100 Mrad(SiO_2) and 1 Grad(SiO_2). However, they show the highest pre-irradiation leakage current and, although pMOS from all manufacturers exhibit severe degradation when exposed to 1 Grad(SiO_2), the device from Man. C present a relatively high degradation already at 100 Mrad(SiO_2). This trend is confirmed looking at Table 7.1,

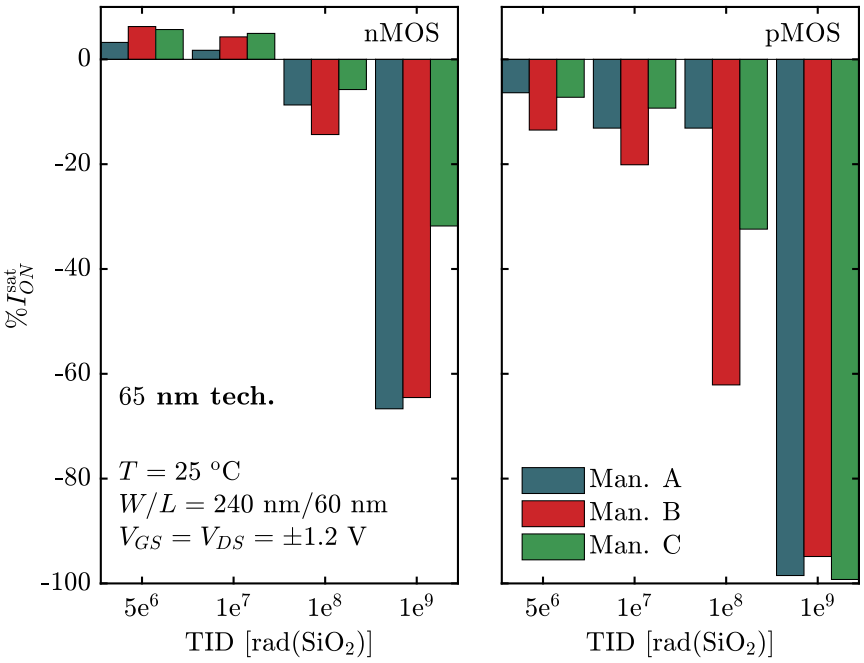


Figure 7.1: I_{ON}^{sat} variation for 65 nm technology nMOS (left) and pMOS (right) with $W/L = 240\,\text{nm}/60\,\text{nm}$ from 3 different manufactures. The symbol $xe^y = x \times 10^y$.

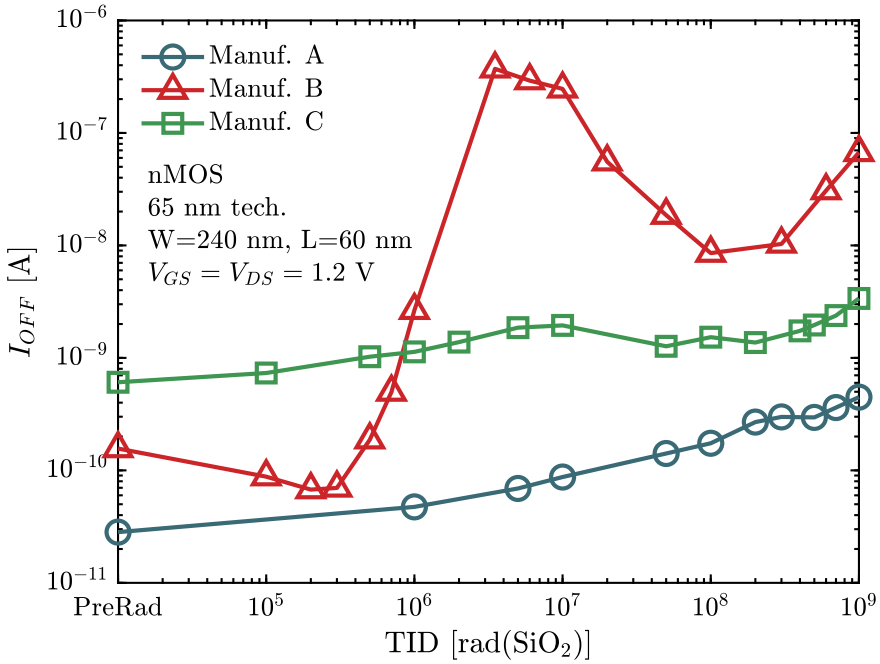


Figure 7.2: Leakage current vs TID for three different manufacturer in 65 nm CMOS technology exposed up to 1 Grad(SiO_2). The I_{OFF} variation is extremely process-dependent, showing in samples from some manufacturers a first peak around 5/10 Mrad(SiO_2) and a late increase after 100 Mrad(SiO_2).

Table 7.1: I_{ON}^{sat} degradation for enclosed layout pMOS transistors (ELT) with a $W/L = 9.95\,\mu\text{m}/4\,\mu\text{m}$. During irradiation: $T = 25\,^{\circ}\text{C}$ and $V_{GS} = V_{DS} = -1.2\,\text{V}$.

Man.	TID Mrad(SiO_2)			
	1	10	100	500
A	−0.09 %	−0.16 %	−1.32 %	−5.691 %
C	−0.08 %	−0.66 %	−2.46 %	−26.74 %

where, at TID = 500 Mrad (SiO_2), the pMOS form Man. C suffers a dramatic degradation. The transistors reported in the table are enclosed layout transistors with a $W/L = 9.95\,\mu\text{m}/4\,\mu\text{m}$, therefore RISCE is strongly reduced and RINCE is avoided by design. Hence, the large current reduction is most likely caused by a relatively soft gate oxide. This means that, unlike manufacturer A, it is not possible to significantly improve the reliability of Man. C's transistors by simply increasing their size. Moreover, samples from Man. A have the lowest leakage current both pre- and post-irradiation (Figure 7.2).

This comparison of various manufacturers of MOS transistors in 65 nm technology shows that Man. A's devices have, overall, the best radiation response.

It is also worth mentioning that the CMOS technology currently in use at CERN is mainly supplied by manufacturer A. It has been therefore decided to extend the process design kit (PDK) for the design tools to include the effects caused by ultra-high levels of irradiation (to 500 Mrad(SiO_2)). We have conducted a long campaign of specific measurements with the aim of modifying a BSIM4 model to describe the behaviour of irradiated transistors [201, 202]. This project was carried out in collaboration with the Technical University of Crete and, to the best of ou knowledge it is the first time a BSIM compact model has been extended to such high levels of radiation. The adopted strategy was to adjust a sets of the compact model, conserving the binning approach of the foundry PDK [201]. Since the dimensions of the available transistors do not coincide with those used by the foundry to define the various bins, it was necessary to adapt the size grid of the PDK model provided by the foundry with the available values of length and width, as indicated by the arrows in Figure 7.3. The model, initially developed only for devices irradiated at $T = 25\,^{\circ}\text{C}$, has then been extended to cover also the radiation response of 65 nm CMOS technology from Man. A exposed at 0 and $-30\,^{\circ}\text{C}$ [202].

From the data obtained from the same measurements performed to develop a compact model for radiation effects in standard transistors, in [203, 204] the TID-induced degradation on ELTs has been analytically described thanks to a simplified EKV model [165, 205], than can accurately predict the radiation-induced variation of the parameters that define the used model.

It is important to remark that the enhanced PDK is now available for CERN designers and it will soon be extended to low- and high-V_{TH} transistors. Moreover, the large amount of data gathered during this process has also proved extremely

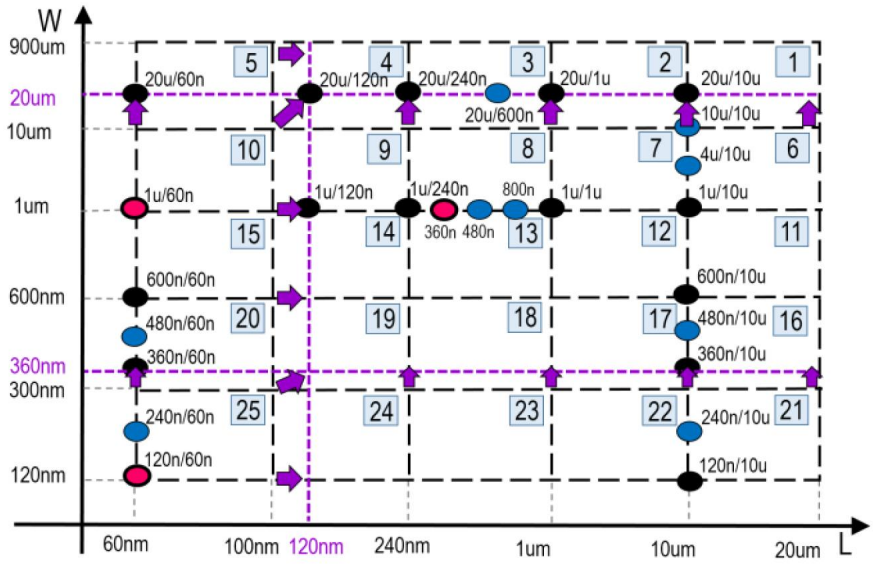


Figure 7.3: Measured devices in the size-grid of the PDK model. The black-dashed lines define the bins, here indicated with numbers from 1 to 25, while the oval markers identify the dimensions of the irradiated devices [201].

useful in improving our knowledge on the radiation response of the 65 nm CMOS technology from Man. A.

We will now compare different technologies from the same Man. A. However, it should be borne in mind that transistors from other manufacturers may have very different behaviours and, in principle, also be more radiation-hard. Figure 7.4 compares the radiation-induced I_{ON}^{sat} percentage variation for 4 different CMOS technology nodes, *i.e.*, 130, 65, 40, and 28 nm, form manufacturer A, measured at 1, 10, 100, 400 Mrad(SiO_2) and 1 Grad(SiO_2). All the transistor have the minimum allowed W/L, except for the pMOS in 65 nm technology, that has a $W = 240$ nm, *i.e.*, the double of the minimum width. Table 7.2 reports the dimensions for all the measured transistors. Note that 1 Grad(SiO_2) measurements are not available for the 130 and 40 nm technologies. Moreover, for the nMOS in 65 nm at 400 Mrad(SiO_2) and for the pMOS, again in 65 nm,at 1, 100 and 400 Mrad(SiO_2) the I_{ON}^{sat} was not actually measured at the reported TID, but has been calculated by linearly interpolating the current measured at the previous and next irradiation step. Although these are estimated values, the trend is clear.

As far as nMOS transistors are concerned, the 65 nm technology clearly shows the largest decrease in the I_{ON}^{sat} , with a maximum current variation of $-72.4\,\%$ at

Table 7.2: Transistor size for the experiment in Figure 7.4.

	Type	technology node			
		130 nm	65 nm	40 nm	28 nm
W nm/L nm	nMOS	150/130	120/60	120/40	100/30
	pMOS	150/130	240/60	120/40	100/30

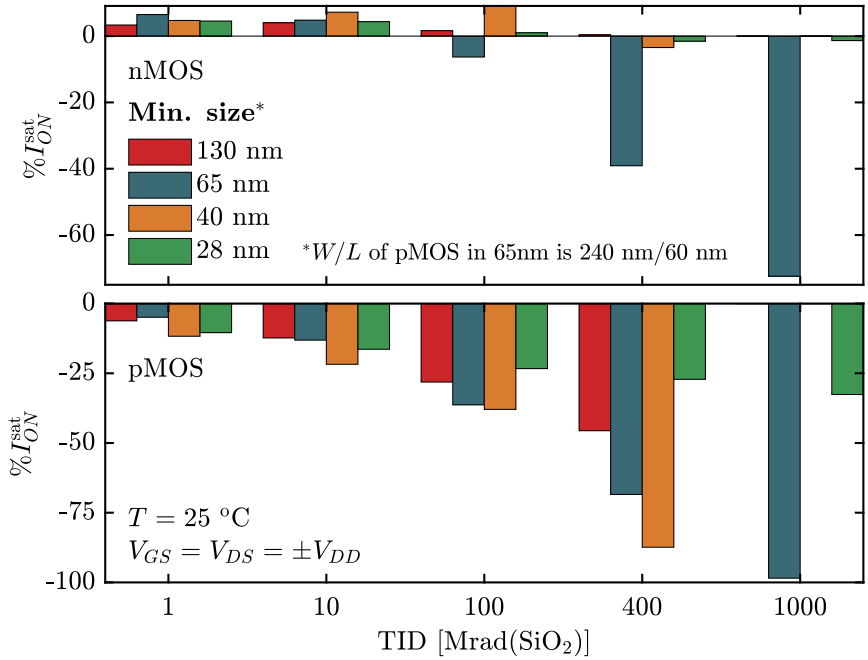


Figure 7.4: Percentage variation of the I_{ON}^{sat} for 4 different CMOS technologies measured at 1, 10, 100, 400 Mrad(SiO_2) and 1 Grad(SiO_2).

TID = 1 Grad (SiO_2). All other technologies remain within a range of $\sim \pm 10\,\%$ up to ultra-high doses. The 65 nm technology presents a significant reduction in its performance also for pMOSFETs, where, however, the worst case is represented by the 40 nm technology.

Despite the 130 nm technology has an overall better radiation response[1] than the 65 nm, is also currently used in the design of particle detectors due to its better performance in terms of speed and high density, which are attractive features for pixel detectors [130, 206, 207]. From this point of view, it is clear that the 28 nm CMOS technology represents a very interesting candidate for the next generation of ASICs, since it combines high performance and an excellent radiation-response.

The main drawback in using this technology is represented by the radiation-induced drain-to-source leakage current, already discussed in Section 4.1. Figure 7.5 shows a comparison of the radiation response of the I_{OFF} for the CMOS technologies studied so far. For the 28 nm technology we report both the results obtained form samples in the process studied in this thesis (solid line) and those obtained by Zhang and co-workers in [164] (dashed line). It is important to note that these technologies, in addition to coming from different manufacturers, can also have a different "flavour". In fact, while some are designed to consume little power and therefore have a low leakage (pre-rad), others are developed to achieve a low threshold voltage, and consequently a higher leakage. The sense of this comparison is therefore to evaluate how much the I_{OFF} varies as the dose increases, rather than comparing the absolute value of the leakage current.

[1]This is true only if the process that lead to the large radiation-induced leakage current increase is avoided (see Figure 4.1).

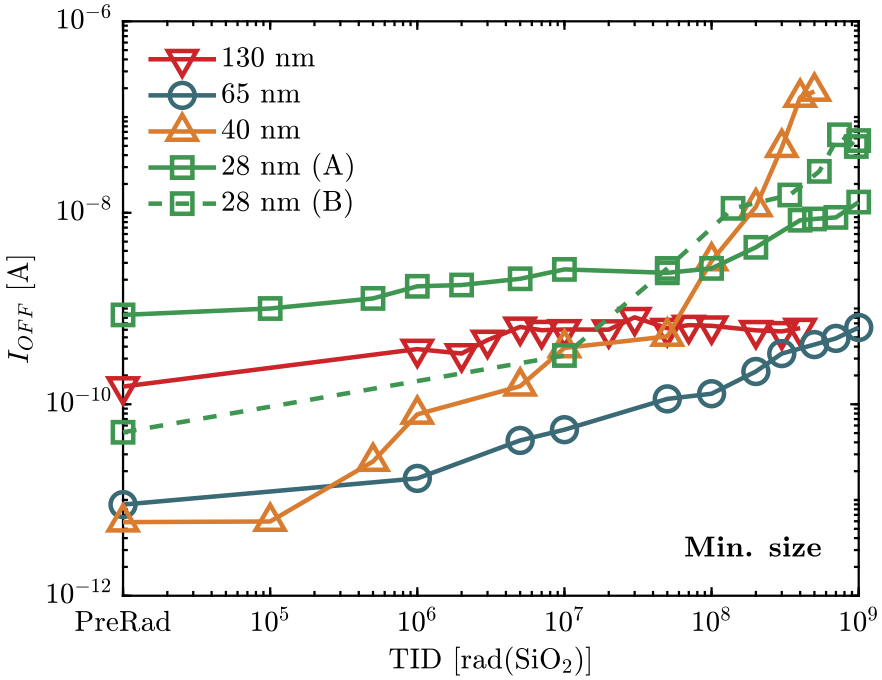


Figure 7.5: TID-induced I_{OFF} variation for 4 different CMOS technology nodes. The size of the transistors are reported in Table 7.2. The dashed line depicts the results obtained by Zhang and co-workers in [164].

Despite the 65 and 40 nm technologies present a similar pre-rad I_{OFF} value ($\sim$ 10 pA), the leakage current in the 40 nm technology overcomes that in the 65 already at 1 Mrad(SiO$_2$), reaching at TID = 500 Mrad (SiO$_2$) an $I_{OFF} =\sim$ 200 nA. At the same total dose, the I_{OFF} in the 65 nm technology is $\sim$ 400 pA. This large radiation-induced leakage current increase, together with the severe I_{ON}^{sat} degradation suffered by pMOS transistors (Figure 7.4), makes it impractical the use of the 40 nm technology from Man. A in particle detectors.

The two processes in 28 nm CMOS technology show a relatively large leakage current already before irradiation. In particular, the process studied in this thesis (process A) has a pre-rad leakage current of $\sim$ 900 pA while the one measured by Zhang and co-workers, which from now on we will identify as "B", has an $I_{OFF} \sim$ 51 pA. However, the situation changes after exposure. At 1 Grad(SiO$_2$), the transistor from process A shows an $I_{OFF} \sim$ 13 nA while the leakage current in process B is $\sim$ 57 nA. The radiation-induced I_{OFF} variation is therefore more evident in process B, while the leakage current in process A does not excessively increase even at ultra-high doses.

The 28 nm CMOS technology is therefore an excellent candidate to replace the 65 nm technology in the design of the next generation of ASICs for the particle detectors in the HL-LHC.

7.2 Qualification Procedure for Ultra-High TID

The complex phenomena induced by the exposure to ultra-high doses make the definition of a qualification procedure for the ASICs intended to be used in

the particle detectors a rather challenging task. In fact, the standard qualification procedures for space application could not be suitable for circuits designed for the HL-HLC. The main problems arise from the post-irradiation high-temperature annealing usually performed in the typical qualification test performed for space applications (see *e.g.* [208]). This step is needed to take into account the build-up of interface traps [123]. However, we have seen in Section 5.1 that few hours at high temperature are sufficient to provoke a large threshold voltage shift in pMOS transistors and a consequent decrease in the drain current (see Figures 5.3 and 5.2). This can lead to a substantial overestimate of the impact of the TID in the real application, since the time-scale of this effect at $-20\,^{\circ}\mathrm{C}$ is in the order of hundreds of years, as depicted in Figure 5.15. Therefore, the irradiation should be performed at the same temperature expected in the application and, for the chip that will be kept at low temperature, *no further high-T annealing is needed*. Clearly, this is true only if the circuit is never allowed to reach high temperatures under bias in the real application. In fact, this late V_{TH} shift is strongly bias-dependent (see Figure 5.6b), showing a larger variation when both a V_{GS} and a V_{DS} voltages are applied.

Since also all the other radiation-induced phenomena depend on the applied voltage, *during irradiation tests the circuits must be biased*.

It is also extremely important to measure the evolution of the chip during all the exposure and not just at the end of the irradiation. In fact, both RINCE and radiation-induced leakage current can have the larger impact in the range between $0.1\,\mathrm{Mrad}(SiO_2)$ and $10\,\mathrm{Mrad}(SiO_2)$ (see Figure 4.11 and 4.1).

To summarize:

- The temperature should be close to the real operating temperature
- During irradiation tests the circuits must be biased
- No further annealing is needed (if in the application the circuit is never allowed to reach high temperatures under bias)
- The chip has to be monitored during the entire exposure

So far, we did not discuss the impact of the dose-rate effects on the qualification procedure. This could be of serious concern, since we measured a larger degradation (a factor of ~ 2) in MOS devices exposed at a dose-rate closer to the real application than in those irradiated at much higher dose-rate in the X-ray CERN facility (Chapter 6). However, additional studies are needed to asses the impact of this effect in the real application. Furthermore, it is worth to stress how the irradiation at high-temperature performed to estimate the ELDRS effect in bipolar transistors is obviously not applicable to the nanoscale CMOS technologies studied in this thesis, as the temperature considerably increases the threshold voltage shift in pMOS already during irradiation (see Figure 5.6a).

Chapter 8

Conclusions

In this thesis we studied the radiation response of nanoscale CMOS technologies exposed to ultra-high levels of ionizing dose, comparable to those that particle detectors at the CERN HL-LHC will have to withstand. The very large amount of data gathered from the study of 4 different CMOS technology nodes, *i.e.*, 130, 65, 40 and 28 nm, provided an unique and complete description of the radiation response of modern MOS transistors and a better understanding of the physical mechanisms underling the TID-induced phenomena. In all technologies, we have investigated the dependence on polarization, temperature and size, showing how the radiation response is clearly dominated by the presence of the STI and the spacers oxide.

For what concerns the effects related to the STI, we pointed out that, despite both RINCE and radiation-induced drain-to-source leakage current are certainly caused by charge trapped in the trench oxides, their dependences on bias, time and temperature are different. We suggested that the reason for this difference may lie in a different location of the charges causing the two effects. In particular, RINCEs are mainly provoked by charge trapped at the trench corner while the I_{OFF} increase is likely due to positive charge trapped relatively far from the STI/gate oxide edge. We also introduced and investigated the Ultra-high-dose Drain Current Increase (UDCI) effect, a phenomenon that we measured in all the examined technologies.

The in-depth study carried out in recent years and summarised in this thesis has clearly shown that the spacers are determinant for the radiation-induced short channel effects (RISCE). The proposed degradation mechanism, which involves the transport of hydrogen ions, has been demonstrated by both charge pumping and noise measurements and further confirmed by TCAD simulations. One of the most significant results reported in this thesis is the estimation of the time needed for the transport of H^+ from the spacers to the gate to cause a significant variation in the threshold voltage. At $T \sim -20\,^{\circ}\mathrm{C}$ the spacer-induced V_{TH} shift will take hundreds of years to become relevant. This has strong consequences in the definition of the qualification procedure, suggesting the the typical post-irradiation high-temperature annealing could significantly overestimate the degradation in the real application.

Another important result is the discovery of an unexpected real dose-rate

sensitivity of nanoscale CMOS technologies. In particular, experiments performed at a lower DR than that typically used in the X-ray irradiation facility showed a larger degradation. This is of serious concern and more investigations are planned in the near future.

We also directly compared the radiation response of four different CMOS technology nodes, showing how the characteristics of the 28 nm technology studied here are certainly attractive for the design of the future generations of particle detectors.

What does the future hold for the study of radiation effects in CMOS technologies exposed to ultra-high doses? Two fundamental elements will guide the research in the coming years: the continuous scaling of CMOS technology and the ambition to overcome the current limits of HL-LHC.

The radiation response of new geometries and materials is already under study [209–215] but at much lower total doses than the electronics for high energy physics applications have to withstand. In addition, the desire to further improve our understanding of fundamental particle physics leads to the design and development of colliders with performances, in terms of energy and intensity, even higher than those planned the HL-HLC.

One of these projects is the Future Circolar Collider (FCC), a particle accelerator with a circumference of ~ 100 km, capable of reaching collision energies up to 100 TeV (see *e.g.* [216, 217]). This extremely high energy combined with an expected luminosity of 5×10^{34} cm^{-2}s^{-2} ($\sim$HL-LHC), will lead to a peak of TID of 500 Grad(SiO_2) [218], 500 times higher than the maximum level reached in the HL-LHC. Figure 8.1 shows the same comparison of radiation environments as seen

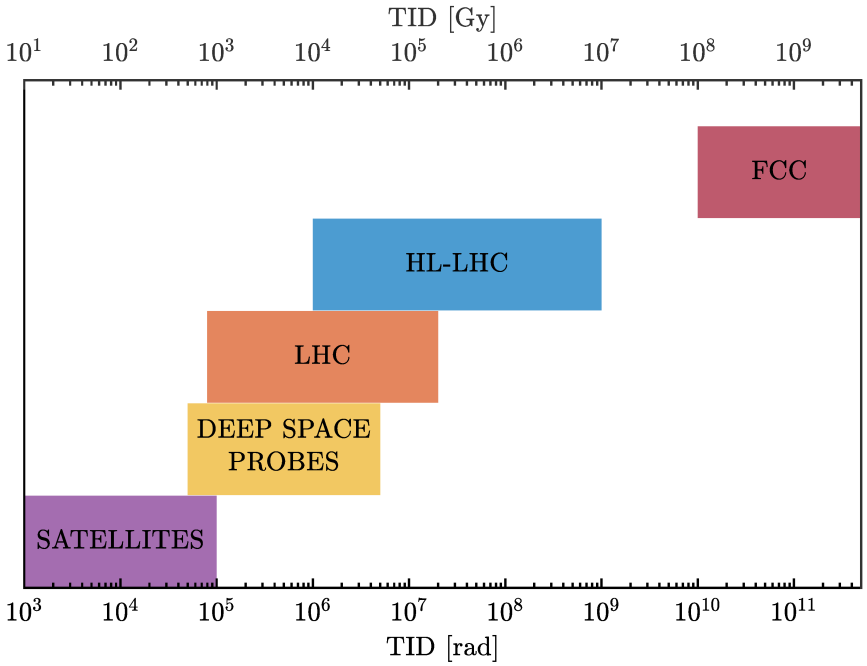


Figure 8.1: Comparison of TID levels in different radiation environments. The FCC is expected to reach unprecedented TID levels, 500 times higher than those expect in the HL-LHC.

in the introduction, to which we have added the doses predicted for FCC [219].

The results presented in this thesis clearly demonstrate that none of the CMOS technologies studied can survive such high radiation levels, including the 28 nm process, which is the last planar CMOS technology produced before moving to FinFETs. This new geometry has proven to be a successful solution in order to continue to follow Moore's law but is certainly not immune to radiation-induced performance degradation. Among the other effects, it can be prone to a substantial increase in drain-to-source leakage current due to positive charge trapped in the STI [215, 220]. A possible evolution in the geometry scaling of MOS devices are the Gate-All-Around (GAA) transistors [221]. Although they seem promising form the radiation-hardness point of view, since no thick oxides are facing the channel [215], their actual robustness to ultra-high TID has to be verified on prototypes and later confirmed in production-grade samples.

Moreover, even the radiation-tests themselves are complicated by the huge TID expected to be reached in application like FCC. In fact, with the dose-rate currently provided by the X-ray irradiation facility at CERN it will take ~ 5 years just to perform a single irradiation to 500 Grad(SiO_2). This is clearly another issue that has to be solved in order to develop a qualification procedure capable of reasonably predicting the evolution of devices exposed at these extremely high TID levels.

Bibliography

[1] D. Binder, E. C. Smith, and A. B. Holman. "Satellite Anomalies from Galactic Cosmic Rays". In: *IEEE Transactions on Nuclear Science* 22.6 (Dec. 1975), pp. 2675–2680.

[2] T. C. May and M. H. Woods. "A New Physical Mechanism for Soft Errors in Dynamic Memories". In: *16th International Reliability Physics Symposium*. Apr. 1978, pp. 33–40.

[3] T. C. May and M. H. Woods. "Alpha-particle-induced soft errors in dynamic memories". In: *IEEE Transactions on Electron Devices* 26.1 (Jan. 1979), pp. 2–9.

[4] K. Bedingfield, R. Leach, and M. Alexander. "Spacecraft System Failures and Anomalies Attributed to the Natural Space Environment". In: (1996).

[5] W. B. Thomas. *Orbital anomalies in Goddard spacecraft for calendar year 1994*. Tech. rep. NASA Goddard Space Flight Center, Office of Flight Assurance., Greenbelt, MD United States, July 1996.

[6] D. M. Fleetwood, P. S. Winokur, and P. E. Dodd. "An overview of radiation effects on electronics in the space telecommunications environment". In: *Microelectronics Reliability* 40.1 (2000), pp. 17–26.

[7] D. M. Harland and R. Lorenz. *Space systems failures: disasters and rescues of satellites, rocket and space probes*. Springer Science & Business Media, 2007.

[8] W. N. Hess. "The artificial radiation belt made on July 9, 1962". In: *Journal of Geophysical Research* 68.3 (1963), pp. 667–683.

[9] W. L. Brown, J. D. Gabbe, and W. Rosenzweig. "Results of the Telstar Radiation Experiments". In: *Telstar I*. Vol. 32. NASA Special Publication. 1963, p. 1505.

[10] J. S. Mayo, H. Mann, F. J. Witt, D. S. Peck, H. K. Gummel, and W. L. Brown. "The command system malfunction of the Telstar satellite". In: *The Bell System Technical Journal* 42.4 (July 1963), pp. 1631–1657.

[11] C. Farand. "Radiation levels in one Fukushima reactor high enough to kill a human in two minutes". In: *Independent* (Feb. 18, 2017). URL: `https://www.independent.co.uk/news/world/asia/radiation-fukushima-nuclear-plant-high-enough-kill-human-two-minutes-a7587646.html#comments` (visited on 10/23/2018).

[12] M. Fackler. "Six Years After Fukushima, Robots Finally Find Reactors' Melted Uranium Fuel". In: *The New York Times* (Nov. 19, 2017). URL: https://www.nytimes.com/2017/11/19/science/japan-fukushima-nuclear-meltdown-fuel.html (visited on 10/23/2018).

[13] V. Beiser. "The Robot Assault On Fukushima". In: *Wired* (Apr. 26, 2018). URL: https://www.wired.com/story/fukushima-robot-cleanup/ (visited on 10/23/2018).

[14] J. R. Srour and J. M. McGarrity. "Radiation effects on microelectronics in space". In: *Proceedings of the IEEE* 76.11 (Nov. 1988), pp. 1443–1469.

[15] C. Leroy and P.-G. Rancoita. *Principles of radiation interaction in matter and detection*. 2nd ed. World Scientific Publishing Company, 2009.

[16] E. A. Burke. "Energy Dependence of Proton-Induced Displacement Damage in Silicon". In: *IEEE Transactions on Nuclear Science* 33.6 (Dec. 1986), pp. 1276–1281.

[17] G. P. Summers, E. A. Burke, C. J. Dale, E. A. Wolicki, P. W. Marshall, and M. A. Gehlhausen. "Correlation of Particle-Induced Displacement Damage in Silicon". In: *IEEE Transactions on Nuclear Science* 34.6 (Dec. 1987), pp. 1133–1139.

[18] V. A. V. Lint. "The physics of radiation damage in particle detectors". In: *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment* 253.3 (1987), pp. 453–459.

[19] C. J. Dale, P. W. Marshall, E. A. Burke, G. P. Summers, and E. A. Wolicki. "High energy electron induced displacement damage in silicon". In: *IEEE Transactions on Nuclear Science* 35.6 (Dec. 1988), pp. 1208–1214.

[20] M. Huhtinen and P. Aarnio. "Pion induced displacement damage in silicon devices". In: *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment* 335.3 (1993), pp. 580–582.

[21] G. P. Summers, E. A. Burke, P. Shapiro, S. R. Messenger, and R. J. Walters. "Damage correlations in semiconductors exposed to gamma, electron and proton radiations". In: *IEEE Transactions on Nuclear Science* 40.6 (Dec. 1993), pp. 1372–1379.

[22] I. Lazanu, S. Lazanu, U. Biggeri, E. Borchi, and M. Bruzzi. "Non-ionising energy loss of pions in thin silicon samples". In: *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment* 388.3 (1997). Radiation Effects on Semiconductor Materials, Detectors and Devices, pp. 370–374.

[23] G. P. Summers, S. R. Messenger, E. A. Burke, M. A. Xapsos, and R. J. Walters. "Low energy proton-induced displacement damage in shielded GaAs solar cells in space". In: *Applied Physics Letters* 71.6 (1997), pp. 832–834.

[24] I. Jun. "Effects of secondary particles on the total dose and the displacement damage in space proton environments". In: *IEEE Transactions on Nuclear Science* 48.1 (Feb. 2001), pp. 162–175.

[25] J. R. Srour, C. J. Marshall, and P. W. Marshall. "Review of displacement damage effects in silicon devices". In: *IEEE Transactions on Nuclear Science* 50.3 (June 2003), pp. 653–670.

[26] J. R. Srour and J. W. Palko. "A Framework for Understanding Displacement Damage Mechanisms in Irradiated Silicon Devices". In: *IEEE Transactions on Nuclear Science* 53.6 (Dec. 2006), pp. 3610–3620.

[27] J. R. Srour and J. W. Palko. "Displacement Damage Effects in Irradiated Semiconductor Devices". In: *IEEE Transactions on Nuclear Science* 60.3 (June 2013), pp. 1740–1766.

[28] G. Lindström, M. Moll, and E. Fretwurst. "Radiation hardness of silicon detectors – a challenge from high-energy physics". In: *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment* 426.1 (1999), pp. 1–15.

[29] F. A. Junga and G. M. Enslow. "Radiation Effects in Silicon Solar Cells". In: *IRE Transactions on Nuclear Science* 6.2 (June 1959), pp. 49–53.

[30] W. Rosenzweig, H. K. Gummel, and F. M. Smits. "Solar cell degradation under 1-Mev electron bombardment". In: *The Bell System Technical Journal* 42.2 (Mar. 1963), pp. 399–414.

[31] G. Xin, F. Zhan-zu, C. Xin-yu, Y. Sheng-sheng, and Z. Lei. "Performance Evaluation and Prediction of Single-Junction and Triple-Junction GaAs Solar Cells Induced by Electron and Proton Irradiations". In: *IEEE Transactions on Nuclear Science* 61.4 (Aug. 2014), pp. 1838–1842.

[32] C. Dale, P. Marshall, B. Cummings, L. Shamey, and A. Holland. "Displacement damage effects in mixed particle environments for shielded spacecraft CCDs". In: *IEEE Transactions on Nuclear Science* 40.6 (Dec. 1993), pp. 1628–1637.

[33] J. Bogaerts, B. Dierickx, G. Meynants, and D. Uwaerts. "Total dose and displacement damage effects in a radiation-hardened CMOS APS". In: *IEEE Transactions on Electron Devices* 50.1 (Jan. 2003), pp. 84–90.

[34] C. Virmontois, V. Goiffon, P. Magnan, S. Girard, C. Inguimbert, S. Petit, G. Rolland, and O. Saint-Pe. "Displacement Damage Effects Due to Neutron and Proton Irradiations on CMOS Image Sensors Manufactured in Deep Submicron Technology". In: *IEEE Transactions on Nuclear Science* 57.6 (Dec. 2010), pp. 3101–3108.

[35] F. Faccio, B. Allongue, G. Blanchot, C. Fuentes, S. Michelis, S. Orlandi, and R. Sorge. "TID and displacement damage effects in vertical and lateral power MOSFETs for integrated DC-DC converters". In: *2009 European Conference on Radiation and Its Effects on Components and Systems*. Sept. 2009, pp. 46–53.

[36] R. C. Baumann. "Radiation-induced soft errors in advanced semiconductor technologies". In: *IEEE Transactions on Device and Materials Reliability* 5.3 (Sept. 2005), pp. 305–316.

[37] F. W. Sexton, D. M. Fleetwood, M. R. Shaneyfelt, P. E. Dodd, and G. L. Hash. "Single event gate rupture in thin gate oxides". In: *IEEE Transactions on Nuclear Science* 44.6 (Dec. 1997), pp. 2345–2352.

[38] F. W. Sexton. "Destructive single-event effects in semiconductor devices and ICs". In: *IEEE Transactions on Nuclear Science* 50.3 (June 2003), pp. 603–621.

[39] D. Munteanu and J. L. Autran. "Modeling and Simulation of Single-Event Effects in Digital Devices and ICs". In: *IEEE Transactions on Nuclear Science* 55.4 (Aug. 2008), pp. 1854–1878.

[40] G. P. Summers, E. A. Burke, and M. A. Xapsos. "Displacement damage analogs to ionizing radiation effects". In: *Radiation Measurements* 24.1 (1995), pp. 1–8.

[41] R. Gaillard. "Single Event Effects: Mechanisms and Classification". In: *Soft Errors in Modern Electronic Systems*. Ed. by M. Nicolaidis. Boston, MA: Springer US, 2011, pp. 27–54.

[42] P. E. Dodd. "Physics-based simulation of single-event effects". In: *IEEE Transactions on Device and Materials Reliability* 5.3 (Sept. 2005), pp. 343–357.

[43] P. E. Dodd and L. W. Massengill. "Basic mechanisms and modeling of single-event upset in digital microelectronics". In: *IEEE Transactions on Nuclear Science* 50.3 (June 2003), pp. 583–602.

[44] T. R. Oldham and F. B. McLean. "Total ionizing dose effects in MOS oxides and devices". In: *IEEE Transactions on Nuclear Science* 50.3 (June 2003), pp. 483–499.

[45] H. J. Barnaby. "Total-Ionizing-Dose Effects in Modern CMOS Technologies". In: *IEEE Transactions on Nuclear Science* 53.6 (Dec. 2006).

[46] J. R. Schwank, M. R. Shaneyfelt, D. M. Fleetwood, J. A. Felix, P. E. Dodd, P. Paillet, and V. Ferlet-Cavrois. "Radiation Effects in MOS Oxides". In: *IEEE Transactions on Nuclear Science* 55.4 (Aug. 2008), pp. 1833–1853.

[47] D. M. Fleetwood. "Total Ionizing Dose Effects in MOS and Low-Dose-Rate-Sensitive Linear-Bipolar Devices". In: *IEEE Transactions on Nuclear Science* 60.3 (June 2013), pp. 1706–1730.

[48] J. Schwank. "Basic mechanisms of radiation effects in the natural space radiation environment". In: (June 1994).

[49] P. V. Dressendorfer. "Basic mechanisms for the new millennium". In: (Sept. 1998).

[50] T.-P. Ma and P. V. Dressendorfer. *Ionizing radiation effects in MOS devices and circuits*. John Wiley & Sons, 1989.

[51] T. R. Oldham. *Ionizing radiation effects in MOS oxides*. World Scientific, 1999.

[52] L. Evans and P. Bryant. "LHC Machine". In: *Journal of Instrumentation* 3.08 (2008), S08001.

[53] B. Schmidt. "The High-Luminosity upgrade of the LHC: Physics and Technology Challenges for the Accelerator and the Experiments". In: *Journal of Physics: Conference Series* 706.2 (2016), p. 022002. URL: `http://stacks.iop.org/1742-6596/706/i=2/a=022002`.

[54] E. Normand. "Single event upset at ground level". In: *IEEE Transactions on Nuclear Science* 43.6 (Dec. 1996), pp. 2742–2750.

[55] J. F. Ziegler. "Terrestrial cosmic rays". In: *IBM Journal of Research and Development* 40.1 (Jan. 1996), pp. 19–39.

[56] P. Goldhagen. "Cosmic-Ray Neutrons on the Ground and in the Atmosphere". In: *MRS Bulletin* 28.2 (2003), pp. 131–135.

[57] H. H. Tang and K. P. Rodbell. "Single-Event Upsets in Microelectronics: Fundamental Physics and Issues". In: *MRS Bulletin* 28.2 (2003), pp. 111–116.

[58] E. G. Stassinopoulos and J. P. Raymond. "The space radiation environment for electronics". In: *Proceedings of the IEEE* 76.11 (Nov. 1988), pp. 1423–1442.

[59] S. Bourdarie and M. Xapsos. "The Near-Earth Space Radiation Environment". In: *IEEE Transactions on Nuclear Science* 55.4 (Aug. 2008), pp. 1810–1832.

[60] J. Valentin. *The 2007 recommendations of the international commission on radiological protection*. Elsevier Oxford, 2007.

[61] U. N. S. C. on the Effects of Atomic Radiation et al. *UNSCEAR 2008 report to the general assembly with scientific annexes: United Nations*. 2015.

[62] E. J. Daly, G. Drolshagen, A. Hilgers, and H. D. R. Evans. "Space Environment Analysis: Experience and Trends". In: *Environment Modeling for Space-Based Applications*. Ed. by T.-D. Guyenne and A. Hilgers. Vol. 392. ESA Special Publication. Dec. 1996, p. 15.

[63] G. D. Badhwar. "Radiation dose rates in Space Shuttle as a function of atmospheric density". In: *Radiation Measurements* 30.3 (1999), pp. 401–414.

[64] E. R. Benton and E. V. Benton. "Space radiation dosimetry in low-Earth orbit and beyond". In: *Nuclear Instruments and Methods in Physics Research Section B: Beam Interactions with Materials and Atoms* 184.1 (20-01). Advanced Topics in Solid State Dosimetry, pp. 255–294.

[65] W. Herr and B. Muratori. "Concept of luminosity". In: (2006).

[66] C. Collaboration. *The Phase-2 Upgrade of the CMS Tracker*. Tech. rep. CERN-LHCC-2017-009. CMS-TDR-014. Geneva: CERN, June 2017. URL: https://cds.cern.ch/record/2272264.

[67] G. Apollinari, O. Brüning, T. Nakamoto, and L. Rossi. "High Luminosity Large Hadron Collider HL-LHC". In: *arXiv preprint arXiv:1705.08830* (2017).

[68] *ATLAS Phase-II Upgrade Scoping Document*. Tech. rep. CERN-LHCC-2015-020. LHCC-G-166. Geneva: CERN, Sept. 2015. URL: https://cds.cern.ch/record/2055248.

[69] D. Contardo, M. Klute, J. Mans, L. Silvestris, and J. Butler. *Technical Proposal for the Phase-II Upgrade of the CMS Detector*. Tech. rep. CERN-LHCC-2015-010. LHCC-P-008. CMS-TDR-15-02. Geneva, June 2015.

[70] B. Schmidt. "The High-Luminosity upgrade of the LHC: Physics and Technology Challenges for the Accelerator and the Experiments". In: *Journal of Physics: Conference Series* 706.2 (2016), p. 022002.

[71] R. D. Evans. *The atomic nucleus*. McGraw-Hill New York, 1955.

[72] F. B. McLean and T. R. Oldham. *Basic mechanisms of radiation effects in electronic materials and devices*. Tech. rep. HARRY DIAMOND LABS ADELPHI MD, 1987.

[73] J. Srour. *Basic mechanisms of radiation effects on electronic materials, devices, and integrated circuits*. Tech. rep. NORTHROP RESEARCH and TECHNOLOGY CENTERPALOS VERDES PENINSULA CA, 1982.

[74] J. A. Bearden and A. F. Burr. "Reevaluation of X-Ray Atomic Energy Levels". In: *Rev. Mod. Phys.* 39 (1 Jan. 1967), pp. 125–142.

[75] J. M. Benedetto and H. E. Boesch. "The Relationship between 60Co and 10-keV X-Ray Damage in MOS Devices". In: *IEEE Transactions on Nuclear Science* 33.6 (Dec. 1986), pp. 1317–1323.

[76] R. C. Hughes. "Charge-Carrier Transport Phenomena in Amorphous SiO_2: Direct Measurement of the Drift Mobility and Lifetime". In: *Phys. Rev. Lett.* 30 (26 June 1973), pp. 1333–1336.

[77] R. Hughes. "High field electronic properties of SiO2". In: *Solid-State Electronics* 21.1 (1978), pp. 251–258.

[78] D. K. Ferry. "Electron transport and breakdown in SiO2". In: *Journal of Applied Physics* 50.3 (1979), pp. 1422–1427.

[79] M. V. Fischetti, D. J. DiMaria, S. D. Brorson, T. N. Theis, and J. R. Kirtley. "Theory of high-field electron transport in silicon dioxide". In: *Phys. Rev. B* 31 (12 June 1985), pp. 8124–8142.

[80] R. C. Hughes. "Time-resolved hole transport in $a - SiO_2$". In: *Phys. Rev. B* 15 (4 Feb. 1977), pp. 2012–2020.

[81] O. L. C. Jr. and J. R. Srour. "The multiple-trapping model and hole transport in SiO2". In: *Journal of Applied Physics* 48.9 (1977), pp. 3819–3828.

[82] F. B. McLean, H. E. Boesch Jr, and T. R. Oldham. "Electron-hole generation, transport and trapping in SiO2". In: *Ionizing radiation effects in MOS devices and circuits*. 1989.

[83] T. R. Oldham. "Recombination along the tracks of heavy charged particles in SiO2 films". In: *Journal of Applied Physics* 57.8 (1985), pp. 2695–2702.

[84] G. Pfister and H. Scher. "Dispersive (non-Gaussian) transient transport in disordered solids". In: *Advances in Physics* 27.5 (1978), pp. 747–798.

[85] C. J. Nicklaw, Z. Y. Lu, D. M. Fleetwood, R. D. Schrimpf, and S. T. Pantelides. "The structure, properties, and dynamics of oxygen vacancies in amorphous SiO2". In: *IEEE Transactions on Nuclear Science* 49.6 (Dec. 2002), pp. 2667–2673.

[86] D. M. Fleetwood, H. D. Xiong, Z. Y. Lu, C. J. Nicklaw, J. A. Felix, R. D. Schrimpf, and S. T. Pantelides. "Unified model of hole trapping, 1/f noise, and thermally stimulated current in MOS devices". In: *IEEE Transactions on Nuclear Science* 49.6 (Dec. 2002), pp. 2674–2683.

[87] H. E. Boesch, J. M. McGarrity, and F. B. McLean. "Temperature- and Field-Dependent Charge Relaxation in SiO2 Gate Insulators". In: *IEEE Transactions on Nuclear Science* 25.3 (June 1978), pp. 1012–1016.

[88] F. McLean, H. Boesch, and J. McGarrity. "FIELD-DEPENDENT HOLE TRANSPORT IN AMORPHOUS SiO2". In: *The Physics of SiO2 and its Interfaces*. Ed. by S. T. PANTELIDES. Pergamon, 1978, pp. 19–23.

[89] H. E. Boesch, F. B. McLean, J. M. McGarrity, and P. S. Winokur. "Enhanced Flatband Voltage Recovery in Hardened Thin MOS Capacitors". In: *IEEE Transactions on Nuclear Science* 25.6 (Dec. 1978), pp. 1239–1245.

[90] F. B. Mclean, H. Boesch Jr, and J. M. McGarrity. *Dispersive Hole Transport in SiO2*. Tech. rep. HARRY DIAMOND LABS ADELPHI MD, 1987.

[91] L. Tsetseris, D. Fleetwood, R. Schrimpf, X. Zhou, I. Batyrev, and S. Pantelides. "Hydrogen effects in MOS devices". In: *Microelectronic Engineering* 84.9 (2007). INFOS 2007, pp. 2344–2349.

[92] N. S. Saks and D. B. Brown. "Interface trap formation via the two-stage H^+ process". In: *IEEE Transactions on Nuclear Science* 36.6 (Dec. 1989), pp. 1848–1857.

[93] F. J. Feigl, W. Fowler, and K. L. Yip. "Oxygen vacancy model for the E_1' center in SiO_2". In: *Solid State Communications* 14.3 (1974), pp. 225–229.

[94] A. J. Lelis, T. R. Oldham, H. E. Boesch, and F. B. McLean. "The nature of the trapped hole annealing process". In: *IEEE Transactions on Nuclear Science* 36.6 (Dec. 1989), pp. 1808–1815.

[95] W. L. Warren, M. R. Shaneyfelt, D. M. Fleetwood, J. R. Schwank, P. S. Winokur, and R. A. B. Devine. "Microscopic nature of border traps in MOS oxides". In: *IEEE Transactions on Nuclear Science* 41.6 (Dec. 1994), pp. 1817–1827.

[96] D. Fleetwood. "Border traps and bias-temperature instabilities in MOS devices". In: *Microelectronics Reliability* 80 (2018), pp. 266–277.

[97] D. M. Fleetwood. "'Border traps' in MOS devices". In: *IEEE Transactions on Nuclear Science* 39.2 (Apr. 1992), pp. 269–271.

[98] E. H. Snow, A. S. Grove, B. E. Deal, and C. T. Sah. "Ion Transport Phenomena in Insulating Films". In: *Journal of Applied Physics* 36.5 (1965), pp. 1664–1673.

[99] T. P. Ma and R. C. Barker. "Effect of gamma-ray irradiation on the surface states of MOS tunnel junctions". In: *Journal of Applied Physics* 45.1 (1974), pp. 317–321.

[100] H. H. Sander and B. L. Gregory. "Unified Model of Damage Annealing in CMOS, from Freeze-In to Transient Annealing". In: *IEEE Transactions on Nuclear Science* 22.6 (Dec. 1975), pp. 2157–2162.

[101] H. E. Boesch and J. M. McGarrity. "Charge Yield and Dose Effects in MOS Capacitors at 80 K". In: *IEEE Transactions on Nuclear Science* 23.6 (Dec. 1976), pp. 1520–1525.

[102] S. M. Sze and K. K. Ng. *Physics of semiconductor devices*. John wiley & sons, 2006.

[103] B. G. Streetman and S. K. Banerjee. *Solid State Electronic Devices: Global Edition*. Pearson education, 2016.

[104] N. S. Saks, M. G. Ancona, and J. A. Modolo. "Radiation Effects in MOS Capacitors with Very Thin Oxides at 80°K". In: *IEEE Transactions on Nuclear Science* 31.6 (Dec. 1984), pp. 1249–1255.

[105] J. M. Benedetto, H. E. Boesch, F. B. McLean, and J. P. Mize. "Hole Removal in Thin-Gate MOSFETs by Tunneling". In: *IEEE Transactions on Nuclear Science* 32.6 (Dec. 1985), pp. 3916–3920.

[106] F. B. McLean, G. A. Ausman, H. E. Boesch, and J. M. McGarrity. "Application of stochastic hopping transport to hole conduction in amorphous SiO2". In: *Journal of Applied Physics* 47.4 (1976), pp. 1529–1532.

[107] P. M. Lenahan and J. F. Conley. "What can electron paramagnetic resonance tell us about the Si/SiO2 system?" In: *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures Processing, Measurement, and Phenomena* 16.4 (1998), pp. 2134–2153.

[108] S. N. Rashkeev, D. M. Fleetwood, R. D. Schrimpf, and S. T. Pantelides. "Proton-induced defect generation at the $Si - SiO_2$ interface". In: *IEEE Transactions on Nuclear Science* 48.6 (Dec. 2001), pp. 2086–2092.

[109] P. J. Caplan, E. H. Poindexter, B. E. Deal, and R. R. Razouk. "ESR centers, interface states, and oxide fixed charge in thermally oxidized silicon wafers". In: *Journal of Applied Physics* 50.9 (1979), pp. 5847–5854.

[110] F. B. McLean. "A Framework for Understanding Radiation-Induced Interface States in SiO2 MOS Structures". In: *IEEE Transactions on Nuclear Science* 27.6 (Dec. 1980), pp. 1651–1657.

[111] P. M. Lenahan and P. V. Dressendorfer. "Hole traps and trivalent silicon centers in metal/oxide/silicon devices". In: *Journal of Applied Physics* 55.10 (1984), pp. 3495–3499.

[112] P. S. Winokur. "Radiation-induced interface traps". In: *Ionizing radiation effects in MOS devices and circuits*. New York: Wiley, 1989, pp. 193–255.

[113] D. M. Fleetwood, F. V. Thome, S. S. Tsao, P. V. Dressendorfer, V. J. Dandini, and J. R. Schwank. "High-temperature silicon-on-insulator electronics for space nuclear power systems: requirements and feasibility". In: *IEEE Transactions on Nuclear Science* 35.5 (Oct. 1988), pp. 1099–1112.

[114] A. J. Lelis, T. R. Oldham, and W. M. DeLancey. "Response of interface traps during high-temperature anneals [MOSFETs]". In: *IEEE Transactions on Nuclear Science* 38.6 (Dec. 1991), pp. 1590–1597.

[115] N. S. Saks, C. M. Dozier, and D. B. Brown. "Time dependence of interface trap formation in MOSFETs following pulsed irradiation". In: *IEEE Transactions on Nuclear Science* 35.6 (Dec. 1988), pp. 1168–1177.

[116] N. S. Saks, M. G. Ancona, and J. A. Modolo. "Generation of Interface States by Ionizing Radiation in Very Thin MOS Oxides". In: *IEEE Transactions on Nuclear Science* 33.6 (Dec. 1986), pp. 1185–1190.

[117] D. B. Brown and N. S. Saks. "Time dependence of radiation-induced interface trap formation in metal-oxide-semiconductor devices as a function of oxide thickness and applied field". In: *Journal of Applied Physics* 70.7 (1991), pp. 3734–3747.

[118] *CERN EP-ESE-ME group X-rays irradiation system*. URL: `http://proj-xraymic.web.cern.ch/proj-xraymic/`.

[119] L. J. Palkuti and J. J. LePage. "X-Ray Wafer Probe for Total Dose Testing". In: *IEEE Transactions on Nuclear Science* 29.6 (Dec. 1982), pp. 1832–1837.

[120] S. Healthcare. *XRaySpectrum*. 2018. URL: `https://www.oem-xray-components.siemens.com/x-ray-spectra-simulation` (visited on 09/17/2018).

[121] M. Guthoff, O. Brovchenko, W. de Boer, A. Dierlamm, T. Müller, A. Ritter, M. Schmanau, and H.-J. Simonis. "Geant4 simulation of a filtered X-ray source for radiation damage studies". In: *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment* 675 (2012), pp. 118–122.

[122] G. F. Derbenwick and H. H. Sander. "CMOS Hardness Prediction for Low-Dose-Rate Environments". In: *IEEE Transactions on Nuclear Science* 24.6 (Dec. 1977), pp. 2244–2247.

[123] D. M. Fleetwood. "Evolution of Total Ionizing Dose Effects in MOS Devices with Moore's Law Scaling". In: *IEEE Transactions on Nuclear Science* (2017), pp. 1–1.

[124] K. Terada, K. Nishiyama, and K.-I. Hatanaka. "Comparison of MOSFET-threshold-voltage extraction methods". In: *Solid-State Electronics* 45.1 (2001), pp. 35–40.

[125] A. Ortiz-Conde, F. J. García-Sánchez, J. Muci, A. T. Barrios, J. J. Liou, and C.-S. Ho. "Revisiting MOSFET threshold voltage extraction methods". In: *Microelectronics Reliability* 53.1 (2013). Reliability of Micro-Interconnects in 3D IC Packages, pp. 90–104.

[126] L. Dobrescu, M. Petrov, D. Dobrescu, and C. Ravariu. "Threshold voltage extraction methods for MOS transistors". In: *2000 International Semiconductor Conference. 23rd Edition. CAS 2000 Proceedings.* Vol. 1. Oct. 2000, 371–374 vol.1.

[127] A. Ortiz-Conde, F. G. Sánchez, J. Liou, A. Cerdeira, M. Estrada, and Y. Yue. "A review of recent MOSFET threshold voltage extraction methods". In: *Microelectronics Reliability* 42.4 (2002), pp. 583–596.

[128] M. Bohr. "A 30 Year Retrospective on Dennard's MOSFET Scaling Paper". In: *IEEE Solid-State Circuits Society Newsletter* 12.1 (2007), pp. 11–13.

[129] URL: `http://www.europractice-ic.com/technologies.php` (visited on 07/19/2018).

[130] G. Traversi, L. Gaioni, M. Manghisoni, L. Ratti, and V. Re. *Perspectives of 65nm CMOS technologies for high performance front-end electronics in future applications.* Sept. 2012. URL: `https://indico.cern.ch/event/190941/contributions/1466437/attachments/271602/380058/traversi.pdf` (visited on 07/19/2018).

[131] D. James. "High-k/metal gates in leading edge silicon devices". In: *2012 SEMI Advanced Semiconductor Manufacturing Conference.* May 2012.

[132] D. K. Schroder. "Negative bias temperature instability: What do we understand?" In: *Microelectronics Reliability* 47.6 (2007). Modelling the Negative Bias Temperature Instability, pp. 841–852.

[133] C. Hu, S. C. Tam, F.-C. Hsu, P.-K. Ko, T.-Y. Chan, and K. W. Terrill. "Hot-electron-induced MOSFET degradation—Model, monitor, and improvement". In: *IEEE Transactions on Electron Devices* 32.2 (Feb. 1985), pp. 375–385.

[134] S. Gerardin, M. Bagatin, D. Cornale, L. Ding, S. Mattiazzo, A. Paccagnella, F. Faccio, and S. Michelis. "Enhancement of Transistor-to-Transistor Variability Due to Total Dose Effects in 65-nm MOSFETs". In: *IEEE Transactions on Nuclear Science* 62.6 (Dec. 2015), pp. 2398–2403.

[135] M. R. Shaneyfelt, P. E. Dodd, B. L. Draper, and R. S. Flores. "Challenges in hardening technologies using shallow-trench isolation". In: *IEEE Transactions on Nuclear Science* 45.6 (Dec. 1998), pp. 2584–2592.

[136] G. U. Youk, P. S. Khare, R. D. Schrimpf, L. W. Massengill, and K. F. Galloway. "Radiation-enhanced short channel effects due to multi-dimensional influence from charge at trench isolation oxides". In: *IEEE Transactions on Nuclear Science* 46.6 (Dec. 1999), pp. 1830–1835.

[137] A. Scarpa, A. Paccagnella, F. Montera, G. Ghibaudo, G. Pananakakis, G. Ghidini, and P. G. Fuochi. "Ionizing radiation induced leakage current on ultra-thin gate oxides". In: *IEEE Transactions on Nuclear Science* 44.6 (Dec. 1997), pp. 1818–1825.

[138] M. Ceschia, A. Paccagnella, A. Cester, A. Scarpa, and G. Ghidini. "Radiation induced leakage current and stress induced leakage current in ultra-thin gate oxides". In: *IEEE Transactions on Nuclear Science* 45.6 (Dec. 1998), pp. 2375–2382.

[139] L. Larcher, A. Paccagnella, M. Ceschia, and G. Ghidini. "A model of radiation induced leakage current (RILC) in ultra-thin gate oxides". In: *IEEE Transactions on Nuclear Science* 46.6 (Dec. 1999), pp. 1553–1561.

[140] R. C. Lacoe, J. V. Osborn, D. C. Mayer, S. Brown, and D. R. Hunt. "Total-dose radiation tolerance of a commercial 0.35 μm CMOS process". In: *1998 IEEE Radiation Effects Data Workshop. NSREC 98. Workshop Record. Held in conjunction with IEEE Nuclear and Space Radiation Effects Conference (Cat. No.98TH8385)*. July 1998, pp. 104–110.

[141] G. U. Youk, P. S. Khare, R. D. Schrimpf, L. W. Massengill, and K. F. Galloway. "Radiation-enhanced short channel effects due to multi-dimensional influence from charge at trench isolation oxides". In: *IEEE Transactions on Nuclear Science* 46.6 (Dec. 1999), pp. 1830–1835.

[142] W. K. Henson, N. Yang, S. Kubicek, E. M. Vogel, J. J. Wortman, K. D. Meyer, and A. Naem. "Analysis of leakage currents and impact on off-state power consumption for CMOS technology in the 100-nm regime". In: *IEEE Transactions on Electron Devices* 47.7 (July 2000), pp. 1393–1400.

[143] F. T. Brady, J. D. Maimon, and M. J. Hurt. "A scaleable, radiation hardened shallow trench isolation". In: *IEEE Transactions on Nuclear Science* 46.6 (Dec. 1999), pp. 1836–1840.

[144] Z. Hu, Z. Liu, H. Shao, Z. Zhang, B. Ning, M. Chen, D. Bi, and S. Zou. "Impact of within-wafer process variability on radiation response". In: *Microelectronics Journal* 42.6 (2011), pp. 883–888.

[145] C.-M. Zhang, F. Jazaeri, G. Borghello, F. Faccio, S. Mattiazzo, A. Baschirotto, and C. Enz. "Characterization and Modeling of GigaRad-TID-Induced Drain Leakage Current in a 28 nm Bulk CMOS Technology". In: (Apr. 2018).

[146] G. Niu, S. J. Mathew, G. Banerjee, J. D. Cressler, S. D. Clark, M. J. Palmer, and S. Subbanna. "Total dose effects on the shallow-trench isolation leakage current characteristics in a 0.35 /spl mu/m SiGe BiCMOS technology". In: *IEEE Transactions on Nuclear Science* 46.6 (Dec. 1999), pp. 1841–1847.

[147] M. Turowski, A. Raman, and R. D. Schrimpf. "Nonuniform total-dose-induced charge distribution in shallow-trench isolation oxides". In: *IEEE Transactions on Nuclear Science* 51.6 (Dec. 2004), pp. 3166–3171.

[148] I. S. Esqueda, H. J. Barnaby, and M. L. Alles. "Two-dimensional methodology for modeling radiation-induced off-state leakage in CMOS technologies". In: *IEEE Transactions on Nuclear Science* 52.6 (Dec. 2005), pp. 2259–2264.

[149] M. McLain, H. J. Barnaby, K. E. Holbert, R. D. Schrimpf, H. Shah, A. Amort, M. Baze, and J. Wert. "Enhanced TID Susceptibility in Sub-100 nm Bulk CMOS I/O Transistors and Circuits". In: *IEEE Transactions on Nuclear Science* 54.6 (Dec. 2007), pp. 2210–2217.

[150] V. Re, L. Gaioni, M. Manghisoni, L. Ratti, and G. Traversi. "Comprehensive Study of Total Ionizing Dose Damage Mechanisms and Their Effects on Noise Sources in a 90 nm CMOS Technology". In: *IEEE Transactions on Nuclear Science* 55.6 (Dec. 2008), pp. 3272–3279.

[151] A. H. Johnston, R. T. Swimm, G. R. Allen, and T. F. Miyahira. "Total Dose Effects in CMOS Trench Isolation Regions". In: *IEEE Transactions on Nuclear Science* 56.4 (Aug. 2009), pp. 1941–1949.

[152] N. Rezzak, M. L. Alles, R. D. Schrimpf, S. Kalemeris, L. W. Massengill, J. Sochacki, and H. J. Barnaby. "The sensitivity of radiation-induced leakage to STI topology and sidewall doping". In: *Microelectronics Reliability* 51.5 (2011), pp. 889–894.

[153] F. Faccio and G. Cervelli. "Radiation-induced edge effects in deep submicron CMOS transistors". In: *IEEE Trans. Nucl. Sci.* 52 (2005), pp. 2413–2420.

[154] F. Faccio, H. J. Barnaby, X. J. Chen, D. M. Fleetwood, L. Gonella, M. McLain, and R. D. Schrimpf. "Total ionizing dose effects in shallow trench isolation oxides". In: *Microelectronics Reliability* 48.7 (2008). 2007 Reliability of Compound Semiconductors (ROCS) Workshop, pp. 1000–1007.

[155] P. J. McWhorter and P. S. Winokur. "Simple technique for separating the effects of interface traps and trapped-oxide charge in metal-oxide-semiconductor transistors". In: *Applied Physics Letters* 48.2 (1986).

[156] G. Anelli, M. Campbell, M. Delmastro, F. Faccio, S. Floria, A. Giraldo, E. Heijne, P. Jarron, K. Kloukinas, A. Marchioro, P. Moreira, and W. Snoeys. "Radiation tolerant VLSI circuits in standard deep submicron CMOS technologies for the LHC experiments: practical design aspects". In: *IEEE Transactions on Nuclear Science* 46.6 (Dec. 1999), pp. 1690–1696.

[157] W. Snoeys et al. "Layout techniques to enhance the radiation tolerance of standard CMOS technologies demonstrated on a pixel detector readout chip". In: *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment* 439.2 (2000), pp. 349–360.

[158] W. J. Snoeys, T. A. P. Gutierrez, and G. Anelli. "A new NMOS layout structure for radiation tolerance". In: *2001 IEEE Nuclear Science Symposium Conference Record (Cat. No.01CH37310)*. Vol. 2. Nov. 2001, 822–826 vol.2.

[159] F. Faccio. *Large scale application of design hardening, or how to save 150M$*. May 2005. URL: http://www.in2p3.fr/actions/formation/microelectronique07/Faccio_IN2P3_2public.pdf.

[160] F. Faccio, S. Michelis, D. Cornale, A. Paccagnella, and S. Gerardin. "Radiation-Induced Short Channel (RISCE) and Narrow Channel (RINCE) Effects in 65 and 130 nm MOSFETs". In: *IEEE Transactions on Nuclear Science* 62.6 (Dec. 2015), pp. 2933–2940.

[161] M. Gaillardin, V. Goiffon, S. Girard, M. Martinez, P. Magnan, and P. Paillet. "Enhanced Radiation-Induced Narrow Channel Effects in Commercial 0.18 μm Bulk Technology". In: *IEEE Transactions on Nuclear Science* 58.6 (Dec. 2011), pp. 2807–2815.

[162] H. D. Koch, F. Faccio, and G. Borghello. "Effects of Ultra-High Total Ionizing Dose in Nanoscale Bulk CMOS Technologies". Presented 2018. 2018.

[163] S. Bonaldo, S. Mattiazzo, A. Paccagnella, S. Gerardin, A. Baschirotto, and X. Jin. "Influence of Halo Implantations on the Total Ionizing Dose Response of 28 nm P-MOSFETs Irradiated to Ultra-High Doses". In: 2018. Poster presented at NSREC 2018, Kona, Hawaii (USA).

[164] C. M. Zhang, F. Jazaeri, A. Pezzotta, C. Bruschini, G. Borghello, F. Faccio, S. Mattiazzo, A. Baschirotto, and C. Enz. "Characterization of GigaRad Total Ionizing Dose and Annealing Effects on 28-nm Bulk MOSFETs". In: *IEEE Transactions on Nuclear Science* 64.10 (Oct. 2017), pp. 2639–2647.

[165] C. M. Zhang, F. Jazaeri, A. Pezzotta, C. Bruschini, G. Borghello, S. Mattiazzo, A. Baschirotto, and C. Enz. "Total ionizing dose effects on analog performance of 28 nm bulk MOSFETs". In: *2017 47th European Solid-State Device Research Conference (ESSDERC)*. Sept. 2017, pp. 30–33.

[166] C. M. Zhang, F. Jazaeri, A. Pezzotta, C. Bruschini, G. Borghello, F. Faccio, S. Mattiazzo, A. Baschirotto, and C. Enz. "GigaRad total ionizing dose and post-irradiation effects on 28 nm bulk MOSFETs". In: *2016 IEEE Nuclear Science Symposium, Medical Imaging Conference and Room-Temperature Semiconductor Detector Workshop (NSS/MIC/RTSD)*. Oct. 2016, pp. 1–4.

[167] A. Pezzotta, C. M. Zhang, F. Jazaeri, C. Bruschini, G. Borghello, F. Faccio, S. Mattiazzo, A. Baschirotto, and C. Enz. "Impact of GigaRad Ionizing Dose on 28 nm bulk MOSFETs for future HL-LHC". In: *2016 46th European Solid-State Device Research Conference (ESSDERC)*. Sept. 2016, pp. 146–149.

[168] M. T. Bohr, R. S. Chau, T. Ghani, and K. Mistry. "The High-k Solution". In: *IEEE Spectrum* 44.10 (Oct. 2007), pp. 29–35.

[169] M. M. Frank. "High-k/metal gate innovations enabling continued CMOS scaling". In: *2011 Proceedings of the ESSCIRC (ESSCIRC)*. Sept. 2011, pp. 50–58.

[170] S. Ogura, P. J. Tsang, W. W. Walker, D. L. Critchlow, and J. F. Shepard. "Design and characteristics of the lightly doped drain-source (LDD) insulated gate field-effect transistor". In: *IEEE Transactions on Electron Devices* 27.8 (Aug. 1980), pp. 1359–1367.

[171] B. Pelletier, M. Juhel, C. Trouiller, D. Beucher, J. Autran, and P. Morin. "Boron out-diffusion mechanism in oxide and nitride CMOS sidewall spacer: Impact of the materials properties". In: *Materials Science and Engineering: B* 154-155 (2008). Front-End Junction and Contact Formation in Future Silicon/Germanium Based Devices, pp. 252–255.

[172] F. Faccio, G. Borghello, E. Lerario, D. M. Fleetwood, R. D. Schrimpf, H. Gong, E. X. Zhang, P. Wang, S. Michelis, S. Gerardin, A. Paccagnella, and S. Bonaldo. "Influence of LDD spacers and H+ transport on the total-ionizing-dose response of 65 nm MOSFETs irradiated to ultra-high doses". In: *IEEE Transactions on Nuclear Science* 65.1 (Jan. 2018), pp. 164–174.

[173] F. .-.-. Hsu and H. R. Grinolds. "Structure-enhanced MOSFET degradation due to hot-electron injection". In: *IEEE Electron Device Letters* 5.3 (Mar. 1984), pp. 71–74.

[174] D. Fleury, A. Cros, G. Bidal, J. Rosa, and G. Ghibaudo. "A New Technique to Extract the Source/Drain Series Resistance of MOSFETs". In: *IEEE Electron Device Letters* 30.9 (Sept. 2009), pp. 975–977.

[175] A. Dixit, A. Kottantharayil, N. Collaert, M. Goodwin, M. Jurczak, and K. D. Meyer. "Analysis of the parasitic S/D resistance in multiple-gate FETs". In: *IEEE Transactions on Electron Devices* 52.6 (June 2005).

[176] J. P. Campbell, K. P. Cheung, J. S. Suehle, and A. Oates. "A Simple Series Resistance Extraction Methodology for Advanced CMOS Devices". In: *IEEE Electron Device Letters* 32.8 (Aug. 2011), pp. 1047–1049.

[177] J. P. Campbell, K. P. Cheung, S. A. Drozdov, R. G. Southwick, J. T. Ryan, A. S. Oates, and J. S. Suehle. "Channel length-dependent series resistance?" In: *2012 IEEE Silicon Nanoelectronics Workshop (SNW)*. June 2012, pp. 1–2.

[178] S. Bonaldo, S. Gerardin, X. Jin, A. Paccagnella, F. Faccio, G. Borghello, and D. M. Fleetwood. "Charge Buildup and Spatial Distribution of Interface Traps in 65 nm pMOSFETs Irradiated to Ultra-high Doses". In: *2018 IEEE Radiation Effects on Components and Systems (RADECS)*. 2018.

[179] D. H. Huang, E. E. King, J. J. Wang, R. Ormond, and L. J. Palkuti. "Correlation between channel hot-electron degradation and radiation-induced interface trapping in N-channel LDD devices". In: *IEEE Transactions on Nuclear Science* 38.6 (Dec. 1991), pp. 1336–1341.

[180] G. Borghello, F. Faccio, E. Lerario, S. Michelis, S. Kulis, D. M. Fleetwood, R. D. Schrimpf, S. Gerardin, A. Paccagnella, and S. Bonaldo. "Dose-Rate Sensitivity of 65-nm MOSFETs Exposed to Ultrahigh Doses". In: *IEEE Transactions on Nuclear Science* 65.8 (Aug. 2018), pp. 1482–1487.

[181] J. R. Schwank, D. M. Fleetwood, M. R. Shaneyfelt, P. S. Winokur, C. L. Axness, and L. C. Riewe. "Latent interface-trap buildup and its implications for hardness assurance (MOS transistors)". In: *IEEE Transactions on Nuclear Science* 39.6 (Dec. 1992), pp. 1953–1963.

[182] S. R. Hofstein. "Proton and sodium transport in SiO_2 films". In: *IEEE Transactions on Electron Devices* 14.11 (Nov. 1967), pp. 749–759.

[183] N. S. Saks and D. B. Brown. "Observation of H/sup +/ motion during interface trap formation". In: *IEEE Transactions on Nuclear Science* 37.6 (Dec. 1990), pp. 1624–1631.

[184] J. S. Brugler and P. G. A. Jespers. "Charge pumping in MOS devices". In: *IEEE Transactions on Electron Devices* 16.3 (Mar. 1969), pp. 297–302.

[185] P. Heremans, J. Witters, G. Groeseneken, and H. E. Maes. "Analysis of the charge pumping technique and its application for the evaluation of MOSFET degradation". In: *IEEE Transactions on Electron Devices* 36.7 (July 1989), pp. 1318–1335.

[186] D. S. Ang and C. H. Ling. "A new assessment of the self-limiting hot-carrier degradation in LDD NMOSFET's by charge pumping measurement". In: *IEEE Electron Device Letters* 18.6 (June 1997), pp. 299–301.

[187] R. R. Troutman. "VLSI limitations from drain-induced barrier lowering". In: *IEEE Journal of Solid-State Circuits* 14.2 (Apr. 1979), pp. 383–391.

[188] D. M. Fleetwood and H. A. Eisen. "Total-dose radiation hardness assurance". In: *IEEE Transactions on Nuclear Science* 50.3 (June 2003), pp. 552–564.

[189] D. M. Fleetwood, P. S. Winokur, and J. R. Schwank. "Using laboratory X-ray and cobalt-60 irradiations to predict CMOS device response in strategic and space environments". In: *IEEE Transactions on Nuclear Science* 35.6 (Dec. 1988), pp. 1497–1505.

[190] S. C. Witczak, R. C. Lacoe, J. V. Osborn, J. M. Hutson, and S. C. Moss. "Dose-rate sensitivity of modern nMOSFETs". In: *IEEE Transactions on Nuclear Science* 52.6 (Dec. 2005), pp. 2602–2608.

[191] M. R. Shaneyfelt, J. R. Schwank, S. C. Witczak, D. M. Fleetwood, R. L. Pease, P. S. Winokur, L. C. Riewe, and G. L. Hash. "Thermal-stress effects and enhanced low dose rate sensitivity in linear bipolar ICs". In: *IEEE Transactions on Nuclear Science* 47.6 (Dec. 2000), pp. 2539–2545.

[192] R. L. Pease, L. M. Cohn, D. M. Fleetwood, M. A. Gehlhausen, T. L. Turflinger, D. B. Brown, and A. H. Johnston. "A proposed hardness assurance test methodology for bipolar linear circuits and devices in a space ionizing radiation environment". In: *IEEE Transactions on Nuclear Science* 44.6 (Dec. 1997), pp. 1981–1988.

[193] R. L. Pease, R. D. Schrimpf, and D. M. Fleetwood. "ELDRS in bipolar linear circuits: A review". In: *2008 European Conference on Radiation and Its Effects on Components and Systems*. Sept. 2008, pp. 18–32.

[194] D. M. Fleetwood, S. L. Kosier, R. N. Nowlin, R. D. Schrimpf, R. A. Reber, M. DeLaus, P. S. Winokur, A. Wei, W. E. Combs, and R. L. Pease. "Physical mechanisms contributing to enhanced bipolar gain degradation at low dose rates". In: *IEEE Transactions on Nuclear Science* 41.6 (Dec. 1994), pp. 1871–1883.

[195] A. H. Johnston, G. M. Swift, and B. G. Rax. "Total dose effects in conventional bipolar transistors and linear integrated circuits". In: *IEEE Transactions on Nuclear Science* 41.6 (Dec. 1994), pp. 2427–2436.

[196] A. H. Johnston, B. G. Rax, and C. I. Lee. "Enhanced damage in linear bipolar integrated circuits at low dose rate". In: *IEEE Transactions on Nuclear Science* 42.6 (Dec. 1995), pp. 1650–1659.

[197] D. M. Fleetwood, L. C. Riewe, J. R. Schwank, S. C. Witczak, and R. D. Schrimpf. "Radiation effects at low electric fields in thermal, SIMOX, and bipolar-base oxides". In: *IEEE Transactions on Nuclear Science* 43.6 (Dec. 1996), pp. 2537–2546.

[198] S. C. Witczak, R. C. Lacoe, D. C. Mayer, D. M. Fleetwood, R. D. Schrimpf, and K. F. Galloway. "Space charge limited degradation of bipolar oxides at low electric fields". In: *IEEE Transactions on Nuclear Science* 45.6 (Dec. 1998), pp. 2339–2351.

[199] S. N. Rashkeev, C. R. Cirba, D. M. Fleetwood, R. D. Schrimpf, S. C. Witczak, A. Michez, and S. T. Pantelides. "Physical model for enhanced interface-trap formation at low dose rates". In: *IEEE Transactions on Nuclear Science* 49.6 (Dec. 2002), pp. 2650–2655.

[200] H. P. Hjalmarson, R. L. Pease, S. C. Witczak, M. R. Shaneyfelt, J. R. Schwank, A. H. Edwards, C. E. Hembree, and T. R. Mattsson. "Mechanisms for radiation dose-rate sensitivity of bipolar transistors". In: *IEEE Transactions on Nuclear Science* 50.6 (Dec. 2003), pp. 1901–1909.

[201] A. Nikolaou, M. Bucher, N. Makris, A. Papadopoulou, L. Chevas, G. Borghello, H. D. Koch, K. Kloukinas, T. S. Poikela, and F. Faccio. "Extending a 65nm CMOS process design kit for high total ionizing dose effects". In: *2018 7th International Conference on Modern Circuits and Systems Technologies (MOCAST)*. May 2018, pp. 1–4.

[202] L. Chevas, A. Nikolaou, M. Bucher, N. Makris, A. Papadopoulou, A. Zografos, G. Borghello, H. D. Koch, and F. Faccio. "Investigation of scaling and temperature effects in total ionizing dose (TID) experiments in 65 nm CMOS". In: *2018 25th International Conference" Mixed Design of Integrated Circuits and System"(MIXDES)*. IEEE. 2018, pp. 313–318.

[203] M. Bucher, A. Nikolaou, A. Papadopoulou, N. Makris, L. Chevas, G. Borghello, H. D. Koch, and F. Faccio. "Total ionizing dose effects on analog performance of 65 nm bulk CMOS with enclosed-gate and standard layout". In: *2018 IEEE International Conference on Microelectronic Test Structures (ICMTS)*. Mar. 2018, pp. 166–170.

[204] A. Nikolaou, M. Bucher, N. Makris, A. Papadopoulou, L. Chevas, G. Borghello, H. D. Koch, and F. Faccio. "Modeling of High Total Ionizing Dose (TID) Effects for Enclosed Layout Transistors in 65 nm Bulk CMOS". In: *2018 International Semiconductor Conference (CAS)*. Oct. 2018.

[205] C. C. Enz and E. A. Vittoz. *Charge-based MOS transistor modeling: the EKV model for low-power and RF IC design*. John Wiley & Sons, 2006.

[206] V. Re. *The 65 nm CMOS technology for analog processing in mixed-signal pixel readout circuits*. May 2015. URL: `http://www.in2p3.fr/actions/formation/microelectronique15/IN2P3_2015_Re_65nm.pdf`.

[207] F. Anghinolfi. *65nm Technology Development for electronics in the LHC at CERN*. June 2016. URL: `https://indico.esa.int/event/102/contributions/28/attachments/59/70/AMICSA_4-3_6.pdf`.

[208] ESCC. *ESCC Basic Specification No. 22900*. June 2016. URL: `https://escies.org/webdocument/showArticle?id=229`.

[209] M. L. Alles, R. D. Schrimpf, R. A. Reed, L. W. Massengill, R. A. Weller, M. H. Mendenhall, D. R. Ball, K. M. Warren, T. D. Loveless, J. S. Kauppila, and B. D. Sierawski. "Radiation hardness of FDSOI and FinFET technologies". In: *IEEE 2011 International SOI Conference*. Oct. 2011, pp. 1–2.

[210] F. E. Mamouni, E. X. Zhang, R. D. Schrimpf, D. M. Fleetwood, R. A. Reed, S. Cristoloveanu, and W. Xiong. "Fin-Width Dependence of Ionizing Radiation-Induced Subthreshold-Swing Degradation in 100-nm-Gate-Length FinFETs". In: *IEEE Transactions on Nuclear Science* 56.6 (Dec. 2009), pp. 3250–3255.

[211] E. X. Zhang, D. Fleetwood, F. El-Mamouni, M. Alles, R. Schrimpf, W. Xiong, C. Hobbs, K. Akarvardar, and S. Cristoloveanu. "Total Ionizing Dose Effects on FinFET-Based Capacitor-Less 1T-DRAMs". In: *IEEE Transactions on Nuclear Science* 57.6 (Dec. 2010), pp. 3298–3304.

[212] E. S. Comfort, M. P. Rodgers, W. Allen, S. C. Gausepohl, E. X. Zhang, M. L. Alles, H. L. Hughes, P. J. McMarr, and J. U. Lee. "Intrinsic Tolerance to Total Ionizing Dose Radiation in Gate-All-Around MOSFETs". In: *IEEE Transactions on Nuclear Science* 60.6 (Dec. 2013), pp. 4483–4487.

[213] H. Hughes, P. McMarr, M. Alles, E. Zhang, C. Arutt, B. Doris, D. Liu, R. Southwick, and P. Oldiges. "Total Ionizing Dose Radiation Effects on 14 nm FinFET and SOI UTBB Technologies". In: *2015 IEEE Radiation Effects Data Workshop (REDW)*. July 2015, pp. 1–6.

[214] S. Ren, M. Si, K. Ni, X. Wan, J. Chen, S. Chang, X. Sun, E. X. Zhang, R. A. Reed, D. M. Fleetwood, P. Ye, S. Cui, and T. P. Ma. "Total Ionizing Dose (TID) Effects in Extremely Scaled Ultra-Thin Channel Nanowire (NW) Gate-All-Around (GAA) InGaAs MOSFETs". In: *IEEE Transactions on Nuclear Science* 62.6 (Dec. 2015), pp. 2888–2893.

[215] M. Gaillardin, C. Marcandella, M. Martinez, M. Raine, P. Paillet, O. Duhamel, and N. Richard. "Total ionizing dose effects in multiple-gate field-effect transistor". In: *Semiconductor Science and Technology* 32.8 (2017), p. 083003.

[216] M. Benedikt. "Future Circular Collider Study". In: (May 2014). URL: http://cds.cern.ch/record/2206380.

[217] A. Ball, M. Benedikt, L. Bottura, O. Dominguez, F. Gianotti, B. Goddard, P. Lebrun, M. Mangano, D. Schulte, E. Shaposhnikova, R. Tomas, and F. Zimmermann. *Future circular collider study hadron collider parameters*. Tech. rep. CERN, 2014.

[218] A. Infantino, R. G. Alía, M. Brugger, and F. Cerutti. "Radiation environment assessment in the FCChh and FCCee machines". FCC week 2018. 2018. URL: https://indico.cern.ch/event/656491/contributions/2915679/attachments/1629768/2601671/20180412_INFANTINO_ST_R2E_overview.pdf.

[219] G. Borghello. "FCC radiation environment: an unprecedented challenge for MOS transistors". FCC week 2018. 2018. URL: https://indico.cern.ch/event/656491/contributions/2947274/.

[220] M. P. King, X. Wu, M. Eller, S. Samavedam, M. R. Shaneyfelt, A. I. Silva, B. L. Draper, W. C. Rice, T. L. Meisenheimer, J. A. Felix, E. X. Zhang, T. D. Haeffner, D. R. Ball, K. J. Shetler, M. L. Alles, J. S. Kauppila, and L. W. Massengill. "Analysis of TID Process, Geometry, and Bias Condition Dependence in 14-nm FinFETs and Implications for RF and SRAM Performance". In: *IEEE Transactions on Nuclear Science* 64.1 (Jan. 2017), pp. 285–292.

[221] IRDS. *More Moore*. Tech. rep. IEEE - International Roadmap for Devices and Systems, 2017. URL: https://irds.ieee.org/images/files/pdf/2017/2017IRDS_MM.pdf.