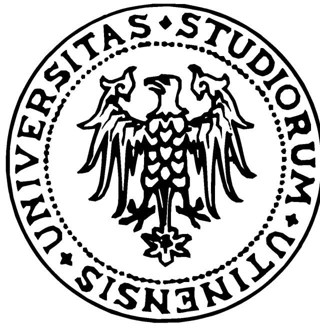

Università degli Studi di Udine
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PhD Thesis

Ferroelectric Negative Capacitance Transistors as Beyond Tunnel-FETs, Steep-Slope Devices: a Modeling, Simulation and Design Study

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Abstract

THE *Internet of Things* (IoT) is one of the most trending businesses of modern times and has already opened a new world of opportunities for academic and industrial research. The IoT concept relies on a huge number of heterogeneous smart devices (i.e. *things*) that can communicate autonomously over the Internet, and also on a solid infrastructure to support the immense amount of data continuously exchanged. Projections on the future of the IoT suggest a number of connected devices amply overcoming 50 billion within ten years, and with a predicted cost in terms of electricity consumption of over the 20% of the world energy demand.

In this context, IoT needs to be energy efficient under several aspects: for example by reducing the power consumption of each node of the smart grid and in the big data centers, and even by developing advanced software tools to nimbly manage the fluxes of information. For these reasons different branches of electronic engineering can contribute to solve the overall efficiency issue.

This thesis addresses the problem from a nano-electronic perspective, analyzing possible solutions to limit the power dissipation in digital integrated circuits (ICs), in particular at the transistor level. In fact, in the last twenty years different strategies have been proposed to limit energy consumption in ICs but, due to some physical limitations of conventional Complementary Metal-Oxide-Semiconductor (CMOS) technology, an effective solution is still missing.

The main avenue to lower power dissipation in ICs has been for years the reduction of supply voltage V_{DD}, according to a *Dennardian scaling*, but for modern scaled devices this cannot be done any more without encountering important drawbacks in terms of process, voltage and temperature (PVT) variability. This led to an era known as *Dark Silicon* age, where a substantial area of a chip is kept underclocked or underpowered to meet power constraints, thus meaning that the full potential performance cannot be exploited and a huge number of devices is wasted. This approach is clearly a palliative and becomes more and more inefficient at each technology node as the number of devices approximately doubles inside the chip, so that is has become important to improve the energy efficiency at transistor level.

To address the problem from a device perspective, we need to consider

the two main contributions to the total energy dissipation: the dynamic and the standby energy. The first contribution scales quadratically with V_{DD}, but at very low V_{DD} the standby energy becomes the most critical contribution, which is related to the sub-threshold-swing of the current-voltage relation: the steeper the characteristic is, the lower the leakage current. Unfortunately, the conventional CMOS technology has a limitation under this perspective due to the thermionic-emission transport mechanism that physically restricts the lowest possible swing.

The investigation of new device concepts that can overcome this limit is an active and challenging field of research for modern electronics, and two of the most interesting technologies in this sense are the *Tunnel FET* (TFET) and the *Negative-Capacitance* transistor (NC-FET). In this thesis we focus on the promising NC-FET concept, which integrates *ferroelectric* materials in the gate-stack to improve both the on- and the off-state performances of the transistor.

In this work we present an extensive study on the negative-capacitance feature in ferroelectrics, according to the Landau-Khalatnikov theory, and investigate several original designs for ferroelectric NC-FETs in order to reduce energy consumption in ICs. Moreover, a comparison against experiments is carried out in order to validate our results and in the last chapter the sensitivity of NC-FETs to temperature, process variations and interface defects are also examined.

Terminology

Abbreviations and acronyms

BTBT	Band-to-Band Tunneling
CB	Conduction Band profile
CMOS	Complementary Metal-Oxide-Semiconductor
DG	Double Gate
DIBL	Drain-induced Barrier Lowering
DOS	Density of States
FeFET	Ferroelectric FET
FET	Field Effect Transistor
HH	Heavy Holes band
IoT	Internet of Things
LH	Light Holes band
MOSFET	Metal-Oxide-Semiconductor FET
NC-FET	Negative Capacitance FET
PAT	Phonon-Assisted Tunneling
SCE	Short Channel Effect
SRH	Shockley-Read-Hall
SS	Sub-threshold Swing
TFET	Tunnel FET
UTB	Ultra Thin Body
VB	Valence Band profile
WKB	Wentzel-Kramers-Brillouin

Symbols

a_0	Lattice constant	m
E_C	Conduction band energy	J
E_F	Fermi Level	J
E_V	Valence band energy	J
E_G	Energy gap	J
$\mathbf{k}$	Wave-vector	1/m
L_G	Channel Lenght	m
$n(z)$	Volumetric electron carrier density	$1/\mathrm{m}^3$
λ	Natural Lenght	m

Physical constants

h	Planck's constant	6.62607×10^{-34} Js
$\hbar$	Reduced Planck's constant	$h/(2\pi)$
K_B	Boltzmann's constant	1.38065×10^{-23} JK^{-1}
m_0	Electron rest mass	9.10938×10^{-31} Kg
q	Positive electron charge	1.60217×10^{-19} C
ε_0	Vacuum permittivity	8.85419×10^{-12} $\mathrm{CV}^{-1}\mathrm{m}^{-1}$

Index

Abstract **iii**

Terminology **v**

1 Introduction **1**
- 1.1 General context: the IoT era . . . 1
- 1.2 Energy efficiency in CMOS technology . . . 6
- 1.3 Rationale behind steep-slope transistors . . . 8
- 1.4 Structure and purpose of this work . . . 11

2 Tunnel FETs **13**
- 2.1 Intuitive working principle . . . 13
- 2.2 Modeling of BTBT . . . 15
  - 2.2.1 Direct BTBT in semiconductors . . . 16
  - 2.2.2 Indirect BTBT in semiconductors . . . 19
- 2.3 State of the art - TFET Technologies . . . 19
  - 2.3.1 Silicon TFETs . . . 20
  - 2.3.2 Simulation of strained-silicon TFET . . . 20
  - 2.3.3 III-V semiconductors TFETs . . . 24
- 2.4 Essential physics of the off-state operation of FETs . . . 25
  - 2.4.1 Semi-analytical models for the electrostatics and the off-state current . . . 26
  - 2.4.2 Off-current minimum and SS . . . 27
- 2.5 Final remarks and perspectives for TFETs . . . 29

3 Negative Capacitance in ferroelectrics **33**
- 3.1 Ferroelectric materials . . . 33
  - 3.1.1 Ferroelectric oxides . . . 36
- 3.2 Physical models for ferroelectrics . . . 37
  - 3.2.1 Landau-Khalatnikov (LK): homogeneous model . . . 37
  - 3.2.2 Landau-Ginzburg theory: inhomogeneous model . . . 41
  - 3.2.3 Preisach model . . . 42
- 3.3 Numerical models for dynamic LK equations . . . 44
- 3.4 Stabilization of ferroelectrics and negative capacitance . . . 47
- 3.5 Energetic behavior of NC devices . . . 49

3.6 Experimental evidence of negative capacitance 52

4 Ferroelectric Negative-Capacitance FETs 59

4.1 Modeling of the NC-FETs 59

4.1.1 Quantum effects and electrostatics 61

4.1.2 A simple transport model 64

4.1.3 Interface traps 67

4.1.4 Numerical solution of the model system 70

4.2 Calibration against experiments 72

4.3 State-of-the-art of experimental NC devices 76

5 NC-FETs Design 81

5.1 Design space for NC-FETs 84

5.2 Focus on the off-state operation: steep-slope devices . . . 85

5.3 Focus on the on-state operation: g_m-boosted devices . . . 90

5.4 Role of interface traps 95

5.5 Sensitivity and variability 101

6 Conclusions and future perspectives 111

6.1 Summary of the work 111

6.2 Future outlook 113

A The Pseudo Spectral method 115

B List of Publications 123

List of Figures

1.1 Pictorial view of IoT 1
1.2 2010 IoT roadmap 2
1.3 SENSE table: differences between IoT and "old" Internet 3
1.4 Growth of IoT device number 5
1.5 Delay time T_D versus V_{DD} for CMOS technology 8
1.6 Sketch of energy trends in CMOS technology 9
1.7 Sketch of the I-V characteristic of a steep-slope device . . 9

2.1 Conventional n-MOSFET bands profile and a sketch of a DG device 14
2.2 Sketches of direct and indirect bandgap semiconductors . 15
2.3 Sketch of the two-band Kane's model 17
2.4 Plot and fitting of real and imaginary bands in unstrained silicon 21
2.5 Hole effective masses and related energy-gaps 22
2.6 Comparison of generation rates versus maximum electric field in Si-TFETs 25
2.7 I_{DS} versus V_G at V_{DS}=0.3V of an InAs NW TFET . . . 28
2.8 TFET band-structure referring to figure 2.7 28
2.9 SS versus L_G/λ_n ratio for III-V TFETs and MOSFETs . 29
2.10 Experimental TFET characteristics: state-of-the-art 31

3.1 Sketch of $BaTiO_3$ crystal cell in different phases 34
3.2 Experimental hysteretic characteristics from [1] of ferroelectric Si-doped HfO_2 35
3.3 Energy-polarization relations for ferroelectric and paraelectric materials 39
3.4 Example of static and dynamic P-V relations for ferroelectric HfO_2 40
3.5 Sketch of the ideal switch of the Preisach model 43
3.6 Preisach model bloch diagram and example of output . . . 44
3.7 Discrete inhomogeneous ferroelectric representation for numerical computation 45
3.8 Field-polarization curves comparison beteween multi- and single-domain approaches 47

3.9 Negative capacitance as a positive feedback: sketch and block diagram 48
3.10 Setup for the demonstration of NC stabilization 48
3.11 Numerical setup for the analysis on the energies 50
3.12 Free Gibb's energy relation for a retrograde NC-FET . . 53
3.13 Voltage-charge relations for a retrograde NC-FET 53
3.14 Setup used by Khan to demonstrate experimentally negative capacitance 54
3.15 Experimental results by Khan on the evidence of negative capacitance 55
3.16 Experimental results by Appleby on the evidence of negative capacitance 56
3.17 Experimental evidence for negative capacitance behavior by Hoffmann 57

4.1 Sketch of the simulated DG transistor 59
4.2 Band diagram in quantization direction of the DG-FET . 60
4.3 Diagram of the Schrödinger-Poisson solver 61
4.4 Equivalent circuit of NC-FET with SCE model 63
4.5 I-V characteristic of a DG MOSFET with SCE 65
4.6 Transport model: band diagram in the direction x 65
4.7 Bandstructure and intuitive SRH recombination mechanism 67
4.8 Frequancy-energy relation for trap's emission rates 69
4.9 Calibration of LKE coefficients against experiments [2] . 73
4.10 Comparison between numerical and experimental [3] IV characteristics 75
4.11 Experimental P-F characteristic for 10nm $HfYO_x$ [4] . . 76
4.12 Measured I-V curves for a NC-FET from [4] 77
4.13 Experimental results from Globalfoundires [3] on NC-FETs 78

5.1 DG-UTB NC-FET architecture and its equivalent electrostatic circuit 82
5.2 Transfer characteristics of the baseline transistor 83
5.3 Qualitative sketch of the design space for the NC-FETs . 85
5.4 I_{DS}-V_G curves for a stepp-slope NC-FET design and for different T_{Fe} 87
5.5 Capacitance versus polarization P for a steep-slope NC-FET 88
5.6 Sketch of a bulk retrograde ferroelectric NC-FET 89
5.7 Retrograde doping profile for simulated NC-FET and depletion widths 90
5.8 I-V and C-V characteristics for the retrograde NC-FET . . 91
5.9 Capacitances and voltage drops versus V_G for a g_m-boosted NC-FET 92
5.10 Conductance versus V_G curves for a g_m-boosted device . 93
5.11 Oxide field versus V_G for a g_m-boosted NC-FET 94

5.12 NC-FET design space for T_{Fe} and temperature 95
5.13 Equivalent capacitive network for the NC-FET with interface traps 96
5.14 Influence of interface traps on g_m-boosted NC-FETs . . . 98
5.15 Influence of interface traps on steep-slope NC-FETs . . . 98
5.16 Corresponding capacitances $|C_{di}|$ (with negative C_{di}) and $[C_{sct}+C_{it}]$ versus charge density Q. The crossing points between $[C_{sct}+C_{it}]$ and $|C_{di}|$ correspond to the forward and backward switching points of the hysteresis highlighted in figure 5.15 for the case of trap density D_{it}=3·10^{12} cm^{-2}/eV. The shape of the capacitance in the sub-threshold region is coherent with a static Fermi-Dirac distribution of traps in the energy-gap that extends till the first subband of the CB. 99
5.17 I_{DS}-V_G curves for a steep-slope NC-FET obtained with the dynamic SRH trap model 100
5.18 Occupation probability P_t for traps at 100MHz in a NC-FET 101
5.19 Design space: C_{di} versus thicknesses T_{Fe} and T_{ox} 103
5.20 Design space: g_m-boosted gain G versus T_{Fe} and P_r/F_C ratio 104
5.21 Sensitivity: g_m-boosted NC-FET I-V characteristics for different EOTs 105
5.22 Sensitivity: NC-FET I_{ON} boosting versus EOT and T_{Fe} . 106
5.23 Sensitivity: polarization versus field of Si:HfO_2 at different temperatures 107
5.24 Sensitivity: I-V characteristics of NC-FETs at different temperatures 108
5.25 Sensitivity: Q_{T0} versus T_{Fe} and a_0 curves 109

A.1 Sketch of the Chebyshev 1D discretization grid 117
A.2 Sketch of an heterogeneous domain discretized with Chebyshev points. The two domains share the same boundary point b, that corresponds to the superposition of the coordinates x_{α,N_α} and $x_{\beta,0}$. 119

List of Tables

2.1 Contribution of different tunneling paths to the generation rates in [mA/μm^2/V] reported in figure 2.6 for unstrained and (001) 1% strained silicon. 24

4.1 LKE coefficients extracted from experimental P-F characteristics with the proposed procedure. 74

5.1 LKE coefficients extracted from experimental P-F characteristics in [2] and used in figure 5.4. 87

Chapter 1

Introduction

"The global industrial sector is poised to undergo a fundamental structural change akin to the industrial revolution as we usher in the IoT. Equipment is becoming more digitized and more connected, establishing networks between machines, humans, and the Internet, leading to the creation of new ecosystems that enable higher productivity, better energy efficiency, and higher profitability."

Goldman Sachs, *The Internet of Things: The Next Mega-Trend*, 2014

1.1 General context: the IoT era

FIGURE 1.1. Pictorial view of the IoT network: all the devices are connected to the same grid and communicate with each other through the internet. The data are shared and elaborated autonomously by data centers and by the *cloud*.

THE original term *IoT*, which is an acronym for *Internet of things*, was first presented to the world during a presentation at Procter & Gamble in 1999 by Kevin Ashton, a British technologist working at the

MIT. In his presentation he showed how the Radio-frequency Identification (RFID) could be considered as an enabling technology for efficient and effective communication between computers and surrounding things [5,6].

We can try to describe IoT as a convergence of multiple technologies, in particular a network of different and heterogeneous electronic devices that can cooperate with one another on the internet, interacting with the surroundings through sensors and actuators, gathering and exchanging data in a cooperative manner (see the illustration in figure 1.1). Nowadays the IoT embraces several aspects of modern technologies and has been introduced in many aspects of everyday life, including consumer applications in automotive, home automation and wearables, medical and healthcare applications (often called *Smart Healthcare*), transportation systems, manufacturing and agriculture. The roadmap of IoT, illustrated in figure 1.2, is still an open path continuously evolving, but important goals can be identified as the increase of the energy efficiency of all the systems connected to the internet, the enabling of new services and benefits in terms of health, safety or environment.

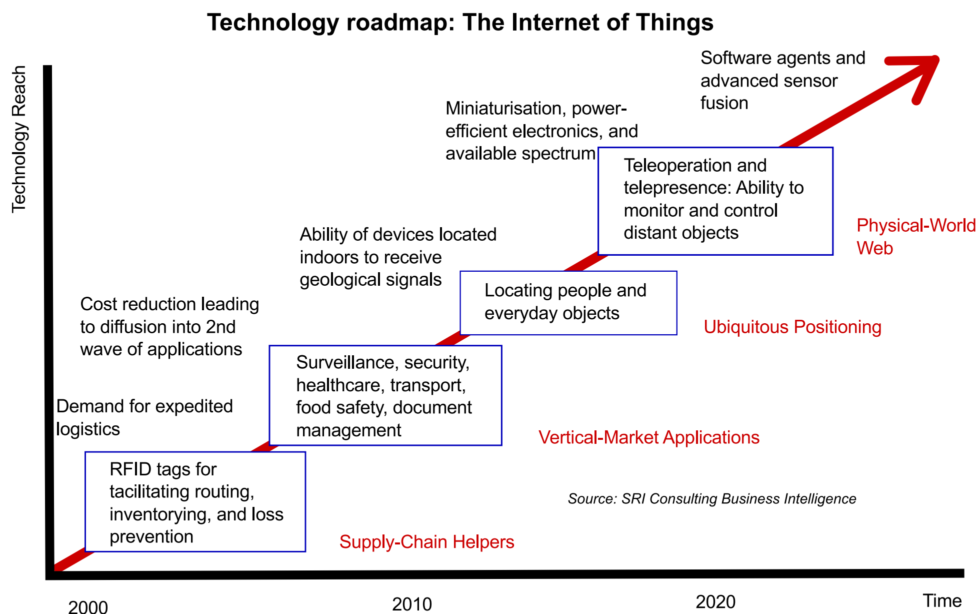

Figure 1.2. IoT roadmap, created in 2010, with projections for the next years: evolution of enabling technologies, expectations and main goals are also reported [7].

Not without a reason the advent of IoT is usually defined as the *third wave* (i.e. a milestone) in the development of the internet [8] and it is expected to deeply change the technology landscape. To put this in the correct perspective, the *first wave* has been identified as the time when the fixed-line internet connected over a billion users in the nineties, while

S-E-N-S-E	IoT features	Differences with 'old' Internet
SENSING	Leverages sensors attached to things (e.g. temperature, presure, acceleration, etc.)	More data generated by sensors than people
EFFICIENT	Adds intelligence to manual process to reduce power consumption	Extends the Internet productivity gains to things, not only people
NETWORKED	Connects objects to the network	Some of the intelligence shifts from the cloud to the network's edge
SPECIALIZED	Customizes technology and process to specific purposes	Unlike general purpose PCs and smartphones, the IoT is very fragmented
EVERYWHERE	Deployed pervasively (e.g. on the body, cars, homes, cities, etc.)	Ubiquitous presence with an order of magnitude more devices (with more security issues)

FIGURE 1.3. In this table are summarized the five main differences between the IoT and the "old" internet concept (related to the previous *waves*) [8]. The most evident difference, essentially, is the shift towards a internet where the larger part of connections and exchanges of data happen between things instead of people.

the *second* arrived in years 2000 when mobile connections reached over two billions people. Figure 1.3 marks well the difference between the old and the new perceived concept of internet, highlighting the five most distinctive aspects.

The original idea of networks collecting smart devices has older roots. In fact in the 1982 a group of students at the Carnegie Mellon University, for an internal project, connected a modified Coke-machine to the internet: this was the first internet-connected appliance able to report its status remotely [9]. During the following years, and thanks also to the development of the idea of *ubiquitous* and *cloud computing*, this breakthrough in the technology started to acquire the shape of the contemporary vision of IoT [10–12], gaining importance in the academic world and also starting to attract the interest of big companies, such as Cisco Systems [13]. To further support the fact that the IoT is becoming a driving business for the future, also the Goldman Sachs investigated this industrial trend and reported that the IoT is going to strongly affect the world economy, as it is considered one of the most relevant opportunities for tech companies nowadays, with an expected value on the financial markets of $2 trillion by 2020 [8].

Another prospect that figure 1.3 suggests is that tech companies have to massively invest in several directions to realize such a vast network of efficient smart devices: from key enabling technologies, to the creation of suitable infrastructures, to software development. For *key enabling technologies* we define all the devices and the basic concepts that can start and drive an innovation in a technology framework and can embrace

a large number of subjects. For example, as the IoT relies on a distributed grid of miscellaneous sensors, new branches of academic and industrial research are required to open new possibilities in the field of sensing: examination of exotic materials (e.g. particular dichalcogenides [14] and graphene configurations [15]) and design of advanced sensors (for instance, biosensors made with nanocapacitor arrays for particles detection [16]) are currently active and fruitful fields. Furthermore, a new set of infrastructures is mandatory to effectively support the enormous amount of information provided by the grid, in terms both of data centers and communication networks. Finally, together with the hardware progress, it is in high demand the development of powerful software tools for *Big Data* analysis, to facilitate the exchange of information and improve the security of information systems. The safety of such an extended network, in particular, is one of the main concerns for all engineers and software developers: the fact that everyone is surrounded by connected smart devices may threaten our personal sensitive information and privacy, if the devices and the data are not effectively protected [17].

However, from the large number of presented opportunities for scientific research, companies and world economy will also derive some relevant issues and drawbacks that cannot be neither neglected nor easily solved: on top of these concerns we have the energy efficiency-related problems [18, 19] .

Energy efficiency of IoT

Even if IoT inherently makes use of a low-power technology, the number of connected devices is rocketing and it is expected to exceed 50 billion in the next years [13, 20]. Moreover, bigger data centers are required to manage all the information provided by the smart grid and, for these reasons, by 2025 the whole system is expected to absorb over the 20% of the world electricity [21].

It is easy to understand that, from the perspective of electronic engineers, these problems can be addressed from different angles: for instance, we can improve energy efficiency of each circuit, that is a more *nanoelectronics* perspective, or we can enhance the power supply management, which is a *power-electronics* approach. The latter, in particular, has to solve the issues concerning both the big data factories, where innovative and effective voltage converters are mandatory [22], and the management of power supply for each node of the network, where battery with enhanced capabilities would be helpful [23]. A promising topic related to these aspects, which needs more research work, is the *energy-harvesting* concept. The basic idea behind energy harvesting is to recover from the

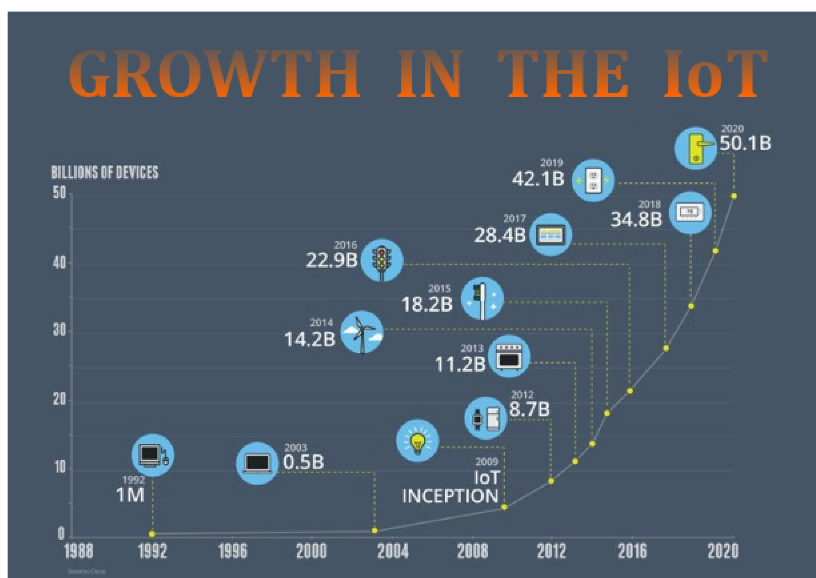

FIGURE 1.4. Trend and expected growth of the number of devices of IoT in next years (from Cisco Reports [13]).

environment energy from different sources, an energy which would be otherwise wasted, and re-utilize it thanks to specific devices [24–26]. This can, in principle, limit the demand of large batteries or fixed power supplies. However, for now, the amount of energy obtained from scavenging is very small, making it difficult to fulfill alone the energetic demands of IoT.

Moving to the nanoelectronic viewpoint, the IoT pushes towards innovative solutions to reduce power consumption in integrated circuits, in particular one of the most challenging aspects is to reduce power directly at the transistor level. This requires the investigation of new device concepts that go beyond the Complementary-Metal-Oxide-Semiconductor (CMOS) technology. According to the IRDS roadmap [27] this research field belongs to the so called $Beyond\ CMOS\ More-Moore$ framework. In recent years a lot of new transistor types have been proposed, exploiting different materials (e.g. III-V group semiconductors, graphene or dichalcogenides), new device architectures (e.g. FinFETs, GAA or nanowires), physical working principles (e.g. band-to-band tunneling, negative-capacitance or junctionless). The silicon-based CMOS technology, however, still is the workhorse of modern consumer electronics.

To better understand the problems of power consumption in transistors, in the next section we discuss the main strategies adopted to limit energy dissipation in conventional modern CMOS digital circuits.

1.2 Energy efficiency in modern CMOS technology

The strategies for the reduction of energy demand in modern CMOS ICs are challenging because, as it will be discussed in the next sections, there are some physical limitations due to the silicon technology itself that are hard to overcome. For several years the most adopted and convenient solution was to manage the energy consumption at chip-level, instead of replacing CMOS devices with new specific low-power transistors. The main idea was essentially to keep on increasing the density of transistors inside the chip to improve performance but, at the same time, to meet power constraints by using clock gating or dynamic voltage scaling techniques [28]. As a result of this approach, at any given time, it was necessary to keep a large part of the chip in idle or under-clocked mode. This approach, that limits the full chip performance due to energy reasons, led to the *Dark Silicon* age [29] and, unfortunately, it tends to create a large inefficiency at system level. For every technology node, in fact, the number of devices inside the chip was expected to double, as predicted by the Moore law, but this would also lead to larger areas to be kept idle. It is clear that this solution cannot be pursued any further, so that improving the energy efficiency at the transistor level becomes a mandatory objective.

In order to discuss energy efficiency at device level, it is appropriate to analyze the main contributions to power dissipation in modern CMOS technology integrated circuits. There are several terms contributing to the total power consumption in digital ICs: we have power due to the switching of interconnections, and terms intrinsic of the transistors. We here focus on the two terms due to transistor switching and transistor leakage. We will refer to these power terms as *dynamic* and *static* respectively.

The dynamic power P_{dyn} of a digital gate is the term of dissipation due to its switching activity, thus it will intuitively depend on the switching frequency of the circuit. In fact we can write P_{dyn} as

$$P_{dyn} = \alpha_{0\rightarrow 1} f C_L V_{DD}^2 \tag{1.1}$$

where $\alpha_{0\rightarrow 1}$ is the switching probability of the gate working at the frequency f, C_L is the load capacitance and V_{DD} is the power supply voltage. This formula suggests that the corresponding energy per operation (obtained by integrating P_{dyn} over the time necessary to perform the operation), can be reduced linearly by lowering the switching activity or quadratically by reducing the supply voltage.

The static energy E_{st}, on the other hand, has a more involved de-

pendence. We can actually evaluate the static power according to the following system

$$E_{st} = I_{off} T_D V_{DD} \tag{1.2a}$$

$$I_{off} \simeq I_{Sth} \cdot \exp\left(\frac{-2.3 \cdot V_T}{SS}\right) \tag{1.2b}$$

$$T_D \simeq \frac{C_L V_{DD}}{2 I_{on}(V_{DD})} \quad . \tag{1.2c}$$

System (1.2) contains the supply voltage, the nominal value of the off-current I_{Sth} and the value of the I_{off} current, which has itself a dependence on the threshold voltage V_T of the transistor and on the SS coefficient. T_D is the elementary delay of the digital gate and is expressed in terms of the effective load capacitance C_L, V_{DD} and the on-state current I_{on} [30]. The I_{on} used in the third equation of (1.2) is an approximation for the saturation current in the sub-threshold region and depends inversely on the exponential of V_{DD}: this degrades T_D with the V_{DD} scaling at fixed V_T, as can be seen in figure 1.5 for values lower than V_T. The SS coefficient, that is the *subthreshold-swing* and is defined as the inverse of the slope s of the I-V characteristic in semi-logarithmic scale, is further discussed in the following sections and plays an important role in the reduction of the total energy consumption.
This behavior can be qualitatively explained as follows: if we want to limit the static energy by reducing the operative V_{DD} of the transistor, the delay time will increase exponentially in the sub-threshold, as can be seen in figure 1.5. For this reason, if we want to reduce V_{DD} and maintain a given delay T_D, then we should reduce also the threshold voltage V_T but, according to the second equation of 1.2, this heavily effects the I_{off} current, making it increasing exponentially. This detrimental effect on the I_{off} due to the V_{DD} reduction will eventually tend to rocket the static energy contribution.

The total energy consumption per clock E_{tot} in a conventional digital CMOS technology is mainly due to the sum of those two contributions, thus E_{tot}=E_{st}+E_{dyn}, and the most interesting fact is that the energy versus V_{DD} relation has a non-monotonic behavior. The energy-voltage relation in figure 1.6 shows a minimum at V_{OPT} and this is essentially due to the increase of E_{st} that is in turn produced by the growth of the delay time T_D when V_{DD} is reduced below V_T. It is understood that in the energy versus V_{DD} plots, as in figure 1.6, the clock frequency decreases when the voltage supply is scaled, and it is also interesting to note that the minimum of energy typically occurs in sub-threshold, where T_D depends exponentially on V_{DD}. We want to remark that is the presence of the leakage that sets a minimum to the total energy, otherwise the energy per cycle would be a monotonic expression of V_{DD}.

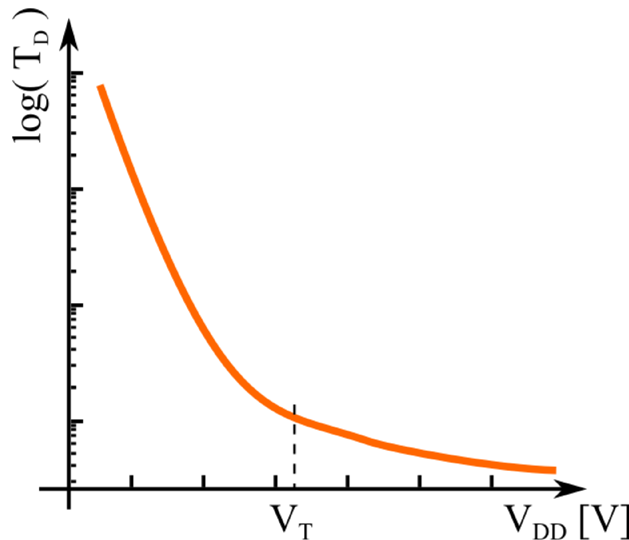

FIGURE 1.5. Illustration of the dependence of time delay T_D in equation 1.2 versus the supply voltage V_{DD}: the exponential increase of T_D when scaling V_{DD} is clearly visible below V_T and it is the reason for the growth of E_{st} in the sub-threshold condition.

From a device design perspective, limiting the static energy to reduce the total energy dissipation offers a lot of new opportunities: in fact it is possible to engineer new types of transistors for low-power applications with competitive performances (compared to traditional CMOS devices). A path to enable these low-power technologies is to focus on the SS parameter in the second equation of (1.1), which governs the steepness of the I-V characteristic in the sub-threshold region: in fact, reducing the SS allows a transition from the off-state to the on-state with a smaller voltage swing. As it can be seen, the reduction of V_{DD} is an important step for leakage energy suppression and it is further discussed in the next section.

1.3 Rationale behind steep-slope transistors

The reduction of SS, as depicted in figure 1.7, can in principle be used to achieve very low I_{off} and static energy, and also keep the dynamic performances intact, preserving a high value for the on-state current I_{ON}. The design of such a transistor concept is extremely challenging due to some physical limitations, in fact conventional CMOS transistors have a lower limit on the SS due to *thermionic emission*. This mechanism, as the name may suggest, relies on the emission of electrons from source above the maximum of the potential energy profile in the channel region, thanks to the thermal tail of the electron Boltzmann energy distribution

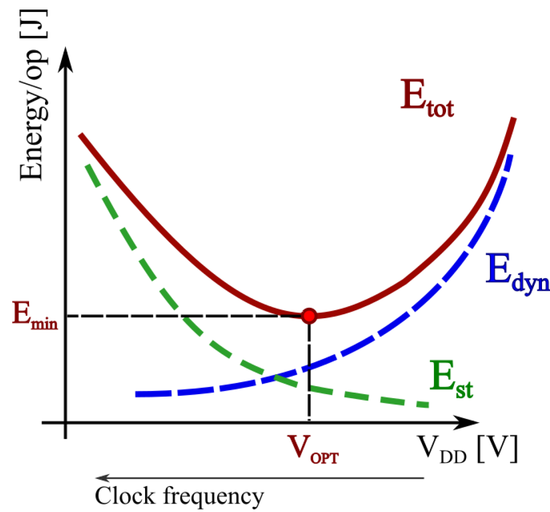

FIGURE 1.6. Sketch showing the trends of the static E_{st} and the dynamic E_{dyn} energies versus V_{DD}. The total energy E_{tot}=E_{st}+E_{dyn} per operation is reported, which shows a minimum at a specific supply voltage V_{DD}=V_{OPT} [31]. It is assumed that the clock frequency scales with V_{DD}. Different circuits that have been investigated experimentally showed values of V_{OPT} in the range of 300-400mV. [32–34]

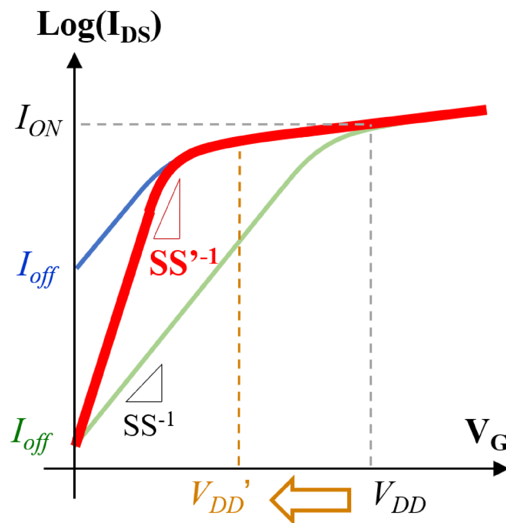

FIGURE 1.7. Sketch of the I-V characteristic of a possible steep-slope device (red) compared to the I-V curves of conventional devices (green and blue are the same as curves in figure 1.5). The steep-slope device allows a V_{DD} and V_T scaling without the exponential increase of the off-state current.

inside the source region [35, 36]. To understand the effect of temperature on the SS parameter we need to analyze a simple definition of SS [35] for a conventional CMOS FET:

$$SS = \left(\frac{d(\log_{10} I_{DS})}{dV_G} \right)^{-1} = ln(10)\, \frac{K_B T}{q} \cdot m \tag{1.3a}$$

$$m = \left(1 + \frac{C_{sct}}{C_{ox}} \right) \tag{1.3b}$$

where the C_{sct} and C_{ox} are the semiconductor capacitance below the gate stack and the oxide capacitance, respectively, while the other parameters have their standard meaning. The presence of the logarithm and of the term $[K_B T/q]$ comes from the derivative with respect to V_G of the current, which in turn stems from the thermionic emission. The parameter m is a sort of body-factor depending on the architecture of the device and is larger than one as it is given by a capacitance ratio.

Even if it is possible to manage the design of the device to make the capacitance ratio as small as possible, the term $[ln(10)K_B T/q]$, which is approximately equal to 60mV/dec at room temperature (i.e. T=300K), relies only on physical constants and on the temperature T. This condition essentially translates into a fundamental lower limit for SS. In fact at room temperature conventional MOSFETs cannot achieve swings lower than 60mV/dec, whereas the SS can be substantially degraded by defects and poor electrostatic control.

In order to enable transistors with SS smaller than the thermal limit, that is a task also known as overcoming the *Boltzmann's tyranny*, it is important to investigate different physical mechanisms to replace thermionic emission: this family of devices is called *steep-slope transistors*. For several years electron devices community has focused its attention on substituting the transport mechanism to flee from the Boltzmann's limitations: one of the main objectives was to replace the thermionic emission with band-to-band tunneling [37], that is not limited by the tails of the Boltzmann's distribution (see chapter 2). The TFET concept has been investigated for a long time but, due to some fundamental as well as design challenges, the interest for this type of transistor has been partially obscured by new device concepts. Quite recently, for example, some promising solutions have been proposed to reduce the m factor in equation 1.3b below one, as an alternative means, compared to changing the transport mechanism, to reduce SS below 60mV/dec. In this framework, in particular, the use of new materials as gate dielectrics, such as *ferroelectric* materials [38], has attracted a lot of attention in the electron device community [39–43].

The research on steep-slope devices is nowadays a dynamic research field and it offers a lot of challenges in terms of trade-off solutions between dynamic performance and energy efficiency. In this PhD project we focused on one of the most recent and innovative device concept that aims to reduce the body-factor m thanks to ferroelectrics.

1.4 Structure and purpose of this work

The main goal of this thesis is to present, investigate and model new device concepts for nanoscale transistors that can improve energy efficiency of digital circuits, compared to a conventional CMOS technology. In particular the design guidelines for such devices are focused either on the improvement of the off-state (enabling an SS below 60mV/dec), or on the on-state, and in particular on trasconductance and on-current. One of the most promising technology in this framework is the ferroelectric *negative-capacitance* FET: we present here an effective approach to model the behavior of such a device. Moreover, with the support of numerical simulations, we also discuss the best design strategies for respectively the off- or the on-state.

This is the organization of the thesis: chapter 2 analyzes one of the most studied steep-slope transistor concepts of the last decade, namely the *Tunnel*-FET (or simply $TFET$). This transistor aims at reducing power consumption in ICs by reducing the sub-threshold swing below the physical limit of 60mV/dec, thanks to the quantum mechanical band-to-band tunneling mechanism along the transport direction. We start from a study on the state-of-the-art of such devices, then we move to report our most important contributions to the device-modeling and, finally, we discuss the future perspectives and the limitations of TFETs.

Starting from the limitations of TFETs, in chapter 3 we introduce the *negative-capacitance* (NC) concept, a physical behavior that can be exploited in transistors to enable low-power operations and reduce power consumption in ICs. As discussed in the same chapter, the NC effect is an interesting property of ferroelectric materials (hereafter $ferroelectrics$), that can be embodied into the gate stack.

In chapter 4 we illustrate the physical models developed during the PhD project, as well as the numerical simulator implemented and used to describe different negative-capacitance devices. In the same chapter we also discuss the methodology for calibration against experiments and discuss the present state-of-the-art of ferroelectric devices.

Chapter 5 reports the design guidelines for different NC-FET concepts, highlighting both the strengths and the weaknesses of the different design strategies. Our analysis of NC-FETs comprised also the sensitivity and variability to dielectric thickness and temperature, addressing also the influence of interface traps in the context of a negative capacitance operation.

The last part of the present thesis presents conclusions and an outlook about the future perspectives for ferroelectric NC-FETs. Some details on numerical models are reported into the appendixes section.

Chapter 2

Tunnel Field Effect Transistors (TFETs)

2.1 Intuitive working principle

ONE of the most innovative and investigated transistor concept of the past ten years [44] is the Tunnel-FET: a CMOS transistor where the current is governed by band-to-band tunneling (BTBT) mechanism instead of thermionic emission. The fundamental idea behind this device is to overcome the limit of 60mV/dec (at room temperature) for the sub-threshold swing (SS) of conventional MOSFETs by replacing the transport mechanism: for a n-type Tunnel-FET, for example, electrons are injected into the channel from the valence band (VB) of the source, rather than from the conduction band (CB).

The TFET has an asymmetric structure (see Fig.2.1(b)), as opposed to the conventional MOSFETs where source and drain terminal can in principle be exchanged (Fig.2.1(a)), and it is essentially a p-i-n junction controlled by a gate-terminal, with possible different architectural solutions (such as double-gate, DG, or gate-all-around, GAA). In a conventional n-type MOSFET, as seen from the left figure 2.1(a), only the conduction band profile $CB(x)$ is relevant for transport: electrons are emitted from source over the top of the CB(x) profile in the channel region and thus contribute the main component of the I_{DS} current, whereas possible tunneling paths through the barrier should be negligible in a well tempered MOSFET (this latter process should not be confused with a BTBT mechanism). When the gate voltage, V_G, is lowered and the energy barrier is raised, I_{DS} is suppressed following the exponential decay of the source occupation function $f(E)$ at high energies. For energies large enough (i.e. higher than the source Fermi level E_{FS}), the occupation function can be approximated with the Boltzmann's distribution, leading to the well known thermal limit of 60mV/dec for SS.

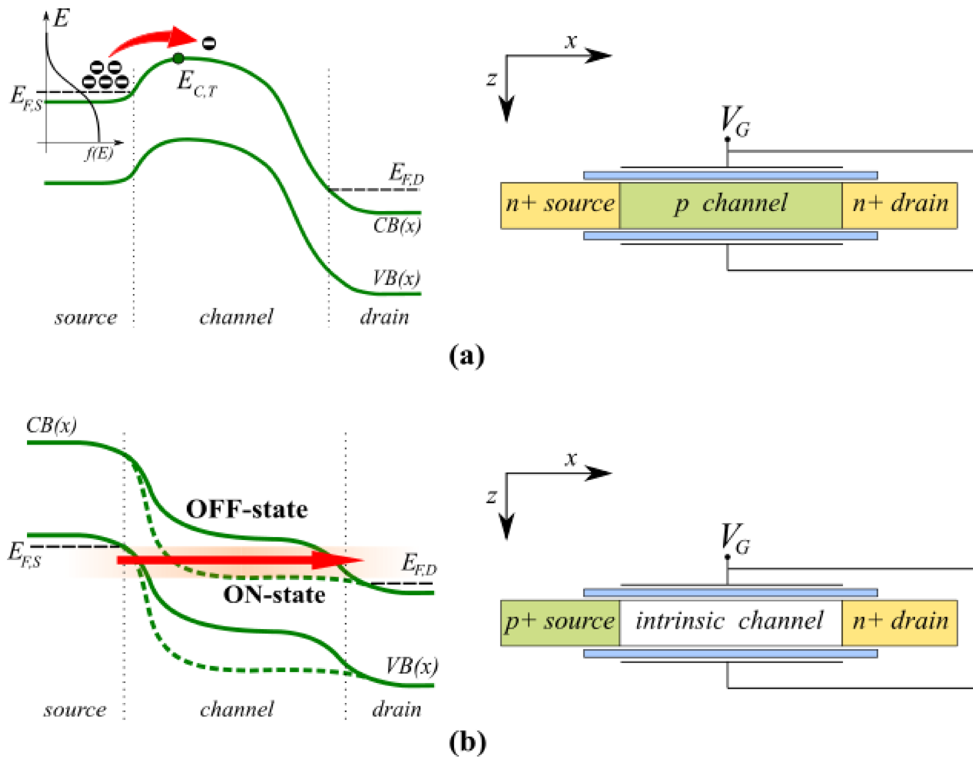

FIGURE 2.1. a) Conventional n-MOSFET conduction and valence band profile (left) and a sketch of a DG device (right). The thermionic emission mechanism is represented by electrons in source region, with a $f(E)$ occupation function and $E_{F,S}$ Fermi level, emitted above the channel top-of-the-barrier $E_{C,T}$. b) At left we have a DG TFET conduction and valence band profile for both on- and off-states (dashed and solid green line respectively) and the sketch of the device is at right: the BTBT mechanism allows the I_{DS} current to run from VB of the source to the CB of drain region.

In an n-type TFET, instead, the current is sustained by the BTBT mechanism: electrons are injected from the valence band of the source into the CB of the channel region, as can be seen in the left figure 2.1(b). The gate voltage V_G moves the channel bands, resulting in an energy filtering mechanism which broadens or reduces the tunneling path through the energy-gap E_G in the transport direction x. The BTBT process is very different from the thermionic emission, as BTBT does not directly depend on the Boltzmann distribution of the electrons at source, and thus the SS can in principle be reduced below 60mV/dec and also be fairly temperature independent.

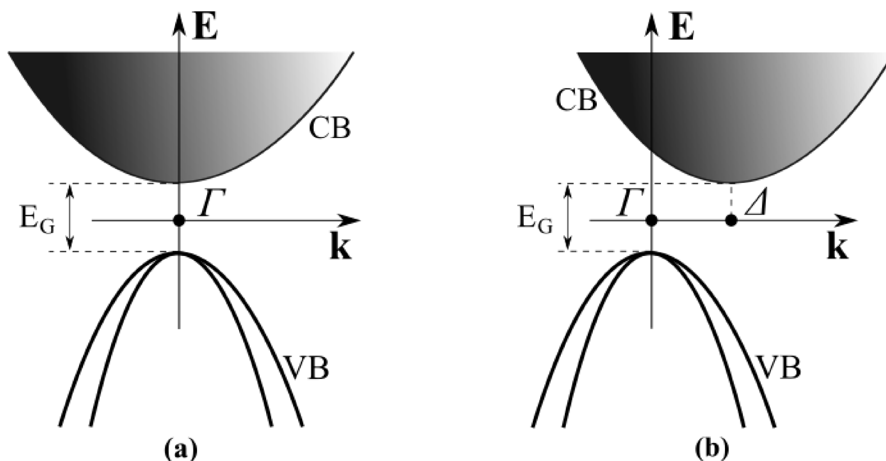

FIGURE 2.2. Simplified sketches of (a) direct and (b) indirect bandgap semiconductors, where the conduction and valence bands are separated by the energy-gap E_G: in the first case the band minima are both positioned at the Γ point, while in the second case the minima are placed at different **k.**

2.2 Modeling of BTBT

In the last decade many models for BTBT have been proposed for a large variety of devices, such as reverse-biased diodes [45, 46], MOSFETs with high drain biases [47, 48] and non-volatile memories (NVM) [49, 50], moreover the development of Tunnel FETs has renewed the interest in the topic, revisiting old models and proposing new ones.

In principle the BTBT mechanism is a purely quantum-mechanical process producing a flux of electrons from the VB to the CB by tunneling through the forbidden energy gap, but from a modeling stand point it can be interpreted as a semi-classical carrier generation mechanism. In this modeling framework a hole and an electron are generated at the extrema of the tunneling path, respectively in the valence and conduction band, giving rise to two currents in opposite directions. While there exist quite many different types of BTBT models, it is possible to write a general expression for the generation rate, $G_T(E)$:

$$G_T(E) = |F|\frac{\Delta J(E)}{\Delta E} \tag{2.1}$$

here ΔJ is the current density, ΔE is the energy window where the process occurs and F is the electrical field present in that region.

There are several possible criteria to divide models into groups, but one a simple criterion is to distinguish between *direct* and *indirect* tunneling mechanisms. The first one occurs when the minimum of the CB and the maximum of the VB of the semiconductor are located both at the same point in the Brillouin zone, usually the Γ point. Such semiconductors

are labelled *direct-bandgap* semiconductors (e.g. III-V compounds, like $InAs$ or $InGaAs$, as can be seen in figure 2.2(a)). Silicon, instead, is a *indirect-bandgap* semiconductor, meaning that the extrema of conduction and valence bands are at different points in the Brillouin zone, in particular they are placed at the Δ and Γ points respectively (Fig. 2.2(b)). The indirect BTBT mechanism is usually a *phonon-assisted* tunneling (PAT) because, as the two band extrema are not located at the same point in the Brillouin zone, a process involving phonons is required to conserve the overall energy and momentum.

In the next sections we describe some of the most used models, in particular for numerical analyses, based on the post-processing of the bandstructure and the wave-functions obtained by solving the Schrödinger equation: we will refer to those models as *non-self-consistent* quantum models [37]).

2.2.1 Direct BTBT in semiconductors

The approach for direct BTBT in semiconductors was originally proposed by Kane in 1959 [45], and here we illustrate it in a slightly different version, using the Landauer conduction formula [51], the WKB approximation and the *local-model* (assuming an approximately constant field along the tunneling path).

Starting from the Landauer model, the current density can be written as:

$$\begin{aligned} J &= \frac{q}{\pi\hbar A}\int_{-\infty}^{\infty}\sum_{\mathbf{k}_\perp} T\left(E,\mathbf{k}_\perp\right)\left[f_\nu - f_c\right]dE \\ &= \frac{q}{4\pi^3\hbar}\int_{-\infty}^{\infty}\int_A T\left(E,\mathbf{k}_\perp\right)\left[f_v - f_c\right]d\mathbf{k}_\perp dE \end{aligned} \tag{2.2}$$

where A is the area perpendicular to the tunneling direction x, $\mathbf{k}_\perp$ is the transverse wave-vector, $T(E,\mathbf{k}_\perp)$ is the transmission coefficient, $f_{(v,c)}$ are the local occupation functions at the extrema of the path (valence and conduction bands) and other symbols have their standard meaning. The generation rate of equation (2.1) can be derived directly from equation (2.2) for a given structure. The transmission probability, $T(E,\mathbf{k}_\perp)$, for the path between $[x_i, x_f]$ can be described by the WKB approximation [52,53] as:

$$T(E,\mathbf{k}_\perp) = \frac{\pi^2}{9}\exp\left(-2\int_{x_i}^{x_f}\mathrm{Im}\left(k_x\right)dx\right) \tag{2.3}$$

In order to properly compute equation (2.3), an expression for the energy relation $E(\mathbf{k})$ in the energy gap is required; moreover it is important to highlight that the direct BTBT is an elastic process, meaning that the energy and the momentum are conserved. A simple set of $E(\mathbf{k})$ relations for the conduction band, the valence band and the gap is given by the

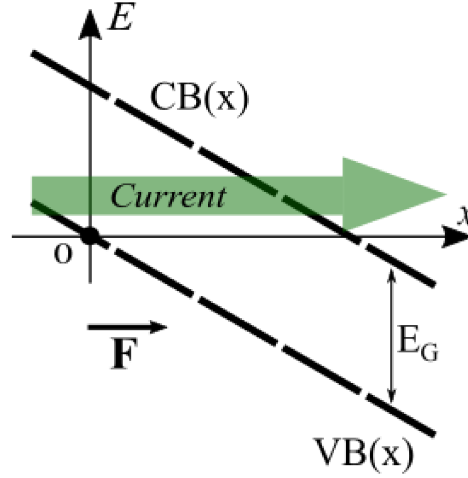

FIGURE 2.3. Sketch of the two-band Kane's model with the energy and direction references assumed in equations (2.4) and (2.6).

Kane's two-bands expressions:

$$E_{valence}(k) = \frac{E_G}{2} + \frac{\hbar^2 k^2}{2m_0} - \frac{1}{2}\sqrt{E_G^2 + \frac{E_G \hbar^2 k^2}{m_r}} \tag{2.4a}$$

$$E_{conduction}(k) = \frac{E_G}{2} + \frac{\hbar^2 k^2}{2m_0} + \frac{1}{2}\sqrt{E_G^2 + \frac{E_G \hbar^2 k^2}{m_r}} \tag{2.4b}$$

$$E_{gap}(\kappa) = \frac{E_G}{2} - \frac{\hbar^2 \kappa^2}{2m_0} \pm \frac{1}{2}\sqrt{E_G^2 - \frac{E_G \hbar^2 \kappa^2}{m_r}} \tag{2.4c}$$

where m_r=$(m_c^{-1} + m_v^{-1})^{-1}$ is known as *reduced mass* with m_c, m_v being the conduction and valence band effective masses) and k=$|\,(k_x, \mathbf{k}_\perp)\,|$ is the magnitude of the wave-vector. As the wave-vector inside the gap is purely imaginary, it is simpler to express equation (2.4c) as a function of κ^2=$-k^2$ while the $\pm$ sign indicate that two energy values exist at a given κ. Equations (2.4) express essentially the relation between the energy E and the wave-vector k. Referring now to figure 2.3 and making the assumption of constant electric field F in the tunneling direction, we can describe the band profiles along x as:

$$E_{valence}(x) = -q|F|x \quad , \quad E_{conduction} = -q|F|x + E_G \tag{2.5}$$

Combining equations that describe the Kane's model (2.4) and (2.5), we can obtain the expression for the imaginary wave-vector along the tunneling direction that can be used to compute the transmission coefficient:

$$\mathrm{Im}(k_x) = \sqrt{\frac{m_r}{E_G \hbar^2}}\ \sqrt{E_G^2 + E_G \frac{\hbar^2 \mathbf{k}_\perp}{m_r} - 4\left(q|F|x - \frac{E_G}{2}\right)^2}\,. \tag{2.6}$$

By substituting eq.(2.6) into equation (2.3) and integrating with integration limits defined as x_i=0 and x_f=$qE_G/|F|$, the tunneling probability

can be evaluated to be

$$T(k_\perp) = \frac{\pi^2}{9} \exp\left(-\pi \frac{\sqrt{m_r} E_G^{3/2}}{2\hbar q|F|}\right) \exp\left(-\frac{\pi \hbar k_\perp^2}{2q|F|}\sqrt{\frac{E_G}{m_r}}\right) \tag{2.7}$$

that can be used to analytically compute the tunneling generation rate in eq.(2.1) and finally obtain the well-known formula [45]

$$G_T = \frac{q^2|F|^2\sqrt{m_r}}{18\pi\hbar^2\sqrt{E_G}} \exp\left(-\pi \frac{\sqrt{m_r} E_G^{3/2}}{2\hbar q|F|}\right) . \tag{2.8}$$

The derivation presented above, which is the description of a *local* model, results in a tunneling coefficient T(E) independent of the energy E if $|F|$ is constant. When F is not constant the local model leads to an overestimation of the currents [37]. In order to overcome this limitation, and still remain in a semi-classical framework, *non-local* models are required [54, 55]: these models allow one to take into account also rapid variations of the electrical field over small distances. As an illustrative example, it is possible to slightly modify the Kane's two-band expression for the **k**-vector in the gap to obtain a *non-local* model; in which case κ can be expressed by the following analytical equation:

$$\begin{aligned} \kappa(x) &= \frac{1}{\hbar}\sqrt{m_r E_G\left(1-\alpha^2(x)\right)} \\ \alpha(x) &= -\frac{m_0}{2m_r} + 2\sqrt{\frac{m_0}{2m_r}\left(\frac{E - E_V(x)}{E_G} - \frac{1}{2}\right) + \frac{m_0^2}{16m_r^2} + \frac{1}{4}} \ . \end{aligned} \tag{2.9}$$

where E is the energy inside the forbidden gap (i.e. $E_V(x) \leq E \leq E_V(x) + E_G$).
This formulation, together with eq.(2.3) and in the hypothesis of small $k_\perp$ (that implies $\mathrm{Im}(k_x) \simeq \kappa + k_\perp^2/2\kappa$) [37], leads to an expression of the generation rate frequently used in commercial TCAD simulators [55], also known as *dynamic-path non-local model*:

$$\begin{aligned} G_T(E) = &\left|\frac{dE_V}{dx}\right|_{x_i} \frac{q}{36\hbar}\left(\int_{x_i}^{x_f}\frac{dx}{\kappa}\right)^{-1} \times \left[1 - \exp\left(-k_m^2\int_{x_i}^{x_f}\frac{dx}{\kappa}\right)\right] \\ &\times \exp\left(-2\int_{x_i}^{x_f}\kappa dx\right)(f_c - f_v) \end{aligned} \tag{2.10}$$

Equation (2.10), as opposed to equation (2.1) of the local model, describes a generation rate of holes at the x_i coordinate and of electrons at x_f, while the constant field is replaced by the derivative of the E_V profile calculated at the start of the path. Finally k_m is the maximum value of $k_\perp$ and is given by:

$$k_m^2 = \min\left(\frac{2m_v\left(E_{MAX} - E\right)}{\hbar^2}, \frac{2m_c\left(E - E_{min}\right)}{\hbar^2}\right) \tag{2.11}$$

where E_{min}, E_{MAX} are the minimum of the conduction band and the maximum of the valence band, and the energy E must be in the range $[E_{min},E_{MAX}]$.

2.2.2 Indirect BTBT in semiconductors

In indirect-gap semiconductors, such as silicon or germanium, the BTBT mechanism is more complex because the minima of the bands are not located at the same point in the Brillouin zone: this requires also the involvement of phonons to change the momentum. Keldysh [56] and Tanaka proposed models for the band-to-band PAT: the interband coupling, due to electron–phonon interaction, in the deformable ion model is used for interband coupling elements of the Wannier equation. The wave-functions necessary to define an expression for the tunneling probability are obtained by correcting the plane wave solutions (of classically allowed regions) with the decaying components of the WKB theory.

The tunneling transmission coefficient for the PAT can be calculated as:

$$T^{abs,em}(E) = \frac{D_{ph}^2\hbar^2}{2\rho E_{ph}} \sum_{\alpha',\alpha} \int A_{v,\alpha'}(z,E) A_{c,\alpha}(z,E \pm E_{ph}) dz \tag{2.12}$$

where the $\pm$ sign stands for respectively the phonon absorption or emission process, D_{ph} and E_{ph} are the deformation potential and the energy of the phonon, ρ is the mass density of the material and A_α is the spectral function for the 2D gas of the α subband [57]. Eventually, the total current for the BTBT mechanism assisted by phonons can be calculated as the sum of the emission and absorption terms:

$$\begin{aligned} J_{ph} = -\frac{q}{\pi\hbar} \int (&\{f_v(E)\,[1 - f_c(E - E_{ph})]\,[n_B(E_{ph}) + 1] \\ &- f_c(E - E_{ph})\,[1 - f_v(E)]\,n_B(E_{ph})\}T^{em}(E) \\ &+ \{f_v(E)\,[1 - f_c(E - E_{ph})]\,n_B(E_{ph}) \\ &- f_c(E - E_{ph})\,[1 - f_v(E)]\,[n_B(E_{ph}) + 1]\}T^{abs}(E))dE. \end{aligned} \tag{2.13}$$

In equation (2.13), $f_{(v,c)}$ are the occupation functions as in eq.(2.2), while $n_B(E_{ph})$ is the Bose-Einstein occupation function of phonons. For a rapidly variating field in the structure, equation (2.13) still holds if a proper set of wave-functions approximation is introduced, leading also to the so called *dynamic-path non-local PAT* model used in commercial TCADs [55].

2.3 State of the art - TFET Technologies

In recent years several options for the TFET design have been investigated, including non conventional architectures (e.g. nanowires or vertical

structures), different semiconductor materials (e.g. III-V compounds and 2D materials) or even specific mechanism to ease the BTBT process (e.g. van der Waals hetero-structure TFET) in the structure.

2.3.1 Silicon TFETs

One obvious choice, due to the maturity of conventional CMOS technology and the possibility of co-integration with CMOS FETs, was to implement tunnel FETs with group IV semiconductors (silicon, germanium or their compounds) and an extended set of analyses have been done with TCAD simulations to evaluate their performances. The major limit of these bulk materials is the presence of an indirect bandgap: this implies that the I_{DS} current is dominated by the PAT mechanism (that is less efficient compared to direct BTBT), but several subtleties have been pointed out about the physics of these devices. It is worth noting that in very narrow cross-section silicon nanowires (NW), the PAT could eventually be neglected, as the tunneling current is small anyway [58].

A good electrostatic control is fundamental to enhance the tunneling and, for this reason, in general SOI, DG or NW structures have been typically analyzed. On the other hand, the induced quantum mechanical confinement in ultra-thin layers of silicon tends to enlarge the energy bandgap, resulting in a suppression of BTBT. Several Si-TFETs simulations have reported low on-currents [37, 59], which is also consistent with available experimental data showing currents in the $\mu A/\mu m$ range [44, 60–62] and only for relatively large gate and drain voltages. If extrapolated to supply voltages around 0.5V, the experimental on-currents decrease to values of few $nA/\mu m$ [63].

It has been reported that one way to improve the on-current of IV-group TFETs is to introduce an appropriate amount of strain (uniaxial or biaxial) in the lattice of the semiconductor film [64–67]: this is well known to modify the bandstructure of the material in the near-gap region, enhancing the BTBT mechanism. Strain, in fact, changes the energy gap and induces bands splitting between some otherwise degenerate valleys of the conduction and valence bands, and also modifies the effective masses, both inside the bands and in the energy gap.

2.3.2 Simulation of strained-silicon TFET

Before moving to the III-V semiconductors TFET section, we present one of the original results of this thesis: an effective procedure that we have developed to simulate the performances of strained silicon TFETs using

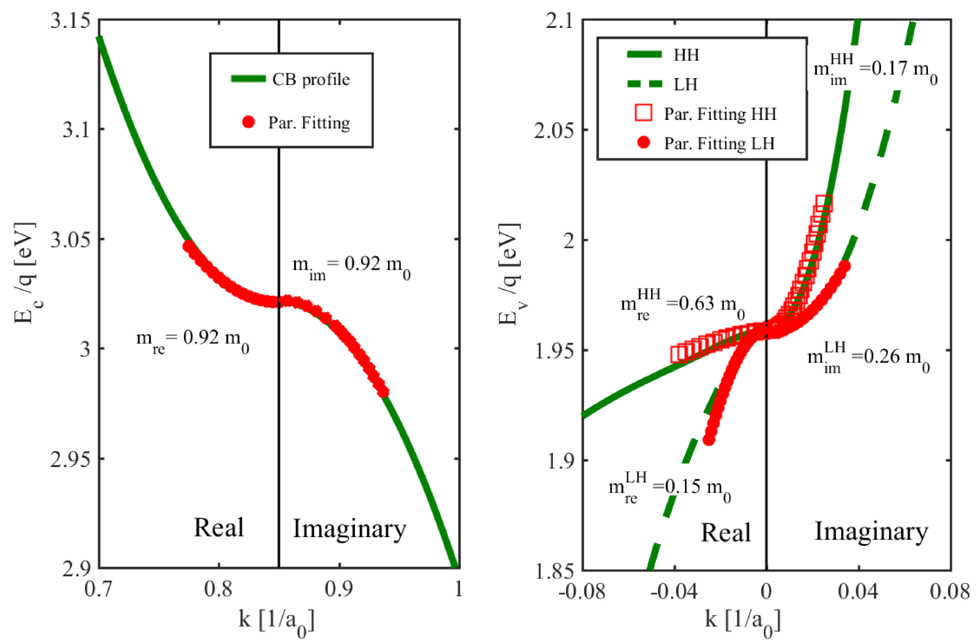

FIGURE 2.4. Plot of real and imaginary bands in unstrained silicon for the Δ valley of the CB in the [100] direction (left) and for VB valley in the [110] direction. Extracted values of the effective masses are also reported in the plots, and the parabolic fitting (symbols) tracks well the bands, in particular for small energies.

a commercial TCAD [55], after calibrating the models against relaxed silicon experiments.

The first step of this analysis is to extract, with a specific *tool* of the TCAD suite, *sband*, the values of the effective masses of the semiconductor, both in the bands (real branches of the dispersion relation) and in the gap (imaginary branches). We verified that the values obtained for the real band masses agree well with the values reported in the literature [68,69], both for the strained and unstrained material (as reported in figure 2.4 for CB and VB of unstrained silicon in different directions). For the CB we observed that the masses in the gap are almost the same as the masses corresponding to real branches, suggesting a fairly parabolic shape of the imaginary bands. On the other hand, an interesting property has been found for the VB: in the gap the effective masses tend to swap their behaviour compared to the corresponding real branches, in particular the imaginary HH valley has a mass comparable to the one of the real LH valley, and the imaginary LH branch has higher effective mass than its real counterpart (see figure 2.5). As it can be also seen in figure 2.4, the use of a parabolic expression can reproduce fairly well all the band features for the CB, while for valence band this approximation holds only for small energies. The effect of biaxial strain on the mass values and gap is illustrated in figure 2.5.

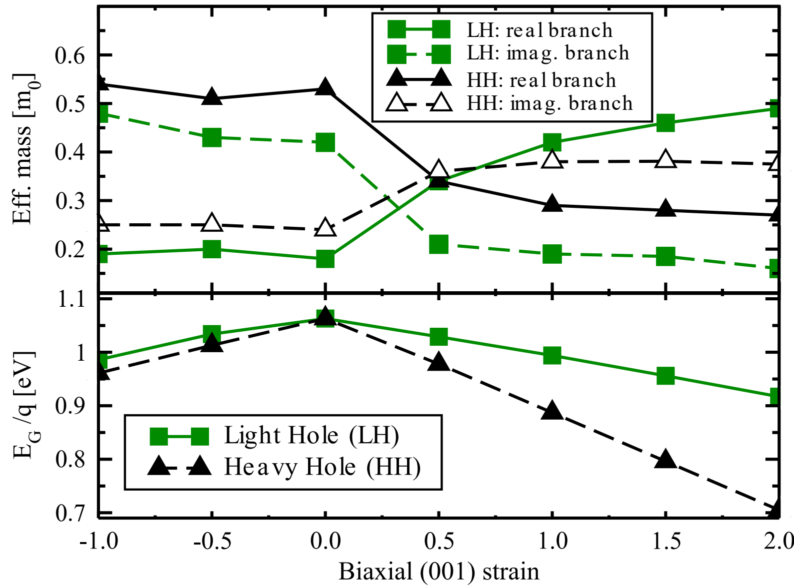

FIGURE 2.5. Hole effective masses and energy-gap behavior (depending on LH and HH valleys) in silicon versus applied biaxial strain in the (100) plane.

The following step to simulate the whole TFET structure is to describe more realistically the BTBT process in silicon and, in particular, the

TCAD approach uses the following set of equations to solve the PAT generation rate for one tunneling path, similarly to eq.(2.10).

$$
\begin{aligned}
G_T &= |\nabla E_v(0)| \cdot C_p \exp\left(-2\int_0^l \kappa_{im} dx\right)[f_v - f_c], \\
C_p &= \frac{C_{path}}{2^6\pi^2 E_G}\sqrt{\frac{m_c m_v}{h\sqrt{2m_r E_G}}}\left(\int_0^l \frac{dx}{\kappa_{im}}\right)^{-1} \\
&\times \left[1-\exp\left(-k_{v,max}^2\int_0^{l_c}\frac{dx}{\kappa_v}\right)\right] \\
&\times \left[1-\exp\left(-k_{c,max}^2\int_{l_c}^{l}\frac{dx}{\kappa_c}\right)\right], \\
\kappa_{im} &= \min(\kappa_c, \kappa_v), \ \kappa_c = \frac{1}{\hbar}\sqrt{2m_c(E_C - E)}, \\
\kappa_v &= \frac{1}{\hbar}\sqrt{2m_v(E - E_V)}
\end{aligned}
\tag{2.14}
$$

Here the whole tunneling path $[0, l]$ has been split into two contributions: the first one, governed by the imaginary term κ_v (related to the VB), extends between $[0, l_c]$, while the second is described by κ_c and extends between $[l_c, l]$. The terms $k_{c,max}$ and $k_{v,max}$ have the same meaning of k_m in equation (2.10) and C_{path} describes the phonon interaction of the PAT process.

Equation (2.14) refers to one specific tunneling path, that in unstrained silicon is frequently enough to approximately describe the BTBT current by accounting for appropriate valley multiplicity. In a strained silicon device, on the other hand, the mechanical stress breaks the symmetry of the Δ valleys of the CB, making it necessary to describe separately different contributions. To this purpose we used six paths to connect the LH and HH bands with the three Δ valleys of the CB, and for each of them the corresponding values of mass and energy gap extracted from *sband* have been used. The effective masses m_c and m_v in equation 2.14 are the masses describing the imaginary branches of the dispersion relation in the gap.

An example of computed path is reported in table (2.1) for particular values of F_{MAX}: in unstrained silicon the BTBT process is dominated by the transition from HH to Δ_y and Δ_z, as all the tunneling masses take the lowest values possible in the electric field direction x. In the case of biaxial 1% (001) stress, the energies of the Δ_z valleys are decreased and the masses reduced, leading to an enhancement of the contribution of HH$\rightarrow\Delta_z$ and LH$\rightarrow\Delta_z$ paths.

The main limit of equation (2.14) is that it does not take into account

Paths	J_{unstr}/V $F_{MAX} = 1.45MV/cm$	$J_{tens,1\%}/V$ $F_{MAX} = 1.3MV/cm$
LH→Δ_x	5.5×10^{-13}	5.4×10^{-11}
HH→Δ_x	5.9×10^{-10}	5.3×10^{-11}
LH→Δ_y	9.3×10^{-9}	9.0×10^{-10}
HH→Δ_y	4.5×10^{-7}	3.9×10^{-9}
LH→Δ_z	9.3×10^{-9}	1.1×10^{-6}
HH→Δ_z	4.5×10^{-7}	2.9×10^{-6}

TABLE 2.1. Contribution of different tunneling paths to the generation rates in [mA/μm^2/V] reported in figure 2.6 for unstrained and (001) 1% strained silicon.

the anisotropy of the CB minima, using m_c to calculate both the transmission probability (where the use of the imaginary mass is consistent) and the DOS involved in the tunneling. To solve this problem, a corrective pre-factor has been introduced and computed as a ratio between the DOS and the imaginary masses, and then included in C_{path} as:

$$C_{path} = C_{path,0} \left(\frac{m_{dos,c} m_{dos,v}}{m_c m_v} \right)^{3/2} \tag{2.15}$$

where $C_{path,0}$ is the phonon deformation potential of the unstrained silicon. This implies that, within this modeling framework, the strain does not affect the phonon behaviour modes. The used $C_{path,0}$ parameter has been calibrated against experiments on Si-diodes in [60, 70], once the effective masses have been extracted from the *sband* tool.

The results of this analysis are reported in figure 2.6 where the generation rates versus maximum field are plotted for slabs of unstrained and strained silicon with a constant electric field: the proposed six-path procedure shows a good agreement with unstrained silicon experiments [60, 70] and suggest that a 2% biaxial strain would increase the BTBT rate more than an order of magnitude. Experiments confirm an enhancement of the I_{ON} currents of sSi TFETs, but the measured enhancements are smaller than suggested by figure 2.6 [71, 72].

2.3.3 III-V semiconductors TFETs

The III-V compound semiconductors, such as antimonides or arsenides, are more suitable for TFET applications as they have more favourable properties for tunneling: reduced effective masses and smaller energy gap compared to silicon and germanium [73] and, in particular, direct band-gap at the Γ point, which means that no phonon-assisted process is required. On the other hand, the main disadvantage of these materials

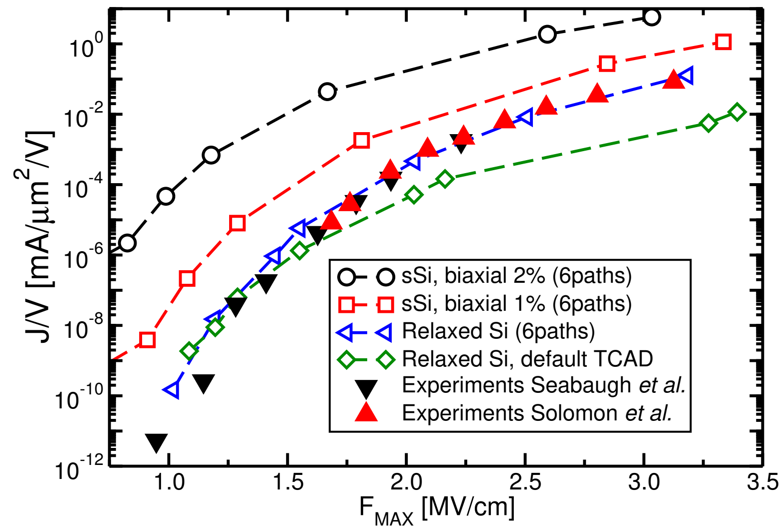

FIGURE 2.6. Generation rate versus maximum electric field obtained from the proposed 6-paths procedure and comparison against experiments [60, 70] and TCAD default setup.

is that the technology is not mature as it is for group IV semiconductors, and in particular the contact resistances and oxide-semiconductor interfaces are still worse compared to silicon counterpart devices.

For III-V based TFETs several experiments reported quite large on-currents thanks to high BTBT rates [74–76], but also a SS higher than the thermal limit [44], which is probably due to a poor gate electrostatic control and a high density of defects [77, 78]. Thanks to new device architectures the $[I_{ON}/I_{OFF}]$ ratio can be further improved, as demonstrated in a recent work [79] where a vertical InAs/GaAsSb/GaSb TFET, where the tunneling direction is aligned with the electric field induced by the gate.

2.4 Essential physics of the off-state operation of FETs

In this section we present an original analysis that we carried out about the physics of the off-state of TFETs and conventional CMOS transistors [80]). This is of particular interest as the ITRS roadmap projects channel lengths, L_G, of around 10nm by the year 2020 [27]: even though the adoption of non-planar structures (such as FinFETs [81, 82]) allowed

an aggressive scaling of conventional CMOS transistors, experimental reports for TFETs with an improved SS and low I_{OFF} still have L_G in the range of 100nm [44, 83].
In the following part of the section we consider a GAA device (the 3D version of the device sketched in figure 2.1(a)), but the same considerations can be applied also to FinFETs or double-gate SOI devices, while they do not directly apply to vertical TFETs (i.e. when the tunneling direction is aligned with the gate field) [84–86].

2.4.1 Semi-analytical models for the electrostatics and the off-state current

It is important to highlight again that this analysis is focused on the off-state of the transistors, and in this situation the influence of carrier concentrations on the electrostatics can be neglected: this is the basic assumption for most semi-analytical models describing the potential profile along the device channel. We here consider a simple model that is linked to the natural length of the transistors, λ_n [87–89].
Assuming a parabolic potential profile in the yz plane of the transistor, the potential $\varphi_c(x)$ in the center of the channel region can be written as [87, 90]:

$$\begin{aligned}\varphi_c = V_{GS,FB} + [\varphi_c(L_G) - V_{GS,FB}]\,\frac{sinh(x/\lambda_n)}{sinh(L_G/\lambda_n)} \\ + [\varphi_c(0) - V_{GS,FB}]\,\frac{sinh((L_G - x)/\lambda_n)}{sinh(L_G/\lambda_n)}\end{aligned} \tag{2.16}$$

where $V_{GS,FB}$=$(V_{GS} - V_{FB})$ and V_{FB} is the flat-band voltage when $\varphi_c(x) \simeq 0$ in the central region of a long channel device (i.e. $L_G \gg \lambda_n$).

The potential profile in the transport direction, $\varphi_c(x)$, is univocally determined by specifying boundary conditions, namely $\varphi_c(0)$ and $\varphi_c(L_G)$, that are the values of the potential at the source and drain junctions. This model can be used both for MOSFETs and TFETs, the only differences stem from the boundary conditions, that for an n-MOSFET correspond to n-type drain and source regions, while for a n-TFET correspond to a p-type source and a n-type drain. From equation (2.16) it can be seen that for a well-tempered transistor (i.e. for $[L_G/\lambda_n]$ ratios at least of 5 or 6) the potential profile in the channel region is quite flat, suggesting an almost ideal gate control for both the device type. In fact at x=$L_G/2$ we can write:

$$\frac{\partial\varphi_c(L_G/2)}{\partial V_G} = 1 - \left[2 - \frac{\partial\varphi_c(0)}{\partial V_G} - \frac{\partial\varphi_c(L_G)}{\partial V_G}\right] \frac{sinh(L_G/(2\lambda_n))}{sinh(L_G/\lambda_n)} \tag{2.17}$$

Equation (2.17) shows that $[\partial\varphi_c(x)/\partial V_G]$ at x=$L_G/2$ tends to 1.0 for increasing values of $[L_G/\lambda]$.

Once the band profile has been determined, the ballistic current can be expressed by using again the Landauer formula:

$$I_{DS} = \frac{q}{\pi\hbar}\int_{-\infty}^{\infty} T(E)\,[f_{0,S}(E) - f_{0,D}(E)]\; dE\ . \tag{2.18}$$

Here $T(E)$ is the transmission coefficient, while $f_{0,(S,D)}(E)$ are the Fermi-Dirac occupation functions of the source and drain reservoirs respectively. Equation (2.18) is the simplified version of equation (2.2) and it applies to a single mode, as it is a good approximation for very narrow nanowires. For MOSFETs the total I_{DS} corresponds to the sum of the contribution of the thermionic emission above the top-of-the-barrier of the channel, $E_{C,T}$, and a tunneling current between E_C and $E_{C,T}$, as depicted in figure 2.1(a). In TFETs, instead, the total I_{DS} is due only to the tunneling component in the energy window between the source VB and the drain CB (see figure 2.1(b)).

The transmission coefficient $T(E)$ can be expressed using different approaches (e.g. analytical models or NEGF [58,80]), but for the purpose of this work we use the WKB theory (equation 2.3) which, again, is very effective for direct bandgap semiconductors. To compute the imaginary wave-vector $\mathbf{k_{im}}$ inside the energy gap we here used another model, known as the Flietner's two-band model [91], that can be written in terms of energies and (generic) effective masses m^* as

$$\mathbf{k_{im}}(E,x) = \frac{\sqrt{2m^*}}{\hbar}\sqrt{\frac{[E - VB(x)[CB(x) - E]}{E_G}}\ . \tag{2.19}$$

Equation (2.19) suggest that k_{im}(E,x), at any position x, reaches a maximum value k_M=$\sqrt{2m^* E_G}/(2\hbar)$ for the mid-gap energy.

2.4.2 Off-current minimum and SS

Figure 2.7 illustrates the I_{DS} versus V_{GS} curves for different L_G and that were obtained using the equations presented in this section, employing numerical integration firstly over x to evaluate $T(E)$ and then over E to compute the total current. Similar results can be found for CMOS devices, as can be seen in [80].

The I-V characteristics show an I_{OFF} that tends to increase exponentially with the decrease of L_G and a strong ambipolar behavior: those features result from a detrimental effect on the SS of the device when the channel length is scaled. By focusing on the ambipolar behavior, we can

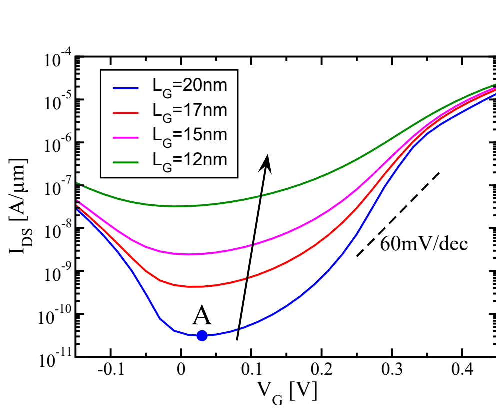

FIGURE 2.7. Simulated I_{DS} versus V_G at V_{DS}=0.3V of a InAs NW TFET, with a diameter of 5nm, $T_{ox} = 1$nm and a gate workfunction Φ_M=5.05eV at different L_G. The dopings are N_D=10^{19}cm^{-3} and N_S=5·10^{19}cm^{-3} for drain and source regions, while E_G=0.8eV and m^*=0.04m_0 [92]. The point A in the sub-threshold region is used to study the bands in figure 2.8.

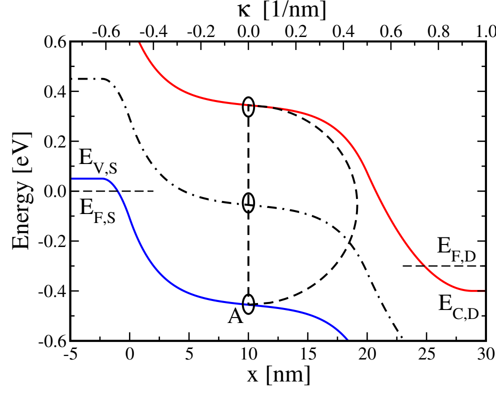

FIGURE 2.8. TFET bandstructure for the V_G corresponding to point A and the transistor with L_G=20nm. The source Fermi-level $E_{F,S}$ is used as energy reference, the mixed lines represent the mid-gap energy and the top x-axis refers to the imaginary $\mathbf{k_{im}}$ vector in the center of the channel (dashed line).

see in figure 2.8 that the minimum of the I_{DS} occurs when V_{GS} makes the mid-gap energy in the center of the channel cross the tunneling window (in particular close to $E_{F,S}$). This situation corresponds to the maximum value of k_{im}, thus the minimum value of $T(E)$ (see Eq.(2.3)).

Similarly consideration based on the WKB theory can be used to investigate the minimum value of the current: if we approximate the integral as a product of k_{im} evaluated at the center of the channel (i.e. $x = L_G/2$) and the difference between the integration extrema, the transmission probability becomes

$$T(E) \approx \exp[-2\mathbf{k_{im}}(E)\,(x_f - x_i)] \approx \exp[-2\mathbf{k_{im}}L_G] \; . \qquad (2.20)$$

The previous equation suggests that the minimum I_{DS} produced by tunneling increases exponentially with the reduction of L_G [93], and this effect can be clearly seen in figure 2.7.

Before concluding this section, we would like to emphasize that is possible to use the natural length of a MOSFET transistor λ_n, as a metric to evaluate the presence of SCEs also for TFETs, even if the SS degradation in MOSFET is dependent on the $[L_g/\lambda_n]$ ratio while in the BTBT devices is more sensitive to the absolute value of L_G. Figure 2.9 shows the average SS of experimental and simulated devices versus $[L_g/\lambda_n]$, and highlights how the TFET swing is degraded faster than in their MOSFET

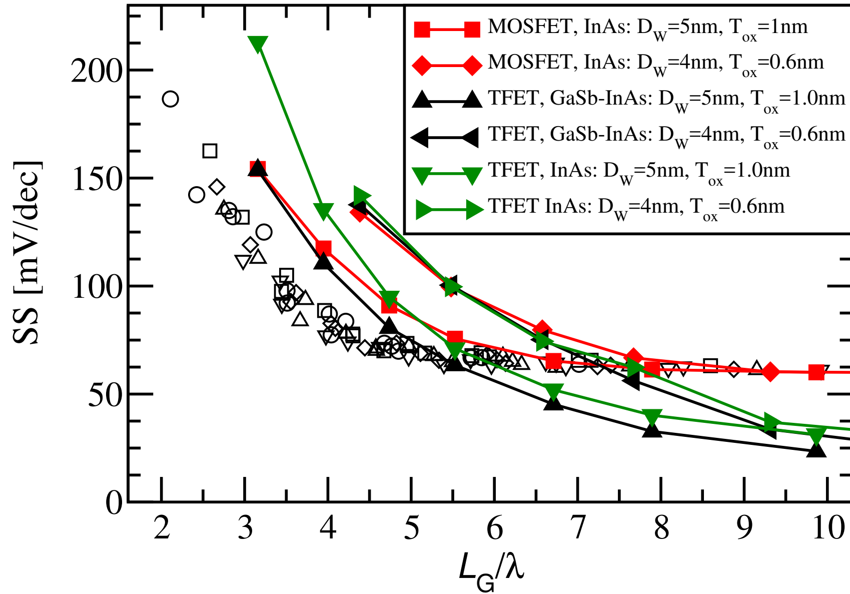

FIGURE 2.9. Simulated (lines) and experimental [89](symbols) subthreshold swings SS versus $[L_G/\lambda_n]$ ratio for III-V semiconductor TFETs and MOSFETs [80].

counterpart when the channel length is reduced below 4-5 times λ_n.
All those considerations and results suggest that the SS degradation is intrinsically due to the tunneling current, both in TFET (where it is the major component) and in MOSFETs (where is an undesired feature that becomes relevant in ultra-scaled devices).

Finally, even though the above discussion links the minimum I_{DS} value and the unwanted ambipolar behavior in ultra-scaled Tunnel FETs (and MOSFETs) to quite elementary physical mechanisms, the device design and the choice for the channel material still have a great impact on the quantitative manifestations of such mechanisms.

2.5 Final remarks and perspectives for TFETs

In previous sections we have discussed the general properties and the fundamental working principles of TFETs, describing some of the models frequently used to describe and design TFETs. As already explained, the design of such devices is very demanding in terms of electrostatic integrity, requiring thin semiconductor films (for conventional MOSFETs) or small effective diameters (for NW or FinFETs) [73, 80, 94, 95]: the side effect is a significant bandgap widening due to the strong quantization that leads to a suppression of the tunneling probability. Furthermore the sub-

threshold region is very susceptible to interface defects, such as dangling bonds at the interfaces, which are a main obstacles to the achievement of sub-thermal swings [73].

One possible solution to these material and device design problems is to employ 2D materials as semiconductor films, such as graphene or transition-metal dichalcogenides monolayers (e.g. MoS_2): these materials are promising for TFETs because, due to their native two-dimensional nature, they are in principle free of dangling bonds and have sub-nanometer thicknesses. Different types of architectures have been proposed to exploit 2D material properties, ranging from conventional lateral structures (similar to the ones used for 3D materials) [96, 97], to several vertical embodiments based on van der Waals hetero-structures between 2D materials or 2D and 3D crystals [86, 98].

In this scenario, and to our present knowledge, one of the most competitive experimental result for TFETs has been reported in 2016 for a III-V groups device with a nanowire structure [79]. This device features a vertical low-defect InAs/GaAsSb/GaSb heterostructure with a diameter of 20nm, a height of the pillar of 600nm and an estimated EOT of 1.4nm. This nanowire gate-all-around structure ensures a good electrostatic control on the channel region, which is also confirmed by the extracted low DIBL value of 25mV/V. The $I_{DS} - V_{GS}$ characteristics and the subthreshold swing versus I_{DS} curves for the best sample and for different V_{DS} are shown in figure 2.10. As it can be seen these devices can attain I_{off} values between 0.1nA/μm and 1nA/μm, and maximum I_{ON} is reported to be around 90 $\mu A/\mu m$ for V_{DS}= 0.5V; the SS is lower than 60mV/dec over two decades of current (with a minimum of 48mV/dec).

The proposed nanowire heterostructure seems to guarantee a very appealing on-state enhancement when compared to other traditional tunnel FET concepts [74, 79] and also a few improvements if compared to some conventional low-power MOSFET designs operating at V_{GS} lower than 0.3V. Even though these improvements can be considered promising for some low-power applications, this TFET concept is still lacking a [I_{ON}/I_{OFF}] ratio good enough to meet the IRDS requirements [27], in particular when compared to the conventional CMOS-based technologies, and it does not completely suppress the ambipolar behavior.

The concerns presented in the previous section, that are mainly related to the heavily degraded electrostatic control in TFETs for nanometric L_G and to the critical presence of interface defects, have steered the main focus of the electron devices community towards alternative steep-slope transistors concept that may be more scalable, have better [I_{ON}/I_{OFF}]

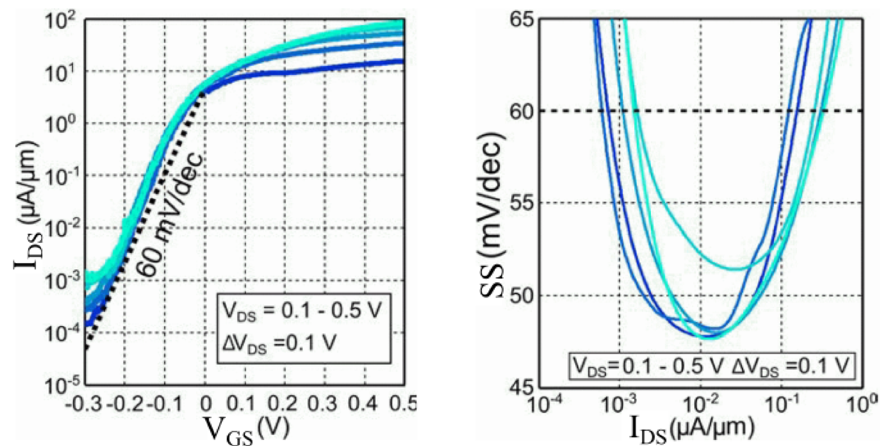

FIGURE 2.10. a) Experimental $I_{DS} - V_{GS}$ characteristics for different V_{DS}: the subthreshold region is steeper than the 60mV/dec reference and reaches a minimum value for the SS of 48mV/dec [79]. b) SS versus I_{DS} curves for different values of V_{DS} where we can see that the device operates as a steep-slope device over two decades of current.

ratios compared to TFETs and be more silicon technology compatible. A prominent example of such device concepts is the $Negative-Capacitance$ FET (NC-FET).

Chapter 3

Negative Capacitance in ferroelectrics

NEGATIVE capacitance (NC) is a concept used to describe an unusual behavior of some devices, where an increase in the electric field produces a reduction of the total charge of the device itself, so that $\partial Q/\partial F$ is negative, with Q being the charge and F the field. This characteristic is a natural feature of some materials, called *ferroelectrics*, or can be obtained with particular structures, such as suspended gates in a FET device (SG-FETs) [43], where the gate terminal is not placed in contact with the insulator and can move loosely in the vertical direction, getting closer or further from the channel in response to an electrostatic force. Another fundamental property of negative capacitance is its inherent instability: this implies that every system that exploits the NC concept requires a proper design to stabilize that behavior.

The main focus in this thesis is on ferroelectric materials and related devices. In the following sections we describe, within an engineering framework, the working principle of ferroelectrics, the possible techniques to stabilize them to operate in the negative capacitance region and some of the most useful and popular physical and numerical models related to ferroelectric materials.

3.1 Ferroelectric materials

Ferroelectricity was observed for the first time by J. Valasek in 1921 [99] while analyzing the side properties of a piezoelectric material, called "*Rochelle salt*" (i.e. potassium sodium tartrate tetrahydrate). He discovered that the salt had a non-linear response in polarization when a varying electric field was applied to the sample, in particular he saw a *hysteretic* response similar to the one of ferromagnetics in a variable magnetic field (the name *ferroelectric*, in fact, was chosen for this analogy).

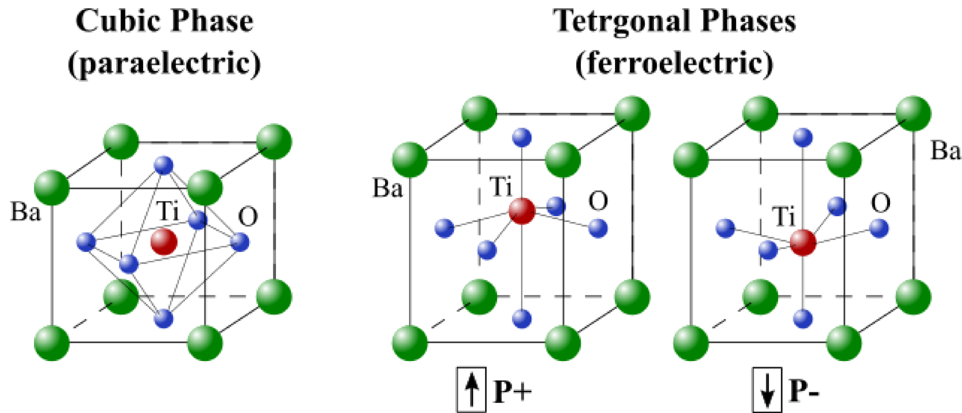

FIGURE 3.1. Exemplified structure of a $BaTiO_3$ crystal cell in different phases: the cubic phase does not show any electric momentum and has a paraelectric behavior, while the tetragonal phase can appear in two different configurations with opposite electric momentum, and this is the phase that shows ferroelectricity [102]. The atom displacements are emphasized to illustrate the two ferroelectric configurations.

Ferroelectric materials are well known in integrated electronics since the nineties as they have been exploited successfully in alternative RAM memory devices (called Fe-RAMs): the advantage is that, thanks to the hysteresis, a single Fe-RAM cell can directly store a bit, thus being promising as a high-integration memory [100, 101]. Only in the last decade [38] these materials attracted the attention of researchers in connection with the reduction of energy dissipation in digital integrated circuits (ICs). It is important to note that exploiting the hysteretic behavior of ferroelectrics is very different from the negative capacitance operation, and the two operations are suitable for different types of devices and design.

A ferroelectric is, in general, an insulating crystalline material showing two stable (or metastable) states of the electric dipole moment, referred to as "*spontaneous*" or "*remnant*" polarizations (P_r), when zero electric field is applied and, moreover, it is possible to switch between them by properly sweeping the external field. This mechanism is due to the anisotropy of the material, where is possible to identify specific macroscopic regions called *domains* with a specific polarization: these portions of material are close to each others, separated by the so called *domain walls*, and show different polarizations. Moreover the characteristics of each region tend to influence its neighbour dynamics and, eventually, the final value of the polarization of the whole sample. In particular, looking at the arrangement of atoms within the crystal structure, the ferroelectrics are characterized by the simultaneous coexistence of different symmetries (also known as *phases*) in the crystal, meaning that each region can have spontaneous polarization oriented differently: these sectors are called *domains* and

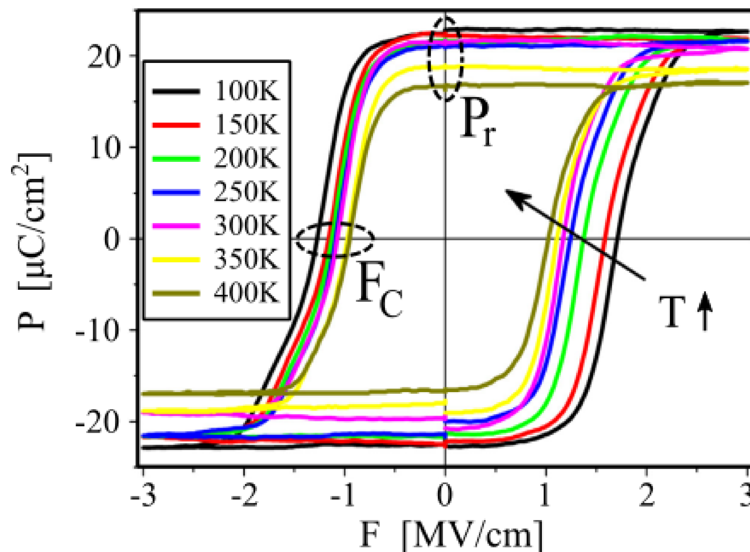

FIGURE 3.2. Experimental hysteretic characteristics from [1] of ferroelectric Si-doped HfO_2 for different temperatures T, obtained as a response of the material to a sequence of positive and negative pulses of the external electrical field. In this figure are easily visible (as the hysteretic eye is wide open) the remnant polarizations, P_r, of all the curves and the coercive fields F_C (at which correspond a polarization P_C). The temperature dependence will be discussed with more detail in the next chapters.

are commonly represented with oriented squares. In figure 3.1 we have exemplified the phases of a generic titanium-based *perovskite* oxide, a well known class of ferroelectrics: the left most case is a cubic phase and has a paraelectric non-polar behavior (i.e. no spontaneous polarization is present), while the other two sketches correspond to the tetragonal phases associated to the ferroelectric behavior, and the position of the titanium atom defines the direction of the polarization [103].

Returning to a more engineering description focussed on the macroscopic properties, the most evident characteristic of a ferroelectric material is its experimental hysteretic polarization-electric field characteristic (or similarly polarization-voltage), as can be seen in figure 3.2. The hysteresis is expected to be symmetric in large pieces of material, but as the samples are often analyzed in a stacked-capacitor device and the experimental setup can also have some parasitic components [104, 105], usually some asymmetries are observed in actual measurements [2, 106].

In figure 3.2 we have also marked two fundamental points of the characteristic, frequently used to describe the ferroelectric itself: the remnant polarization P_r is the residual polarization when the electric field across the sample is zero, while the *coercive field* F_C is the field that causes the polarization to switch (i.e. to change sign). Often it is preferred to consider the voltages rather than the electric fields, and V_C is thus defined

as the *coercive voltage* corresponding to F_C. When we quote coercive voltages we are also implicitly considering the thickness of the ferroelectric.

Ferroelectrics also depend moderately on thickness and strongly on temperature: thin layers behave differently compared to bulk material [2, 107, 108], while high temperatures reduce the ferroelectricity until it completely vanishes when the so called *Curie temperature* is reached and surpassed, leading to the paraelectric phase of the material [103,109].

3.1.1 Ferroelectric oxides

In recent years a large range of materials with ferroelectric properties have been discovered, each one with different ferroelectric parameters and, in particular, different $[P_r/F_C]$ ratios. The $[P_r/F_C]$ ratio has the units of [F/m], it is frequently reported in terms of ε_0 (i.e. the permittivity of the vacuum) and it can be used as effective metric to sort ferroelectrics based on the application. Different combinations of the values P_r and F_C, in fact, essentially determine the amplitude of the hysteretic loop, both in terms of voltages and polarizations: this can allow, for example, the tuning of the memory window in FeRAMs, or the value of the *negative-capacitance* in transistor designs [2, 3, 110, 111](that is introduced in section 3.4).

Here we discuss two famous and interesting class of such materials:

- *Perovskites* are the most studied and experimentally characterized class of ferroelectric crystals. These materials are often labelled as ABO_3 which refers to their general cell composition, where A and B is a combination of cation elements while the oxygen acts as an anion (e.g. $BaTiO_3$, $CaTiO_3$, $SrTiO_3$, $LiNbO_3$ or $PbZr_{1-x}Ti_xO_3$, that are also known as PZT) [38, 103, 112, 113]. The bulk materials offer very high $[P_r/F_C]$ ratios, in the order of magnitude of several hundreds to a few thousands ε_0. Critical temperatures of most popular perovskites are generally between 350K and 500K [103, 107], which are compatible with the range of operating conditions of some circuits, making their use highly application-dependent. The last critical aspect about perovskites that is worth discussing is the feasibility for their integration in CMOS processes. These materials can not be embodied directly in conventional architectures, because the large densities of induced defects would compromise the production yield. In order to avoid these issues in experiments, the transistors are connected to external perovskite capacitors [114,115], consisting of ferroelectric material between two metal contacts.

- *Hafnium-based* ferroelectrics have been recently discovered in the world of large-scale electronics [116] and extensively investigated [1, 117, 118], and have two main appealing aspects: the first is that these compounds are versatile as the ferroelectricity can be tuned by properly doping the hafnium oxide (e.g. with silicon, yttrium or zirconium, that are also known as HZO compounds) [1, 116, 119, 120]. The second important point is that hafnium is already integrated in conventional CMOS processes, as it is widely used as *high-κ* dielectric [121].The same material can show $[P_r/F_C]$ between a few dozens to some hundreds of ε_0 [110], that makes them a lot more flexible than perovskites both for RAM cells and for transistors with integrated ferroelectric. The temperature dependence of such materials strongly depends on the growth process and on the stoichiometry of reactants, but the Curie temperatures seem to be higher than perovskite counterparts [122], allowing in principle more robust devices.

For these reasons in a large part of the recent literature, the ferroelectric considered for device integration is HZO [2, 3]. In the next section we present two widely used physical models for ferroelectric crystals, that can also be implemented in FET simulators.

3.2 Physical models for ferroelectrics

There are several models for the physical behavior of ferroelectrics, in particular for the switching mechanism and the most relevant points of the polarization versus voltage characteristic, such as the remnant polarizations and the coercive fields. The first model we consider is the *Landau-Khalatnikov* equation [123], and it is the most frequently used theory for ferroelectrics applied to electronics since 2008 [38]. The second model relies on a mathematical description of hysteresis, known as *Preisach* model, and it has been introduced recently to describe ferroelectrics [2]. Those two models give slightly different results but are both predicting well the switching behavior of large ferroelectrics and naturally capture the anisotropic structure (i.e. the domains) of the material; the similarities in the two models suggest that the choice between the two approaches might be only application-dependent.

3.2.1 Landau-Khalatnikov (LK): homogeneous model

Lev Landau developed and published in the 1937 two famous physics works on the general theory of phase transitions in materials with a

change in their symmetry [124]. His theory had a strong influence, in the following years, on material physics and has been widely extended or applied yo several other scientific disciplines [125]. His theory was probably applied for the first time to ferroelectrics in a static framework by A.F. Devonshire in 1949 [126,127], but its modern dynamic formulation results from a reworking of a paper by Landau and Khalatnikov of 1954 [123].

The model by Devonshire stems directly from an energy-minimization process of the total Gibb's energy of the system: in fact, directly from thermodynamics principles, the total Gibb's free energy G_T can be expressed as function of different internal variables (that are strain η, polarization P and temperature T) and external stimuli (electric field F and stress σ). In the case of bulk ferroelectrics we will neglect the stress/strain components and we can expand G_T in powers of the internal and external variables [103, 107, 128] as:

$$G_T(P) = \frac{1}{2}aP^2 + \frac{1}{4}bP^4 + \frac{1}{6}cP^6 - FP \tag{3.1}$$

where the expansion is usually truncated at sixth order (but in some cases it can be reduced to fourth order [129–131], or extended to the eighth order [110]). In equation (3.1) F is the electric field in the ferroelectric sample, P its polarization and a, b, c are material-dependent coefficients. We highlight that, in principle P is a three component vector, so that the free energy should be written by using all the vector components. Here, for simplicity, we consider only a scalar value of P, which is a good approximation for thin ferroelectrics with no inhomogeneities. The values of the coefficients a, b, c can change over orders of magnitude depending on the material (see table 4.1), but ferroelectric phase requires a to be negative, while different phase transition types can lead to both positive or negative values of b and c.

In equation (3.1) we can find the non-linear response in polarization of the ferroelectric, that corresponds to the sixth order polynomial, and the external supply voltage generator term, that is the linear term in polarization [128]. For completeness, we want also to remark that in the literature of the physics community [132] and in a recent work on *Nanoscale* [133], in G_T we read also an additional term $[\varepsilon_0 \varepsilon_{Fe} F^2/2]$ that seems to account for the natural background dielectric response of the ferroelectric. However, it is not so easy to harmonize this concept with the Landau-Khalatnikov models, also because it has been argued that the additional term has an empirical nature, as opposed to a fundamental physical foundation [134]. For these reasons we decided to neglect the term $[\varepsilon_0 \varepsilon_{Fe} F^2/2]$, which is consistent with what it has been done almost universally in the electron devices community.

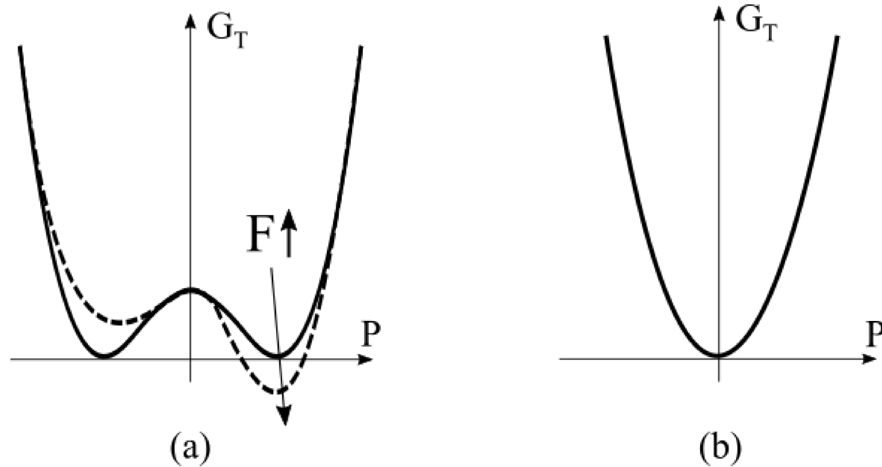

FIGURE 3.3. (a) Energy-polarization relation of ferroelectric material with the typical two-well characteristic: the two stable minima are separated by a region that has non-stable state (for P=0). The depth of each well can be modulated by the presence of an electrical field applied to the ferroelectric sample. In (b) we show the well known energy-polarization relation of a paraelectric dielectric, that is parabolic and thus it has only one minimum.

The energetic configuration of the material, described by the even sixth order polynomial, appears to be a two-well characteristic (see figure 3.3(a)): this means that more than one minimum can be found in the energy-polarization characteristic. This is a different behavior compared to the case of conventional (paraelectric) dielectrics with capacitance C, having a parabolic energy function [G_T=$P^2/2C$] (see figure 3.3(b)). The role of the electric field F is to make one minimum more favourable compared to the second one, thus allowing for the switch between the two stable states.

The equilibrium points can be found by minimizing the total energy in equation (3.1) with respect to polarization, which leads to:

$$\frac{\partial G_T}{\partial P} = 0 \qquad \Rightarrow \qquad F = aP + bP^3 + cP^5 \ . \tag{3.2}$$

Equation (3.2) is governed by an odd polynomial that is symmetric with respect to P=0 and describes the static behavior of the ferroelectric material. Figure 3.4 illustrates the "S-shaped" characteristic in the polarization-electric field plane, corresponding to equation (3.2). It is important to notice that this static curve shows a central negative-slope branch intersecting the origin of the plot, that corresponds to a negative differential capacitance C_{Fe}=[$\partial P/\partial F$]<0. This negative capacitance branch is not directly observed in experiments, in fact the static characteristic is very different from hysteretic P-F curve actually reported in experimental curves [1, 2], because the negative capacitance region is intrinsically unstable. In the following section, and in chapter 5 , it is explained how the

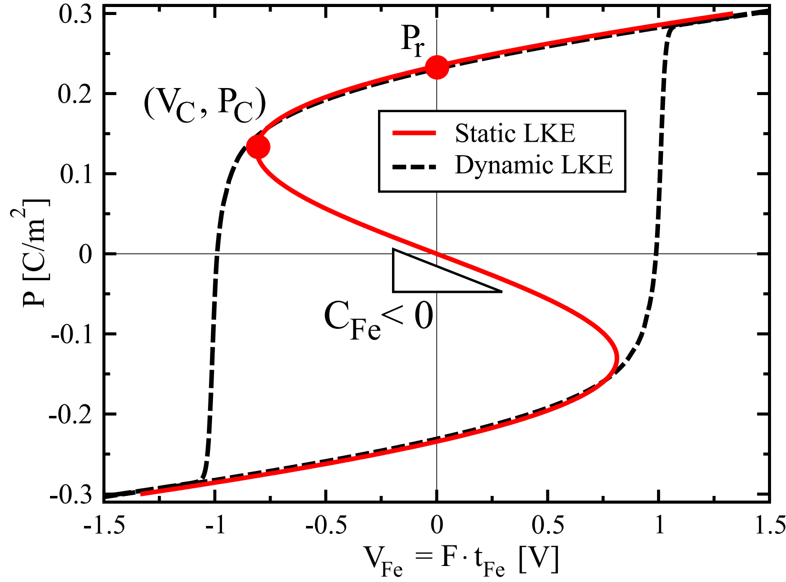

FIGURE 3.4. Typical polarization versus voltage characteristics obtained with the static (red) and the dynamic (dashed) Landau-Khalatnikov equations for a uniform HfO_2 ferroelectric placed between two metal contacts. The coefficients used here are extracted from [1], with a thickness of t_{Fe}=10nm, ρ=5Ωm and obtained with a triangular voltage waveform with a frequency of 5MHz. The S-shaped characteristic clearly shows a negative slope branch that is associated to the negative capacitance C_{Fe} behavior, while the dynamic relation has a hysteretic behavior that switches between the two saturation branches. Some important points of the characteristics are highlighted and labelled.

negative capacitance branch can be, in principle, stabilized to exploit its properties [38, 135].

Before proceeding with the dynamic version of Eq.(3.2), it is important to highlight that this model takes into account the critical temperature dependence of ferroelectrics by assuming that the coefficient a is linearly dependent on the absolute temperature T minus the Curie temperature T_0 which is, also, a ferroelectric property. Actually a is written as follows

$$a = a_0 (T - T_0) \tag{3.3}$$

where a_0 is a positive coefficient, so that a is negative only when the temperature is below the Curie point. A more extensive analysis on temperature sensitivity is presented in the device-design chapter.

Dynamics of the ferroelectric material

In order to describe the behavior of ferroelectrics a dynamic theory is needed to describe the switching mechanism of the polarization: for this reason Landau and Khalatnikov have shown [123] that in homogeneous

ferroelectric (i.e. in a single-domain framework) this can be obtained combining the Lagrange and the Gibb's free-energy equation, as:

$$\rho\frac{dP}{dt} = -\frac{\partial G_T}{\partial P} = -\left(aP + bP^3 + cP^5 - F\right) \tag{3.4}$$

where ρ is a damping factor (or a resistivity) governing the switching kinetics of the domains and other variables have the meaning already explained above [136]. This equation will be referred to as dynamic Landau-Khalatnikov equation or, simply, LKE. The dashed P-V_{Fe} characteristic shown in figure 3.4 is obtained from equation (3.4) by removing the time-dependence.

It is important to note that this theory, despite it is describing only a uniform material, can be still considered valid for the characterization of ultra-scaled ferroelectric devices, where the size of transistor is comparable to the dimensions of a domain (estimated from a few to a few tens of nanometers [137]), so that a nanoscale device may consist of a single domain.

3.2.2 Landau-Ginzburg theory: inhomogeneous model

Due to the presence of domains in ferroelectric samples, a homogeneous theory is expected to fail in the description of experiments when the dimension of the sample is large compared to the domain size. The Landau-Ginzburg approach extends the static and dynamic LKE to a multi-domain framework, taking into account spatial fluctuations of the order parameter, namely the polarization. [103, 138].
We usually consider the polarization in the vertical direction z but, due to the presence of inhomogeneities, changes of the polarization are expected to arise also in the x-y plane orthogonal to the axis z (see figure 3.7). Slow spatial variations of the polarization vector lead to an additional contribution to equation (3.1), that is proportional to the gradient of the polarization $|\nabla P|^2$ [139], so that the free energy reads

$$G_T(P) = \left(\frac{1}{2}aP^2 + \frac{1}{4}bP^4 + \frac{1}{6}cP^6 - FP\right) + \gamma\int_\Omega |\nabla P|^2 \tag{3.5}$$

where the last term is the energy contribution due to inhomogeneities and Ω is the ferroelectric volume. This equation includes the polarization-polarization interactions, estimating the additional cost of the free-energy when the polarizations in different locations are not parallel, and it can be also applied to the dynamic definition of the LKE (Eq.(3.4)) leading to a dynamic multi-domain description ($MD - LKE$).

The Landau-Ginzburg model describes continuous variations in an

inhomogeneous material, and in the following sections we will present a discrete version of the dynamic Landau-Ginzburg equation that has been used in this work.

It is worth mentioning that another recent and interesting explanation of the microscopic nature of ferroelectricity has been presented at the *2018 International Electron Device Meeting (IEDM)* by A. Khan [140]. The proposed explanation, which also seems to directly support the phenomenological Landau-Khalatnikov theory, starts by considering multiple polarizable units that electrostatically interact with each other. The paper shows that such an electrostatic interaction generates a microscopic positive feedback action (also known as *polarization catastrophe*) that triggers the hysteresis loop. In particular the final step of this demonstration, within the simplified analysis proposed, directly leads to the static LKE polynomial when considering an ordered set of polarizable units.

3.2.3 Preisach model

The Preisach model will only be briefly introduced in this thesis, as it was not directly used in our simulations. Ferenc (Franz) Preisach proposed his model for the first time in 1935 to describe intuitively hysteretic magnetization-related processes [141]. The original theory has been vastly studied, extended [142–144] and eventually generalized in a purely mathematical form in the seventies [145], allowing alternative applications of the model in different fields [2,146,147]. In general, according to Preisach, any type of hysteresis can be obtained by combining multiple ideal hysteretic loops, each one with its set of parameters. It is important to note that this approach is intrinsically an inhomogeneous model, thus it cannot be used to describe uniform materials or ultra-scaled ferroelectrics consisting of very few or possibly a single domain.

It is possible to consider an infinite set of simple hysteresis operators $\hat{\gamma}_{\alpha\beta}$, represented as an ideal rectangular hysteresis in the input-output diagram, similarly to a two-state switch, as it can be seen in Fig.(3.5) [148].

The values α and β correspond to coordinate of the input at which the characteristic switches "up" and "down" respectively, and from now on it is assumed $\alpha \geq \beta$. The output of the system can switch only between the values -1 and 1. As the input signal $u(t)$ is increased monotonically, the ascending path *abcde* is followed, while when the input is reversed, the branch *edfba* is traced. Together with the operators $\hat{\gamma}_{\alpha\beta}$, we also introduce an arbitrary weight function $\mu(\alpha, \beta)$, called $Preisach\ function$, that leads

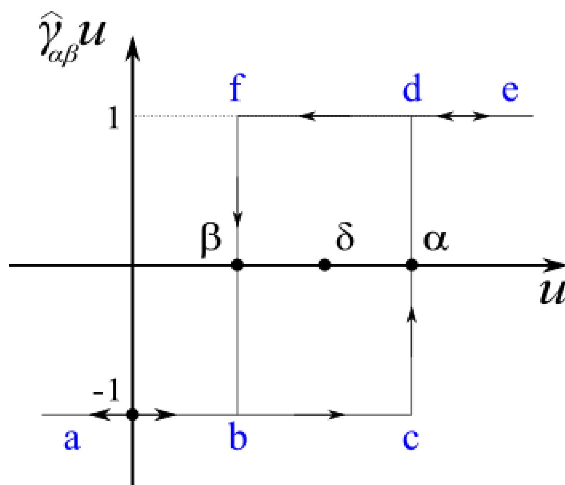

FIGURE 3.5. Representation of the ideal switch (or fundamental cell) of the Preisach model: the values α and β are the inputs that make the output value switch and δ is the coordinate of the center of the hysteresis. The letters inserted are used to describe the forward switching path, *abcde*, or the backward switching path, *edfba*.

to the Preisach continuous model:

$$f(t) = \hat{\Gamma}u(t) = \int\int_{\alpha\geq\beta} \mu(\alpha,\beta)\hat{\gamma}_{\alpha\beta}u(t)\, d\alpha\, d\beta \; . \tag{3.6}$$

Here $\hat{\Gamma}$ is used for the short notation of the Preisach operator that is defined by the function above. Equation (3.6) can be interpreted as a system of infinite two-state ideal switches (represented in figure 3.5) connected in parallel, with the same input $u(t)$ applied. The individual outputs are multiplied by the corresponding Preisach function and then integrated over all appropriate values of α and β: this is schematically represented as a block diagram in figure 3.6(a) and leads to the final result $f(t)$ that is exemplified in figure 3.6(b). The model can be easily discretized with a finite number of ideal loops that add up to build the overall hysteresis loop.

The application of this model to ferroelectric materials is fairly straightforward: every domain can be associated to a specific two-state switch, the switching points α and β correspond to the coercive fields, while the weight function can be used to describe the remnant polarizations. It is important to highlight that the characteristic in figure 3.5 can be in principle asymmetric with respect to the origin of the plot, allowing to have the center of the hysteretic eye, δ, as a supplementary degree of freedom.

Is worth to highlight that the Preisach model for the numerical description of ferroelectrics inherently entalis a switching behavior of each domain, thus the alleged negative-slope branch of the ferroelectric P-V

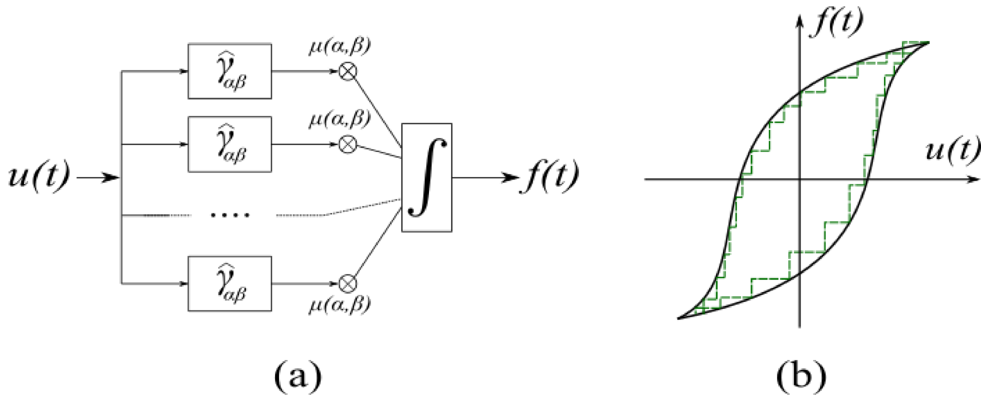

FIGURE 3.6. On the left we show the graphical representation of the complete Preisach model with a simple block diagram, that refers to equation (3.6). On the right we have an example of the output $f(t)$: the dashed lines illustrate a discrete case for a limited number of fundamental cells, while the black line is the result for a very high number of elements (that tends to the continuous solution of equation (3.6)) .

static characteristic is not predicted by this model. In this sense the model seems to be very useful to characterize devices that exploit the complete switching mechanism, such as in FeRAMs or in switching FETs [2], rather than the possible negative-capacitance feature.

Adding more details to this section goes beyond the scope of the thesis, but the Preisach model is an interesting example of how a collection of similar and ideal components can be composed into a realistic and non-ideal characteristic.

3.3 Numerical models for dynamic LK equations

It is also worth to discuss the discrete numerical models, used to obtain a large part of the results of this thesis, both for single- and multi-domain problems, and understand the differences with the continuous models.

The single-domain numerical implementation is obtained in a fairly straightforward way from the continuous dynamic LKE, as the only difference is the discretization of the time derivative of the polarization. In general, in this thesis, all the time-derivative discretizations have been approximated with the 4th order Runge-Kutta algorithm [149], which includes also an adaptive time-step based on an estimate of the numerical error (see the Appendix A).
The LKE is a differential time-dependent equation, thus the numerical

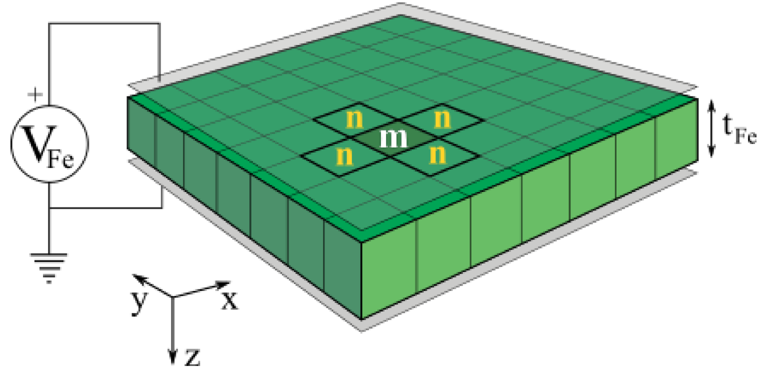

FIGURE 3.7. Discrete multi-domain representation of a ferroelectric sample placed between two electrodes, with thickness t_{Fe} and with an applied external voltage signal V_{Fe}, as described by equation (3.8): the m-th domain is surrounded and coupled to the domains labeled as n.

procedure to solve it is well known: at each time step the external voltage signal is updated and the correspondent polarization is calculated. The numerical expression solved in this case is:

$$P_i = P_{(i-1)} - \frac{\delta t}{\rho} \cdot t_{Fe} \left(aP_{(i-1)} + bP^3_{(i-1)} + cP^5_{(i-1)} \right) + V_{Fe,i} \tag{3.7}$$

where i is the index referring to the time-step δt, t_{Fe} is the ferroelectric thickness and $V_{Fe,i}$ is the voltage drop across the ferroelectric at the instant i, that for a simple ferroelectric capacitor corresponds to the external applied signal.

In the case of the inhomogeneous model, here referred to as *multi-domain* LKE, the computation of the time derivative is similar, but it is necessary to take into account the domain-domain interaction, that can be considered as a discrete version of the $|\nabla P|^2$ term in Eq.(3.5). Here it is presented the simplified but effective version of the discretized Landau-Ginzburg equation firstly proposed in [150] and here implemented also in the device-simulation context to obtain most of the results presented in this manuscript. The dynamic multi-domain problem illustrated in figure 3.7 results in a set of coupled LKE equations, each one describing the kinetics of one domain when influenced by its neighbours (for the sake of clarity, the left-hand-side is maintained as a continuous derivative to avoid the introduction of other indexes):

$$\rho \frac{dP_m}{dt} = -t_{Fe} \left(aP_m + bP^3_m + cP^5_m \right) + V_{Fe,m} + k \sum_{m \neq n} (P_n - P_m) \ . \tag{3.8}$$

Equation (3.8) is written for the m-th domain whose dynamics is coupled to the dynamics of the nearest neighbours with a linear coupling factor k, and it can be discretized in time similarly to Eq.(3.7). The number of domains and the value of the coupling factor k (that corresponds to γ in

equation (3.5)) have a large influence on the simulation results. While it is not clear which k value can be considered representative of actual ferroelectric materials, it can be estimated by comparing the experimental curves to simulations (see the calibration section 4.2 in the next chapter).

To emulate the inhomogeneities of the material, to each domain we assigned a different set of coefficients a, b, c (and in principle even ρ), that can be computed from a statistical dispersion of remnant polarizations and coercive fields. In particular this procedure starts with the definition of the *nominal* values, extracted from the calibration procedure discussed in section 4.2 and according to figure 3.8, for the coercive point of coordinates (F_C^{nom}, P_C^{nom}) and for the remnant polarization, which is positioned at (0,P_r^{nom}). The following step consists in associating a statistical dispersion (in our case a constant distribution) around the nominal values: this allows us to randomly pick, within this range, values of F_C, P_C and P_r for each domain. By using linear equations in (3.9) it is then possible to calculate the correspondent a, b, c for all the domains of the array and use them in the multi-domain LKE:

$$\begin{cases} a \cdot P_r + b \cdot P_r^3 + c \cdot P_r^5 = 0 \\ F_C = a \cdot P_C + b \cdot P_C^3 + c \cdot P_C^5 \\ \dfrac{dF_C}{dP_C} = 0 = a + 3b \cdot P_C^2 + 5c \cdot P_C^4 \end{cases} \tag{3.9}$$

The system (3.9) is a set of three linear equations that are used to calculate a, b and c. The first equation refers to the (0,P_r) point of the polarization-field characteristic in figure 3.8, while the second describes the switching point of the characteristic at (F_C,P_C). The last equation is obtained by differentiating the static LKE at the switching point and setting it to zero: this is consistent with the fact that the (F_C,P_C) point in figure 3.8 corresponds to a local minimum of the static LKE relation (this can be seen by inverting the axes of the P-V characteristic in figure 3.8).

It is interesting to compare the simulation results from single- and multi-domain LKE for the same ferroelectric material: as can be seen in figure 3.8, the single-domain LKE shows an almost abrupt switch at the (V_C^{nom}, P_C^{nom}) point, while the multi-domain characteristic has a smoother transition, which is mainly due to the dispersion of the coercive voltage introduced by our approach.

The presented numerical models are the ones implemented in our simulator to describe the entire ferroelectric NC-FET structure, and in the next chapter we will explain how our device simulator links the LKE theory with semiconductor and interface descriptions. In particular, the numerical multi-domain LKE offers good results when compared to char-

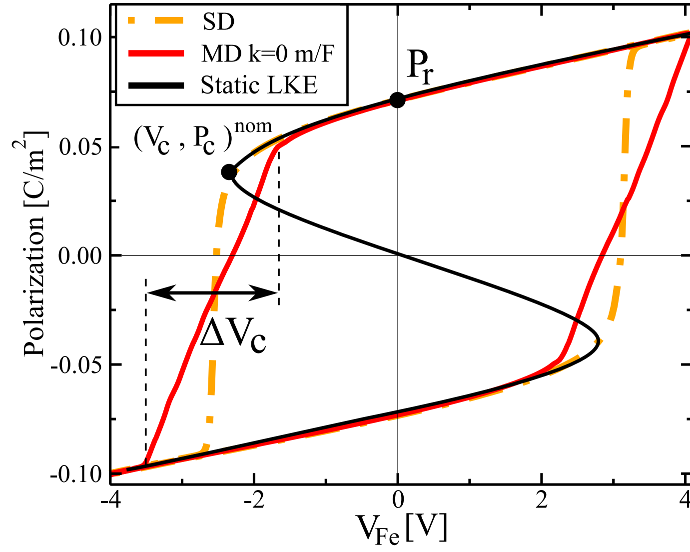

FIGURE 3.8. Comparison between voltage-polarization characteristic of a 10nm thick ferroelectric HZO [2, 110], for the multi-domain (MD), the single-domain (SD) and the polynomial static LKE. The important points and the dispersion ΔV_c (that is here set to $\pm 1V$ around V_C^{nom}) in the coercive voltage are highlighted.

acterization experiments on ferroelectric materials, and it has been used here mainly to calibrate LKE coefficients (see next chapter).

3.4 Stabilization of ferroelectrics and negative capacitance

The main focus of this section is the presentation of the negative capacitance in ferroelectric materials and how it is directly related to the stabilization concept. As already mentioned the negative-slope branch of the P-V curves cannot be seen in characterization experiments of ferroelectric capacitors due to its non-favourable energetic profile, but it can be stabilized with the use of a proper value of (positive) capacitance in series [38, 151].

According to Salahuddin and Datta [38], the negative capacitance concept can be explained as a positive feedback mechanism [152], within the framework of conventional systems theory. As is illustrated in figure 3.9(a), our system consists of a positive linear capacitor C_0, with a charge Q on its plates, at which it is directly applied an input voltage V plus a feedback contribution αQ, thus we can write the response of the closed-loop system as

$$Q = C_0(V + \alpha Q) \;\Rightarrow\; Q = \frac{\mathbf{C_0}}{\mathbf{1} - \alpha \mathbf{C_0}} V = C_{Fe} V \qquad (3.10)$$

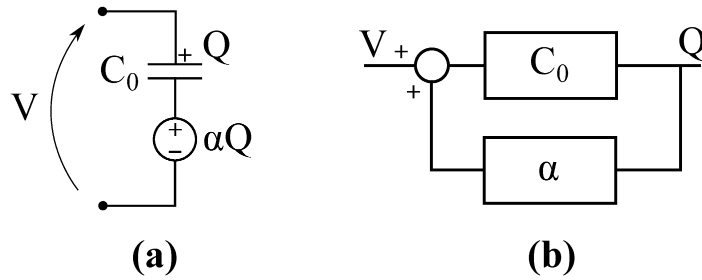

FIGURE 3.9. In (a) is reported the equivalent circuit which is used to describe the positive feedback of the negative capacitance. In (b) is reported the correspondent block diagram of the closed-loop system.

where $\alpha>0$ and the bold fraction in equation (3.10) is the transfer function of the system and corresponds to a overall capacitance C_{Fe}. Equation (3.10) is describing a positive feedback, as shown in figure 3.9(b), and for $\alpha Q>1$ the C_{Fe} becomes negative, leading to an increase of the charge and to an unstable overall behavior that is essentially described by a hysteretic curve.

Hence, to exploit the negative capacitance within a system it is necessary to put in series to the negative C_{Fe} a positive capacitance C_s, making the whole transfer function stable again, in fact:

$$Q = \left[\frac{1}{C_{Fe}} + \frac{1}{C_s}\right]^{-1} V = \frac{C_{Fe}C_s}{C_{Fe}+C_s} V = \frac{|C_{Fe}|C_s}{|C_{Fe}|-C_s} V \ . \tag{3.11}$$

The above equation is written to explicitly highlight the negative contributions of C_{Fe} and it suggests, in particular, that only some C_s values can stabilize the entire system: when $C_s<|C_{Fe}|$ the overall capacitance is positive and the $[C_s/|C_{Fe}|]$ ratio can be tuned to shape the Q-V relation.

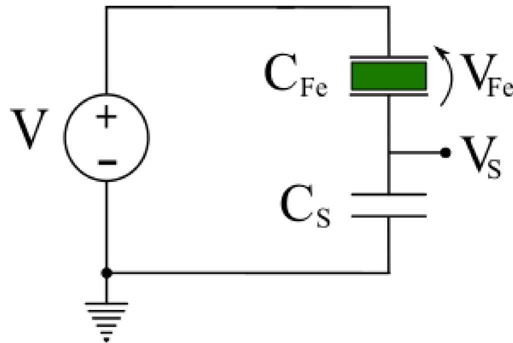

FIGURE 3.10. Setup used to analyze the stabilization of the negative capacitance of a ferroelectric capacitor C_{Fe}: a voltage generator is placed in series to a ferroelectric and to a dielectric capacitance C_S.

The latter result is very interesting because we can use the negative-positive capacitance series to obtain a sort of voltage gain between the

capacitances themselves, hence a sort of step-up voltage transformer that relies only on capacitances and can be, in principle, embodied in the gate-stack of a device. This can be easily demonstrated by considering the voltage divider described by the series of negative capacitance C_{Fe} and positive linear capacitance C_s, as depicted in figure 3.10: if we apply a voltage V to the series and analyze the internal voltage V_s, we can write:

$$V_s = V \frac{C_{Fe}}{C_{Fe} + C_s} \Rightarrow \frac{\partial V_s}{\partial V} = \left[1 - \frac{C_s}{C_0}(\alpha C_0 - 1)\right]^{-1} . \quad (3.12)$$

The relation (3.12) suggests that the gain $[\partial V_s/\partial V]$ can be maintained stable and made very large by properly tuning the capacitance magnitudes, and, in particular, it is the distance between the two values of C_{Fe} and C_s that controls the resulting gain value: for this reason we will refer to this condition as *capacitance matching*.

This general treatment, and in particular the stability condition, can be extended to series of multiple capacitors, including non-linear capacitances such as the ones shown by semiconductor layers: this allows us to tune, within certain limitations, the stability of the ferroelectric into FET structures, leading to different operative conditions that will be described in the details in the device design chapter.

3.5 Energetic behavior of NC devices

When the series of a ferroelectric and a generic non-ferroelectric capacitor (linear or not) is subject to an external voltage V_T, we can conceive two possible approaches to calculate the steady-state V_c(Q) relation of the internal node, according to figure 3.11.

The almost universally employed approach [41, 129, 153, 154] involves the well known Kirchhoff's laws: the ferroelectric voltage-charge relation V(Q) is described by the LKE, and the Kirchhoff's laws for the series connection (i.e. the elements in series share the same amount of charge Q and the sum of their voltage drops is equal to the total applied voltage V_T) are enforced in the vertical direction of the device. It has been argued [155], however, that this approach may provide a Q value that does not minimize the Gibb's energy of the whole NC-FET, leading to a wrong result in terms of thermodynamics. We have demonstrated in our work [128], instead, that the two approaches for the NC-FETs are indeed equivalent and, even if we introduced some simplifying assumptions, we believe that our results can be extended also to more general cases.

We start by analyzing the results of the two approaches when consid-

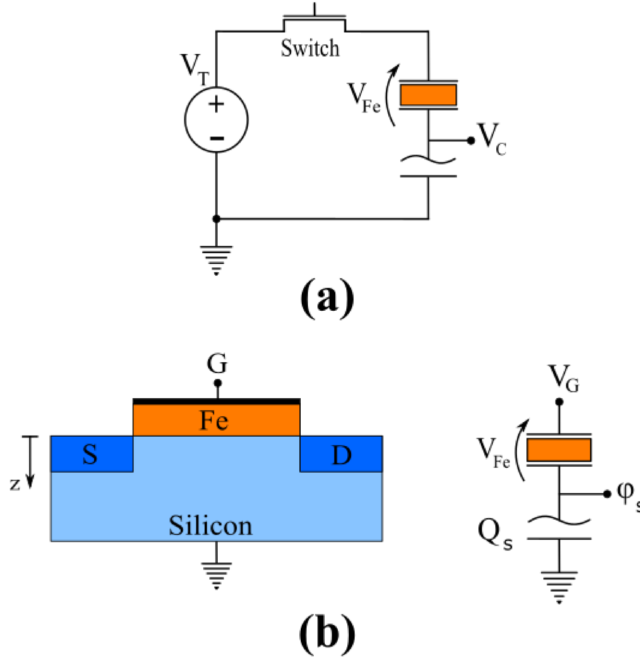

FIGURE 3.11. In (a) there is the sketch of a series of a ferroelectric and a general non-linear non-ferroelectric capacitance connected to a voltage supply V_T through an electronic switch. In (b) there is the representation of the device and its equivalent circuit.

ering a ferroelectric in series with a linear capacitor (figure 3.11(a)) and then move to the ferroelectric-dielectric-semiconductor series case (figure 3.11(b)), always in a 1D modeling framework.
Recalling equation (3.1) for a ferroelectric, assuming that the total charge Q is approximately the value of P, and in the context of no changes in temperature or strain, the variation of Gibb's free energy $G_{Fe}(Q)$ due to the application of the external stimulus V_{Fe} can be re-written as

$$\begin{aligned} G_{Fe}(Q) &= U_{Fe}(Q) - V_{Fe}Q \\ &= t_{Fe}\left(\frac{1}{2}aQ^2 + \frac{1}{4}bQ^4 + \frac{1}{6}cQ^6\right) - V_{Fe}Q \end{aligned} \tag{3.13}$$

where the term U_{Fe} is related only to the ferroelectric material, according to the LK theory, while the other term is the energy variation of the voltage source. As already shown in section 3.2.1, the energy-minimization process applied to the previous equation leads directly to the V(Q) relation (i.e. the static LKE) of the ferroelectric connected to an external voltage source. It is worth noting that, in general, the LKE is a macroscopic thermodynamic approach that allows us to derive the V(Q) relation from an energy minimization process, and without any additional detail about the underlying microscopic physics.

The standard approach to describe a non-ferroelectric capacitor, such

as a dielectric or a non-linear semiconductor-based capacitor, has instead a quite different starting point and procedure. We first solve the electrostatics using the Poisson equation, including the physics needed to take into account possible charge densities, which leads to the V(Q) relation of the capacitor, and eventually this is used to calculate the electrostatic energy stored in the capacitor. For a linear dielectric capacitor, with capacitance C_s, is well known that hold the relations

$$V_c(Q) = \frac{Q}{C_s} \quad U_c(Q) = \frac{Q^2}{2C_s} \; . \tag{3.14}$$

and then, by applying the Kirchhoff's laws, we can calculate the overall voltage drop $V_T(Q)$ of the ferroelectric and dielectric series as the sum of $V_c(Q)$ and V_{Fe}. We can also write the Gibb's free energy for such a capacitor subject to an external voltage V_c, similarly to the case of the ferroelectric, thus obtaining:

$$G_C(Q) = U_c(Q) - V_c Q = \frac{Q^2}{2C_s} - V_c Q \tag{3.15}$$

that can be minimized by setting $dG_C(Q)/dQ$=0, and directly leads to the V_c(Q) relation.

Following now the second approach, that consists in the minimization of the total energy of the series of the capacitances, we can write the derivative of the Gibb's free energy of a generic NC-FET as:

$$\frac{\partial}{\partial Q}\left[t_{Fe}\left(\frac{1}{2}aQ^2 + \frac{1}{4}bQ^4 + \frac{1}{6}cQ^6\right) + U_c(Q) - V_T Q\right] = 0 \tag{3.16}$$

that is an equation that can be solved in Q and assumes that the energy relation of the linear capacitor is known. According to equation (3.14) we can write $[\partial U_c(Q)/\partial Q]$=Q/C=$V_c(Q)$, hence it can be seen that equation (3.16) results in the relation $V_T(Q)$=$V_{Fe}(Q)$+$V_c(Q)$: this is consistent with the outcomes of the first approach that relies on the Kirchhoff's laws.

We can now demonstrate that this equivalence between the two approaches holds even when considering a non-linear capacitance in series with the other two materials. This is readily done by demonstrating that even for non-linear capacitances the voltage-charge relation can be obtained with an energy-minimization methodology. Our analysis started by noticing that, at any time, the power delivered to the non-linear capacitor in figure 3.11(b) is $[\varphi_s(t)(dQ/dt)]$, where φ_s is the voltage drop across it, and consequently the energy U_{sc} stored in the semiconductor when it is charged to Q

$$U_{sc}(Q) = \int_0^\infty \varphi_s(t)\left[\frac{dQ}{dt}\right] dt = \int_0^Q \varphi_s(Q')dQ' \tag{3.17}$$

where the charge in the initial state is taken to be zero. The only assump-

tion in this expression is that the possible time constants and losses in the semiconductor are negligible compared to those introduced by the external switch. Equation (3.17) implies that $[\mathrm{d}U_{sc}/\mathrm{dQ}]=\varphi_s(Q)$ which, similarly to the case of the linear dielectric capacitance, leads to the equivalence between the first approach and the Gibb's energy-minimization methodology. This confirms the validity of both the methodologies in the analysis of a electronic device.

Numerical validation

To support and verify the above analysis, and its main conclusions, we verified the equivalence by numerically simulating the behavior of a NC device with our code (described in the following chapter). The simulations shown here were carried out for a 20nm thick HfO_2 ferroelectric layer with a retrograde channel doping profile to improve the capacitance matching condition (as discussed in the device design chapter) [135], but the results can be easily extended to other structures. The LKE parameters for this material are a=$-3.9e8$m/F, b=$1.0e10\mathrm{m}^5/\mathrm{F}/\mathrm{C}^2$ and c=$-2.65e10\mathrm{m}^9/\mathrm{F}/\mathrm{C}^4$, as also reported in the table 4.1.

The semiconductor energy is computed as in (3.17) and then added to the ferroelectric energy, leading to the free Gibb's energy G_T for the device. In particular, in figure 3.12(a) we show the energy-charge relations for two applied V_T, and in figure 3.12(b) the zoom of the same plot on the minima of the G_T: it can be seen by comparison with figure 3.13 that the values of charge density corresponding to the energy minima belong to the voltage-charge relation of the NC-FET (green curve) and then to the given values of V_T.

The presented numerical analyses are obtained within a simplified framework, but the general results are expected to hold even for more complicated structures and devices, as the treatment relies only on fundamental principles of physics.

3.6 Experimental evidence of negative capacitance

In this section we present and discuss the most important empirical results reported in literature, claiming an experimental evidence of negative capacitance behavior.

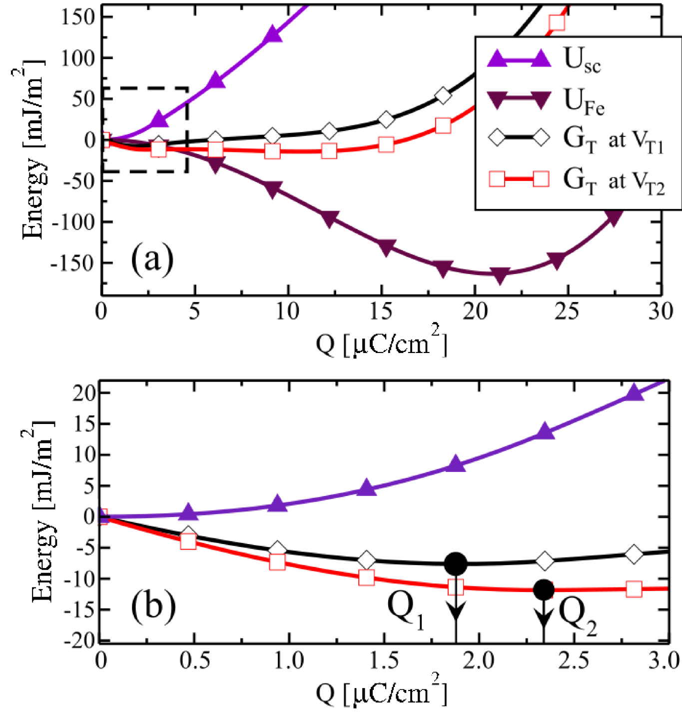

FIGURE 3.12. In (a) there is the energy-charge relation $G_T(Q)$ of a retrograde doping NC-FET [135] and in (b) the respective zoom on the energy minima for V_{T1}=0.15V and V_{T2}=0.35V, corresponding to the dashed square region in (a). The energy minima are placed at Q_1 and Q_2 for applied voltages V_{T1} and V_{T2} respectively.

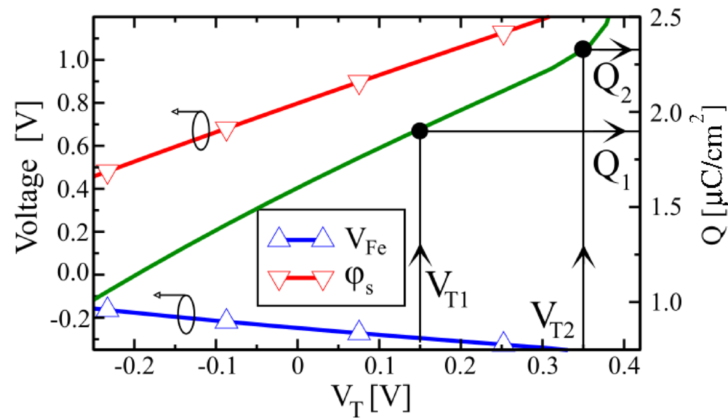

FIGURE 3.13. Voltage-charge relation of the retrograde doping NC-FET [135]: on the left axis there are represented the voltage drops across the semiconductor φ_s and across the ferroelectric V_{Fe}. The green curve is the density of charges versus the applied voltage V_T. The correspondences between V_{T1}, V_{T2} and Q_1, Q_2 respectively are also visible.

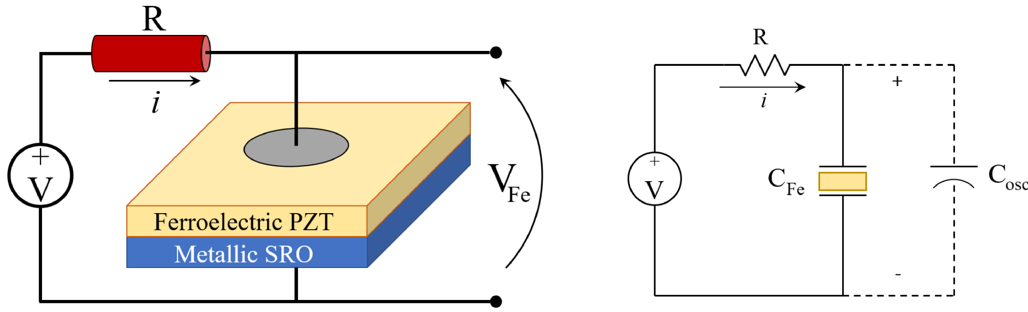

FIGURE 3.14. On the right there is the sketch of the experimental setup used in [105] to observe the negative capacitance: the ferroelectric layer of PZT is grown above a metallic layer of SRO and placed in series to a resistor R=50Ω. On the left there is the equivalent circuit: the voltage V_{Fe} is measured with an oscilloscope that has a parasitic capacitance C_{osc}, while the total charge is calculated from the current i running on R.

As argued in section 3.4, when measuring stand-alone ferroelectric capacitors the negative capacitance described by the *S-shaped* curve remains an elusive property in experiments, and only the hysteretic behavior is observed. On the other hand there are a two widely accepted experimental evidences pointing at a negative C_{Fe}. The first was an experiment originally proposed by A.I. Khan in 2014 [105], where the response of a ferroelectric capacitor in series to a resistance was analyzed with an oscilloscope, and the setup is sketched in figure 3.14 with its equivalent circuit.

The setup is described in details as follows: a 60nm ferroelectric PZT film has been grown between a thick metallic $SrRuO_3$ (also known as SRO) substrate and a square gold electrode, whose area is of $(30\mu m)^2$. This capacitor is placed in series to a 50Ω resistor and then connected to a pulse function generator, then the oscilloscope reads both the input signal and the voltage drop across the ferroelectric sample. Another important role is played by the parasitic capacitance of the oscilloscope (as can be seen in the equivalent circuit in figure 3.14) placed in parallel to the ferroelectric capacitor, as it influences the field across the capacitor itself. Then a series of square voltage pulses of amplitude V=±5.4V are applied to the setup: the voltage drop in the ferroelectric is read by the oscilloscope and the charge Q is obtained by integration of the current running in the resistor R. The result is shown in figure 3.15: it is interesting to note that the region between A and B, or similarly C and D, has a voltage V_{Fe} that changes in the opposite direction compared to the charge Q. The fact that the Q is decreasing while the voltage V_{Fe} is increasing (or *vice versa*) implies that $[dQ/dV_{Fe}]<0$, hence the differential capacitance is negative.

Z. C. Yuan in [150] used this procedure to validate his numerical model for a multi-domain ferroelectric (see section 3.3) and to compare

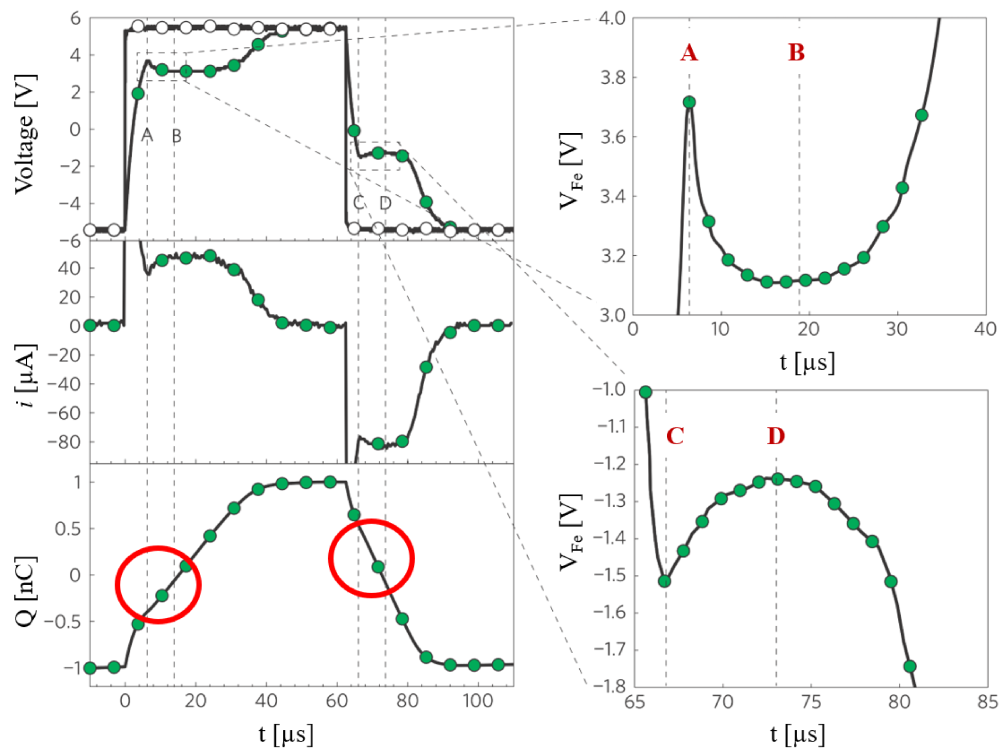

FIGURE 3.15. Results proposed in [105]: on the left, from the top to the bottom, are represented the responses of the ferroelectric (green dots) to the input signal (empty dots) in terms of voltage V_{Fe}, current i and total charge Q, accordingly to the setup in figure 3.14. On the right there are the two magnified portions of the voltage response. It is clearly visible from the comparison between the plots of V_{Fe}-t and Q-t that there are regions (limited by the labels A, B, C and D) where the variations of those quantities is opposite, thus can be described by a negative C_{Fe}.

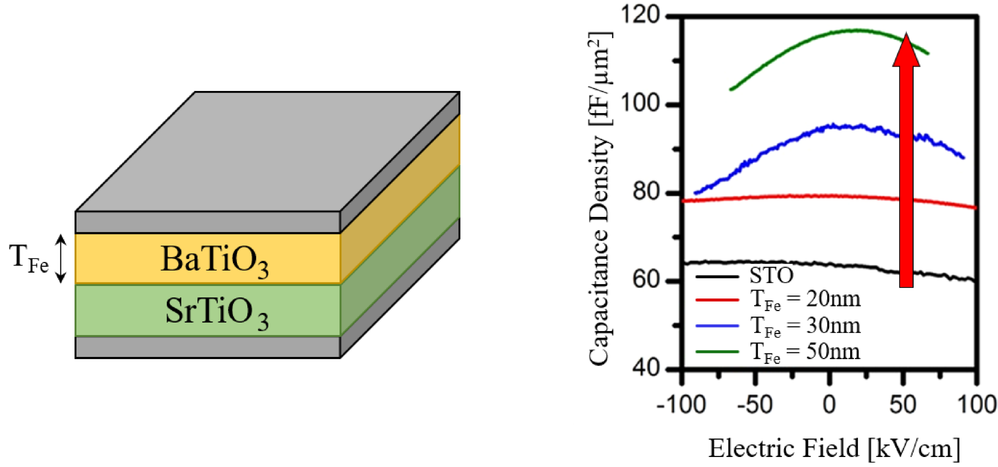

FIGURE 3.16. On the left there is the representation of the ferroelectric device analyzed by Appleby in [156], for different thicknesses of the ferroelectric $BaTiO_3$ layer. On the right are reported the full capacitance scans for the dielectric stand-alone STO layer (fixed thickness of 25nm) and for different thicknesses T_{Fe} of the ferroelectric. The boosting effect on the measured capacitance and due to the ferroelectric is clearly visible.

it against the single-domain LKE.

The second experimental evidence is related to the effect that negative capacitance has when it is placed in series with other positive capacitances. D. Appleby saw in 2014 [156] that when a ferroelectric material is placed in a stack with other conventional materials, the total series-capacitance is greater than the single contributions (if properly tuned). This result is supported by theory: in fact, for a series of ferroelectric and dielectric capacitances (C_s and C_{Fe} respectively), we can write the total capacitance C_{tot} as

$$C_{tot} = [1/C_s + 1/C_{Fe}]^{-1} = \frac{C_{Fe}C_s}{C_{Fe} + C_s} = C_s \left[\frac{|C_{Fe}|}{|C_{Fe}| - C_s} \right] \qquad (3.18)$$

where we have esplicitated the sign of C_{Fe}. The right-hand-side of equation (3.18) suggests that, for a proper combination of $|C_{Fe}|$ and C_s, the term between square brackets can be made greater than one, and thus $C_{tot}>C_s$. The experiments were carried out on a stacked capacitor made with a dielectric layer of $SrTiO_3$ (also known as STO) and different thicknesses of ferroelectric $BaTiO_3$, at room temperature and at a frequency of 10KHz. The results are shown in figure 3.16: as the thickness of the ferroelectric is increased (and thus its capacitance is made smaller in magnitude), the total capacitance of the device exceeds the one of the stand-alone dielectric.

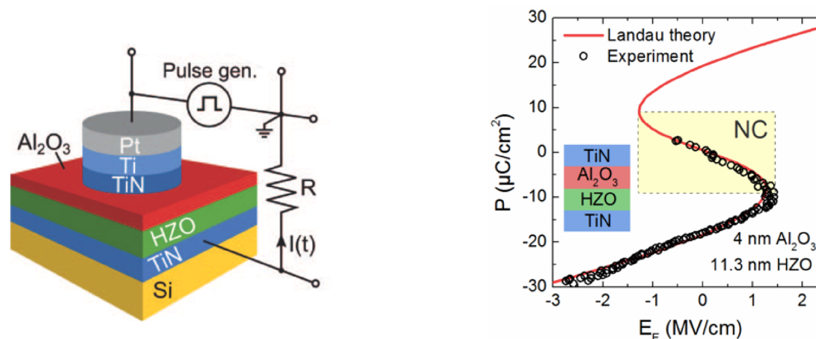

FIGURE 3.17. On the left it is reported the schematic of the setup used by Hoffmann to run the pulsed charge-voltage measurements. On the right there is the comparison between measured and theoretical polarization versus field E_F characteristics for a ferroelectric HZO layer with T_{Fe}=11.3nm and a T_{ox}=4nm: it is clearly visible the experimental NC branch.

This capacitance amplification effect can be usefully exploited also in the design of ferroelectric NC-FETs, and this will be discussed in the design chapter 5.

Before concluding this chapter we want to present another very important experimental result recently reported by M. Hoffmann *et al.* [157] that shows evidence of negative capacitance effect in ferroelectric materials. In this work they start by recalling that in a metal-ferroelectric-metal (MFM) capacitor with multiple domains, the stabilized NC behavior can be achieved only for an anti-parallel configuration of all domains which leads to an average null polarization and thus to a depolarization field equal to zero [158]. For this reason they carried out two sets of measurements of the charge in a MFIM capacitor, for two different HZO thicknesses, and plotted them against the measured electric field of the ferroelectric. The results seem to track very closely the theoretical S-shaped static LKE characteristic, as can be seen in figure 3.17. It is worth noting that no capacitance-enhancement effect is observed in this experiment, which seems to be due to fixed charges at the ferroelectric-dielectric interface that screen the polarization when no voltage is applied at the stack [159].

The results in figure 3.17 are obtained by applying 500ns ascending and descending pulses to the MFIM structure, and the absence of any type of hysteresis in the polarization-field plot is claimed to confirm the presence of a stable NC effect. In this work authors also reduce the applied pulse width to 100ns in order to test the kinetics of the negative-slope branch in HZO, reporting that also in this case the measurements follow precisely the theoretical curves without any hysteretic behavior. This may suggest that a device can reach, in principle, high speed operations exploiting

the stable NC effect [157], while any possible speed limitation due to the ferroelectric material seems to be related to the kinetics of the complete switching of domains.

Chapter 4

Ferroelectric Negative-Capacitance FETs

In previous chapters we have described in the details both the physical and the numerical models for ferroelectric materials, and in this chapter those models are applied to the characterization of a negative capacitance MOS transistor, a NC-FET. In particular, during the PhD project we have developed from scratch a simulator that has been improved over the time by adding models for interface defects, and a simple description of short channel effects (SCE) in aggressively scaled FETs .

4.1 Modeling of the NC-FETs

We focus on an n-type silicon double-gate (DG) architecture (see figure 4.1) for all the analyses and simulations proposed in this thesis, where z is the vertical direction that corresponds to the quantization direction normal to the semiconductor interface. The ferroelectric models used are both the multi- and the single-domain formulation of the Landau-Khalatnikov

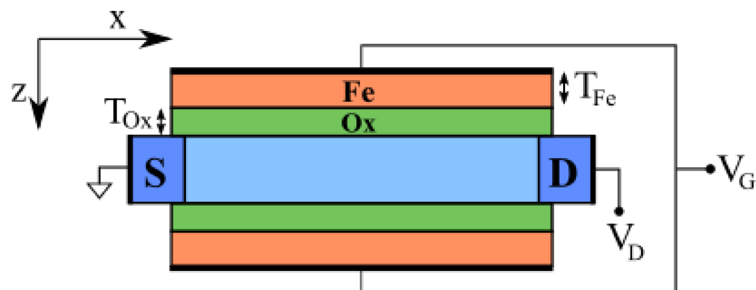

FIGURE 4.1. Sketch of the double-gate (DG) transistor used in our analyses. The embodiment of a dielectric oxide between the ferroelectric layer and the semiconductor is justified by its presence in actual devices [2,108] and by the fact that it is an important design parameter, as discussed in the following chapter.

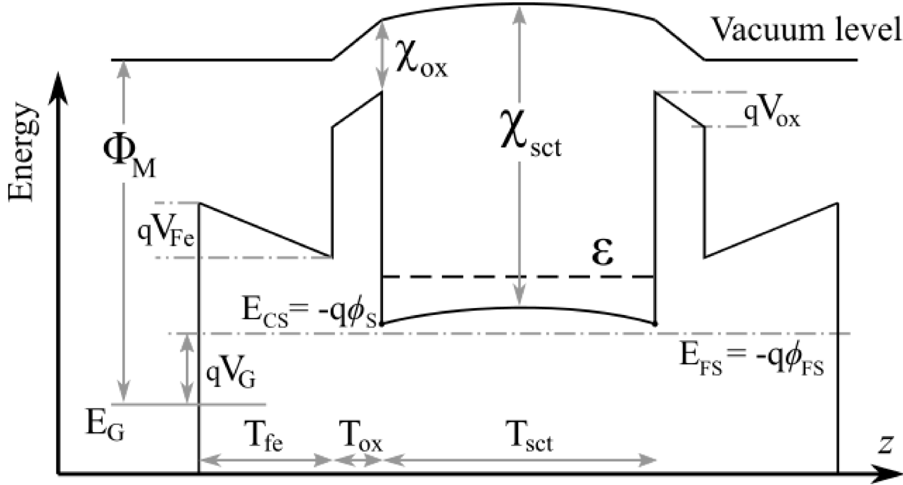

FIGURE 4.2. Band diagram in the quantization direction z for the DG device in figure 4.1. The values of electron affinities χ of the materials, the work-function Φ_M of the metal, the Fermi-Levels and the lowest subband minimum ε are also illustrated.

equation, depending on the size of the device to study. For large devices, such as capacitors, we expect a large number of inhomogeneities thus the use of multi-domain approach appears to be appropriate, while for nanometric FETs we decided to use the single-domain LKE. To compute the ballistic current and conductance the simulator uses a simple top-of-the-barrier model [68], which also takes into account 2D electrostatic effects due to scaling by implementing a capacitive coupling between the top-of-the barrier point and the source and drain regions. Finally we decided to include both a static and a dynamic model for interface traps (essentially a Shockley–Read–Hall recombination model, *SRH* [160–162]) to study the non-trivial influence of such defects in negative-capacitance devices.

Before explaining in detail how our simulator works, it is important to consider the underlying physics of the device, in particular how each layer is electrically linked to the others. This is obtained by using the continuity of the electrical displacement vector D, that is defined as [152]:

$$\mathbf{D} = \varepsilon_0 \mathbf{F} + \mathbf{P} \tag{4.1}$$

where F is the electric field vector permeating the region of interest while P is a charge density or the polarization vector. As we are considering a 1D structure, it is possible to consider equation (4.1) as a scalar relation providing a continuity condition for the electric field. Moreover we notice that, in the ferroelectric material, the term proportional to the electric field is negligible compared to the polarization term, mainly due to the big values of P in the ferroelectrics. For this reason, hereafter, we will consider P approximately equal to the charge density Q. Once the charge

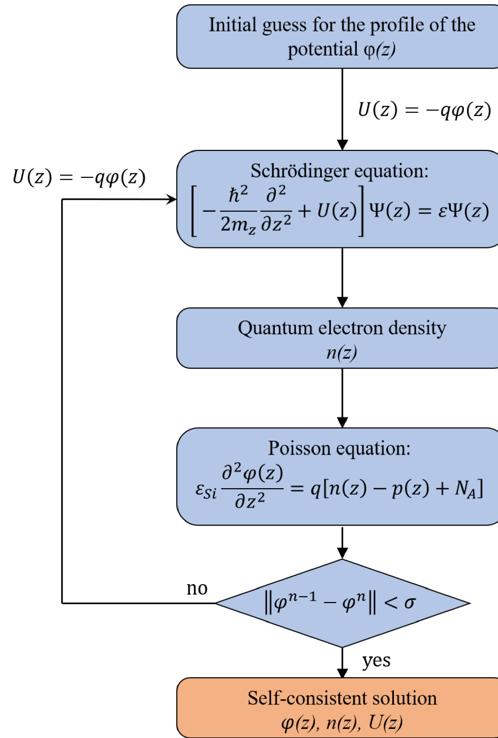

FIGURE 4.3. Block diagram of the Schrödinger-Poisson numerical solver. The n index represent the n-th cycle of the solver, while σ represent a proper potential threshold to check the convergence of the simulator.

in the vertical direction is known, it is possible to obtain the voltage drop across every material by evaluating the respective voltage-charge relations, leading to the description of the entire NC-FET voltage-charge behavior.

4.1.1 Quantum effects and electrostatics

The p-type semiconductor film is described by a $self$-$consistent$ Schrödinger-Poisson solver, whose flowchart is shown in figure 4.3. The computation starts from an initial guess on the potential profile $\varphi(z)$ of the semiconductor (calculated by neglecting quantization effects), and then the simulator cycles between the solutions of the Poisson and Schrödinger equations until convergence is reached. The semiconductor layer of the structure shown in figure 4.1 has been discretized with the Pseudo-Spectral method, that is a powerful and efficient numerical algorithm which is discussed in the details in the Appendix A.

This module of the code describes quantization effects only for electrons and thus the value $\varphi(z)$ is used to compute the energy profile for

the conduction band minimum, according to figure 4.2:

$$U(z) = -q\,\varphi(z) \tag{4.2}$$

which assumes that the Fermi-level at the source is the energy reference $E_{F,S}$=0. Once $U(z)$ is defined for that potential profile, the Schrödinger equation in the well known parabolic *effective-mass* approximation (EMA) [68, 163] can be solved as an eigenvalue problem:

$$\left[\frac{-\hbar^2}{2m_z}\frac{\partial^2}{\partial z^2} + U(z)\right]\Psi(z) = \varepsilon\,\Psi(z) \tag{4.3}$$

where Ψ is the wavefunction associated to the sub-band energy ε (i.e. the eigenvalue of the problem), and m_z is the effective mass in the quantization direction. It is important to note that equation (4.3) is solved for both valleys of silicon having effective masses m_z=0.92m_0 and m_z0.19m_0, where each valley gives its partial contribution to the total electron carrier density $n(z)$ according to its multiplicity. In more details, the value of $n(z)$ for a specific valley is itself a sum of two contributions: the electrons coming from the source reservoir, n_S, and those from the drain region, n_D, and each of those contributions can be written as [68]

$$\begin{aligned} n_{S(D)}(z) &= \sum_{\nu,n} |\Psi_{\nu,n}(z)|^2 \frac{\mu_\nu m_{d,\nu} K_b T}{\pi\hbar^2} \ln\left(1 + e^{\eta_{\nu,n}^{S(D)}}\right) \\ \eta_{\nu,n}^{S(D)} &= \frac{E_{F,S(D)} - \varepsilon_{\nu,n}}{K_B T} \end{aligned} \tag{4.4}$$

where (ν,n) are the (valley, subband), μ_ν is the multiplicity of the valley ν in the chosen direction, m_d is the DOS mass for silicon (for a specific interface) and m_z is the quantization effective mass.

Once the charge density is determined, it is applied to the Poisson equation for the semiconductor, which can take into account several contribution to the total charge density ρ (such as interface-trap density or fixed charges):

$$\varepsilon_{Si}\frac{\partial^2\varphi(z)}{\partial z^2} = \rho = q\left[n_S(z) + n_D(z) - p(z) + N_A\right]\ . \tag{4.5}$$

In equation (4.5) N_A is the acceptor doping concentration, ε_{Si} is the permittivity of the silicon, and n_s, n_D are the carrier densities defined in equation (4.4). It is important to note that we include in our simulations the degeneracy of the Fermi-levels in the computation of the hole densities $p(z)$. The Poisson equation is solved iteratively with a Newton-Raphson algorithm until convergence, defined with a proper threshold, is reached. The output of equation (4.5), that is the potential profile $\varphi(z)$, can be used to restart the cycle from the equation (4.2) and then again into the Schrödinger equation.

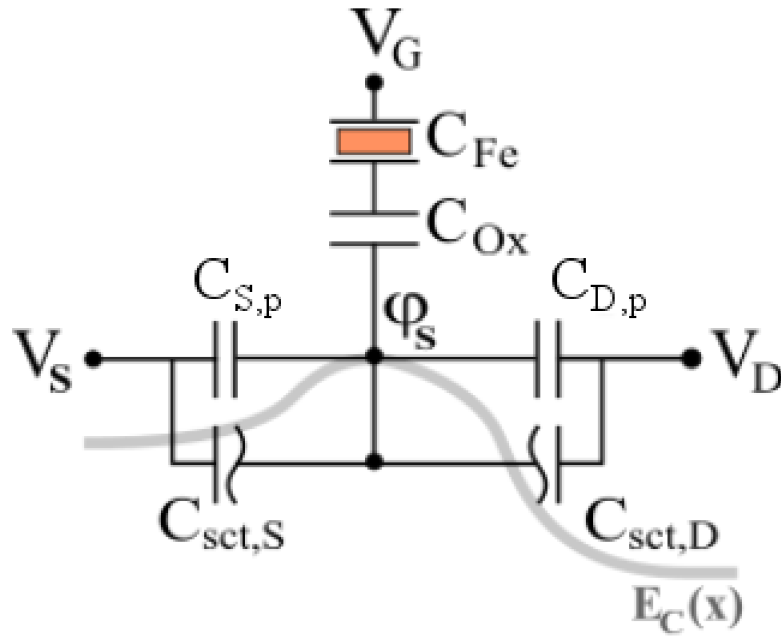

FIGURE 4.4. Equivalent circuit of the electrostatics of the double gate NC-FET in figure 4.1 that includes also SCE. The capacitance C_{Fe} is associated to the ferroelectric, C_{Ox} to the dielectric oxide and $C_{sct,(S,D)}$ to the semiconductor film. $C_{S,p}$ and $C_{D,p}$ are parasitic capacitances expressing a direct coupling between source-drain and the top-of-the barrier.

As already mentioned, each layer of our device shares the same charge per unit area (due to the continuity of vector D), thus we used the polarization as a Neumann-type boundary condition, instead of using a Dirichlet boundary condition set by the external voltage [135]. These two approaches are indeed equivalent as all the voltage-charge relations are determined, but our choice eases the resolution of the static LKE when considering a NC-FET. In particular this is because the 5-th grade V(Q) relation expressed by the LKE cannot be inverted analytically, thus the inverse Q(V) relation should be solved numerically and would increase the computational cost.

Short Channel Effects

The models previously presented describe an ideal transistor, where the electrostatics allows a perfect control on the channel barrier in the quantization direction, and thus is not degraded by 2D effects related to the scaling of the channel length. It is possible to include in the model the influence of V_S and V_D on φ_s by adding a capacitive coupling between the top-of-the barrier and the source and drain regions through the parasitic capacitances $C_{S,p}$ and $C_{D,p}$, as can be seen in figure 4.4. In this model C_S and C_D have constant values and are tuned to obtain a SS value and

a drain-induced barrier lowering (DIBL) consistent with the reference technology [122, 164]. It is important to note that also the semiconductor intrinsic capacitance C_{sct} has been split between the drain and source terminals, as there is no bulk electrode for the silicon film, leading to:

$$C_{sct} = C_{sct,S} + C_{sct,D} \tag{4.6}$$

The parasitic capacitances $C_{S,p}$ and $C_{D,p}$ influence the electrostatics when calculating the energy profile at the interface, as they are responsible for a charge density contribution Q_P that affect the Neumann boundary condition of the Poisson equation as

$$Q_P = C_{S,p}(\varphi_s - V_S) + C_{D,p}(\varphi_s - V_D) \ . \tag{4.7}$$

Due to the symmetry of our device we considered $C_{S,p}$=$C_{D,p}$ so that the contributions from source and drain differ only due to applied V_S and V_D values. Another important remark we want to highlight is that equation (4.7) assumes a surface potential φ_s at the flat-band condition equal to zero. The potential profile obtained in such a way is representative of a nanoscaled device even if the 2D Poisson problem is not actually solved, and it can be effectively used to analyze SCE in MOSFETs and NC-FETs.

An example of a I_{DS} characteristic obtained from our simulator, for a conventional scaled DG MOSFET, is reported in figure 4.5 and compared against an ideal MOSFET current-voltage relation having 60mV/dec sub-threshold swing. The details on the effects of SCE due to parasitic capacitances on NC-FETs will be discussed in the following chapters.

4.1.2 A simple transport model

To calculate the current and the conductance of a 1D semiconductor, we used a simple ballistic top-of-the barrier model sketched in figure 4.6 [68, 164, 165]. It is important to highlight that, as the model is purely ballistic, scattering effects are ignored, while the degradation of the output conductance due to aggressive scaling are included via the $C_{S,p}$ and $C_{D,p}$ parasitic capacitances discussed in the previous section.

The ballistic model of the current derives directly from a simplified version of the Boltzmann Transport Equation (BTE) [166], in which we also assume translational invariance in the direction y. This means that we analyze the transport only in the x direction and that the total current will be proportional to the width W of the device. Entering the detail of the BTE solutions for the ballistic regime goes beyond the scope of this thesis, but a basic discussion is reported here for completeness.

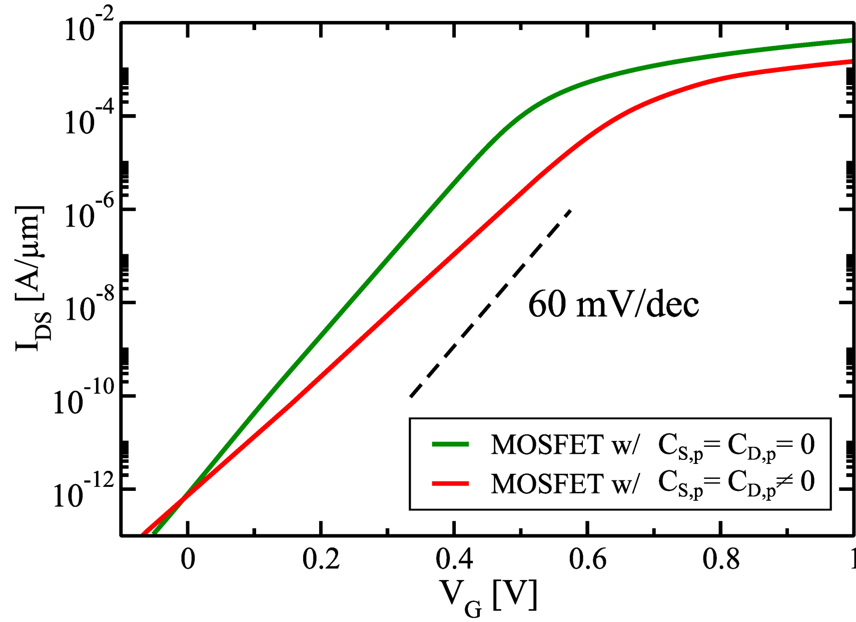

FIGURE 4.5. Comparison between an ideal DG MOSFET, with a SS=60mV/dec, and a more realistic device affected by SCE, with a SS ≈75mV/dec. The simulation setup is characterized by a device with an EOT=0.5nm and a silicon thickness T_{Si}=7nm and an applied V_{DS}=0.5V. The values for $C_{S,p}$=$C_{D,p}$ are set to zero for the ideal MOSFET and to 7.3fF/μm^2 for the SCE case. The curves are matched at I_{off}=1 pA/μm.

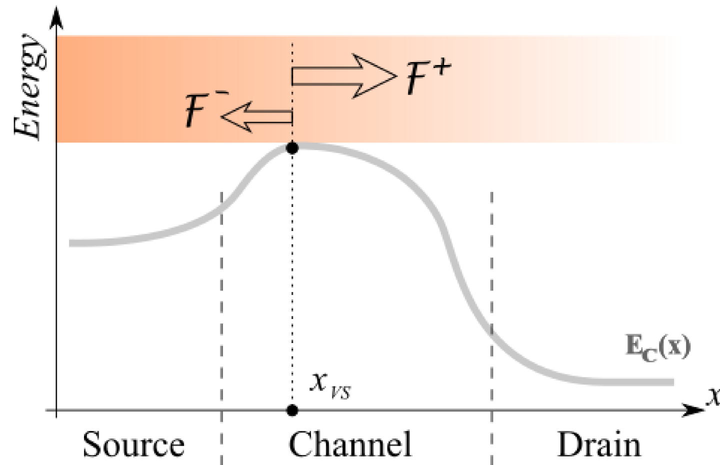

FIGURE 4.6. Conduction band profile along the transport direction x. The virtual source, whose coordinate is x_{VS}, is the maximum point of the CB profile in the channel and discriminates the states of source and drain that contribute to the current fluxes $\mathcal{F}^{\pm}$.

We can essentially identify two carrier fluxes moving in opposite directions, here denoted with $\mathcal{F}^+$ and $\mathcal{F}^-$ for the fluxes from source to drain (i.e. $k_x > 0$) and in the opposite direction (i.e. $k_x < 0$) respectively:

$$\mathcal{F}_i^{\pm} = \left(\frac{K_B T}{\pi}\right)^{3/2} \frac{\sqrt{m_{tr}}}{\sqrt{2}\hbar^2} F_{1/2}(\eta_i^{(S,D)}) \ . \tag{4.8}$$

Here the equation is written for the contribution of the i-th subband that has an effective mass m_{tr} in the transport direction, the $F_{1/2}$ is the Fermi-integral of order 1/2 and η_i is the same coefficient as in equation (4.4), but computed for the subband energy ε_i (for a specific valley) and at the coordinate x_{VS} of the virtual-source.

For the top-of-the-barrier model of figure 4.6 that consider a Fermi-Dirac distribution of charges at the source and drain, the current I_{DS} per width can be written as sum of the difference between the carrier fluxes injected from source and drain, for each subband-valley (ν, n):

$$\begin{aligned} I_{DS} &= q \sum_{\nu,n} \left(\mathcal{F}^+_{(\nu,n)} - \mathcal{F}^-_{(\nu,n)}\right) \\ &= \frac{q(K_B T)^{3/2}\sqrt{m_{tr}}}{\sqrt{2}\pi^{3/2}\hbar^2} \sum_{\nu,n} n_\nu \left(F_{1/2}(\eta^S_{\nu,n}) - F_{1/2}(\eta^D_{\nu,n})\right) \end{aligned} \tag{4.9}$$

It is important to note that the difference of the fluxes in equation (4.9) is due to the voltage V_{DS} between the source and drain regions, thus for V_{DS}=0 there is no net flux of carriers that contributes to the I_{DS}, as $\mathcal{F}^+_{(\nu,n)}$=$\mathcal{F}^-_{(\nu,n)}$. We also mention that this model has been recently extended [122] to a quasi-ballistic regime by introducing a proper *back-scattering* (o reflection) coefficient, that was originally proposed to describe the qualitative behavior of I-V characteristic in nanoscale devices by Lundstrom [165, 167–169].

Equation (4.9) allows us also to extract the value of the ballistic conductance G_d [68], that we have also used to evaluate the NC-FET performances [110, 170], as discussed in the following chapters. The expression of G_d, for a V_{DS} that tends to zero, can be obtained by definition G_d=$[\partial I_{DS}/\partial V_{DS}]$:

$$G_d = \left(\frac{K_B T}{\pi}\right)^{3/2} \frac{q}{\sqrt{2}\hbar^2 V_{th}} \sum_{\nu,n} n_\nu \sqrt{m_{tr}}\, F_{1/2}(\eta^S_{\nu,n}) \tag{4.10}$$

where n_ν is the valley degeneracy and all the other symbols have their standard meaning.

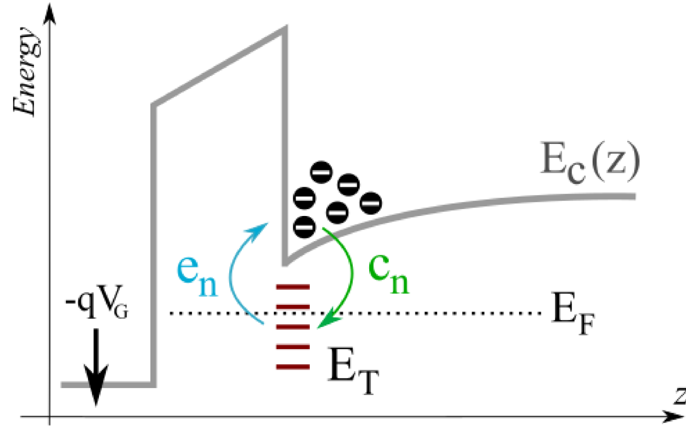

FIGURE 4.7. Band profile in the quantization direction z: the trap states are here placed at the oxide-semiconductor interface at different energetic levels E_T. e_n and c_n are the emission and capture rates respectively and describe the probability of the transitions between E_T and E_C, as depicted in the figure.

4.1.3 Interface traps

An original part of our research on NC-FETs refers to the numerical analysis of the behavior of the device when different concentrations of interface traps are introduced in simulations [122, 170]. To properly characterize the dynamics of those defects we relied on the simple but effective Shockley-Read-Hall (SRH) recombination model [160, 161].

We also decided to limit our analysis to acceptor-like traps in the upper part of the energy-gap, and to consider emission and capture only with conduction band (see figure 4.7). Such trap-states are electrically neutral when the electron is absent and become negatively charged when the electron is captured (similarly to dopants). The starting point to describe this generation-recombination problem is the balance of charges in the semiconductor [35, 162]:

$$\begin{cases} \dfrac{\partial n}{\partial t} + U_n - \dfrac{1}{q}\nabla \cdot \mathbf{J}_n = G_n \\ \dfrac{\partial p}{\partial t} + U_p + \dfrac{1}{q}\nabla \cdot \mathbf{J}_p = G_p \end{cases} \tag{4.11}$$

where n and p are the electron and hole charge densities, $\mathbf{J}_{(n,p)}$ are the current densities in the transport direction, $U_{(n,p)}$ are the thermal recombination rates while $G_{(n,p)}$ are the non-thermal recombination rates. To introduce the trap-assisted transitions, we have to add a continuity equation for traps:

$$\frac{\partial n_a}{\partial t} + U_{na} - \frac{1}{q}\nabla \cdot \mathbf{J}_{na} = G_{na} \quad . \tag{4.12}$$

The continuity condition in equation (4.12) can be further simplified

by observing that in crystalline semiconductors the trap current density $\mathbf{J}_{na}$ can be neglected that, for $G_{na} \approx 0$, simplifies equation (4.12) as

$$\frac{\partial n_a}{\partial t} = -U_{na} \ . \tag{4.13}$$

In our framework we neglect the non-thermal recombination terms, meaning that in equations (4.11) and (4.12) we set G_n=G_p=G_{na}=0, then we can observe that the total current density is the sum of the separate contributions $\mathbf{J}$=$\mathbf{J}_n$+$\mathbf{J}_p$+$\mathbf{J}_{na}$. Adding together equations (4.11) and (4.12) we obtain the continuity conditions for all the charges involved:

$$q\frac{\partial [p-n-n_a]}{\partial t} + \nabla \cdot \mathbf{J} = q\left(U_n + U_{na} - U_p\right) \ . \tag{4.14}$$

The following step is to properly express the SRH thermal-recombination rate in the right-hand-side of equation (4.13), in particular this theory describes the phenomena related to a specific trapping level E_t, but it can be easily extended to multiple levels by adding the single contributions. The trap recombination term is expressed as [35, 171]

$$U_{na} = e_n n_a - c_n\left(N_t - n_a\right) \ \Rightarrow \ \frac{\partial n_a}{\partial t} = c_n\left(N_t - n_a\right) - e_n n_a \tag{4.15}$$

where e_n and c_n are the emission and capture rates respectively (in [s^{-1}]), while N_t is the density of traps at that specific energy level. It is necessary then to characterize quantitatively e_n and c_n for the semiconductor under test to compute correctly the dynamics of the traps:

$$\begin{cases} e_n = \sigma v_{th} N_C \cdot \exp\left(\dfrac{E_t - E_C}{K_B T}\right) \\ c_n = e_n \cdot \exp\left(\dfrac{E_{FS} - E_t}{K_B T}\right) \end{cases} \tag{4.16}$$

Equations in the system (4.16) contain only physical semiconductor parameters and distances in energy levels: σ is the interaction cross section of the trapping state, v_{th} is the thermal velocity for the majority carriers, N_C is the density of states in the CB, E_C and E_{FS} are in our case the energy associated to the lowest subband of the CB and the Fermi-level at the source. The total surface charge density due to interface traps can then be computed as $Q_{t,n}$=-q$\sum_{E_t} n_a(E_t)$. In figure 4.8 we report the response frequency of interface traps versus the distance of the trap energy level from the CB: the further the energy level is from the CB (i.e. *deep* into the energy-gap), the smaller the emission rate is. This means that the response of traps to an external signal depends on their depth and, obviously, on the frequency of the signal itself.

The right equation in (4.15) can be rearranged to express the probability of trap occupation by simply dividing the left- and the right-hand

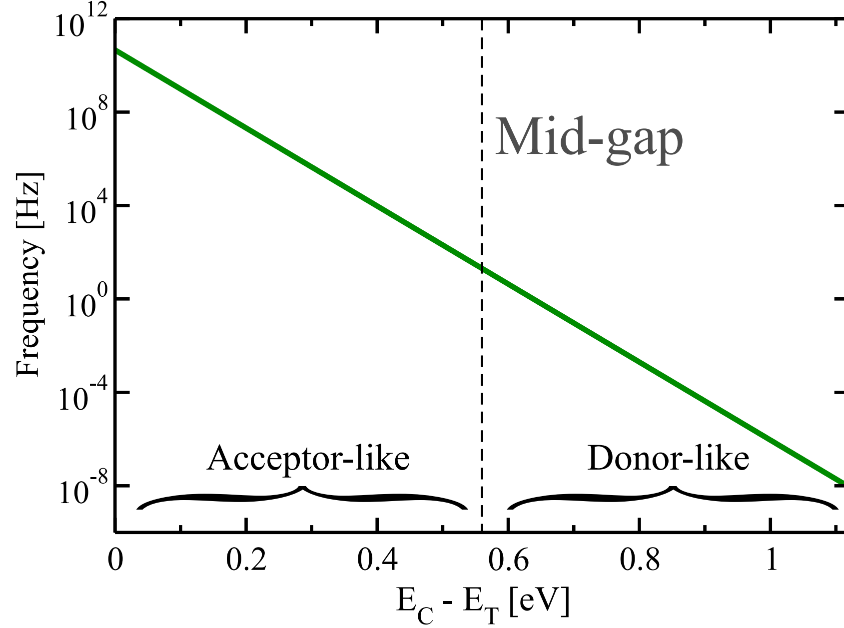

FIGURE 4.8. Response frequency of interface traps in p-silicon [171], according to the SRH model, on their depth E_C-E_T. The frequency is computed as f=[$1/2\pi\tau$], where τ=e_n^{-1} is the time constant of the trap at a specific energy level. The acceptor-like traps are usually placed in the upper part of the energy gap.

side by N_t, in fact we can set P_t=n_a/N_t and then obtain the dynamic behavior of P_t:

$$\frac{\partial P_t}{\partial t} = c_n(1 - P_t) - e_n P_t = e_n \left[\exp\left(\frac{E_{FS} - E_t}{K_B T}\right) \cdot (1 - P_t) - P_t\right] \quad (4.17)$$

This equation is the one actually implemented in our device simulator [122], and also suggests an interesting result for the static behavior of traps, within the validity of the proposed framework. In fact it is easy to see that setting to zero the time derivative in equation (4.17) we obtain a Fermi-Dirac occupation for traps:

$$\begin{aligned} 0 &= e_n \left[\exp\left(\frac{E_{FS} - E_t}{K_B T}\right) \cdot (1 - P_t) - P_t\right] = \\ &= \exp\left(\frac{E_{FS} - E_t}{K_B T}\right) \cdot (1 - P_t) - P_t \\ \Rightarrow P_t &= \frac{1}{1 + \exp\left(\frac{E_{FS} - E_t}{K_B T}\right)} \end{aligned} \quad (4.18)$$

The static framework implies that all the traps are responding to the external stimulus without any delay, thus all of them are contributing to the whole electrostatics of the device: this is the framework we used in our first contribution about the influence of interface traps in NC-FETs [170], and the results will be discussed in the next chapter.

4.1.4 Numerical solution of the model system

The simulator developed in the PhD project to describe the NC-FET essentially considers the device as a series of capacitances, thus we can exploit the Kirchhoff's law for the series and apply it to the voltage-charge relations of each capacitor. This allows us to easily describe different combinations of materials, thicknesses and time-dependent input signals, and analyze all the internal quantities of the device, such as charge densities, energies and voltages.

Static simulations

The static simulations of NC-FETs, as no dynamics is involved neither for the ferroelectric nor for interface traps, are obtained directly from the Schrödinger-Poisson solver. This module enforces a polarization P as boundary condition at the silicon-oxide interface, which is shared between layers due to the continuity of vector D. Each polarization P value univocally determines the voltage drop in the semiconductor (and also the currents, according to our ballistic model), as well as the voltage drops across the dielectric and the ferroelectric layers (V_{Ox} and V_{Fe} respectively). Consequently, for each value of polarization, the external voltage at the gate terminal V_G is computed as one of the outputs of the solver, as we can always write the Kirchhoff's law:

$$V_G(P) = \varphi_s(P) + V_{ox}(P) + V_{Fe}(P) + V_{FB} \tag{4.19}$$

where φ_s is the surface potential of the semiconductor, V_{Fe} is computed with the static LKE and V_{FB}=[Φ_M-χ_{sct}] is the voltage drop due to the alignment of Fermi-levels at zero electric field (corresponding to the concept of *flat-band* voltage in planar MOSFETs [68]). Once the $V_G(P)$ relation is obtained, it is possible to analyze also other output characteristics for the device, such as I-V curves, by mapping the correspondence between P, V_G and the desired quantity (e.g. I_{DS}, G_d or C_{sct}). The traps behavior is here implemented in its static description: the traps density D_{it} follows a Fermi-Dirac distribution centered in the gap and with a given density, and directly computed in the Schrödinger-Poisson iterative solver.

The limitations of this type of simulations are evident and tend to give unrealistic results, as real NC-FETs are strongly dependent on dynamic effects (due both to ferroelectric and traps), but can still lead to some insightful suggestions on the behavior of ferroelectric devices and on the device of NC-FETs [135].

Dynamic simulations

The NC-FET dynamic simulator, however, works with a somewhat different approach: it essentially solves the dynamic LKE (both for the single- or multi-domain case) together with the dynamic SRH problem for a generic time-dependent voltage input, leading to a consistent value for the polarization which allows us to calculate the voltage drops across other materials.

As first step the code requires a look-up table for the voltage-charge relation of the semiconductor: this is provided by the Schrödinger-Poisson solver which saves into a text file the total charge density in the silicon (we recall that in our analyses we assume $P \approx Q$) and the correspondent values of the surface potential $\varphi_s(P)$. This procedure univocally determines the φ_s(P) relation for a given type of semiconductor, giving us a complete description of the electrostatics of this layer. In this look-up table we also insert, for each value of P, the corresponding currents (at a given V_{DS}), capacitances, conductances and energies for the band minima in the semiconductor.

The second step is the characterization of the physical structure of the device, such as thicknesses and material properties (e.g. electric permittivities and coefficients for the LKE and interface traps), and the shape of the desired input voltage signal $V_G(t)$. Once the simulation setup is described, the code starts solving the dynamic LKE (see equations (3.7) and (3.8)) and the dynamics of traps at each n-th time-bin with a Runge-Kutta algorithm. This leads to a specific value at the n-th step for P_n and $Q_{t,n}$, that is the trapped charge density, and in particular we can set

$$V_{Fe,n} = V_G(t_n) - V_{Ox,n} - \varphi_{s,n} \tag{4.20}$$

in equations (3.7) and (3.8) to take into account the specific applied voltage and the voltage drops across other layers. Due to the screening effect of traps on the semiconductor potential, the φ_s-P relation need to be adjusted to take into account the charge sheet $Q_{t,n}$ at the oxide semiconductor interface: for this reason the look-up table is read with the value [P_n-$Q_{t,n}$] instead of simply using P_n.

As the system is described by differential equations , the code employs an automatic time-step adjustment to obtain an accurate result at each iteration: in this case the threshold to accept or reject the new step is based on the variation of the surface potential computed in two subsequent time-bins. Other characteristics of the device can be calculated as post-processes [149] in fact, once the simulation ends and the definitive polarization-time $P(t)$ relation is saved, we can re-map the values stored in the look-up table according to evolution of $P(t)$ and obtain other quan-

tities such as currents, capacitances or conductances.

A final remark on the multi-domain NC-FET simulation is that this problem connects a 2D ferroelectric to a semiconductor described by a 1D model. The procedure in this case is actually similar to the one described above, but with two main differences: the first is that the LKE is computed in parallel for each domain with all the coupling factors needed to describe their interactions, and the second is that the look-up table for the semiconductor is read by averaging the value of the polarizations from the ferroelectric. The latter solution is an approximation as, in principle, a full 2D simulator including a description for the semiconductor in the transport plane would be more appropriate. For this reason the multi-domain simulator has been mainly used to reproduce experiments on the ferroelectric characterization (i.e. done typically on large area metal-ferroelectric-oxide-semiconductor capacitors) in which the transport in the semiconductor is not relevant, while for nanometric NC-FETs has been used the more realistic single-domain approach [3,122].

4.2 Calibration against experiments

An important part of our work was the calibration of our models against different sets of experiments on different kind of ferroelectrics capacitors (e.g. HZO [2,108,111], Si:HfO2 [1,3] and BaTiO3 [38]). The calibration of the coefficients a, b, c for the LKE has been done with the multi-domain simulator and with the procedure explained in section 3.3.

The procedure starts by digitalizing the P-F (or P-V) experimental curves in the literature and then extracting the values of the remnant polarization P_r at zero field, the coercive polarization P_c and the coercive field F_C (or the correspondent voltage V_C). The following step is to simulate the device structure within our code by setting the material parameters and the physical thicknesses. In particular is important to choose the number of domains that may be present in the ferroelectric and also the dispersion related to F_C and P_r. This procedure assumes a symmetric P versus field characteristic, and thanks to the matrix in (A.14) it is possible to extract a first set of parameters for the LKE. With those coefficients we are now able to run the simulation with the same setup as in the experiment. The results obtained from this approach usually show already a good agreement with experiments, but further adjustment directly on the coefficients are useful to enhance the quality of the calibration. For the calibration of the damping factor ρ we assume that, if not otherwise indicated, the reported results are not affected by dynamic effects of ferroelectrics at the used frequency.

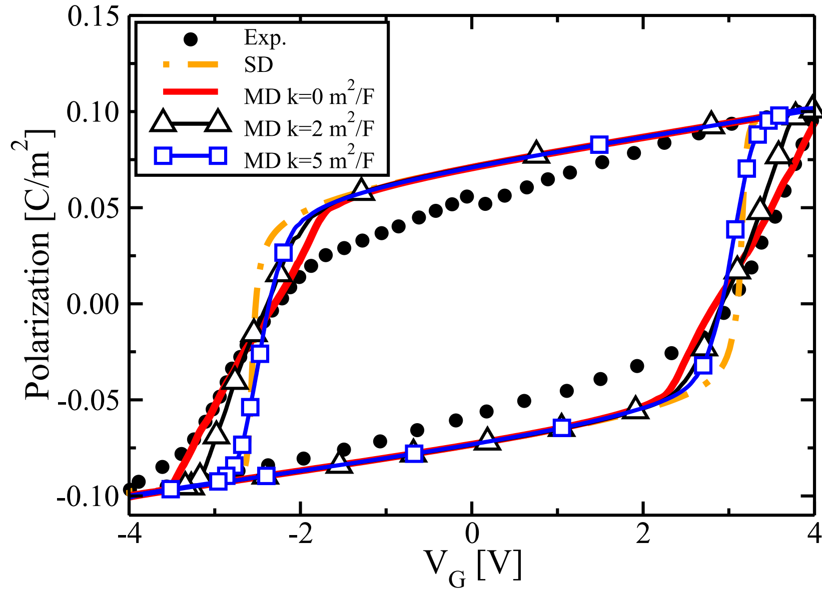

FIGURE 4.9. Polarization versus voltage for an HZO/SiO_2/n+Si test structure with T_{Fe}=10nm [2]. Calibrations with single- and multi-domain simulations are compared to experiments: the best fitting is obtained with a value of k=0m^2/F, meaning that the coupling between domains is negligible in this case. Both experiments and simulations are run with a triangular V_G waveform input with f=3.5KHz, that corresponds to a case with negligible dynamic effect for this sample.

Sometimes is necessary to extend the LKE equation to the seventh grade polynomial in order to obtain a better matching with experimental results [110]: this introduces another coefficient in the LKE, thus it is required an additional equation for the linear system in (A.14) that can be obtained by choosing another point on the P-F characteristic. As the seventh grade also introduces another inflection point in the curve, it is important to calibrate its coefficient in order to move this critical point outside the operating region of interest.

Possible asymmetries in the experiments, such as rigid shifts of the curves on the F-axis or different slopes in the switching regions, this can be explained by the presence of semiconductor layers used, for instance, as substrates or contacts (if heavily doped). This solution is widely used and results in an asymmetric voltage-charge relation, that depends on the operative region of the semiconductor, such as inversion, depletion or accumulation. Our approach allows us to consider those effects and we verified that this helps improve the agreement with experiments.

Another property that emerges from multiple sets of experiments is the dependence of the P_r on the thickness T_{Fe}. This dependence is difficult

Material	a $[m/F]$	b $[m^5/F/C^2]$	c $[m^9/F/C^4]$	d $[m^{13}/F/C^6]$
HZO 10nm [2]	$-1.28\cdot10^{10}$	$2.53\cdot10^{12}$	$-1.62\cdot10^{14}$	$4.01\cdot10^{15}$
HZO 10nm [111]	$-1.51\cdot10^{9}$	$3.32\cdot10^{10}$	$2.2\cdot10^{11}$	-
HZO 5nm [108]	$-6.21\cdot10^{9}$	$4.48\cdot10^{12}$	$-1.72\cdot10^{14}$	$1.12\cdot10^{16}$
Si:HfO_2 8nm [3]	$-4.99\cdot10^{8}$	$3.98\cdot10^{9}$	$2.47\cdot10^{10}$	-
Si:HfO_2 5nm [3]	$-2.59\cdot10^{8}$	$7.90\cdot10^{9}$	$2.76\cdot10^{8}$	-
Si:HfO_2 10nm [1]	$-8.57\cdot10^{8}$	$2.01\cdot10^{10}$	$-5.11\cdot10^{10}$	-
$BaTiO_3$ 200nm [38]	$-1.01\cdot10^{7}$	$-8.9\cdot10^{8}$	$4.5\cdot10^{9}$	-

TABLE 4.1. LKE coefficients extracted from experimental P-F characteristics with the proposed procedure.

to characterize, hence also hard to include into our calibration process. There are two possible approaches that can be followed to address this issue: the first is to assume a simple linear dependence of P_r on T_{Fe}, and this works well for small variations of the thickness around the nominal value, while the second solution is to extract different sets of coefficients for each T_{Fe} from the available measurements.

The figure 4.9 exemplifies a calibration performed by using a set of experiments, reported by the University of Notre Dame [2], and used for a large part of our analyses. It can be easily seen that, in that specific case, the best-fit is obtained with the multi-domain model and for a coupling factor k=0 m^2/F, while higher values of k or the single-domain model give steeper switching branches compared to experiments. The slope and the smoothness of the switching branches depend, respectively, on the dispersion of the coercive voltage and on the number of domains used in the numerical model. In this respect the single-domain approach is not expected to be suitable for characterization of big layers of ferroelectrics. The extracted coefficients for the measurements in figure 4.9 and for sets of other materials are reported in the table 4.1.

It is important to note that this calibration method is more effective and precise when the experimental P-V curve has a large hysteresis, because the switching point (i.e. the values of P_C and V_C) can be easily located.

To further validate the effectiveness of our calibration method for ferroelectric LKE coefficients, we decided to compare the results at device level by running some simulations to reproduce the experimental transfer characteristics described in [3], as can be seen in figure 4.10. The simulated NC-FET has a T_{Fe}=8nm of HZO (with the calibrated coefficients reported in table (4.1)) deposited over a dielectric hafnia layer of T_{ox}=1.5nm, while the baseline device has only the dielectric oxide with

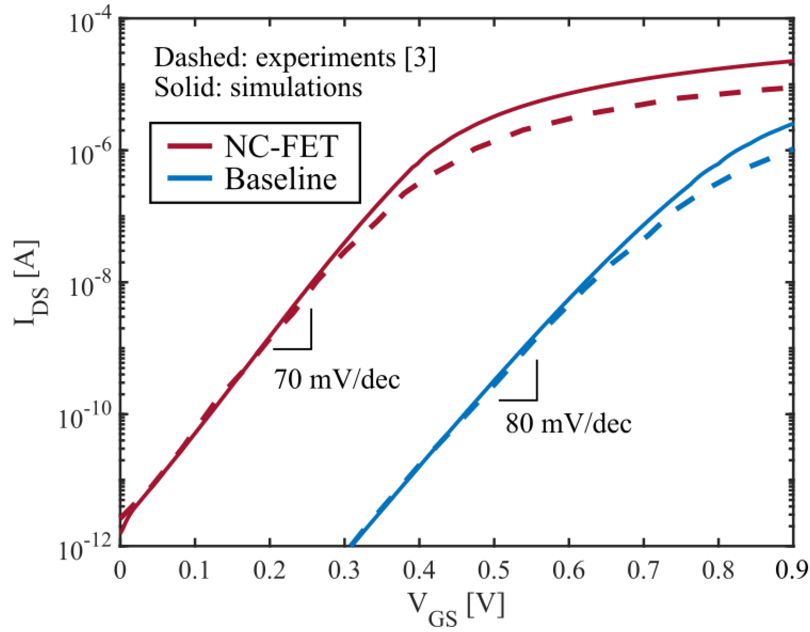

FIGURE 4.10. Comparison between numerical and experimental [3] IV characteristics for both NC-FET and corresponding baseline. The simulated devices are similar to the actual one (consistently with the limited informations reported in the paper), and the the LKE coefficients are calibrated as described in the previous section. The simulated current is normalized to the reported effective width W_{eff}=90nm of the actual device.

the same thickness T_{ox}. The applied input signal at the gate terminal has a frequency of 1MHz, which is slow enough compared to the dynamics of the ferroelectric, and the V_{DS} is set to 50mV. Accordingly to the experiments, the subthreshold swing of the simulated baseline device is degraded to a realistic value of 80mV/dec, and this is obtained by employing the simple description of 2D electrostatic effects in a scaled transistor described in section 4.1.1.

From figure 4.10 it is possible to see that the results for the simulated transistors are consistent with experiments in the subthreshold region, while current in the on-state is overestimated: this can be due to the neglect of series resistances and to the simple monodimensional top-of-the-barrier description employed in our simulator.
This result further suggest the validity of our calibration process for such devices.

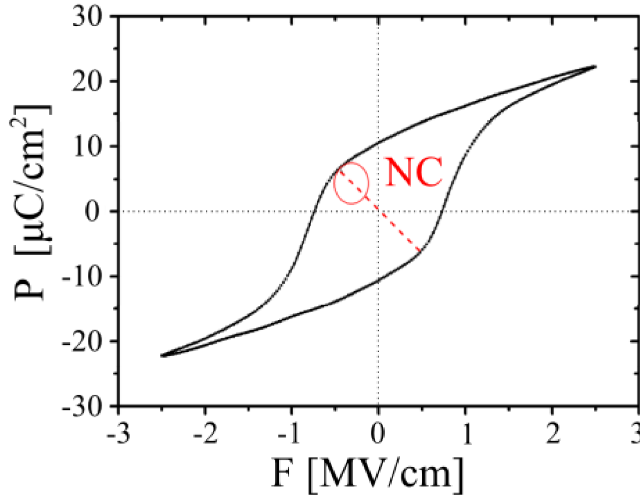

FIGURE 4.11. Experimental P-F curve for a TiN/$HfYO_x$/TiT 10nm ferroelectric capacitor [4]. The negative-slope branch corresponding to the NC behavior, according to LKE, is highlighted by a dashed line.

4.3 State-of-the-art of experimental NC devices

There are several devices described in literature that are supposed to work by exploiting the negative capacitance principle, and we reiterate that this is conceptually different from using the hysteresis of ferroelectrics, in FeRAMs and in ferroelectric neurons for neuromorphic computing [172].

One of the most recent device reaching an SS lower than 60mV/dec over 3 decades of current was presented at the *Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon* by a group of researchers from the Juelich Research Center (Germany) [4]. They analyzed a fully-depleted SOI (FDSOI) MOSFET with a 5nm ferroelectric hafnia doped with Yttrium ($HfYO_x$), and with a large area of 2×2 μm^2. The measurements have been performed firstly on a ferroelectric capacitor to characterize the behavior of the material, as illustrated in figure 4.11, and then on the described NC-FET by applying three different voltage sweeps (from -2V to 2V, from -3V to 3V and then from -4V to 4V): the I_{DS}-V_G curves are reported in figure 4.12.

A robust ferroelectricity is confirmed in 10nm $HfYO_x$ thanks to experiments performed on ferroelectric capacitors: in particular this showed values of 0.72 MV/cm and 12 μC/cm^2 for the coercive field and for the remnant polarization respectively. The results on the NC-FET show subthreshold swings well below the thermal limit of 60mV/dec, but they

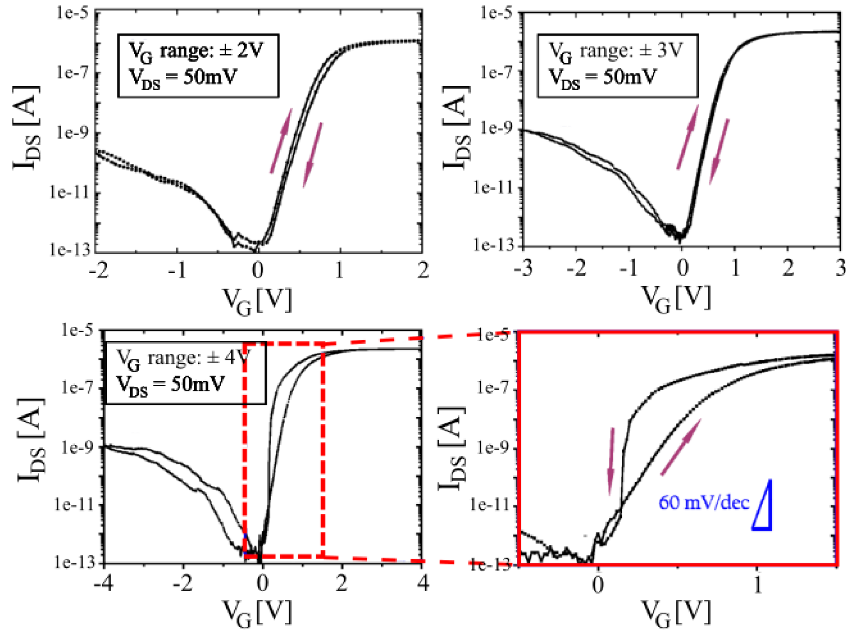

FIGURE 4.12. Experimental I-V transfer characteristics of a NC-FET [4] for three different gate-voltage sweeps and for a V_{DS}=50mV. The lower figure on the right (with a red frame) is a magnification of the case with a V_G=±4V showing an hysteretic characteristic with a SS well below 60mV/dec.

also show an undesired hysteretic behavior, meaning that the ferroelectric is in its unstable state. This suggest that, according to the LKE theory, the matching condition between semiconductor and dielectric-ferroelectric stack tends to fail: this can easily happen when the near- or above-inversion operation for the semiconductor is reached.

Experimental results on NC-FETs, that are designed explicitly for steep-slope operations, show SS lower than 60mV/dec but always accompanied with hysteresis. This feature seems to be hardly avoidable in transistors, due to the difficulties in obtaining a good matching condition as the capacitance of the semiconductor is strongly bias-dependent. The qualitative behavior of these NC devices, in particular the presence of hysteresis, is similar to the one reported in other recent experimental works [2, 173–176], confirming that this is a challenge from a design perspective.

To avoid the problematic presence of large hysteresis in NC-FET characteristics, we probably need to sacrifice the steep-slope operation in the subthreshold region (as will be discussed in the following chapter): in this case the ferroelectric can still be exploited to enhance the ON-state of the device. In fact, in a work presented by Globalfoundries at the

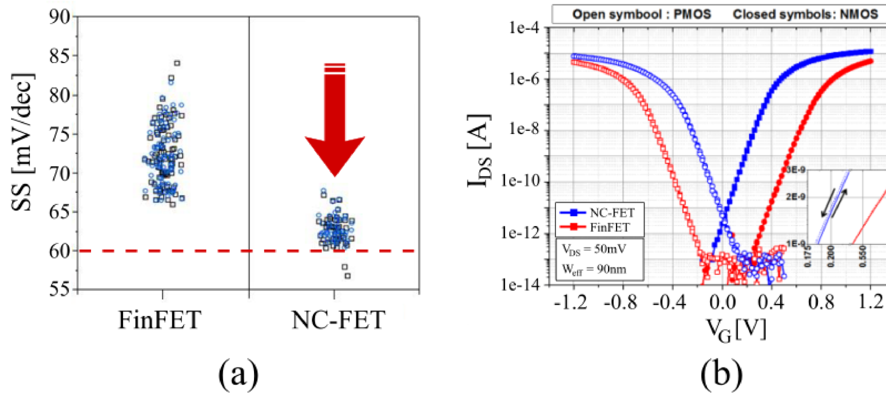

FIGURE 4.13. On the left are reported the values for the average sub-threshold swings measured for both the dielectric (i.e. FinFETs) and the negative-capacitance (i.e. NC-FETs) devices. On the right are presented the I-V characteristics of n-MOS and p-MOS devices, both for conventional FinFETs and NC-FETs: a negligible hysteresis of few millivolts can be barely seen, while the enhancement in the ON-current of NC-FETS is clearly visible.

2017 *IEEE International Electron Devices Meeting* (*IEDM*) [3]. I-V characteristics of a NC-FET exhibit no actual reduction of the SS, but a large ON-current gain compared to its conventional MOSFET counterpart. Experiments were performed by using two large sets of 14nm technology-node FinFETs, one set consisting of conventional CMOS transistors and one set consisting of negative-capacitance devices. The NC-FETs were obtained by growing a ferroelectric layer (silicon-doped hafnia) over the dielectric of the CMOS FinFET, so that the two sets only differ for the presence of the ferroelectric. The comparison between the sets show two important advantages of the NC-FETs: the first is a reduction of the SS, that in conventional FinFETs was over 70mV/dec on average, while in NC-FETs it is reduced almost to the ideal thermal limit (seen figure 4.13(a)). The second effect on transistors, that can be seen in figure 4.13(b), are almost non-hysteretic I-V characteristics with high on-currents, while there are essentially no curves with SS lower than 60mV/dec.

One possible explanation on the working principle of this new NC-FET perspective is presented in our recent work [110] (and explained in the details in the next chapter): essentially the ferroelectric is stabilized directly with the dielectric layer, which has a constant capacitance, so that the semiconductor can no longer induce the instability of the device leading to the desired non-hysteretic behavior.

In the next chapter we will discuss the design options we developed for NC-FETs, focusing in particular on the two possible options: one design aims at a sub-threshold swing reduction below 60mV/dec, while the second option is more focused on the on-state and, in particular, on the

enhancement of the I_{ON} current.

Chapter 5

NC-FETs Design

In this chapter we discuss the design space for negative capacitance transistors, in particular we focus on two important design options corresponding to two different perspectives: the *steep-slope* transistor and the g_m-boosted transistor [110]. Both the approaches are analyzed in details, discussing the differences, the role of interface traps and also the sensitivity to process and temperature variations [122, 170].

For the sake of clarity we report again in figure 5.1(a) the sketch of the double-gate transistor analyzed in our simulations, and the corresponding capacitance network (b). The ferroelectric material, of thickness T_{Fe} and capacitance C_{Fe}, is separated from the channel semiconductor by a dielectric interfacial layer (IL) of capacitance C_{Ox}=T_{ox}/ε_{Ox}: the series capacitance of the gate stack is C_{di}. It is important to note that the capacitance C_{di} is used to discriminate between the two design options discussed in the following sections. For these simulations we used a nanoscale device model comprising a capacitive coupling between the virtual source and the active regions of source and drain, as described in the previous chapter. Moreover we also make use of a reference, *baseline* device that is a conventional UTB-DG MOSFET, with the same characteristics as the NC-FET depicted in figure 5.1, but without the ferroelectric film. Finally, the largest part of our simulations rely on the single-domain dynamic LKE model, which is a simplified but yet defendable model for nanoscale FETs. However, in some cases we have used the multi-domain LKE solver and for such simulations the results are reported in terms of conductances G_d at V_{DS}=0V, in order to remain in a quasi-equilibrium operation, so that inhomogeneities of the semiconductor potential along the transport direction can be considered small.This is essentially due to the transport model employed in this study, which is not able to take into account 2D effects in the semiconductor. Similarly it is not clear which is the actual effect of the ferroelectric inhomogeneous polarization on the physics of the semiconductor, which makes it difficult to describe the semiconductor

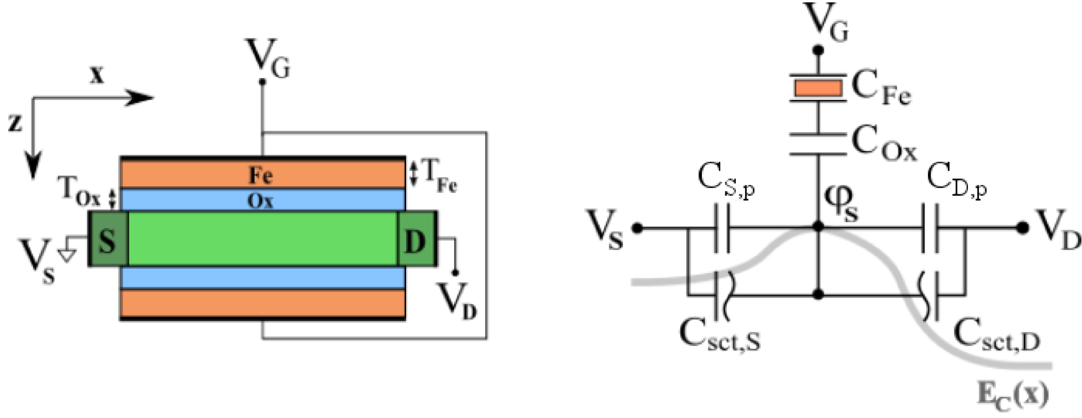

FIGURE 5.1. In (a) we report the sketch of the DG-UTB NC-FET discussed in this chapter, with its capacitive equivalent network (b). This structure is also used as reference for the baseline transistor by setting the ferroelectric thickness T_{Fe}=0nm. The capacitance C_{di} is the series of C_{Fe} and C_{ox} for the NC-FET (for the baseline it is C_{di}=C_{ox}), while $C_{S,p}$ and $C_{D,p}$ are used to describe electrostatic short channel effects. The intrinsic semiconductor capacitance is defined as C_{sct}=$C_{sct,S}$+$C_{sct,D}$.

behavior with the average polarization value.

Conventional baseline DG MOSFET

A conventional UTB-DG MOSFET, with realistic features of electrostatics integrity, has been simulated in order to evaluate the results of our NC-FET designs. Even for the architecture of this device we refer to figure 5.1: this structure is obtained by using an acceptor doping N_A=5·10^{17}cm^{-3}, a semiconductor thickness T_{Si}=7nm, an equivalent oxide thickness for the interfacial layer EOT=T_{ox}=0.5nm and T_{Fe}=0nm, meaning that no ferroelectric is embodied in the gate stack. In figure 5.2 we show the characteristics of this device in terms of I-V and C-V curves, that are obtained from the numerical simulation. The capacitances used as a coupling between the top-of-the barrier and drain/source regions, namely $C_{D,p}$ and $C_{S,p}$, were set so as to have an *SS* of approximately 75mV/dec and a DIBL of 92mV/V, resulting in $C_{D,p}$=$C_{S,p}$=7.2 fF/μm^2. Moreover, in figure 5.1 it can be seen that, according to the DG-UTB structure, the total intrinsic capacitance of the semiconductor C_{sct} is split into two contributions related to source and drain regions, such that C_{sct}=$C_{sct,S}$+$C_{sct,D}$, while the total internal parasitic capacitance is defined as C_P=$C_{D,p}$+$C_{S,p}$.

In figure 5.2(b) it can be seen that the total capacitance of the semiconductor C_T=C_{sct}+C_P in the sub-threshold region, is essentially dominated by the value of the parasitic components C_P. The I-V characteristics confirm that, due to the capacitances C_S and C_P, the *SS* is higher than

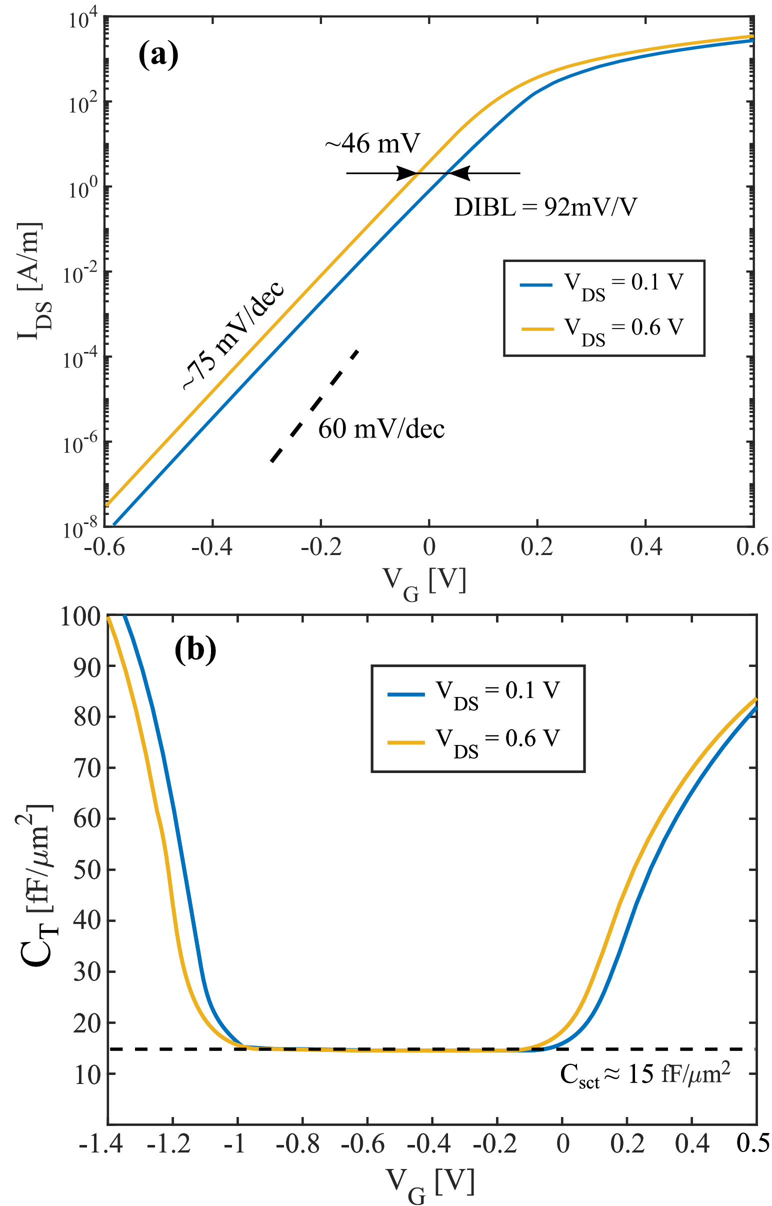

FIGURE 5.2. Transfer characteristics of the conventional CMOS baseline transistor. In (a) we report the I_{DS}-V$_G$ curves for two source-drain voltages: it is clearly observable the presence of DIBL due to the presence of parasitic components C_P that degrade the electrostatic integrity. In figure (b) we show C_T=[C_{sct}+C_P] versus V_G characteristics, and it is evident that the floor value in the subthreshold region is practically equal to the parasitic component C_P.

60mV/dec and also the DIBL is 92mV/V.

The simulations on this conventional transistor are used as reference to evaluate the negative capacitance design concept proposed in our recent works [110, 122, 170].

5.1 Design space for NC-FETs

As it can be inferred from the discussion in previous chapters, the NC-FET is a device that can be designed with two different perspectives. We recall, from the previous chapter, that the stability of the negative capacitance operation essentially depends on the difference between the magnitude of the ferroelectric negative capacitance $|C_{Fe}|$ and the value of the total positive capacitance in series to it. We want to emphasize that this aspect plays a fundamental role also in the description of NC-FETs, where we are considering the more general relation between C_{di} and the semiconductor, thus we will refer to this dependence on the difference between capacitances in the transistor as *capacitance matching*. The capacitance matching condition contribute to identify the different regions of our design space in terms of operative temperatures and thicknesses of ferroelectric and interfacial layers.

The qualitative picture is illustrated in figure 5.3 for different temperatures and thicknesses.

For C_{di}<0, that corresponds to $|C_{Fe}|$<C_{ox}, we have a $steep - slope$ NC-FET design, that allows sub-60mV/dec operation in the sub-threshold region. This operation can be achieved for large T_{Fe} and small enough EOTs, once the material properties of the ferroelectric (i.e. P_r, F_c and P_c) and of the IL (i.e. ε_r) are set. This design option will be further discussed in the following section in more details.

For C_{di}>0 (namely $|C_{Fe}|$>C_{ox}) the transistor is not operating as a steep-slope device, but the NC operation of the ferroelectric can still be exploited to improve the on-state, by boosting the I_{on} current: for this reason we labelled this design as $g_m - boosted$ device. This design region is relatively narrow compared to the previous one, because the boosting effect requires to stay close to the C_{ox}=$|C_{Fe}|$ condition (see the next sections). The features of this concept are very promising and are interesting also from a manufacturing point of view.

The C_{ox}=$|C_{Fe}|$ condition is considered as a boundary condition that discriminates between the two approaches, and is both thickness and temperature dependent. The thicknesses affect directly the values of the capacitances, while the temperatures strongly affects the ferroelectricity

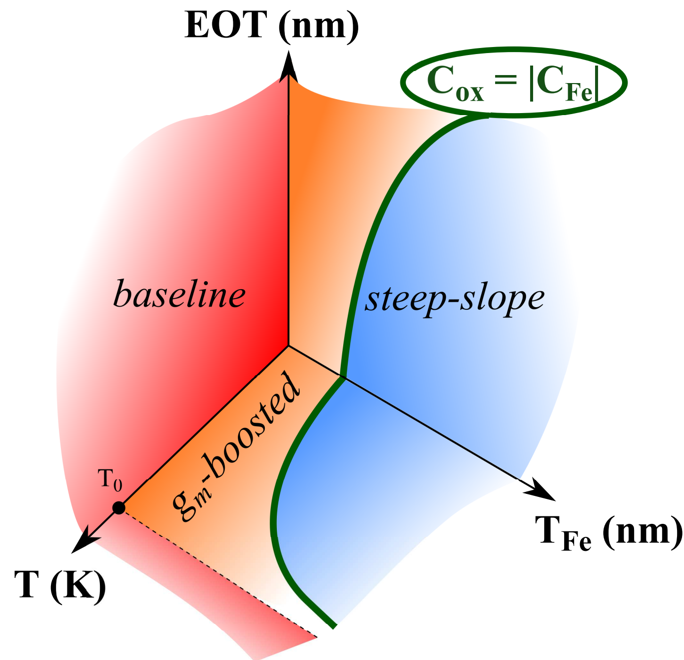

FIGURE 5.3. Qualitative design space for the NC-FETs in terms of ferroelectric thickness T_{Fe}, EOT of the interfacial layer and temperature T. The baseline transistor space corresponds to the case in which T_{Fe}=0nm or for a temperature above the Curie temperature T_0. The green line describes the condition of C_{ox}=$|C_{Fe}|$, which is the limiting case that discriminates between the two NC designs.

itself. Moreover when the temperature reaches the Curie temperature T_0, the ferroelectric behavior tends to completely vanish, dragging the transistor back to a conventional CMOS operation.

In the following sections the different design approaches are discussed in more details, and compared with the conventional MOS technology.

5.2 Focus on the off-state operation: steep-slope devices

We start by focusing on the off-state region of the transistor, in particular on the improvement of the swing of the I-V characteristic in the subthreshold region: this reflects the original idea by S. Salahuddin for a *steep-slope* NC-FET [38]. The fundamental requirement for this design approach is the presence of a negative capacitance in the gate stack. In the original case analyzed in [38] there was only C_{Fe}, but here we consider the whole stack capacitance C_{di}.

Before proceeding in analyzing the off-state of the device, we need to

introduce a simple expression for the subthreshold swing, based on the voltage-divider model reported in figure 5.1 and obtained neglecting the influence of possible interface traps (for now):

$$SS = \frac{K_B T}{q} ln(10) \cdot \left(\frac{\partial \varphi_s}{\partial V_G}\right)^{-1} = 60mV/dec \cdot \left(1 + \frac{C_{sct} + C_P}{C_{di}}\right) \quad (5.1)$$

where C_{sct} is the semiconductor intrinsic capacitance and C_P=$C_{S,p}$+$C_{D,p}$ is the capacitance due to the SCE model (see section 4.1.1). In this case we want the C_{di} to be negative and explicitly write it as C_{di}=-$|C_{di}|$, so that the term $[\partial\varphi_s/\partial V_G]^{-1}$ in equation (5.1) can be made smaller than one by tuning the capacitance matching:

$$\left(\frac{\partial \varphi_s}{\partial V_G}\right)^{-1} = \left(1 - \frac{C_{sct} + C_P}{|C_{di}|}\right) < 1 \quad \Rightarrow \quad SS < 60mV/dec \ . \quad (5.2)$$

It is important to note that, in principle, the voltage gain expressed in equation (5.2) can also assume negative values, which is an undesired effect leading to instability and thus to hysteresis (as discussed in section 3.4). This behavior, in particular, arises when the capacitance (C_{sct}+C_P) becomes larger than $|C_{di}|$, and for this reason we refer to this situation as *capacitance crossing*.

We here recall that C_{sct} is strongly bias dependent and, in particular, in UTB devices it tends to be much smaller than $|C_{di}|$ in the sub-threshold region, which makes it difficult to obtain a good capacitance matching to effectively lower the SS value. One possible way to improve the situation might be the increase of C_P, but this also tends to degrade SS and the DIBL of the baseline transistor. For this reason in a well behaved FET C_P is typically a small fraction of C_{Ox}. The role of interface traps will be discussed in the details in the following section, but the qualitative contribution to the SS is similar to the one of C_P and, in principle, they can improve the SS when C_{di}<0.

Figure 5.4 presents several NC-FET I-V characteristics for different ferroelectric thicknesses and with an EOT=0.5nm. Here the ferroelectric parameters are independent of T_{Fe}, and the matching condition between the ferroelectric and dielectric capacitance changes with T_{Fe}. The simulation was run for a NC-FET with a silicon thickness of 7nm, an EOT=0.5nm and three T_{Fe} values of HZO, whose ferroelectric parameters were calibrated against experimental data from [2] and reported in table 5.1.The input signal V_G(t) is a triangular voltage waveform, ranging from -0.5V to 0.4V, and with a frequency of 1MHz. The frequency an the resistivity of the ferroelectric, ρ= $5\Omega m$, are chosen so that the dynamic effects due to domain switching are negligible. Figure 5.4 also shows that the sub-60mV/dec operation is inevitably accompanied by hysteresis, in

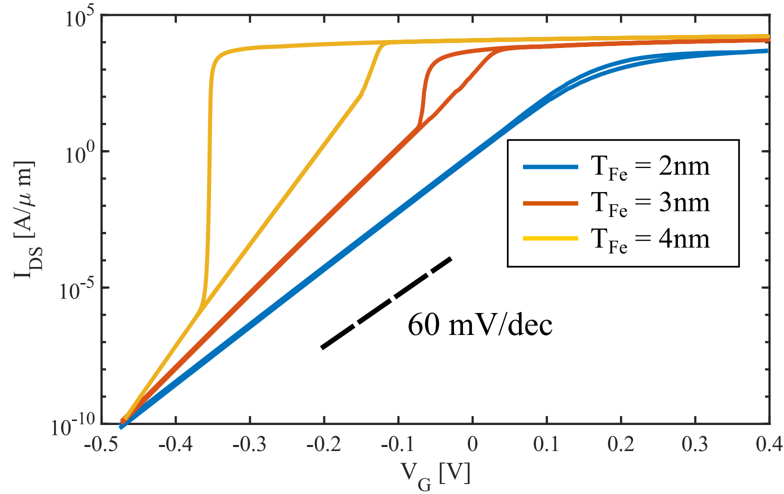

FIGURE 5.4. I_{DS} versus V_G characteristics for a steep-slope UTB NC-FET and for three different T_{Fe}. The EOT and the work-function are set to 0.5nm and 4.05eV, while V_{DS}=0.6V. It is visible the enhancement of the slope in the sub-threshold region, accompanied with the enlargement of hysteresis, when the T_{Fe} is increased.

Material:HZO	Thickness: 10nm
a $[m/F]$	-1.28·10^{10}
b $[m^5/F/C^2]$	2.53·10^{12}
c $[m^9/F/C^4]$	-1.62·10^{14}
d $[m^{13}/F/C^6]$	4.01·10^{15}
k $[m^2/F]$	1.0e-3
ρ $[\Omega m]$	5.0

TABLE 5.1. LKE coefficients extracted from experimental P-F characteristics in [2] and used in figure 5.4.

qualitative agreement with experiments [2, 42, 177].

Figure 5.5 reports the capacitances versus the polarization P obtained from our numerical solver, that can be used to explain the onset of the hysteretic behavior in figure 5.4. In fact, the hysteresis arises when the capacitance of the semiconductor C_{sct} increases exponentially when entering the inversion region, eventually leading to $[C_{sct}+C_P]>|C_{di}|$ [110, 122, 151]. Moreover, the two crossing points between the capacitances in figure 5.5 correspond respectively to the onset of the forward and backward switchings, occurring respectively along the increasing and decreasing sweeps of the V_G input signal.

There are two main issues related to this design concept where C_{di} is negative to obtain a voltage gain between φ_s and V_G. The first is that

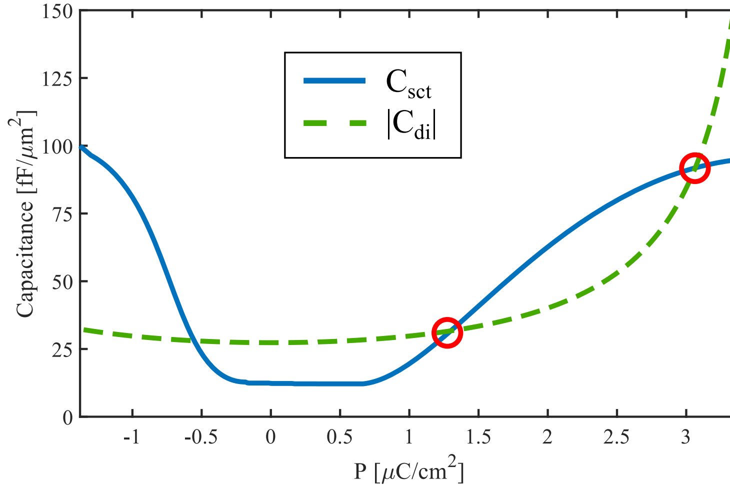

FIGURE 5.5. Capacitance versus polarization P curve corresponding to the case of T_{Fe}=4nm in figure 5.4. The onset of both the forward and the backward switchings are identified by the capacitance crossing points, namely when $[C_{sct}+C_P]$ is larger than $|C_{di}|$, that are highlighted by the red circles. The value of C_{sct} in the sub-threshold region is dominated by parasitic capacitances C_P.

the capacitance matching in the subthreshold region is hard to obtain, due to the usually large difference between the values of $|C_{di}|$ and C_{sct}, making it difficult to reduce SS well below 60mV/dec. The second problem, which is tightly linked to the first one, is that the C_{sct} in the near and above inversion region inevitably increases and then tends to cross the $|C_{di}|$. While the first issue might be solved with 2D materials (such as MoS_2 [175]), or with particular doping strategies (such as devices with a retrograde-doping profile [135]), the second problem seems harder to be overcome. The hysteresis, moreover, tends to produce huge vertical fields that can be hardly tolerated by conventional oxide and semiconductor layers (see figure 5.11 in the following section).

Retrograde steep-slope NC-FET

A device design to achieve very steep I-V characteristics in bulk NC-FETs has been proposed in [135], and it is sketched in figure 5.6, and it exploits a retrograde-doping profile. This device has a conventional bulk MOSFET structure, with a thick semiconductor substrate and no dielectric interfacial layer (i.e. $C_{Fe} \equiv C_{di}$). The equivalent capacitance network for the device sketched in the figure 5.6 shows that the total capacitance of the semiconductor can be split into two main components: the depletion C_{dpl} and the inversion C_{inv} capacitances, thus C_{sct}=C_{dpl}+C_{inv}

The *retrograde* profile, that is reported in figure 5.7, has a particular shape that limits the depletion width, improving the capacitance

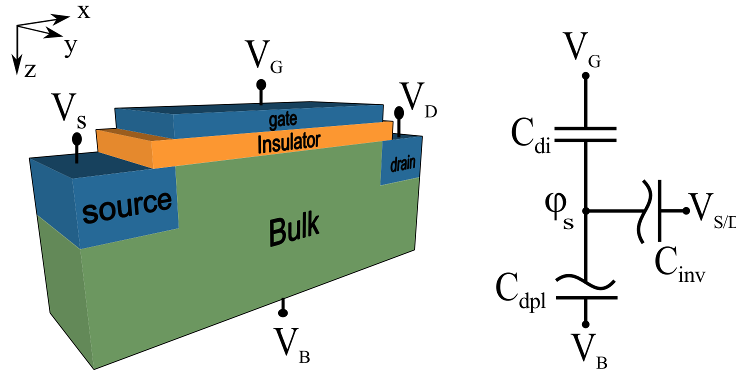

FIGURE 5.6. Sketch (on the left) and capacitive equivalent network (on the right) for a bulk retrograde NC-FET device with a ferroelectric insulator: in this case the V_B is grounded and the overall semiconductor capacitance is split into depletion and inversion contributions, namely C_{dpl} and C_{inv}.

matching between the C_{Fe} and the capacitance $C_{dpl} \simeq C_{sct}$ of the semiconductor in the subthreshold region. Retrograde channel doping profiles have been widely used to contrast short channel effects and enable scaling in advanced CMOS technologies [178, 179], and very steep profiles can be obtained by using Si:C diffusion blocking layer [178], or by selective epitaxy of silicon incorporating partial monolayers of oxygen [180].

This study has been carried out by using the steady-state single-domain LKE for a Si:HfO_2 ferroelectric [1], so that all the reported curves neglect possible dynamic effects. In our simulations we employed a gaussian profile for the retrograde acceptor doping profile, with a peak doping N_{Peak}=6·10^{19}cm^{-3} placed at 9nm from the interface (i.e. z_p=21nm), and a decay length of about 3.3nm/dec. The additional constant doping profiles in the vertical direction are N_{sub}=5·10^{18}cm^{-3}, for the substrate region between z_p and the bulk contact, and N_{surf}=5·10^{16}cm^{-3} at the interface, as illustrated in figure 5.7. It can be also seen in figure 5.7 that the depletion width tends to be limited by this doping profile, as it can be inferred from the behavior of the three profiles for hole concentrations, corresponding to three different gate voltages.

The benefit of the steep retrograde doping profile in terms of capacitance matching can be clearly observed in figure 5.8(a), that reports the numerically calculated $|C_{Fe}|$ and C_{sct} versus the gate voltage V_G for several values of T_{Fe}. Figure 5.8(a) also reports, as a reference, the C_{sct} for a NC-FET with a constant substrate doping profile (i.e. UD NC-FET) that shows a negligible capacitance in the sub-threshold region compared to the retrograde device. The improvement in the SS can be seen in the corresponding I_{DS} versus V_G characteristics of figure 5.8(b): the *S-shaped* characteristic in the inversion region is typical of static LKE simulations,

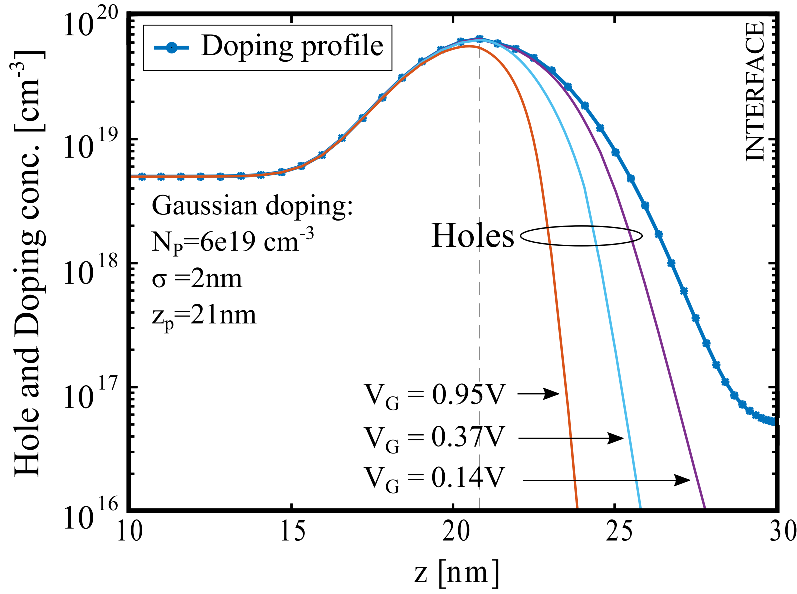

FIGURE 5.7. Retrograde doping profile obtained with a gaussian function for a NC-FET with T_{sc}=30nm, T_{Fe}=15nm and the values reported in the figure. To demonstrate the depletion-width blocking feature allowed by the retrograde doping, we also report three hole profiles for three different V_G values.

and it is representative of the hysteretic behavior that is observed in dynamic simulations.

In figure 5.8(b) it can be seen that, even for this design, the onset of the hysteresis (i.e. the inflection points of the I-V curves in inversion) due to the capacitance crossing is still an issue, and it tends to become more and more relevant when increasing the thickness of ferroelectrics.

5.3 Focus on the on-state operation: g_m-boosted devices

An interesting design approach to avoid the undesired hysteretic behavior is to keep C_{di} positive. Even if this choice forces us to abandon the idea of a sub-60mV/dec slope operation (as implied by equations (5.1) and (5.2)), it is still possible to exploit the step-up voltage conversion of ferroelectrics to enhance the device performance in the on-state [110]. We here refer again to the DG device sketched in figure 5.1, as the presence of the dielectric oxide is playing here an important role.

According to a simple voltage divider model, it is possible to write

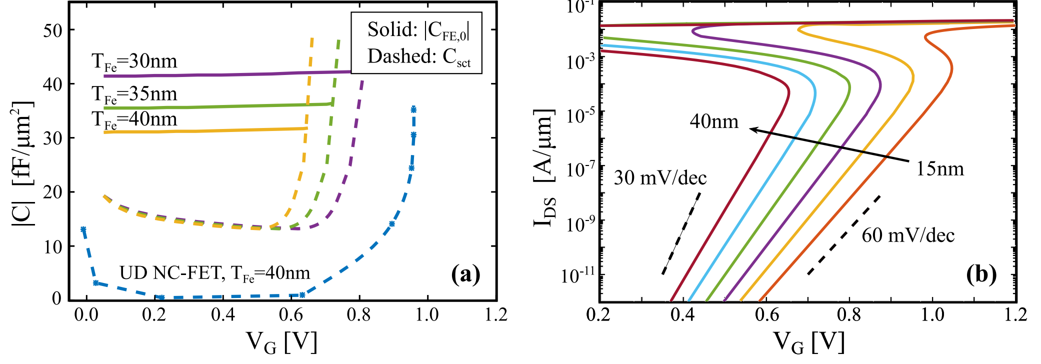

FIGURE 5.8. In (a) we report the capacitance versus V_G curves for the retrograde NC-FET and for different thicknesses T_{Fe}. It is also shown the capacitance of a uniform-doped (UD) bulk NC-FET as reference. In (b) are reported several I_{DS}-V_G characteristics for different T_{Fe} obtained from the static LKE solver.

the voltage gain across the dielectric layer as:

$$\frac{\partial V_{ox}}{\partial V_G} = 1 + \frac{C_{ox}(C_{sct} - |C_{Fe}|)}{|C_{Fe}|C_{ox} + C_{sct}(|C_{Fe}| - C_{ox})} \tag{5.3}$$

where the negative value of the ferroelectric capacitance has been made explicit by writing C_{Fe}=-$|C_{Fe}|$. We argue that if C_{di} is positive, which requires C_{ox}<$|C_{Fe}|$, we can still obtain a $[\partial V_{ox}/\partial V_G]$>1 from equation (5.3) when the capacitance of the semiconductor is larger than $|C_{Fe}|$. In particular, we see that for $C_{sct} \gg |C_{Fe}|$ equation (5.3) simplifies as:

$$\frac{\partial V_{ox}}{\partial V_G} \simeq \frac{|C_{Fe}|}{|C_{Fe}| - C_{ox}} \tag{5.4}$$

which can be much larger than one if C_{ox} is close to $|C_{Fe}|$. This condition has an important implication for the overall gate stack capacitance C_G, in fact we can write:

$$C_G = \frac{\partial(-Q)}{\partial V_G} = \frac{\partial(-Q)}{\partial V_{ox}} \cdot \frac{\partial V_{ox}}{\partial V_G} = C_{ox} \cdot \left[\frac{\partial V_{ox}}{\partial V_G}\right] , \tag{5.5}$$

where Q is the total charge density in the vertical direction of the stack, and it is shared by each layer. Equation (5.5) states that it is possible to have a gate capacitance C_G larger than the capacitance C_{ox} of the dielectric, when the gain $[\partial V_{ox}/\partial V_G]$ is made greater than one. The capacitance amplification effect of ferroelectrics, as already discussed in section 3.6, is supported by measurements on superlattice capacitors reporting experimental evidence of overall capacitances larger than the capacitances of the constitutive layers. In the bias range where C_G is larger than C_{ox}, we can effectively boost the transconductance in the NC-FET compared to conventional counterparts, and thus enable a large $[I_{ON}/I_{OFF}]$ improvement for a given supply voltage V_{DD}: for this reason we refer to this device concept as g_m-*boosted* NC-FET.

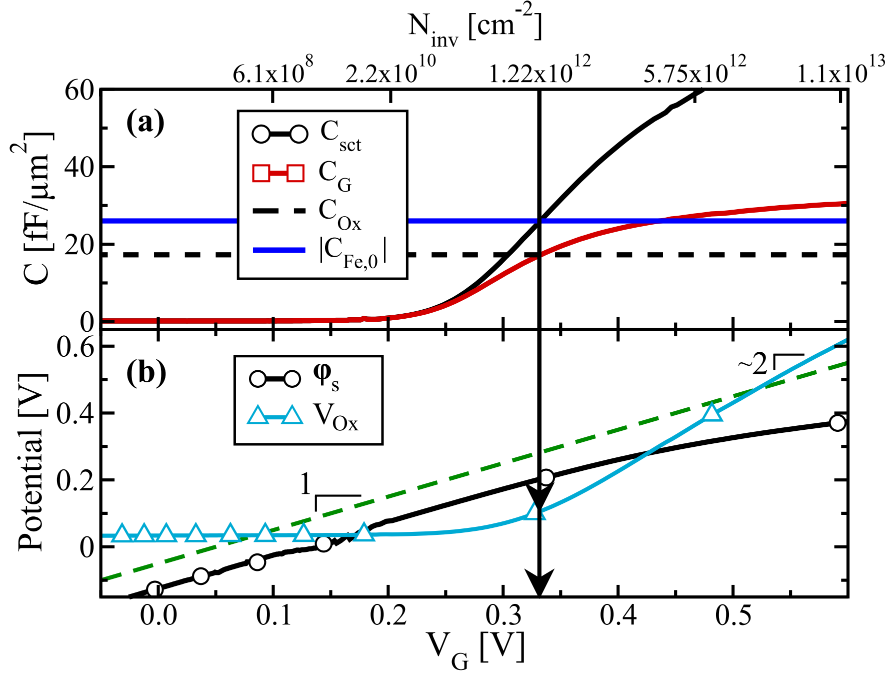

FIGURE 5.9. In (a) are reported the capacitances of the NC-FET, in particular C_G is the total device gate capacitance and $C_{Fe,0}$ is the ferroelectric capacitance for small polarizations (P$\simeq$0). In (b) are reported the voltage drops across the oxide, V_{ox}, and across the semiconductor, φ_s versus the applied voltage V_G. The crossing point of the capacitances coincides with the boosting of the $[V_{ox}/V_G]$, as highlighted by the arrows.

We would like to emphasize the fact that, for the g_m-boosted NC-FET, C_G is always positive and the capacitance matching involves two fairly bias independent capacitances, C_{ox} and $|C_{Fe}|$. This makes it easier to avoid complete domain switching and the hysteretic behavior when compared to the steep-slope design.

Figures 5.9(a) and (b) report respectively the numerically computed C_{sct} and C_G versus V_G and the corresponding curves for φ_s and V_{ox} for an NC-FET with T_{ox}=2nm, T_{Fe}=3nm of HZO [2] and silicon film thickness of 7nm. As expected, in the sub-threshold region $[\partial\varphi_s/\partial V_G]$ is approximatively one (in fact the black curve of φ_s in figure 5.9(b) is parallel to the dashed line with unitary shape), meaning that no steep-slope operation is achieved. In near- and above-threshold region, however, C_{sct} increases rapidly and eventually becomes greater than $|C_{Fe,0}|$, which induces a C_G larger than C_{ox} and allows $[\partial V_{ox}/\partial V_G]$ to become grater than one.

The conductance versus V_G characteristics of the device for different values of T_{Fe} are shown in figure 5.10, using both linear and semi-logarithmic scales. As it can be seen the NC-FET provides a remarkable enhancement of the I_{ON} current, reported as a boost of the conductance

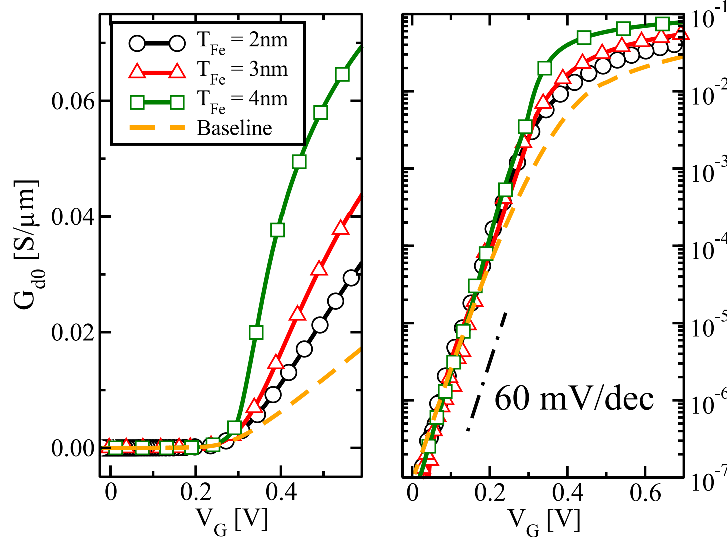

FIGURE 5.10. Conductance versus V_G curves for the described g_m-boosted NC-FET and for different T_{Fe}. The linear scale shows the enhancement of the on-state conductance compared to the reference baseline device, while the semi-logarithmic scales show that no improvement in the SS is obtained.

G_d in the figure, compared to the non-ferroelectric FET, particularly for T_{Fe}=3nm and 4nm. According to figure 5.11, when T_{Fe} is further increased to 6 nm, however, $|C_{Fe}|$ becomes smaller than C_{ox}, so that C_G becomes negative (according to equation (5.5)), which drives the system towards instability, eventually triggering complete domain switching and hysteresis.

Figure 5.11 shows that the hysteretic behavior results in an oxide field F_{ox} approaching 10MV/cm. Such a strong F_{ox} is problematic from a gate leakage perspective [106], and it is also hazardous in terms of bias-temperature instability and/or soft-breakdown [181].

From a design perspective, it is interesting to explore the relation between the temperature and the thickness of the ferroelectric when the gain G is varying. By manipulating equation (5.4), and combining it with the condition of the g_m-boosted design C_{di}>0, we can infer the following expression [122]:

$$a_0(T - T_0)T_{Fe} > \frac{EOT}{\varepsilon_{SiO_2}} \cdot \frac{G-1}{G} \tag{5.6}$$

which describes a region in the design space defined by T_{Fe}, temperature and gain G. Figure 5.12 reports this design space for different gains and also highlights the boundary condition that leads to a steep-slope design. It is clear that the closer we approach the C_{ox}=$|C_{Fe}|$ case, the higher is the gain in the on-current. This sets an upper boundary condition on the g_m-

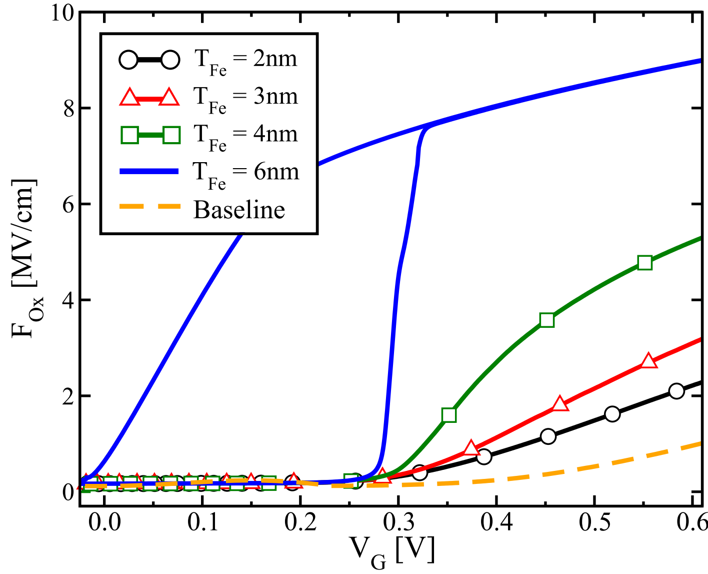

FIGURE 5.11. Electric field across the oxide versus the applied voltage V_G for the NC-FETs at different T_{Fe} and for the baseline. For T_{Fe}=4nm or lower, the device operates as a g_m-boosted device, while for T_{Fe}=6nm the series capacitance C_{di} becomes negative, resulting in a steep-slope NC-FET with an hysteretic characteristic.

boosted design, while the lower boundary is due to the NC operation itself.

Before concluding this section, we want to remark that the proposed g_m-boosted device is a promising design perspective, because the ferroelectric can be stabilized to boost the on-state currents compared to conventional FETs. Moreover we can derive some simple (and approximated) guidelines for the design of such a device; we here recall that the zero field ferroelectric capacitance $|C_{Fe,0}|$ is given by $|C_{Fe,0}|=1/(2|a|T_{Fe})$ and that, for a third order LKE, $|a|$ can be written in terms of F_C and P_r:

$$|a| = \frac{3\sqrt{3}F_C}{2P_r} \ . \tag{5.7}$$

Equation (5.7), together with the definition of $|C_{Fe,0}|$ and equation (5.4), suggest an expression for the T_{Fe} needed to obtain a certain gain $[\partial V_{ox}/\partial V_G]$:

$$T_{Fe} \approx \left[1 - \frac{1}{[\partial V_{ox}/\partial V_G]}\right] \frac{EOT}{\varepsilon_{SiO_2}} \frac{P_r(T_{Fe})}{3\sqrt{3}F_c(T_{Fe})} \ . \tag{5.8}$$

This is an expression that depends on the EOT of the oxide layer and also on ferroelectric material properties, defined by the ratio between the remnant polarization and the coercive field $[P_r/F_C]$. The role of $[P_r/F_C]$ ratio is further discussed in the section dealing with the sensitivity and variability.

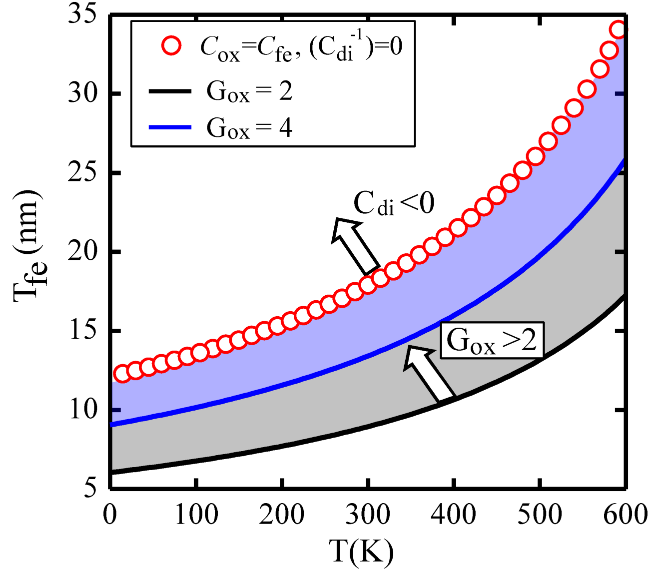

FIGURE 5.12. Design space for the g_m-boosted NC-FET in terms of T_{Fe} and temperature T. The condition C_{ox}=$|C_{Fe}|$ discriminates between the steep-slope and the g_m-boosted designs, and also the curves for two different gains G are shown for reference.

5.4 Role of interface traps

We decided to study the role of interface traps due to the fact that, in certain conditions, they may result in an improvement of the capacitance matching between the C_{di} and C_{sct} [170, 182].

The presence of interface traps in MOSFET with conventional dielectrics is well known to have a relevant influence on the threshold voltage value V_T and also a detrimental effect on the SS [183], while the analysis on NC-FETs received only limited attention [182]. For this reason we analyzed the effect of interface traps in both steep-slope and g_m-boosted NC-FETs when a given distribution of traps is introduced in the energy-gap, using our baseline transistor as benchmark.

We start by recalling equation (5.1) for the sub-threshold swing and then add a capacitive term C_{it}=qD_{it} describing the influence of interface traps, according to the sketch reported in figure 5.13(a), so as to obtain:

$$\begin{aligned} SS &= 60mV/dec \cdot \left(1 + \frac{C_{sct} + C_P + C_{it}}{C_{di}}\right) \\ &= 60mV/dec \cdot \left(1 \pm \frac{C_{sct} + C_P + C_{it}}{|C_{di}|}\right) \end{aligned} \quad (5.9)$$

where the plus-minus sign stands for the positive or negative values of C_{di}, according to the two NC-FET design options. According to the sign of

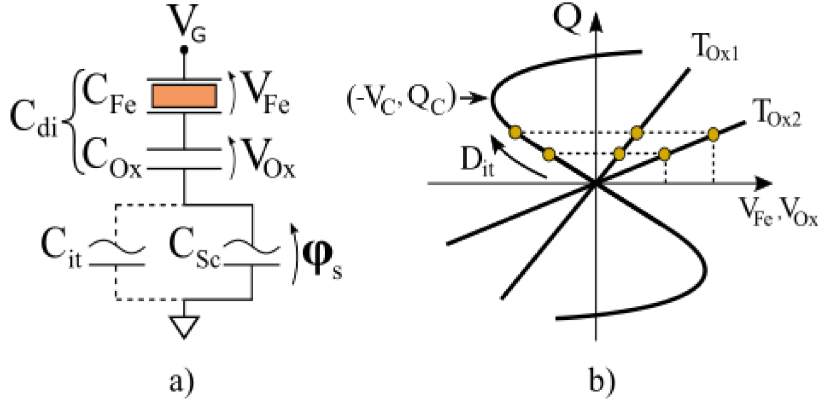

FIGURE 5.13. In (a) is it shown the equivalent capacitive network of the generic NC-FET where the capacitance of the interface traps C_{it} is added in parallel to the semiconductor's C_{sct}. In (b) we show is the relation between the ferroelectric, V_{Fe}, and the oxide, V_{ox}, voltage drop versus the charge Q for two oxide thicknesses $T_{Ox1}<T_{Ox2}$. Moreover, the arrow indicate that an increase of the acceptor type D_{it} drags the forward switching voltage towards the coercive voltage V_c.

the capacitance of the gate-stack, it can be easily inferred from equation (5.9) that the presence of C_{it} can either improve or degrade the subthreshold swing. For a positive C_{di}, that is the case of the baseline and of the g_m-boosted NC-FET, SS will inevitably be larger than 60mV/dec and it is degraded by the presence of C_{di}. For a steep-slope design with $C_{di}<0$, instead, can be reduced well below the thermal limit.

Before discussing the conductance and capacitance curves versus V_G, it is important to clarify the threshold-voltage V_T shift due to the presence of charge density Q_{it} trapped at the interface. To this purpose we write the steady-state gate voltage equation:

$$V_G - V_{FB} = V_{Fe}(Q) + V_{ox}(Q) + \varphi_s(Q_{sc}) \tag{5.10}$$

where φ_s is the surface potential, V_{FB} is the flat-band voltage, Q_{sc} the free semiconductor charge and Q is the overall charge in the quantization direction, that can be expressed in terms of oxide field F_{ox}, polarization and electric field in the ferroelectric as:

$$Q = -[Q_{sc} + Q_{it}] = \varepsilon_{ox} F_{ox} = P + \varepsilon_0 F_{Fe} \ . \tag{5.11}$$

It has been demonstrated that, for instance for a given ultra-thin body double-gate structure, a unique $\varphi_s(Q_{sc})$ relation exists, in fact this is determined only by the electric field, F_s, present at the semiconductor interface (that is consistent to a Neumann boundary condition for the Poisson equation). We can then define V_T as the applied voltage V_G necessary to induce a given free charge density Q_{sc} in the silicon film, allowing us to examine the influence of Q_{it} on V_T thanks to equations (5.10) and (5.11). In particular, for a given architecture and for a free

charge density, the screening effect of trapped charges Q_{it} modifies the value of the total Q (see equation (5.11)). This leads to a change in the values of the voltage drops across both the oxide and the ferroelectric layers, thus shifting the V_T for a given specific charge density Q, according to equation (5.10).

Another peculiar and interesting point of this analysis on NC-FETs is the sign of the V_T shift: in fact, if the ferroelectric is operated in the NC branch, the changes of V_{Fe}(Q) and V_{ox}(Q) at a fixed value of Q have opposite signs, so that the sign of the shift of the global V_T with Q_{it} depends on which of the two contributions is the largest in magnitude (see figure 5.13(b)). An insightful expression for the variations of V_T due to small changes of Q_{it} can be derived from the linearization of equation (5.10):

$$\Delta V_T \approx -\Delta Q_{it}\left[\frac{\partial V_{Fe}}{\partial Q}+\frac{\partial V_{ox}}{\partial Q}\right]=-\frac{\Delta Q_{it}}{C_{di}} \tag{5.12}$$

In equation (5.12) we assumed that $(\partial V_{Fe}/\partial Q)$=$-(\partial V_{Fe}/\partial Q_{it})$=$1/C_{fe}$ and $(\partial V_{Ox}/\partial Q)$ =$-(\partial V_{Ox}/\partial Q_{it})$=$1/C_{Ox}$, and also that $(\partial V_{FB}/\partial Q_{it})\simeq 0$, which is a reasonable approximation if ΔQ_{it} is negligible at the flat-band condition. This equation essentially affirms that the sign of the V_T shift depends on the sign of the overall dielectric capacitance C_{di}.

It is important to recall that our description for the transistor is essentially a 1D model, while in nanoscale NC-FETs operating in the V_{DS}=V_{DD} condition two dimensional effects on both electrostatics and ferroelectric polarization are important. Here we simplify this picture by analyzing the ballistic conductance at V_{DS}=0V, and we apply a slow triangular signal at the gate terminal, so that dynamic effects of the ferroelectric are negligible.

Figure 5.14 reports the simulated curves for a g_m-boosted NC-FET (i.e. with a C_{di}>0) with a silicon film thickness of 10nm, T_{Fe}=3nm of HZO [2] and a T_{Ox}=2nm SiO_2 film, and for different densities D_{it} of acceptor traps. The figure shows that acceptor type traps produce a positive V_T shift and degrade the sub-threshold swing SS similarly to the behavior of a conventional baseline CMOS transistor, which is consistent with equation (5.12).

A remarkably different behaviour is instead observed in figure 5.15, where the simulated structure differs from the previous one only in the oxide thickness, that is now set to T_{ox}=0.5nm, which makes C_{di}<0 and hence enables a steep-slope operation. Compared to the previous case we can clearly see a relevant increase of the slope of the G_d-V_G characteristic in the sub-threshold region when the D_{it} is raised (stemming from an improved capacitance matching) and also a negative V_T shift.

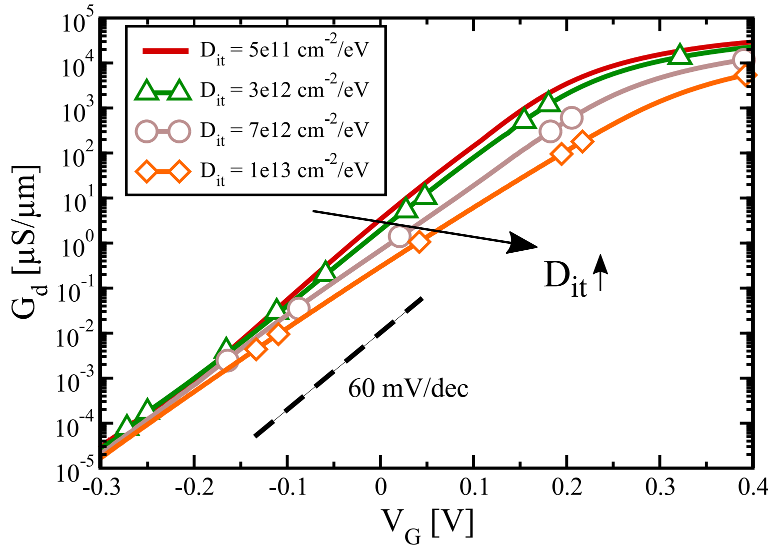

FIGURE 5.14. Influence of interface traps on g_m-boosted NC-FETs: ballistic conductance G_d versus applied voltage V_G characteristics for a g_m-boosted UTB-DG NC-FET, and for different acceptor trap densities D_{it} and with a metal gate workfunction is Φ_M=4.3eV. The increase of SS due to the increase of D_{it} is highlighted by the arrow.

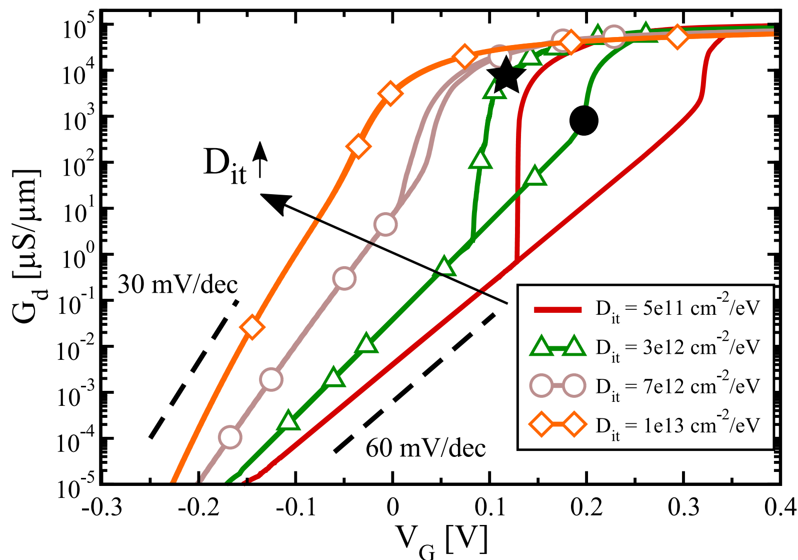

FIGURE 5.15. Influence of interface traps on steep-slope NC-FETs: ballistic conductance G_d versus applied voltage V_G characteristics for a steep-slope UTB-DG NC-FET concept, and for different acceptor trap densities D_{it} and with a metal gate workfunction Φ_M=4.52eV. The increase of D_{it} affects both the slope in sub-threshold and the amplitude of the hysteretic eye.

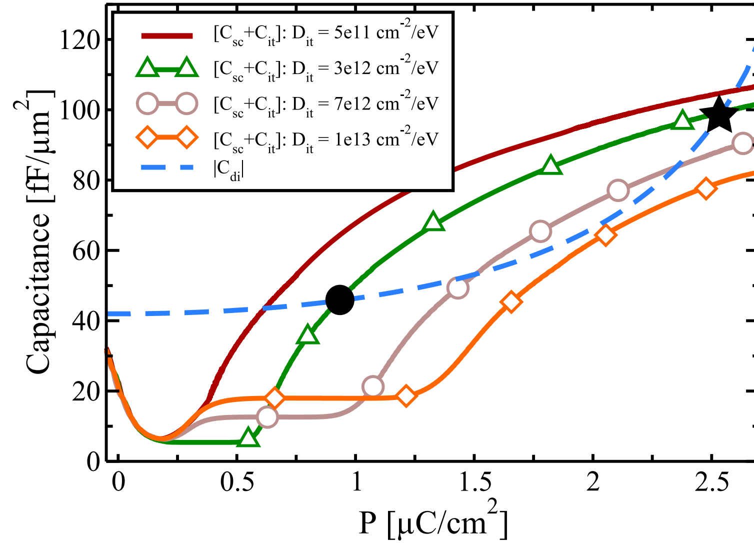

FIGURE 5.16. Corresponding capacitances $|C_{di}|$ (with negative C_{di}) and $[C_{sct}+C_{it}]$ versus charge density Q. The crossing points between $[C_{sct}+C_{it}]$ and $|C_{di}|$ correspond to the forward and backward switching points of the hysteresis highlighted in figure 5.15 for the case of trap density D_{it}=3·10^{12} cm^{-2}/eV. The shape of the capacitance in the sub-threshold region is coherent with a static Fermi-Dirac distribution of traps in the energy-gap that extends till the first subband of the CB.

An additional remark is that the amplitude of the hysteresis tends to reduce when increasing the trap density. This is because the forward switching of the hysteresis occurs when the increasing V_G makes $[C_{sct}+C_{it}]$ rise and cross $|C_{di}|$, and the backward switching similarly occurs when the decreasing V_G brings again $[C_{sct}+C_{it}]$ below $|C_{di}|$. As it can be seen in figure 5.16, by increasing D_{it} also the charge Q corresponding to the forward switching increases, leading to a decrease of the corresponding V_G, essentially for the same reasons already discussed for the negative V_T shift at fixed Q_{sct}. The charge Q at the backward switching, instead, has the opposite behavior and decreases when D_{it} is raised which increases the negative V_{Fe} slightly. However, the V_{ox} and φ_s reductions due to the smaller value of Q more than compensate the V_{Fe} increase, leading to an overall increase of V_G, but to a smaller extent compared to the V_G at the forward switching. The combined effect of the two behaviors above results in a contraction of the hysteretic eye leading to a steep-slope hysteresis-free operation for D_{it}=1·10^{13}cm^{-2}/eV.

This analysis is limited to a static interface-trap description, but it gives a very good insight into the behavior of negative capacitance devices. A final remark, before moving to the results obtained with the dynamic SRH model, is that our analysis was limited to the influence of traps on the electrostatics, but one should not forget that traps have a detrimental

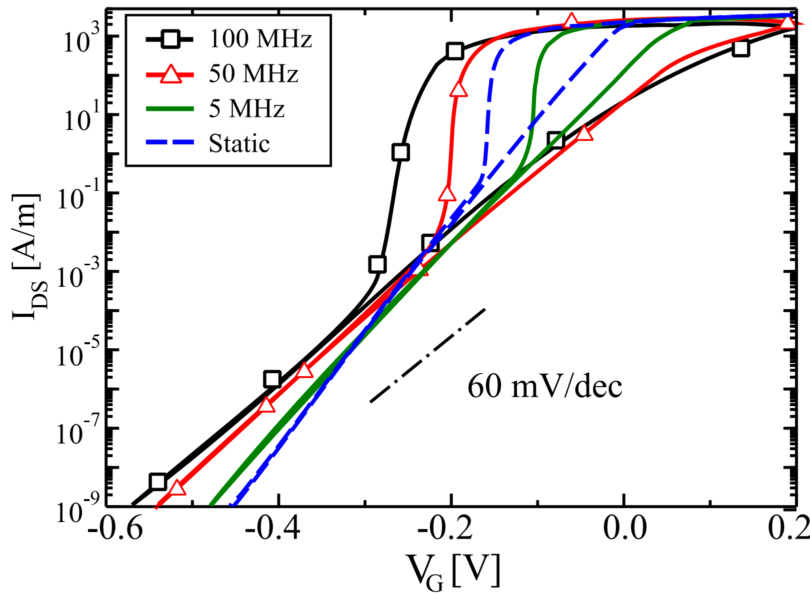

FIGURE 5.17. I_{DS} current (per gate) versus gate voltage V_G for a steep-slope NC-FET with T_{Fe}=20nm of Si:HfO$_2$ [1] and a concentration D_{it}=10^{13}cm^{-2}/eV of acceptor type traps in the upper half of the energy gap. The different curves are obtained for several frequencies and for the static case, according to the description reported in the model chapter and in [170]. Parameters used in simulations are σ=10^{-15}cm^2, v_{th}=2.3·10^7 cm/s, N_C=3.2·10^{19} cm^{-3}, experimentally extracted for a Si-SiO$_2$ interface [171].

effect on the transport [68].

Traps in steep-slope NC-FETs including effects of the traps dynamics

The inclusion of capture and emission dynamics in the trap model of NC-FET has shown interesting results. The frequency response of acceptor-like traps is described in figure 4.8, accordingly to the SRH model reported in section 4.1.3. In this section we report only the dynamic results for the steep-slope concept, as the g_m-boosted device is expected to behave similarly to a conventional MOSFET.

In the simulations reported in this section the damping factor is set to ρ=0.5Ωm, namely in the range necessary for a GHz operation of NC-FETs [184], and low enough so that dynamic effects of the ferroelectric are negligible. Figure 5.17 shows that a constant density D_{it} of acceptor traps in the energy gap can induce a sub-60mV/dec operation at low frequencies. However the beneficial effects of traps tend to vanish already in the tens of MHz, for the dynamic trap parameters from [171], because a progressively larger fraction of traps cannot contribute to C_{it}, hence to the electrostatics. The dynamic response of the traps is clearly illustrated

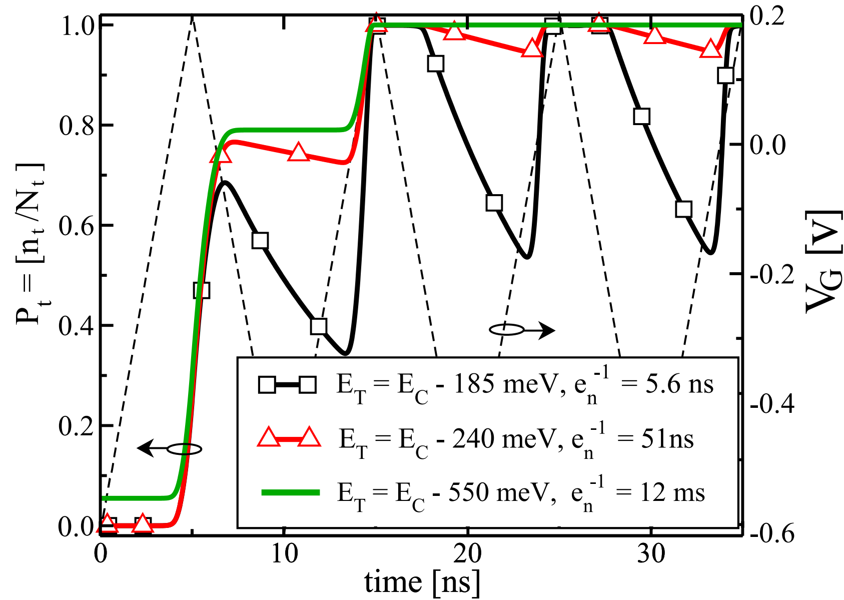

FIGURE 5.18. Occupation probability P_t=n_t/N_t for some trapping levels corresponding to the 100MHz curve in figure 5.17. It is also reported the gate voltage V_G waveform (referring to the right y-axis). Deeper traps have a larger emission time e_n^{-1} and so cannot follow simultaneously the externally applied signal.

in figure 5.18, where we report the occupation probability versus time for traps with different energy depths. As expected from the theory in the previous chapter, deeper traps can capture an electron for positive V_G, but cannot emit it for negative V_G, so that they behave similarly to negative fixed charges [183]. Moreover, the asymmetric capture and emission rates are inherent to the dynamic SRH model: in fact e_n depends only on the trap depth, while c_n becomes even larger than e_n when E_t is driven below the source Fermi-level $E_{F,S}$.

These simulation results highlighted that the enhancement in the SS due to traps is strongly frequency-dependent, and that possible traps induced improvements of the sub-threshold swing tend to vanish at high frequencies.

5.5 Sensitivity and variability

Due to the strong dependence of ferroelectric properties on both temperatures and thicknesses, a study on the sensitivity of NC-FETs to the variations of such parameters is important. The largest part of the analysis has been carried out on the g_m-boosted device concept, as its working principle makes it more sensitive to operating conditions and manufacturing variability. The steep-slope device, in fact, essentially requires only the

condition $|C_{Fe}|<C_{ox}$, while the g_m-boosted operation demands a $|C_{Fe}|$ close to C_{ox}.

Sensitivity to material properties, EOT and T_{Fe}

The sensitivity to thickness variations is simple, in fact both the ferroelectric C_{Fe} and the dielectric C_{ox} capacitances are proportional to the inverse of their thicknesses. Moreover we recall that the sign of the series capacitance C_{di} discriminates between the two operative regions of the NC-FET concept. In fact, as it can be seen in figure 5.19, we can easily identify the operative conditions for a steep-slope (where $C_{ox}>|C_{Fe}|$) rather than a g_m-boosted (where $C_{ox}<|C_{Fe}|$) by varying the values of T_{ox} or T_{Fe}. For this reason it is important to determine a well-defined range of values to safely operate the device in one of the two regions. Eventually, there is also a lower limit to T_{Fe} below which the domains cannot nucleate, thus the whole material loses its ferroelectric features and returns to its pure dielectric phase [185–187].

We want to focus now on the g_m-boosted concept by recalling the simplified expression that relates T_{Fe} to EOT and to the material properties $[P_r/F_C]$ (equation (5.8)):

$$T_{Fe} \approx \left[1 - \frac{1}{G}\right] \frac{EOT}{\varepsilon_{SiO_2}} \frac{P_r(T_{Fe})}{3\sqrt{3}F_c(T_{Fe})} \tag{5.13}$$

where we have set $G=[\partial V_{ox}/\partial V_G]$, and an illustration of the T_{Fe} versus $[P_r/F_C]$ is reported in figure 5.20 for the material parameters used in [2]. This shows the dependence of the ferroelectric thickness against the $[P_r/F_C]$ ratio and for several given voltage gains G: it is clear from the curves that, depending on the material properties, we can use different combinations of EOTs and T_{Fe}. It is important to emphasize that figure 5.20 is obtained through several approximations, but it can still give insightful information from the design perspective. For aggressive nanoscale transistor applications, for instance, figure 5.20 suggests that not all the ferroelectrics with a large $[P_r/F_C]$ ratio are more suitable for a g_m-boosted design of NC-FETs.

Another important analysis about the g_m-boosted device has been carried out in terms of on the sensitivity of the gain G to EOT and T_{Fe}. To evaluate this, we need to recall equation (5.5) that describes the total gate capacitance C_G:

$$C_G = C_{ox} \cdot \left[\frac{\partial V_{ox}}{\partial V_G}\right] = C_{ox} \cdot G \ . \tag{5.14}$$

Equation (5.14) can be differentiated with respect to both EOT and T_{Fe},

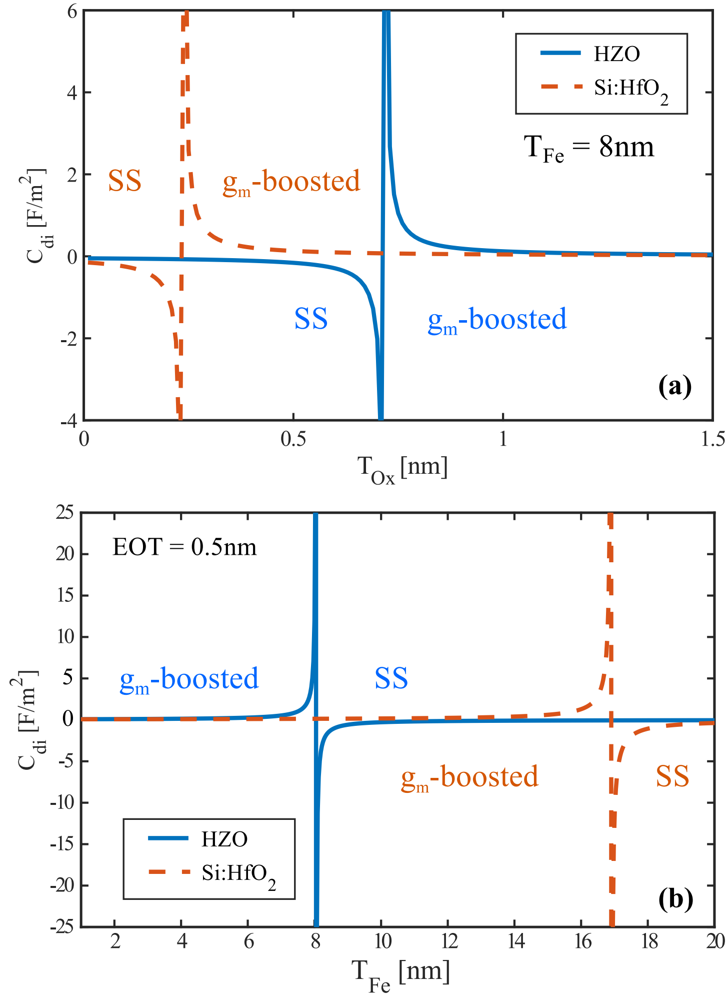

FIGURE 5.19. Series capacitance C_{di} versus T_{ox} in (a) and versus T_{Fe} in (b): it can be see that the thicknesses change the capacitances $C_{Fe,0}$ and C_{ox}, thus the C_{di}. Positive C_{di} correspond to the g_m-boosted design (typically thick T_{ox} or thin T_{Fe}), while negative C_{di} correspond to the steep-slope design (labelled here as SS). Ferroelectric materials reported are HZO from [111] and Si:HfO_2 from [1].

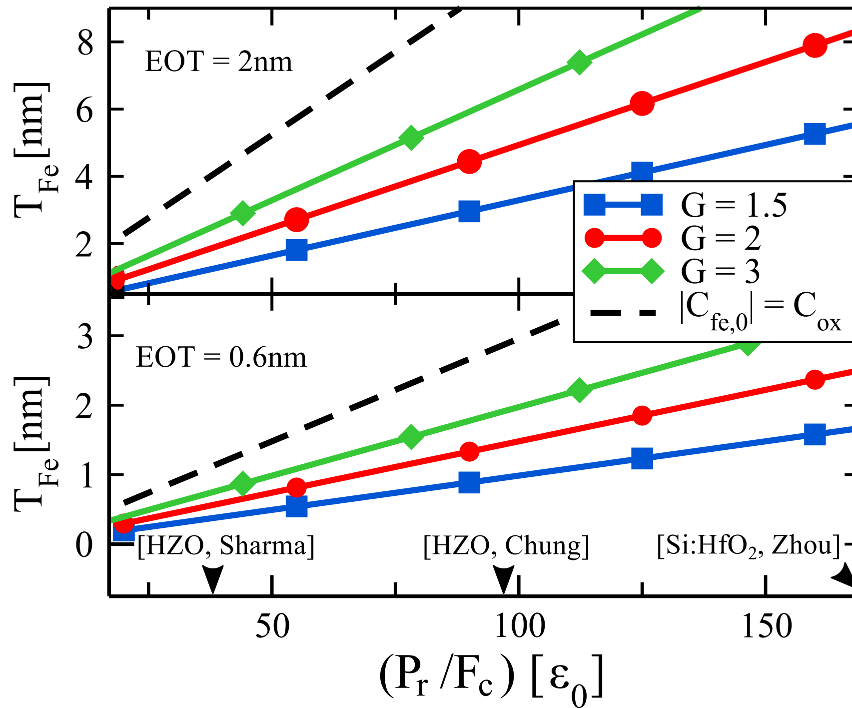

FIGURE 5.20. Design space for the gain G=$[\partial V_{ox}/\partial V_G]$ of the g_m-boosted device for different ferroelectric thicknesses of HZO [2], versus $[P_r/F_C]$ ratio. On the x-axis are also reported some of the typical values of $[P_r/F_C]$ ratios extracted from experimental characterization of ferroelectric materials.

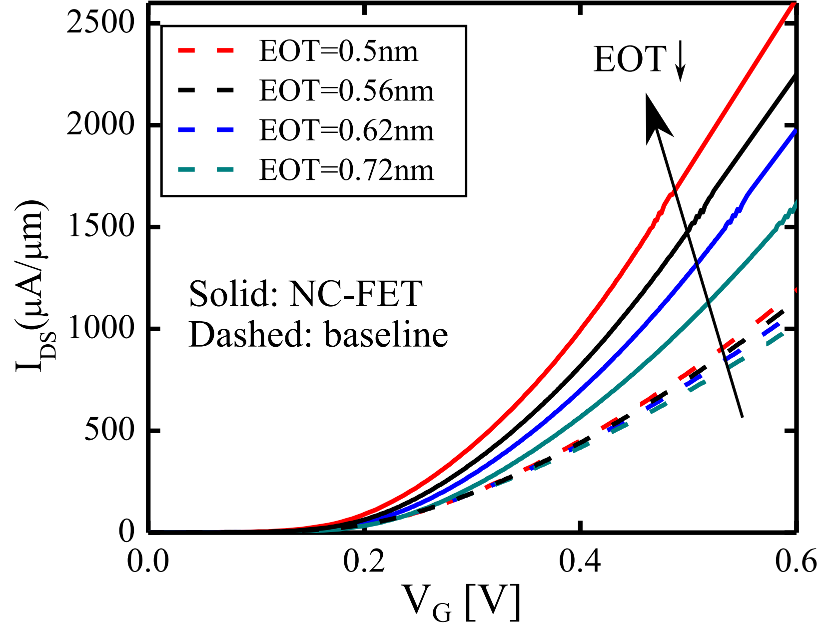

FIGURE 5.21. I_{DS} versus V_G curves at V_{DS}=0.6V for either baseline FETs (dashed lines) and g_m-boosted NC-FETs (solid lines) and for different EOT values. The NC-FETs are simulated with a T_{Fe}=15nm of ferroelectric Si:HfO_2 [1], and the curves show the enhanced sensitivity on EOT variations of such devices compared to conventional FETs.

leading to the equations

$$\frac{\partial C_G}{\partial EOT} = -\frac{-C_{ox}}{EOT}\left[G + \frac{C_{ox}}{|C_{Fe}|}G^2\right] \quad , \quad \frac{\partial C_G}{\partial T_{Fe}} = \frac{C_{ox}^2}{|C_{Fe}|T_{Fe}}G^2 \qquad (5.15)$$

that entail a strong thickness-variability in NC-FETs compared to their conventional counterparts. In particular, the enhancement in the sensitivity with respect to the EOT is due to the amplification of the oxide capacitance. The effects on the device characteristics are clearly shown in figure 5.21, where the currents for a g_m-boosted NC-FET are plotted against the applied gate-voltage. The NC-FET shows a relevant increase, compared to the baseline transistor, of the on-currents when the EOT is decreased. Similarly the sensitivity to both the T_{Fe} and T_{ox} thicknesses are illustrated in figure 5.22, for currents normalized to reference values of I_{ON}. In particular, for figure 5.22(a) we used as reference the I_{ON} for an EOT=0.5nm, while for figure 5.22(b) an I_{ON} obtained from an NC-FET Si:HfO_2 [1,122] and T_{Fe}=15nm. Even in this case we can see a strong dependence on the thicknesses of NC-FETs compared to baseline devices, showing larger on-current boosting for reduced T_{ox} and large T_{Fe}.

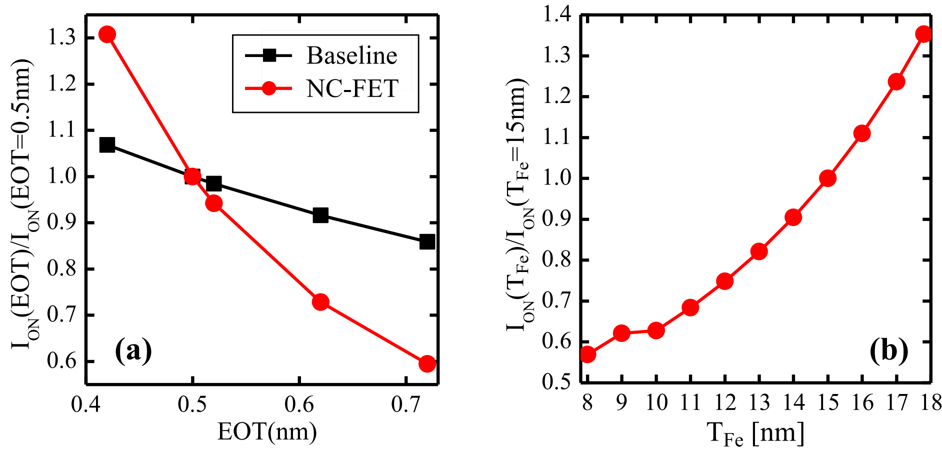

FIGURE 5.22. In (a) is reported the current boosting versus EOT for I_{ON} currents normalized to the I_{ON} simulated for an EOT=0.5nm, T_{Fe} is set to 15nm, I_{off}=100nA/μm and V_{DS}=0.6V. In (b), similarly, are reported the current boosting against T_{Fe} for I_{ON} normalized to a reference I_{ON} obtained with T_{Fe}=15nm and EOT=0.5nm.

Sensitivity to temperature variations

Before discussing the temperature sensitivity of the whole device, it is important to analyze the temperature-behavior of the ferroelectric material. For this reason we calibrated our model against one of the most extensive experimental study we found in literature, namely the work by Zhou on silicon-doped hafnia [1]. We calibrated the LKE coefficients on those experiments with a multi-domain simulation (according to the process described in chapter 4.2), in particular by introducing a statistical a dispersion of the coercive field of about ±0.45MV/cm. From figure 5.23(a) it is possible to see that our calibration tracks very well the experiments, even for different temperatures. Moreover, figure 5.23(b) shows in the detail the fairly linear dependence of the LKE coefficient a on the temperature, allowing us to extract the a_0 coefficient of equation 3.3 as a_0=1.3·10^6m/(F K) for T=923K, and for a Curie temperature consistent with the range reported in [188].

The dependence of the characteristics of conventional MOSFETs with respect to the temperature are well known in the literature [36]: in the off-state all FETs suffer an SS degradation with increasing temperature T. Moreover in the on-state the I_{DS} curve for the baseline conventional FET has a rigid horizontal shift, where the threshold voltage V_T decreases while increasing T [36].

The g_m-boosted NC-FET, instead, has a current I_{DS} that is enlarged at low V_G, but at the same time reduced at large gate voltages. This can be seen in figure 5.24 reporting the comparisons of I-V characteristics,

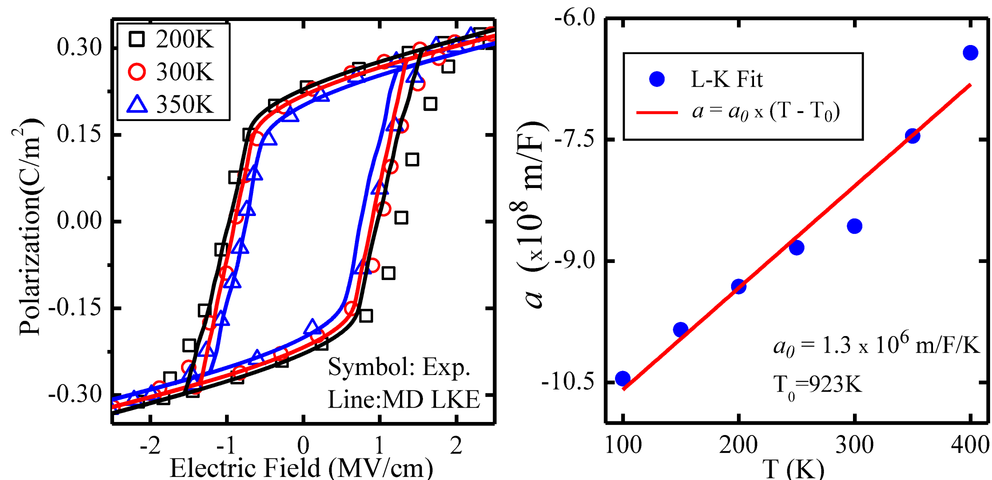

FIGURE 5.23. On the left: polarization versus applied electric field for Si:HfO_2. The calibration is done with multi-domain LKE model (squares, circles and triangles are respectively for temperature T=200, 300, 350K), by comparison to experimental data at different temperatures from [1]. On the right is validated, against fitted values, the model that linearly relates the LKE coefficient a to the temperature.

at different temperatures T NC-FETs and baseline FETs. An interesting behavior can be seen for the NC-FET curves, as all the characteristics at different T are intersecting at a specific V_G in figure 5.24(right). This is interpreted as point of the I_{DS} versus V_{GS} characteristic, that is insensitive to temperature variations. This is interesting also from an applicative point of view, as this feature could be exploited in circuits as a current (or voltage) reference insensitive to temperature. In particular, this behavior is due to the fact that, when T is increased for a fixed charge Q, the surface potential φ_s=-$E_{C,s}$/q decreases, but the negative value of V_{Fe} increases.

We developed an analytical model to predict and explain the temperature variability of such devices, using a few approximations for the semiconductor layer. We focused on an equilibrium, quantum-limit condition, so that the largest part of the charge Q is carried by the lowest subband ε. Such a quantum limit approximately is expected to be fairly accurate for UTB devices. Thanks to this approximation we can express the $[\partial V_G/\partial T]$ analytically, at a fixed value of charge density Q, by simply differentiating the gate voltage relation in equation (4.19):

$$\left.\frac{\partial V_G}{\partial T}\right|_Q = \frac{\partial \varphi_s}{\partial T} + \frac{\partial V_{ox}}{\partial T} + \frac{\partial V_{Fe}}{\partial T} + \frac{\partial V_{FB}}{\partial T} \simeq -\frac{1}{q}\frac{\partial \varepsilon}{\partial T} + \frac{\partial V_{Fe}}{\partial T} - \frac{\partial \chi_{sc}}{\partial T} \quad (5.16)$$

where we assumed that $[\partial V_{ox}/\partial T]$=0. Equation (5.16) also assumes that

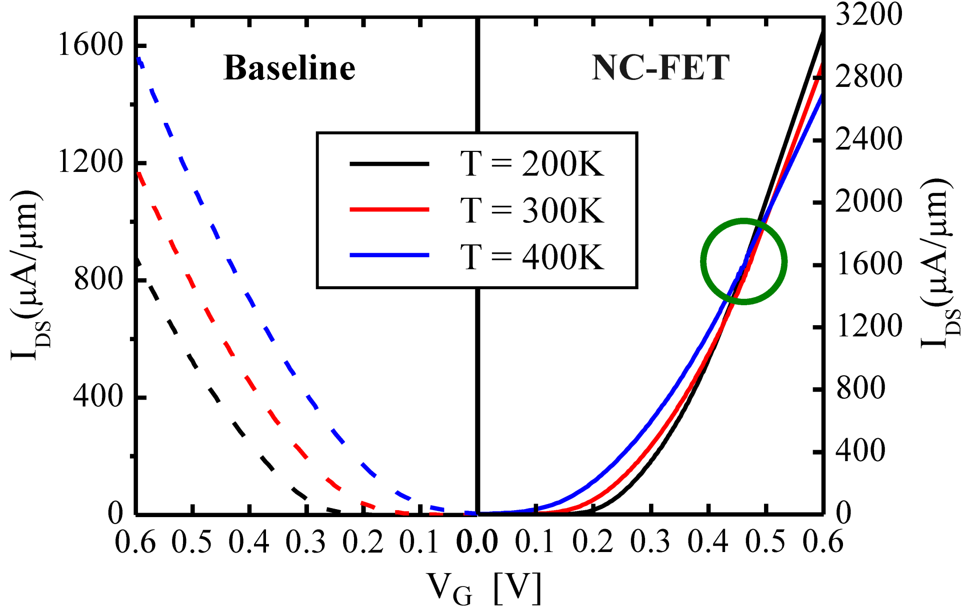

FIGURE 5.24. Sensitivity comparison of currents between baseline and NC-FETs at different temperatures. I_{DS} versus V_G curves at V_{DS}=0.6V for T=200, 300, 400K: on the left are reported the characteristics of the baseline and on the right of the g_m-boosted NC-FET. EOT is set at 0.5nm, T_{Fe}=15nm, a_0=1.34·10^6 m/(F K) and the I_{off}=100nA/μm. The curves at different T have a crossing point, for the NC-FET, that is highlighted with a circle.

the dependence on temperature of metal work-function is negligible, hence $[\partial V_{FB}/\partial T]$≃$[-\partial\chi_{sc}/\partial T]$, where χ_{sc} is the electron affinity of semiconductor and its temperature dependence is obtained from [55]. To calculate $[\partial\varphi_s/\partial T]$, instead, we assumed that the surface potential tends to move rigidly with lowest subband ε, so that for the derivatives with respect to temperature and at fixed charge Q we obtain the following set of equations:

$$\begin{cases} \dfrac{\partial V_{Fe}}{\partial T} & = a_0 T_{Fe} Q \\ \dfrac{\partial \varphi_s}{\partial T} & \simeq \dfrac{-1}{q}\dfrac{\partial \varepsilon}{\partial T} \\ & = \dfrac{-K_B}{q}\left\{\dfrac{Q/(qD_0K_BT)}{1-\exp[-Q/(qD_0K_BT)]} - \ln\left[e^{Q/(qD_0K_BT)}-1\right]\right\} \end{cases} \tag{5.17}$$

In the system of equations (5.17) we describe, for the first equation concerning the quantum-limit approximation, the charge density Q as:

$$Q \simeq qD_0K_BTln\left(1+e^{\eta}\right)) \quad \text{with} \quad D_0 = \frac{\mu_0 m_{d0}}{\pi\hbar^2} \tag{5.18}$$

where μ is the multiplicity, m_d the effective mass of the lowest subband and the other symbols have their standard meaning [68]. If we set to zero the $[\partial V_G/T]$ from equation (5.16) (i.e. $[\partial V_G/\partial T]$=0) and use expressions

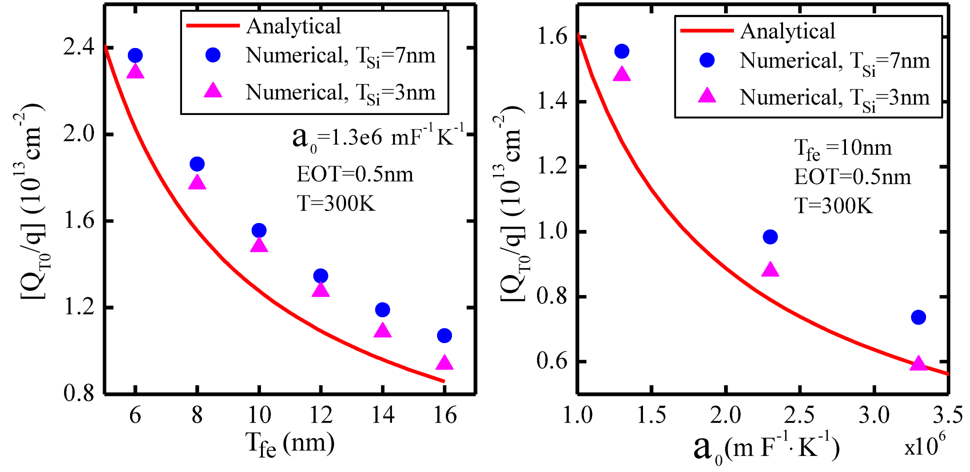

FIGURE 5.25. Charge Q_{T0} corresponding to $[\partial V_{ox}/\partial T]$=0 at fixed Q versus the material parameter T_{Fe}, on the left, and versus a_0 coefficient, on the right. It is clear that thinner T_{si} will result in values closer to the analytical model, as we are approaching the quantum-limit condition.

in equation (5.17), we can readily obtain an equation that can be solved for Q_{T0} and describes the point that is insensitive to temperature in figure 5.25(right).

Another way to analyze this type of variability is shown in figure 5.25. Here we compare the Q_{T0} versus a_0 and T_{Fe} curves obtained from our analytical model with the corresponding values determined from numerical simulations obtained with the Schrödinger-Poisson solver. The agreement between the analytical and numerical results is good and the accuracy improves when the silicon film thickness is scaled, which is an expected behavior for a model based on the quantum limit condition.

Chapter 6

Conclusions and future perspectives

During the PhD project we have addressed the problem of the reduction of energy consumption in integrated circuits at transistor level, in particular focusing on the *negative-capacitance* (NC) FET. The results from our research activity show that this device is an interesting and promising device concept that can effectively reduce the V_{DD} budget required to operate the ICs in the more-Moore era.

6.1 Summary of the work

We started the work in this PhD program by discussing the relevance of the Tunnel FET, one of the most studied *steep-slope* transistor concept in the last ten years, that exploits a shift of the working principle (compared to conventional CMOS FETs) from the thermionic-emission towards the BTB Tunneling. Our numerical simulation framework, consisting of several types of simulations (ranging from commercial TCAD [55] to in-house developed NEGF simulators [37, 80]), allowed us to analyze different aspects of the sub-threshold region of such devices, and showed that an SS lower than 60mV/dec can be reached in long channel TFETs. However we demonstrated also that, for an aggressive scaling of the channel length, the electrostatics of Tunnel FETs tends to degrade faster compared to their conventional MOSFETs counterparts, resulting in a rapid degradation of the sub-60mV/dec swing in nanoscaled transistors. For this reason, and also due to the reduced $[I_{on}/I_{off}]$ ratio compared to CMOS transistor, we shifted our attention to another technology, in particular to transistors that exploit the negative-capacitance in ferroelectric materials.

To explore the feasibility and the effectiveness of ferroelectrics negative capacitance concept in modern CMOS transistors we developed a

numerical solver of the Landau-Khalatnikov Equation (LKE). This simulator solves the dynamics of the ferroelectric material and also takes into account its anisotropic nature by describing the evolution of the polarization of each domain. An effective procedure has been proposed to calibrate the coefficients of the LKE model against several experimental data and for some different materials (such as HZO or perovskites): our results showed a good agreement with experimental electric field versus polarization curves, validating both the procedure and the multi-domain LKE approach. Moreover, the simulator has been extended in order to describe a negative capacitance transistor in a quasi-2D framework, by combining the LKE solver with a Schrödinger-Poisson solver.

We have also implemented in our simulator a Shockley-Read-Hall (SRH) model to describe the dynamics of interface traps, which allowed us to evaluate the influence of such defects in NC-FETs. Quasi-static simulations showed that the presence of interface traps influences differently the two NC-FET designs, depending on the sign of the gate-stack capacitance C_{di} [122]. In particular we have shown that the presence of interface traps can, in principle, improve the capacitance matching between the negative value of C_{di} and the semiconductor capacitance C_{sct} in steep-slope negative-capacitance FETs, leading to an improvement of both the SS and of the amplitude of hysteresis [170]. On the other hand, due to the finite time-response of capture and emission phenomena, fully-dynamic simulations suggest that the effect of interface traps is expected to be limited in real devices operating at medium-high frequencies. Moreover the presence of traps is well known to degrade the carrier transport, suggesting that this solution is not actually practical.

The original numerical analysis presented in this thesis, supported also by some experimental results, demonstrates the promising properties of ferroelectric NC-FETs. The main advantages of such technology can be identified in high $[I_{on}/I_{off}]$ ratios, similar to state-of-the-art MOSFETs, improved on-state transconductance, which means a smaller V_{GS} swing required to reach given values of on-currents. Moreover, the fact that the ferroelectrics can be easily integrated into already existing MOSFET designs, and thus the possibility to exploit fully CMOS-compatible processes to fabricate them, is a very appealing feature both from scaling and manufacturing perspectives. An extensive analysis on the maximum operative frequency is still missing, but recent experiments suggest that a stabilized NC operation allows switching speeds comparable to conventional MOSFETs. The drawbacks in NC-FETs, however, seem to be essentially related to the switching and unstable nature of ferroelectricity, but they may be overcome with a proper engineering of the whole device design.

For these reasons the NC-FET offers better features compared to other steep-slope and low-power devices proposed to go beyond conventional CMOS transistors, such as Band-to-Band tunneling based devices.

6.2 Future outlook

Due to the versatility of their design, ferroelectric-based devices are still attracting the attention of scientists and engineers in several research fields, stimulating different studies on possible improvements and on alternative employments for modern electronics.

We are already working to the improvement of our models in several respects. For example, we are including a more realistic quasi-ballistic transport model: this will also introduce a more complex dependence of the NC-FET characteristics on the temperature. For the part focused on the modeling of ferroelectrics, instead, we are currently improving the simplified framework presented in this thesis by extending the theory reported in [157,158], allowing then a detailed 3D description of the material when deposited on a dielectric layer.Furthermore, we are also working on the improvement of computational efficiency of the LKE solver by exploiting new approaches involving the implicit formulation of discrete differential problems (within the framework of the MIT-FVG exchange project entitled " Negative Capacitance Field Effect Transistors for Highly Energy Efficient Electronics: Modelling, Design and Optimization").

From a device design perspective an interesting idea consists in the fact that, according to the static Landau-Khalatnikov Equation framework that describes the voltage-polarization relation as an S-shaped curve, it should be possible to design the device to exploit the negative-slope branch in the sub-threshold regime of the transistor, and then move to the positive-slope branch when approaching the inversion region. With a proper design and favourable material parameters this could, in principle, improve both the off-state and the on-state of the negative-capacitance FET device.

Recently, moreover, ferroelectric materials have been also proposed as a possible way to increase the speed of operation for *neuromorphic-computing* applications. The main idea is to exploit the switching capabilities of such materials, as opposed to negative-capacitance operations, to modulate the threshold voltage of the transistor that is used as a synapse [172]. The interesting fact is that the presence of domains may allow us to control the resulting threshold voltage and thus the conductance of the Ferroelectric FET in small steps. This can be used to dynamically

change the weight of the ferroelectric based synaptic device.

Negative capacitance transistors, and in general all ferroelectric devices, are indeed promising electron device concepts that deserve future research work. The are in fact promising in terms of both energy efficient devices for the IoT era and in terms of hardware accelerators for the emerging neuromorphic computing.

Appendix A

The Pseudo Spectral method

Differential problems are usually discretized with finite-difference (FD) or finite-element (FE) methods. These methods are largely used due to their flexibility as they are general-purpose numerical solution methods, but their main drawback is a fixed and low order accuracy. The pseudospectral (PS) method, instead, is an alternative numeric method that allows one to obtain a higher order accuracy with respect to FE and FD methods and a remarkable reduction in the CPU time due to the reduced number of discretization points.

For analytic functions, the PS method allows for errors to decay (as the number of discretization points N increases) typically at exponential rates rather than at polynomial rates. Moreover, the approach is surprisingly powerful for many cases in which both solutions and variable coefficients are non-smooth or even discontinuous, and the relatively coarse grids in PS methods result in time and memory reduction [189, 190].

Pseudo Spectral method for bounded domains

The starting point to compute derivatives of generic functions $u(x) \in \mathbb{C}$ with this procedure is similar to the standard first-order finite difference in fact, by truncating the Taylor series at the first order, we can write:

$$\frac{du(x_i)}{dx} = \frac{u(x_i + h) - u(x_i)}{h} \tag{A.1}$$

where h is the discretization step and x_i is a generic point of the grid. According to the matrix formalism, and by writing $u(x_i)$ as a column vector, the first-order FD method leads to a bi-diagonal differentiation matrix, while considering higher order approximations will add elements into the differentiation matrix. By taking this process to its theoretical limit we end up with a differentiation formula of infinite order and with a dense differentiation matrix: this is, in principle, the fundamental idea of

PS method. The PS method, for this reason, is a very powerful method because the derivative calculated in x_i depends on all the points of the domain. From here on, for the sake of simplicity, in the derivation of the PS method we will consider a one-dimensional case within a bounded domain $[a, b]$.

The PS method allows us to approximate the function $u(x)$, defined on a given set of point x_i (with i=0,. . . ,N), as a sum of smooth basis functions using N-degree algebraic or trigonometric interpolating polynomials $p(x)$. To correctly exploit the PS method, we need to go through two main steps, namely the choice of a proper interpolating function to compute the derivatives, and the knowledge of the discrete points x_i where the calculation is computed. The function $p(x)$ is approximated using the interpolating polynomial of the highest degree (i.e. of degree N), which can be written as:

$$u(x) \approx p(x) = \sum_{j=0}^{N} l_j(x) u(x_j) \,, \quad x \in [a, b] \tag{A.2a}$$

$$l_j(x) = \prod_{\substack{i=0 \\ j \neq i}}^{N} \frac{x - x_i}{x_j - x_i} \,, \quad j = 0, \ldots, N \tag{A.2b}$$

where l_j are the N+1 Lagrange polynomials defined in (A.2b) and x_j the N+1 nodes of the discretization grid where the function is computed. It can easily be noted that the $l_j(x_i)$ assumes the value “1” when $i = j$ and “0” when $i \neq j$.

One of the most used and effective discretization technique according to literature [189,190], is obtained with Chebyshev points over the chosen domain, and they are defined by the equation:

$$x_i = \frac{b + a}{2} - \frac{b - a}{2} cos \left(\frac{i\pi}{N} \right) \tag{A.3}$$

and correspond to the projection on the x-axis of the equispaced points on the circle with radius $[(b - a)/2]$, as illustrated in figure A.1. The choice for Chebyshev points has an important strength compared to a uniform grid, as it removes the problem associated with the inability to approximate a smooth function at the boundaries (which, incidentally, is the case of a wave-function of the semiconductor penetrating into the oxide).

The main idea is then to approximate the unknown derivative of the $u(x_i)$ using the derivatives of the approximated $p(x_i)$, in particular we

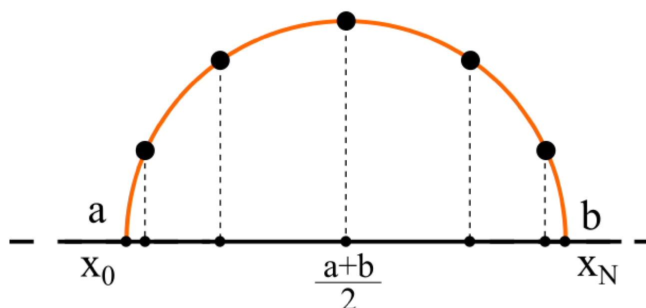

FIGURE A.1. Sketch of the Chebyshev discretization grid in a 1D domain, described as the projections of equispaced points on a semicircle onto the x-axys. The circle has radius $[(b-a)/2]$ where the points a, b are the intersections between the axis and the circumference at the coordinate x_0 and x_N respectively.

can write for $x \in [a, b]$:

$$\left.\frac{du(x)}{dx}\right|_{x_i} \approx \left.\frac{dp(x)}{dx}\right|_{x_i} = \sum_{j=0}^{N} l'_j(x_i)u(x_j) \tag{A.4}$$

where l' is the derivative of the Lagrange polynomial and i, j=[1,N]. As the initial problem is become linear and involves N+1 elements, we can exploit the matrix formalism to write the derivatives as follows:

$$\underbrace{\begin{bmatrix} u'(x_0) \\ u'(x_1) \\ \vdots \\ u'(x_N) \end{bmatrix}}_{\bar{u}'_{N+1}} \approx \underbrace{\begin{bmatrix} l'_0(x_0) & l'_1(x_0) & l'_2(x_0) & \dots & l'_N(x_0) \\ l'_0(x_1) & l'_1(x_1) & l'_2(x_1) & \dots & l'_N(x_1) \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ l'_0(x_N) & l'_1(x_N) & l'_2(x_N) & \dots & l'_N(x_N) \end{bmatrix}}_{\mathbf{D}_{N+1}} \underbrace{\begin{bmatrix} u(x_0) \\ u(x_1) \\ \vdots \\ u(x_N) \end{bmatrix}}_{\bar{u}_{N+1}} \tag{A.5}$$

where $\mathbf{D}_{N+1}$ is the (N+1)×(N+1) first order differentiation matrix and explicit calculations of it are reported in [189]. The interesting fact is that higher order derivatives can be computed recursively, in fact for instance the second order derivative is written as

$$\begin{aligned} \left.\frac{d^2u(x)}{dx^2}\right|_{x_i} = \frac{d}{dx}\left.\left(\frac{du(x)}{dx}\right)\right|_{x_i} &\approx \sum_{j=0}^{N} l'_j(x_i)u'(x_j) = \sum_{j=0}^{N}\sum_{m=0}^{N} l'_j(x_i)l'_m(x_j)u'(x_m) \\ &= \mathbf{D}^2_{N+1}\bar{u}_{N+1} \end{aligned} \tag{A.6}$$

which can be easily extended to the k-order derivative by simply rising the differentiation matrix at the power of k.

Boundary conditions

Partial differential equations that are used to describe physical phenomena are completely defined only when appropriate boundary conditions are

set. The PS method includes these conditions in a very straightforward manner. To address the problem we will consider a second-order derivative which can be, for example, the Poisson equation:

$$\varepsilon\frac{d^2u(x)}{dx^2} = -\rho(x) \ \rightarrow \ \mathbf{D}^2_{N+1}\bar{u}_{N+1} = \mathbf{E}_{N+1}\bar{u}_{N+1} = -\frac{\bar{\rho}_{N+1}}{\varepsilon} \ . \tag{A.7}$$

The next step is to define a set of boundary conditions to univocally solve the problem. These conditions can be written by using Robin's boundary conditions, which are defined as a combination of the values of the functions and their derivatives at the extrema of the domain:

$$\begin{cases} \alpha_a u(a) + \beta_a u'(a) = \gamma_a \ \text{ for } x = a \\ \alpha_b u(b) + \beta_b u'(b) = \gamma_b \ \text{ for } x = b \end{cases} \tag{A.8}$$

where α, β and γ are generic constants for the specific boundary. By substituting into the system (A.8) the definition of the derivative of $u(x)$, according to the PS method, and for the points $x{=}a, b$ we obtain a new system that depends only on the function value (and not on its derivatives):

$$\begin{cases} \alpha_a u(a) + \beta_a \mathbf{D}_{N+1}(0,:)\bar{u}_{N+1} = \gamma_a \\ \alpha_b u(b) + \beta_b \mathbf{D}_{N+1}(N,:)\bar{u}_{N+1} = \gamma_b \end{cases} \tag{A.9}$$

In equations (A.9), the terms that can be expressed generically as $\mathbf{D}_{N+1}$(i,:) denote the [1×(N+1)] row vectors obtained by taking all the columns of the specific i-th row of the $\mathbf{D}_{N+1}$ differentiation matrix. The system, moreover, can be re-arranged in a more compact way as follows:

$$\begin{cases} \mathbf{P}_a\bar{u}_{N+1} = \gamma_a \\ \mathbf{P}_b\bar{u}_{N+1} = \gamma_b \end{cases} \tag{A.10}$$

where $\mathbf{P}_a$ and $\mathbf{P}_b$ are defined as

$$\begin{aligned} \mathbf{P}_a &= \Big[\underbrace{\alpha_a + \beta_a\mathbf{D}_{N+1}(0,0)}_{\mathbf{P}_a^{11}} \ \underbrace{\beta_a\mathbf{D}_{N+1}(0,1:N-1)}_{\mathbf{P}_a^{12}} \ \underbrace{\beta_a\mathbf{D}_{N+1}(0,N)}_{\mathbf{P}_a^{13}}\Big] \\ \mathbf{P}_b &= \Big[\underbrace{\beta_b\mathbf{D}_{N+1}(N,0)}_{\mathbf{P}_b^{31}} \ \underbrace{\beta_b\mathbf{D}_{N+1}(N,1:N-1)}_{\mathbf{P}_b^{32}} \ \underbrace{\alpha_b + \beta_b\mathbf{D}_{N+1}(N,N)}_{\mathbf{P}_b^{33}}\Big] . \end{aligned} \tag{A.11}$$

Our choice for the label of superscripts of the $\mathbf{P}$ vectors will appear clear in the next step. The final set of equations to solve numerically the differential problem in equation (A.7) is obtained by substituting the first and last rows of equation (A.7) with the corresponding equations in (A.9), thus the final system to be solved is:

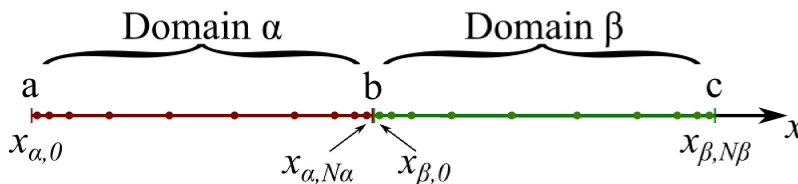

FIGURE A.2. Sketch of an heterogeneous domain discretized with Chebyshev points. The two domains share the same boundary point b, that corresponds to the superposition of the coordinates x_{α,N_α} and $x_{\beta,0}$.

$$\begin{bmatrix} \mathbf{P}_a^{11}\ \mathbf{P}_a^{12}\ \mathbf{P}_a^{13} \\ \varepsilon\mathbf{E}_{N+1}(1:N-1,:) \\ \mathbf{P}_b^{31}\ \mathbf{P}_a^{32}\ \mathbf{P}_a^{33} \end{bmatrix} \begin{bmatrix} \bar{u}_{N+1}(0) \\ \bar{u}_{N+1}(1:N-1) \\ \bar{u}_{N+1}(N) \end{bmatrix} = \begin{bmatrix} \gamma_a \\ \bar{\rho}_{N+1}(1:N-1) \\ \gamma_b \end{bmatrix}. \tag{A.12}$$

Presence of heterostructures

Usually the overall domain in which the numerical problem is solved might consist of several sub-domains with different properties. This is the case, for instance, of the solutions of either the Schrödinger equation, that takes into account also the penetration of the wave-function, and of the Poisson equation. For the description of electron devices, thus, the characterization of heterostructures with the PS method need to be carefully investigated.

For the sake of simplicity hereafter we will consider the case of a two-material domain within a one-dimensional framework, as sketched in figure A.2. In this case we must define two separate domains, namely α and β, with their own differentiation matrices, their number of discretization points N_α, N_β and their boundaries that are, in this case, $a \leq x \leq b$ for α and $b \leq x \leq c$ for β. The solution for the overall problem is then obtained by coupling the two problems by means of appropriate continuity conditions. Let us consider again the case of the Poisson equation that is a second-order derivative problem and hence, according to the PS approach, we can write:

$$\begin{cases} \varepsilon_\alpha \mathbf{E}_{\alpha,N_\alpha+1}\bar{u}_\alpha = -\bar{\rho}_\alpha \\ \varepsilon_\beta \mathbf{E}_{\beta,N_\beta+1}\bar{u}_\beta = -\bar{\rho}_\beta \end{cases} \tag{A.13}$$

where the subscripts relate the quantities to their respective α and β domains, and $\mathbf{E}_{m,N_m+1}$ is the generic second-order matrix derivative of dimensions $[(N_m+1)\times(N_m+1)]$, consistently with equation (A.7). By exploiting again the matrix formalism to describe both the regions and assembling the resulting matrices, we can write the whole system to be

solved as:

$$\begin{bmatrix} \varepsilon_\alpha \begin{bmatrix} \mathbf{E}_\alpha^{11} & \mathbf{E}_\alpha^{12} & \mathbf{E}_\alpha^{13} \\ \mathbf{E}_\alpha^{21} & \mathbf{E}_\alpha^{22} & \mathbf{E}_\alpha^{23} \\ \mathbf{E}_\alpha^{31} & \mathbf{E}_\alpha^{32} & \mathbf{E}_\alpha^{33} \end{bmatrix} & 0 \\ 0 & \varepsilon_\beta \begin{bmatrix} \mathbf{E}_\beta^{11} & \mathbf{E}_\beta^{12} & \mathbf{E}_\beta^{13} \\ \mathbf{E}_\beta^{21} & \mathbf{E}_\beta^{22} & \mathbf{E}_\beta^{23} \\ \mathbf{E}_\beta^{31} & \mathbf{E}_\beta^{32} & \mathbf{E}_\beta^{33} \end{bmatrix} \end{bmatrix} \begin{bmatrix} u_{\alpha,a} \\ \bar{u}_{\alpha,inn} \\ u_{\alpha,b} \\ u_{\beta,b} \\ \bar{u}_{\beta,inn} \\ u_{\beta,c} \end{bmatrix} = - \begin{bmatrix} \rho_{\alpha,a} \\ \bar{\rho}_{\alpha,inn} \\ \rho_{\alpha,b} \\ \rho_{\beta,b} \\ \bar{\rho}_{\beta,inn} \\ \bar{\rho}_{\beta,c} \end{bmatrix}. \tag{A.14}$$

Once the linear system correspondent to our differential problem is defined, we must enforce the boundary and the continuity conditions. Assuming that, for example, we are considering the Poisson equation and $u(x)$ is the potential profile of the structure, the continuity conditions between the two domains α and β can be interpreted as the continuity of the potential and the conservation of the electrical displacement at the interface, respectively:

$$\begin{aligned} & u_{\alpha,b} = u_{\beta,b} \\ & \varepsilon_\alpha \left. \frac{du(x)}{dx} \right|_{x=b^-} = \varepsilon_\beta \left. \frac{du(x)}{dx} \right|_{x=b^+} \end{aligned} \tag{A.15}$$

These conditions, together with the boundary conditions, can be imposed by using a straightforward approach that explicitly substitute the equations (A.15) into the system (A.14). For the boundary conditions, which are assumed to be Robin's conditions (see equation (A.8)), we can just substitute the first and the latter row with their compact formulation as in equations (A.10) and as discussed above. To apply the continuity conditions, similarly, we are going to replace the third and the fourth row with equations (A.15), which leads to the new system of equations describing the whole domain:

$$\begin{bmatrix} \mathbf{P}_a^{11} \ \mathbf{P}_a^{12} \ \mathbf{P}_a^{13} & 0 \\ \varepsilon_\alpha[\mathbf{E}_\alpha^{21} \ \mathbf{E}_\alpha^{22} \ \mathbf{E}_\alpha^{23}] & 0 \\ 0 \quad 0 \quad 1 & -1 \quad 0 \quad 0 \\ \varepsilon_\alpha \mathbf{D}_\alpha(N_\alpha,:) & -\varepsilon_\beta \mathbf{D}_\beta(N_\beta,:) \\ 0 & \varepsilon_\beta[\mathbf{E}_\beta^{21} \ \mathbf{E}_\beta^{22} \ \mathbf{E}_\beta^{23}] \\ 0 & \mathbf{P}_c^{31} \ \mathbf{P}_c^{32} \ \mathbf{P}_c^{33} \end{bmatrix} \begin{bmatrix} u_{\alpha,a} \\ \bar{u}_{\alpha,inn} \\ u_{\alpha,b} \\ u_{\beta,b} \\ \bar{u}_{\beta,inn} \\ u_{\beta,c} \end{bmatrix} = \begin{bmatrix} \gamma_a \\ \bar{\rho}_{\alpha,inn} \\ 0 \\ 0 \\ \bar{\rho}_{\beta,inn} \\ \gamma_c \end{bmatrix} \tag{A.16}$$

where $\mathbf{D}_m$(n,:) denotes the n-th row of the first-order differentiation matrix $\mathbf{D}_m$ for the generic domain m. This is the final system to solve that approximates the initial differential problem, but we recall that the vector of solutions contains two degenerate values for the interface at x=b.

As can be understood, this method is very flexible and can be extended to several other differential problems with an arbitrary amount of different domains. Moreover we can also apply different boundary conditions, like

Dirichlet or Neumann conditions, without any kind of loss in the generalization of the model. For instance, in our Schrödinger-Poisson solver we forced the value of the ferroelectric polarization at the semiconductor-oxide interface, which is a Neumann boundary condition for the Poisson equation in the semiconductor, instead of imposing the outer voltage. This choice ease the solution of the Landau-Khalatnikov equation coupled with the Schrödinger-Poisson problem in the numerical description of the device.

Appendix B

List of Publications

Journal Papers

David Esseni, Manuel Guglielmini, Bernard Kapidani, Tommaso Rollo, Massimo Alioto, "*Tunnel FETs for Ultralow Voltage Digital VLSI Circuits: Part I—Device–Circuit Interaction and Evaluation at Device Level* ", IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 22, no. 12, pp. 2488 - 2498, 2014;

David Esseni, Marco G. Pala, Tommaso Rollo, "*Essential Physics of the OFF-State Current in Nanoscale MOSFETs and Tunnel FETs* ", IEEE Transactions on Electron Devices, vol. 62, no. 9, pp. 3084 - 3091, 2015;

Tommaso Rollo, David Esseni, "*Energy Minimization and Kirchhoff's Laws in Negative Capacitance Ferroelectric Capacitors and MOSFETs* ", IEEE Electron Device Letters, vol. 38, no. 6, pp. 814 - 817, 2017;

David Esseni, Marco G. Pala, Pierpaolo Palestri, Cem Alper, Tommaso Rollo, "*A review of selected topics in physics based modeling for tunnel field-effect transistors* ", Semiconductor Science and Technology , vol. 32, no. 8, pp. 1 - 27, 2017;

Tommaso Rollo, David Esseni, "*New Design Perspective for Ferroelectric NC-FETs* ", IEEE Electron Device Letters, vol. 39, no. 4, pp. 603 - 606, 2018;

Tommaso Rollo, David Esseni, "*Influence of Interface Traps on Ferroelectric NC-FETs* ", IEEE Electron Device Letters, vol. 39, no. 7, pp. 1100 - 1103, 2018;

Conference Papers

Tommaso Rollo, David Esseni, "*Supersteep retrograde doping in ferroelectric MOSFETs for sub-60mV/dec subthreshold swing* ", 46th European Solid-State Device Research Conference (ESSDERC), pp. 360 - 363, Lausanne, 2016;

David Esseni, Oves Badami, Francesco Driussi, Daniel Lizzit, Marco G. Pala, Pierpaolo Palestri, Tommaso Rollo, Luca Selmi, Stefano Venica, "*New device concepts, transistor architectures and materials for high performance and energy efficient CMOS circuits in the forthcoming era of 3D integrated circuits* ", IEEE 2nd Electron Devices Technology and Manufacturing Conference (EDTM), pp. 236 - 238, Kobe, 2018;

Tommaso Rollo, David Esseni, "*Modelling and design of Ferroelectric NC-FETs*", 50th Meeting Società Italiana di Elettronica (SIE), Naples, 2018;

Tommaso Rollo, Hongjuan Wang, Genquan Han, David Esseni, "*A simulation based study of NC-FETs design: off-state versus on-state perspective* ", 2018 IEEE International Electron Devices Meeting (IEDM), San Francisco, 1-5 Dec. 2018;

Bibliography

[1] D. Zhou, Y. Guan, M. Vopson, J. Xu, H. Liang, F. Cao, X. Dong, and J. Mueller, "Electric field and temperature scaling of polarization reversal in silicon doped hafnium oxide ferroelectric thin films," *Acta Materialia*, vol. 99, pp. 240 – 246, 2015.

[2] P. Sharma, K. Tapily, A. K. Saha, J. Zhang, A. Shaughnessy, A. Aziz, G. L. Snider, S. Gupta, R. D. Clark, and S. Datta, "Impact of total and partial dipole switching on the switching slope of gate-last negative capacitance FETs with ferroelectric hafnium zirconium oxide gate stack," in *2017 Symposium on VLSI Technology*, June 2017. doi: 10.23919/VLSIT.2017.7998160 pp. T154–T155.

[3] Z. Krivokapic, U. Rana, R. Galatage, A. Razavieh, A. Aziz, J.Liu, J.Shi, H. Kim, R. Sporer, C. Serrao, A.Busquet, P. Polakowski, J. Mülle, W. Kleemeier, A. Jacob, D. Brown, A. Knorr, R. Carter, and S. Banna, GLOBALFOUNDRIES, "14nm Ferroelectric FinFET Technology with Steep Subthreshold Slope for Ultra Low Power Applications," in *2017 IEEE International Electron Devices Meeting (IEDM)*, December 2017. doi: 10.1109/IEDM.2017.8268393. ISSN 2156-017X pp. 357–360.

[4] Q. Han, T. C. U. Tromm, J. Schubert, S. Mantl, and Q. Zhao, "Steep slope negative capacitance FDSOI MOSFETs with ferroelectric HfYOx," in *2018 Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon (EUROSOI-ULIS)*, March 2018. doi: 10.1109/ULIS.2018.8354733. ISSN 2472-9132 pp. 1–4.

[5] M. Paolo, "Why a Universal RFID Infrastructure Would Be a Good Thing," in *Gartner research report G00106518*, vol. SPA-16-0061, May 2002, pp. 1–4.

[6] P. Magrassi and T. Berg, "A World of Smart Objects: The Role of Auto-Identification Technologies," in *Gartner research report G00109050*, vol. R-17-2243, August 2002, pp. 1–4.

[7] N. I. C. N. USA. (2008) Disruptive Technologies Global Trends 2025. Apendix F, p.27. [Online]. Available: https://www.dni.gov/nic/PDF_GIF_confreports/disruptivetech/appendix_F.pdf

[8] T. G. S. G. Inc., “The Internet of Things: making sense of the next mega-trend,” in *Goldman Sachs Global Investment Research*, Sep 2014, pp. 1–15.

[9] C. M. University. (2014) The Only Coke Machine on the Internet. [Online]. Available: https://www.cs.cmu.edu/~coke/

[10] W. M., “The computer for the 21st century,” in *Scientific American*, vol. 265, no. 3, Sep 1991.

[11] R. S. Raji, “Smart networks for control,” *IEEE Spectrum*, vol. 31, no. 6, pp. 49–55, June 1994. doi: 10.1109/6.284793

[12] M. Friedemann and F. Christian, “From the Internet of Computer to the Internet of Things,” *Informatik-Spektrum*, vol. 3, no. 2, pp. 107–121, 2010. doi: 10.1007/s00287-010-0417-7

[13] D. Evans, “The internet of things: How the next evolution of the internet is changing everything,” *Cisco Internet Business Solutions Group (IBSG)*, vol. 1, pp. 1–11, 01 2011.

[14] M. Yogeesh, H. Chang, W. Li, S. Rahimi, A. Rai, A. Sanne, R. Ghosh, S. K. Banerjee, and D. Akinwande, “Towards wafer scale monolayer MoS2based flexible low-power RF electronics for IoT systems,” in *2016 74th Annual Device Research Conference (DRC)*, June 2016. doi: 10.1109/DRC.2016.7548483 pp. 1–2.

[15] N. Watthanawisuth, T. Maturos, A. Sappat, and A. Tuantranont, “The IoT wearable stretch sensor using 3D-Graphene foam,” in *2015 IEEE SENSORS*, Nov 2015. doi: 10.1109/ICSENS.2015.7370275 pp. 1–4.

[16] S. G. Lemay, C. Laborde, C. Renault, A. Cossettini, L. Selmi, and F. P. Widdershoven, “High-frequency nanocapacitor arrays: Concept, recent developments, and outlook,” *Accounts of Chemical Research*, vol. 49, no. 10, pp. 2355–2362, 2016. doi: 10.1021/acs.accounts.6b00349

[17] S. A. Larry Greenmayer. (2016) IoT Growing Faster Than the Ability to Defend It. [Online]. Available: https://www.scientificamerican.com/article/iot-growing-faster-than-the-ability-to-defend-it/

[18] W. Sousa, E. Souto, T. Rocha, N. Pereira, P. Kool, and P. Rosengren, "Prediction of electrical energy consumption for internet of things in disaggregated databases," in *2016 IEEE Symposium on Computers and Communication (ISCC)*, June 2016. doi: 10.1109/ISCC.2016.7543777 pp. 429–434.

[19] S. S. Prasad and C. Kumar, "An energy efficient and reliable internet of things," in *2012 International Conference on Communication, Information Computing Technology (ICCICT)*, Oct 2012. doi: 10.1109/ICCICT.2012.6398115 pp. 1–4.

[20] P. M. Corcoran, "Third time is the charm - Why the world just might be ready for the Internet of Things this time round," *ArXiv*, pp. 1–5, April 2017.

[21] A. Shehabi, S. J. Smith, D. A. Sartor, R. E. Brown, M. Herrlin, J. G. Koomey, E. R. Masanet, N. Horner, I. L. Azevedo, and W. Lintner, "United States Data Center Energy Usage Report - Berkeley National Laboratory," Tech. Rep., june 2016.

[22] S. Saggini, O. Zambetti, R. Rizzolatti, M. Picca, and P. Mattavelli, "An Isolated Quasi-Resonant Multiphase Single-Stage Topology for 48-V VRM Applications," *IEEE Transactions on Power Electronics*, vol. 33, no. 7, pp. 6224–6237, July 2018. doi: 10.1109/TPEL.2017.2740058

[23] T. Liu, M. Leskes, W. Yu, A. J. Moore, L. Zhou, P. M. Bayley, G. Kim, and C. P. Grey, "Cycling Li-O2 batteries via LiOH formation and decomposition," *Science*, vol. 350, no. 6260, pp. 530–533, 2015. doi: 10.1126/science.aac7730. [Online]. Available: http://science.sciencemag.org/content/350/6260/530

[24] A. Ahmed, I. T. Hassan, P. Song, M. Gamaleldin, A. A. Radhi, N. Panwar, S. C. Tjin, A. Desoky, D. Sinton, K.-T. Yong, and J. Zu, "Self-adaptive bioinspired hummingbird-wing stimulated triboelectric nanogenerators," in *Scientific Reports*, vol. 7, no. 1, 2017. doi: 10.1038/s41598-017-17453-4

[25] P. Lynggaard, "A self-supporting wireless iot node that uses kinetic energy harvesting," in *2017 Internet of Things Business Models, Users, and Networks*, Nov 2017. doi: 10.1109/CTTE.2017.8260986 pp. 1–6.

[26] Y. Hsieh, C. Fang, C. Su, H. Tsai, and Y. Juang, "A hybrid ambient energy harvesting integrated chip (IC) for the Internet of Things (IoT) and portable applications," in *2016 19th International Conference on Electrical Machines and Systems (ICEMS)*, Nov 2016, pp. 1–4.

[27] "International Roadmap for Devices and Systems (IRDS)," https://irds.ieee.org/roadmap-2017, 2017 Edition.

[28] M. Alioto, "Ultra-Low Power VLSI Circuit Design Demystified and Explained: A Tutorial," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 59, no. 1, pp. 3–29, Jan 2012. doi: 10.1109/TCSI.2011.2177004

[29] M. B. Taylor, "Is dark silicon useful? Harnessing the four horsemen of the coming dark silicon apocalypse," in *DAC Design Automation Conference 2012*, June 2012. ISSN 0738-100X pp. 1131–1136.

[30] J. T. Kao, M. Miyazaki, and A. R. Chandrakasan, "A 175-MV multiply-accumulate unit using an adaptive supply voltage and body bias architecture," *IEEE Journal of Solid-State Circuits*, vol. 37, no. 11, pp. 1545–1554, Nov 2002. doi: 10.1109/JSSC.2002.803957

[31] D. Esseni, M. Guglielmini, B. Kapidani, T. Rollo, and M. Alioto, "Tunnel FETs for Ultralow Voltage Digital VLSI Circuits: Part I—Device–Circuit Interaction and Evaluation at Device Level," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 22, no. 12, pp. 2488–2498, Dec 2014. doi: 10.1109/TVLSI.2013.2293135

[32] A. Wang and A. Chandrakasan, "A 180-mV subthreshold FFT processor using a minimum energy design methodology," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 1, pp. 310–319, Jan 2005. doi: 10.1109/JSSC.2004.837945

[33] Y. K. Ramadass and A. P. Chandrakasan, "Minimum Energy Tracking Loop With Embedded DC–DC Converter Enabling Ultra-Low-Voltage Operation Down to 250 mV in 65 nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 1, pp. 256–265, Jan 2008. doi: 10.1109/JSSC.2007.914720

[34] M. Ashouei, J. Hulzink, M. Konijnenburg, J. Zhou, F. Duarte, A. Breeschoten, J. Huisken, J. Stuyt, H. de Groot, F. Barat, J. David, and J. V. Ginderdeuren, "A voltage-scalable biomedical signal processor running ECG using 13pJ/cycle at 1MHz and 0.4V," in *2011 IEEE International Solid-State Circuits Conference*, Feb 2011. doi: 10.1109/ISSCC.2011.5746341. ISSN 2376-8606 pp. 332–334.

[35] T. H. N. Yuan Taur, *Fundamentals of Modern VLSI Devices*, 2nd ed. Cambridge University Press, 2009. ISBN 978-0-523-53294-6

[36] K. K. N. Simon M. Sze, *Physics of Semiconductor Devices*, 3rd ed. John Wiley & Sons, New York, USA, 2006. ISBN 978-0-471-14323-9

[37] D. Esseni, M. Pala, P. Palestri, C. Alper, and T. Rollo, "A review of selected topics in physics based modeling for tunnel field-effect transistors," *Semiconductor Science and Technology*, vol. 32, no. 8, p. 083005, 2017. [Online]. Available: http://stacks.iop.org/0268-1242/32/i=8/a=083005

[38] S. Salahuddin and S. Datta, "Use of Negative Capacitance to Provide Voltage Amplification for Low Power Nanoscale Devices," *Nano Letters*, vol. 8, no. 2, 2008. doi: 10.1021/nl071804g

[39] D. Jimenez, E. Miranda, and A. Godoy, "Analytic Model for the Surface Potential and Drain Current in Negative Capacitance Field-Effect Transistors," *IEEE Transactions on Electron Devices*, vol. 57, no. 10, pp. 2405–2409, Oct 2010. doi: 10.1109/TED.2010.2062188

[40] ——, "Erratum: Analytic Model for the Surface Potential and Drain Current in Negative Capacitance Field-Effect Transistors," *IEEE Transactions on Electron Devices*, vol. 58, no. 8, pp. 2818–2818, Aug 2011. doi: 10.1109/TED.2011.2149532

[41] J. P. Duarte, S. Khandelwal, A. I. Khan, A. Sachid, Y. K. Lin, H. L. Chang, S. Salahuddin, and C. Hu, "Compact models of negative-capacitance FinFETs: Lumped and distributed charge models," in *2016 IEEE International Electron Devices Meeting (IEDM)*, Dec 2016. doi: 10.1109/IEDM.2016.7838514 pp. 30.5.1–30.5.4.

[42] M. H. Lee, S. T. Fan, C. H. Tang, P. G. Chen, Y. C. Chou, H. H. Chen, J. Y. Kuo, M. J. Xie, S. N. Liu, M. H. Liao, C. A. Jong, K. S. Li, M. C. Chen, and C. W. Liu, "Physical thickness 1.x nm ferroelectric HfZrOx negative capacitance FETs," in *2016 IEEE International Electron Devices Meeting (IEDM)*, Dec 2016. doi: 10.1109/IEDM.2016.7838400 pp. 12.1.1–12.1.4.

[43] A. Jain and M. A. Alam, "Prospects of hysteresis-free abrupt switching (0 mv/decade) in landau switches," *IEEE Transactions on Electron Devices*, vol. 60, no. 12, pp. 4269–4276, Dec 2013. doi: 10.1109/TED.2013.2286997

[44] H. Lu and A. Seabaugh, "Tunnel Field-Effect Transistors: State-of-the-Art," *IEEE Journal of the Electron Devices Society*, vol. 2, no. 4, pp. 44–49, July 2014. doi: 10.1109/JEDS.2014.2326622

[45] E. Kane, "Zener tunneling in semiconductors," *Journal of Physics and Chemistry of Solids*, vol. 12, no. 2, pp. 181 – 188, 1960. doi: https://doi.org/10.1016/0022-3697(60)90035-4. [Online]. Available: http://www.sciencedirect.com/science/article/pii/0022369760900354

[46] G. A. M. Hurkx, D. B. M. Klaassen, and M. P. G. Knuvers, "A new recombination model for device simulation including tunneling," *IEEE Transactions on Electron Devices*, vol. 39, no. 2, pp. 331–338, Feb 1992. doi: 10.1109/16.121690

[47] T. Y. Chan, J. Chen, P. K. Ko, and C. Hu, "The impact of gate-induced drain leakage current on mosfet scaling," in *1987 International Electron Devices Meeting*, Dec 1987. doi: 10.1109/IEDM.1987.191531 pp. 718–721.

[48] R. Shirota, T. Endoh, M. Momodomi, R. Nakayama, S. Inoue, R. Kirisawa, and F. Masuoka, "An accurate model of subbreakdown due to band-to-band tunneling and its application," in *Technical Digest., International Electron Devices Meeting*, Dec 1988. doi: 10.1109/IEDM.1988.32741. ISSN 0163-1918 pp. 26–29.

[49] M. Takayanagi and S. Iwabuchi, "Theory of band-to-band tunneling under nonuniform electric fields for subbreakdown leakage currents," *IEEE Transactions on Electron Devices*, vol. 38, no. 6, pp. 1425–1431, June 1991. doi: 10.1109/16.81635

[50] G. Ingrosso, L. Selmi, and E. Sangiorgi, "Monte Carlo Simulation of Program and Erase Charge Distributions in NROM(TM) Devices," in *32nd European Solid-State Device Research Conference*, Sept 2002. doi: 10.1109/ESSDERC.2002.194901 pp. 187–190.

[51] J. Knoch and J. Appenzeller, "Tunneling phenomena in carbon nanotube field-effect transistors," *physica status solidi (a)*, vol. 205, no. 4, pp. 679–694, 2008. doi: 10.1002/pssa.200723528. [Online]. Available: https://onlinelibrary.wiley.com/doi/abs/10.1002/pssa.200723528

[52] L. I. Schiff, *Quantum Mechanics, Third Edition.* McGraw-Hill Companies, 1968.

[53] E. O. Kane, "Theory of tunneling," *Journal of Applied Physics*, vol. 32, no. 1, pp. 83–91, 1961. doi: 10.1063/1.1735965

[54] S. Tanaka, "A unified theory of direct and indirect interband tunneling under a nonuniform electric field," *Solid-State Electronics*, vol. 37, no. 8, pp. 1543 – 1552, 1994. doi: https://doi.org/10.1016/0038-1101(94)90163-5. [Online]. Available: http://www.sciencedirect.com/science/article/pii/0038110194901635

[55] S. Inc., *Sentaurus Device User Guide, Version 2016.* (Mountain View, CA: Synopsys Inc.): Synopsys Inc., 2016.

[56] L. V. Keldysh, "Behaviour of Non-Metallic Crystals in Strong Electric Fields." *Soviet Physics: J. Exptl. Theoret. Phys.*, vol. 33, pp. 994–1003, 1957.

[57] W. Vandenberghe, B. Sorée, W. Magnus, and M. V. Fischetti, "Generalized phonon-assisted zener tunneling in indirect semiconductors with non-uniform electric fields: A rigorous approach," *Journal of Applied Physics*, vol. 109, no. 12, p. 124503, 2011. doi: 10.1063/1.3595672

[58] M. Luisier and G. Klimeck, "Simulation of nanowire tunneling transistors: From the Wentzel–Kramers–Brillouin approximation to full-band phonon-assisted tunneling," *Journal of Applied Physics*, vol. 107, no. 8, p. 084507, 2010. doi: 10.1063/1.3386521

[59] K. Boucart and A. M. Ionescu, "Double-gate tunnel fet with high-κgate dielectric," *IEEE Transactions on Electron Devices*, vol. 54, no. 7, pp. 1725–1733, July 2007. doi: 10.1109/TED.2007.899389

[60] A. C. Seabaugh and Q. Zhang, "Low-Voltage Tunnel Transistors for Beyond CMOS Logic," *Proceedings of the IEEE*, vol. 98, no. 12, pp. 2095–2110, Dec 2010. doi: 10.1109/JPROC.2010.2070470

[61] F. Mayer, C. L. Royer, J. . Damlencourt, K. Romanjek, F. Andrieu, C. Tabone, B. Previtali, and S. Deleonibus, "Impact of SOI, $Si_{1-x}Ge_x$OI and GeOI substrates on CMOS compatible Tunnel FET performance," in *2008 IEEE International Electron Devices Meeting*, Dec 2008. doi: 10.1109/IEDM.2008.4796641. ISSN 0163-1918 pp. 1–5.

[62] J. Wan, C. L. Royer, A. Zaslavsky, and S. Cristoloveanu, "Tunneling FETs on SOI: Suppression of ambipolar leakage, low-frequency noise behavior, and modeling," *Solid-State Electronics*, vol. 65-66, pp. 226 – 233, 2011. doi: https://doi.org/10.1016/j.sse.2011.06.012 Selected Papers from the ESSDERC 2010 Conference. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0038110111002218

[63] A. M. Walke, A. Vandooren, B. Kaczer, A. S. Verhulst, R. Rooyackers, E. Simoen, M. M. Heyns, V. R. Rao, G. Groeseneken, N. Collaert, and A. V. Thean, "Part II: Investigation of Subthreshold Swing in Line Tunnel FETs Using Bias Stress Measurements," *IEEE Transactions on Electron Devices*, vol. 60, no. 12, pp. 4065–4072, Dec 2013. doi: 10.1109/TED.2013.2287253

[64] A. Villalon, C. L. Royer, M. Cassé, D. Cooper, B. Prévitali, C. Tabone, J. . Hartmann, P. Perreau, P. Rivallin, J. . Damlencourt, F. Allain, F. Andrieu, O. Weber, O. Faynot, and T. Poiroux,

"Strained tunnel FETs with record ION: first demonstration of ETSOI TFETs with SiGe channel and RSD," in *2012 Symposium on VLSI Technology (VLSIT)*, June 2012. doi: 10.1109/VLSIT.2012.6242455. ISSN 2158-9682 pp. 49–50.

[65] L. Knoll, S. Richter, A. Nichau, A. Schäfer, K. K. Bourdelle, Q. T. Zhao, and S. Mantl, "Gate-all-around Si nanowire array tunnelling FETs with high on-current of 75 μA/μm @ V_{DD}=1.1V," in *2013 14th International Conference on Ultimate Integration on Silicon (ULIS)*, March 2013. doi: 10.1109/ULIS.2013.6523500 pp. 97–100.

[66] A. Villalon, C. L. Royer, P. Nguyen, S. Barraud, F. Glowacki, A. Revelant, L. Selmi, S. Cristoloveanu, L. Tosti, C. Vizioz, J. . Hartmann, N. Bernier, B. Prévitali, C. Tabone, F. Allain, S. Martinie, O. Rozeau, and M. Vinet, "First demonstration of strained SiGe nanowires TFETs with ION beyond 700μA/μm," in *2014 Symposium on VLSI Technology (VLSI-Technology): Digest of Technical Papers*, June 2014. doi: 10.1109/VLSIT.2014.6894369. ISSN 2158-9682 pp. 1–2.

[67] G. V. Luong, K. Narimani, A. T. Tiedemann, P. Bernardy, S. Trellenkamp, Q. T. Zhao, and S. Mantl, "Complementary Strained Si GAA Nanowire TFET Inverter With Suppressed Ambipolarity," *IEEE Electron Device Letters*, vol. 37, no. 8, pp. 950–953, Aug 2016. doi: 10.1109/LED.2016.2582041

[68] D. Esseni, L. Selmi, and P. Palestri, *Nanoscale MOS Transistors*. Cambridge University Press, 2011.

[69] L. Donetti, F. Gámiz, S. Thomas, T. E. Whall, D. R. Leadley, P.-E. Hellström, G. Malm, and M. Östling, "Hole effective mass in silicon inversion layers with different substrate orientations and channel directions," *Journal of Applied Physics*, vol. 110, no. 6, p. 063711, 2011. doi: 10.1063/1.3639281. [Online]. Available: https://doi.org/10.1063/1.3639281

[70] P. M. Solomon, J. Jopling, D. J. Frank, C. D'Emic, O. Dokumaci, P. Ronsheim, and W. E. Haensch, "Universal tunneling behavior in technologically relevant P/N junction diodes," *Journal of Applied Physics*, vol. 95, no. 10, pp. 5800–5812, 2004. doi: 10.1063/1.1699487

[71] S. Richter, C. Sandow, A. Nichau, S. Trellenkamp, M. Schmidt, R. Luptak, K. K. Bourdelle, Q. T. Zhao, and S. Mantl, "Ω-Gated Silicon and Strained Silicon Nanowire Array Tunneling FETs," *IEEE Electron Device Letters*, vol. 33, no. 11, pp. 1535–1537, Nov 2012. doi: 10.1109/LED.2012.2213573

[72] Q. Zhao, S. Richter, C. Schulte-Braucks, L. Knoll, S. Blaeser, G. V. Luong, S. Trellenkamp, A. Schäfer, A. Tiedemann, J. Hartmann, K. Bourdelle, and S. Mantl, "Strained Si and SiGe Nanowire Tunnel FETs for Logic and Analog Applications," *IEEE Journal of the Electron Devices Society*, vol. 3, no. 3, pp. 103–114, May 2015. doi: 10.1109/JEDS.2015.2400371

[73] M. G. Pala and D. Esseni, "Interface Traps in InAs Nanowire Tunnel-FETs and MOSFETs -Part I and II," *IEEE Transactions on Electron Devices*, vol. 60, no. 9, pp. 2795–2801, Sept 2013. doi: 10.1109/TED.2013.2274196

[74] G. Dewey, B. Chu-Kung, J. Boardman, J. M. Fastenau, J. Kavalieros, R. Kotlyar, W. K. Liu, D. Lubyshev, M. Metz, N. Mukherjee, P. Oakey, R. Pillarisetty, M. Radosavljevic, H. W. Then, and R. Chau, "Fabrication, characterization, and physics of III–V heterojunction tunneling Field Effect Transistors (H-TFET) for steep sub-threshold swing," in *2011 International Electron Devices Meeting*, Dec 2011. doi: 10.1109/IEDM.2011.6131666. ISSN 2156-017X pp. 33.6.1–33.6.4.

[75] G. Dewey, B. Chu-Kung, R. Kotlyar, M. Metz, N. Mukherjee, and M. Radosavljevic, "III–V field effect transistors for future ultra-low power applications," in *2012 Symposium on VLSI Technology (VLSIT)*, June 2012. doi: 10.1109/VLSIT.2012.6242453. ISSN 2158-9682 pp. 45–46.

[76] R. Li, Y. Lu, G. Zhou, Q. Liu, S. D. Chae, T. Vasen, W. S. Hwang, Q. Zhang, P. Fay, T. Kosel, M. Wistey, H. Xing, and A. Seabaugh, "AlGaSb/InAs Tunnel Field-Effect Transistor With On-Current of $78\mu A/\mu m$ at 0.5 V," *IEEE Electron Device Letters*, vol. 33, no. 3, pp. 363–365, March 2012. doi: 10.1109/LED.2011.2179915

[77] S. Mookerjea, D. Mohata, T. Mayer, V. Narayanan, and S. Datta, "Temperature-Dependent I–V Characteristics of a Vertical $In_{0.53}Ga_{0.47}As$ Tunnel FET," *IEEE Electron Device Letters*, vol. 31, no. 6, pp. 564–566, June 2010. doi: 10.1109/LED.2010.2045631

[78] A. Vandooren, A. M. Walke, A. S. Verhulst, R. Rooyackers, N. Collaert, and A. V. Y. Thean, "Investigation of the Subthreshold Swing in Vertical Tunnel-FETs Using H_2 and D_2 Anneals," *IEEE Transactions on Electron Devices*, vol. 61, no. 2, pp. 359–364, Feb 2014. doi: 10.1109/TED.2013.2294535

[79] E. Memisevic, J. Svensson, M. Hellenbrand, E. Lind, and L. . Wernersson, "Vertical InAs/GaAsSb/GaSb tunneling field-effect transistor on Si with S = 48 mV/decade and Ion= 10 μA/μm for Ioff= 1

nA/μm at Vds= 0.3 V," in *2016 IEEE International Electron Devices Meeting (IEDM)*, Dec 2016. doi: 10.1109/IEDM.2016.7838450. ISSN 2156-017X pp. 19.1.1–19.1.4.

[80] D. Esseni, M. G. Pala, and T. Rollo, "Essential Physics of the OFF-State Current in Nanoscale MOSFETs and Tunnel FETs," *IEEE Transactions on Electron Devices*, vol. 62, no. 9, pp. 3084–3091, Sept 2015. doi: 10.1109/TED.2015.2458171

[81] C. Auth, C. Allen, A. Blattner, D. Bergstrom, M. Brazier, M. Bost, M. Buehler, V. Chikarmane, T. Ghani, T. Glassman, R. Grover, W. Han, D. Hanken, M. Hattendorf, P. Hentges, R. Heussner, J. Hicks, D. Ingerly, P. Jain, S. Jaloviar, R. James, D. Jones, J. Jopling, S. Joshi, C. Kenyon, H. Liu, R. McFadden, B. McIntyre, J. Neirynck, C. Parker, L. Pipes, I. Post, S. Pradhan, M. Prince, S. Ramey, T. Reynolds, J. Roesler, J. Sandford, J. Seiple, P. Smith, C. Thomas, D. Towner, T. Troeger, C. Weber, P. Yashar, K. Zawadzki, and K. Mistry, "A 22nm high performance and low-power CMOS technology featuring fully-depleted tri-gate transistors, self-aligned contacts and high density MIM capacitors," in *2012 Symposium on VLSI Technology (VLSIT)*, June 2012. doi: 10.1109/VLSIT.2012.6242496. ISSN 2158-9682 pp. 131–132.

[82] S. Natarajan, M. Agostinelli, S. Akbar, M. Bost, A. Bowonder, V. Chikarmane, S. Chouksey, A. Dasgupta, K. Fischer, Q. Fu, T. Ghani, M. Giles, S. Govindaraju, R. Grover, W. Han, D. Hanken, E. Haralson, M. Haran, M. Heckscher, R. Heussner, P. Jain, R. James, R. Jhaveri, I. Jin, H. Kam, E. Karl, C. Kenyon, M. Liu, Y. Luo, R. Mehandru, S. Morarka, L. Neiberg, P. Packan, A. Paliwal, C. Parker, P. Patel, R. Patel, C. Pelto, L. Pipes, P. Plekhanov, M. Prince, S. Rajamani, J. Sandford, B. Sell, S. Sivakumar, P. Smith, B. Song, K. Tone, T. Troeger, J. Wiedemer, M. Yang, and K. Zhang, "A 14nm logic technology featuring 2nd-generation FinFET, air-gapped interconnects, self-aligned double patterning and a 0.0588 μm2SRAM cell size," in *2014 IEEE International Electron Devices Meeting*, Dec 2014. doi: 10.1109/IEDM.2014.7046976. ISSN 2156-017X pp. 3.7.1–3.7.3.

[83] E. Memisevic, J. Svensson, E. Lind, and L. Wernersson, "Vertical Nanowire TFETs With Channel Diameter Down to 10 nm and Point S_{MIN} of 35 mV/Decade," *IEEE Electron Device Letters*, vol. 39, no. 7, pp. 1089–1091, July 2018. doi: 10.1109/LED.2018.2836862

[84] G. Zhou, R. Li, T. Vasen, M. Qi, S. Chae, Y. Lu, Q. Zhang, H. Zhu, J. . Kuo, T. Kosel, M. Wistey, P. Fay, A. Seabaugh, and H. Xing, "Novel gate-recessed vertical InAs/GaSb TFETs with record high

I_{ON} of 180 μA/μm at VDS= 0.5 V," in *2012 International Electron Devices Meeting*, Dec 2012. doi: 10.1109/IEDM.2012.6479154. ISSN 2156-017X pp. 32.6.1–32.6.4.

[85] L. Lattanzio, N. Dagtekin, L. D. Michielis, and A. M. Ionescu, "On the Static and Dynamic Behavior of the Germanium Electron-Hole Bilayer Tunnel FET," *IEEE Transactions on Electron Devices*, vol. 59, no. 11, pp. 2932–2938, Nov 2012. doi: 10.1109/TED.2012.2211600

[86] M. O. Li, D. Esseni, G. Snider, D. Jena, and H. Grace Xing, "Single particle transport in two-dimensional heterojunction interlayer tunneling field effect transistor," *Journal of Applied Physics*, vol. 115, no. 7, p. 074508, 2014. doi: 10.1063/1.4866076

[87] R. Yan, A. Ourmazd, and K. F. Lee, "Scaling the Si MOSFET: from bulk to SOI to bulk," *IEEE Transactions on Electron Devices*, vol. 39, no. 7, pp. 1704–1710, July 1992. doi: 10.1109/16.141237

[88] J.-P. Colinge, "Multiple-gate SOI MOSFETs," *Solid-State Electronics*, vol. 48, no. 6, pp. 897 – 905, 2004. doi: https://doi.org/10.1016/j.sse.2003.12.020 Silicon On Insulator Technology and Devices. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0038110103004441

[89] C.-W. Lee, S.-R.-N. Yun, C.-G. Yu, J.-T. Park, and J.-P. Colinge, "Device design guidelines for nano-scale MuGFETs," *Solid-State Electronics*, vol. 51, no. 3, pp. 505 – 510, 2007. doi: https://doi.org/10.1016/j.sse.2006.11.013. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0038110106003947

[90] F. Villani, E. Gnani, A. Gnudi, S. Reggiani, and G. Baccarani, "A quasi 2D semianalytical model for the potential profile in hetero and homojunction tunnel FETs," in *2014 44th European Solid State Device Research Conference (ESSDERC)*, Sept 2014. doi: 10.1109/ESSDERC.2014.6948810. ISSN 1930-8876 pp. 262–265.

[91] H. Flietner, "The E(k) Relation for a Two-Band Scheme of Semiconductors and the Application to the Metal-Semiconductor Contact," *physica status solidi (b)*, vol. 54, no. 1, pp. 201–208. doi: 10.1002/pssb.2220540119. [Online]. Available: https://onlinelibrary.wiley.com/doi/abs/10.1002/pssb.2220540119

[92] M. A. Khayer and R. K. Lake, "Performance of n-Type InSb and InAs Nanowire Field-Effect Transistors," *IEEE Transactions on Electron Devices*, vol. 55, no. 11, pp. 2939–2945, Nov 2008. doi: 10.1109/TED.2008.2005173

[93] Q. Zhang, Y. Lu, C. A. Richter, D. Jena, and A. Seabaugh, "Optimum Bandgap and Supply Voltage in Tunnel FETs," *IEEE Transactions on Electron Devices*, vol. 61, no. 8, pp. 2719–2724, Aug 2014. doi: 10.1109/TED.2014.2330805

[94] U. E. Avci, B. Chu-Kung, A. Agrawal, G. Dewey, V. Le, R. Rios, D. H. Morris, S. Hasan, R. Kotlyar, J. Kavalieros, and I. A. Young, "Study of TFET non-ideality effects for determination of geometry and defect density requirements for sub-60mV/dec Ge TFET," in *2015 IEEE International Electron Devices Meeting (IEDM)*, Dec 2015. doi: 10.1109/IEDM.2015.7409828 pp. 34.5.1–34.5.4.

[95] M. Fan, V. P. Hu, Y. Chen, P. Su, and C. Chuang, "Analysis of Single-Trap-Induced Random Telegraph Noise and its Interaction With Work Function Variation for Tunnel FET," *IEEE Transactions on Electron Devices*, vol. 60, no. 6, pp. 2038–2044, June 2013. doi: 10.1109/TED.2013.2258157

[96] Q. Zhang, G. Iannaccone, and G. Fiori, "Two-Dimensional Tunnel Transistors Based onBi_2Se_3Thin Film," *IEEE Electron Device Letters*, vol. 35, no. 1, pp. 129–131, Jan 2014. doi: 10.1109/LED.2013.2288036

[97] H. Ilatikhameneh, Y. Tan, B. Novakovic, G. Klimeck, R. Rahman, and J. Appenzeller, "Tunnel Field-Effect Transistors in 2-D Transition Metal Dichalcogenide Materials," *IEEE Journal on Exploratory Solid-State Computational Devices and Circuits*, vol. 1, pp. 12–18, Dec 2015. doi: 10.1109/JXCDC.2015.2423096

[98] D. Sarkar, X. Xie, W. Liu, W. Cao, J. Kang, Y. Gong, S. Kraemer, P. M. Ajayan, and K. Banerjee, "A subthermionic tunnel field-effect transistor with an atomically thin channel," *Nature*, vol. 526, pp. 91–95, 2015. doi: 10.1038/nature15387

[99] J. Valasek, "Piezo-electric and allied phenomena in rochelle salt," *Phys. Rev.*, vol. 17, pp. 475–481, Apr 1921. doi: 10.1103/PhysRev.17.475. [Online]. Available: https://link.aps.org/doi/10.1103/PhysRev.17.475

[100] J. T. Evans and R. Womack, "An experimental 512-bit nonvolatile memory with ferroelectric storage cell," *IEEE Journal of Solid-State Circuits*, vol. 23, no. 5, pp. 1171–1175, Oct 1988. doi: 10.1109/4.5940

[101] D. Takashima, "Overview of FeRAMs: Trends and perspectives," in *2011 11th Annual Non-Volatile Memory Technology Symposium Proceeding*, Nov 2011. doi: 10.1109/NVMTS.2011.6137107 pp. 1–6.

[102] C. H. Ahn, K. M. Rabe, and J.-M. Triscone, “Ferroelectricity at the Nanoscale: Local Polarization in Oxide Thin Films and Heterostructures,” *Science*, vol. 303, no. 5657, pp. 488–491, 2004. doi: 10.1126/science.1092508. [Online]. Available: http://science.sciencemag.org/content/303/5657/488

[103] K. M. Rabe, M. Dawber, C. Lichtensteiger, C. Ahn, and J. Triscone, *Physiscs of Ferroelectrics, a Modern Perspective.* Springer, 2007.

[104] C. B. Sawyer and C. H. Tower, “Rochelle salt as a dielectric,” *Phys. Rev.*, vol. 35, pp. 269–273, Feb 1930. doi: 10.1103/PhysRev.35.269. [Online]. Available: https://link.aps.org/doi/10.1103/PhysRev.35.269

[105] A. I. Khan, K. Chatterjee1, B. Wang, S. Drapcho, L. You, C. Serrao, S. R. Bakaul, R. Ramesh, and S. Salahuddin, “Negative capacitance in a ferroelectric capacitor,” *Nature Materials Letters*, vol. 14, pp. 182–186, 2015. doi: 10.1038/nmat4148

[106] C.-C. Fan, C.-H. Cheng, Y.-R. Chen, C. Liu, and C.-Y. Chang, “Energy-Efficient HfAlOx NCFET: Using Gate Strain and Defect Passivation to Realize Nearly HysteresisFree Sub-25mV/dec Switch with Ultralow Leakage,” in *2017 IEEE International Electron Devices Meeting (IEDM)*, 2017, pp. 561–564.

[107] V. M. Fridkin and S. Ducharme, “Ferroelectricity at the nanoscale,” *Physics-Uspekhi*, vol. 57, no. 6, p. 597, 2014. [Online]. Available: http://stacks.iop.org/1063-7869/57/i=6/a=597

[108] M. H. Lee, P. . Chen, C. Liu, K. Chu, C. . Cheng, M. . Xie, S. . Liu, J. . Lee, S. . Huang, M. . Liao, M. Tang, K. . Li, and M. . Chen, “Prospects for ferroelectric $HfZrO_x$ FETs with experimentally CET=0.98nm, SS_{for}=42mV/dec, SS_{rev}=28mV/dec, switch-off 0.2V, and hysteresis-free strategies,” in *2015 IEEE International Electron Devices Meeting (IEDM)*, Dec 2015. doi: 10.1109/IEDM.2015.7409759. ISSN 2156-017X pp. 22.5.1–22.5.4.

[109] S. Thomas, B. Kuiper, J. Hu, J. Smit, Z. Liao, Z. Zhong, G. Rijnders, A. Vailionis, R. Wu, G. Koster, and J. Xia, “Localized Control of Curie Temperature in Perovskite Oxide Film by Capping-Layer-Induced Octahedral Distortion,” *Phys. Rev. Lett.*, vol. 119, p. 177203, Oct 2017. doi: 10.1103/PhysRevLett.119.177203. [Online]. Available: https://link.aps.org/doi/10.1103/PhysRevLett.119.177203

[110] T. Rollo and D. Esseni, “New Design Perspective for Ferroelectric NC-FETs,” *IEEE Electron Device Letters*, vol. 39, no. 4, pp. 603–606, April 2018. doi: 10.1109/LED.2018.2795026

[111] W. Chung, M. Si, , and P. D. Ye, “Hysteresis-free Negative Capacitance Germanium CMOS FinFETs with Bi-directional Sub-60 mV/dec,” in *2017 IEEE International Electron Devices Meeting (IEDM)*, 2017, pp. 365–368.

[112] P. Ghosez, *Microscopic Properties of Ferroelectric Oxides from First-principles: Selected Topics*, ser. Troisième cycle de la physique en Suisse romande. Troisième cycle de la physique en Suisse romande, 2002, no. pt. 1. [Online]. Available: https://books.google.it/books?id=ANOxXwAACAAJ

[113] L. Eyraud, *Dielectriques Solides Anisoptropes et ferroelectricite*. Gauthier-Villars, Paris, 1967.

[114] Q. Han, T. C. U. Tromm, M. Hoffmann, P. Aleksa, U. Schroeder, J. Schubert, S. Mantl, and Q. Zhao, “Subthreshold Behavior of Floating-Gate MOSFETs With Ferroelectric Capacitors,” *IEEE Transactions on Electron Devices*, pp. 1–5, 2018. doi: 10.1109/TED.2018.2863727

[115] A. Saeidi, F. Jazaeri, F. Bellando, I. Stolichnov, G. V. Luong, Q. Zhao, S. Mantl, C. C. Enz, and A. M. Ionescu, “Negative Capacitance as Performance Booster for Tunnel FETs and MOSFETs: An Experimental Study,” *IEEE Electron Device Letters*, vol. 38, no. 10, pp. 1485–1488, Oct 2017. doi: 10.1109/LED.2017.2734943

[116] T. S. Böscke, J. Müller, D. Bräuhaus, U. Schröder, and U. Böttger, “Ferroelectricity in hafnium oxide: CMOS compatible ferroelectric field effect transistors,” in *2011 International Electron Devices Meeting*, Dec 2011. doi: 10.1109/IEDM.2011.6131606. ISSN 2156-017X pp. 24.5.1–24.5.4.

[117] M. Pešić, V. D. Lecce, M. Hoffmann, H. Mulaosmanovic, B. Max, U. Schroeder, S. Slesazeck, L. Larcher, and T. Mikolajick, “Physical and circuit modeling of HfO2 based ferroelectric memories and devices,” in *2017 IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S)*, Oct 2017. doi: 10.1109/S3S.2017.8308732 pp. 1–4.

[118] M. Pešić, F. P. G. Fengler, L. Larcher, A. Padovani, T. Schenk, E. D. Grimley, X. Sang, J. M. LeBeau, S. Slesazeck, U. Schroeder, and T. Mikolajick, “Physical Mechanisms behind the Field-Cycling Behavior of HfO2-Based Ferroelectric Capacitors,” *Advanced Functional Materials*, vol. 26, no. 25, pp. 4601–4612, 2016. doi: 10.1002/adfm.201600590. [Online]. Available: https://onlinelibrary.wiley.com/doi/abs/10.1002/adfm.201600590

[119] U. Schroeder, C. Richter, M. H. Park, T. Schenk, M. Pešić, M. Hoffmann, F. P. G. Fengler, D. Pohl, B. Rellinghaus, C. Zhou, C.-C. Chung, J. L. Jones, and T. Mikolajick, "Lanthanum-Doped Hafnium Oxide: A Robust Ferroelectric Material," *Inorganic Chemistry*, vol. 57, no. 5, pp. 2752–2765, 2018. doi: 10.1021/acs.inorgchem.7b03149 PMID: 29446630. [Online]. Available: https://doi.org/10.1021/acs.inorgchem.7b03149

[120] J. Müller, U. Schröder, T. S. Böscke, I. Müller, U. Böttger, L. Wilde, J. Sundqvist, M. Lemberger, P. Kücher, T. Mikolajick, and L. Frey, "Ferroelectricity in yttrium-doped hafnium oxide," *Journal of Applied Physics*, vol. 110, no. 11, p. 114113, 2011. doi: 10.1063/1.3667205. [Online]. Available: https://doi.org/10.1063/1.3667205

[121] J. Choi, Y. Mao, and J. Chang, "Development of hafnium based high-k materials—a review," *Materials Science and Engineering: R: Reports*, vol. 72, no. 6, pp. 97 – 136, 2011. doi: https://doi.org/10.1016/j.mser.2010.12.001. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0927796X10001683

[122] T. Rollo, H. Wang, G. Han, and D. Esseni, "A simulation based study of NC-FETs design: off-state versus on-state perspective," in *2018 IEEE International Electron Devices Meeting (IEDM)*, Dec 2018. doi: 10.1109/IEDM.2018.8614514. ISSN 2156-017X pp. 9.5.1–9.5.4.

[123] L. D. Landau and I. Khalatnikov, "On the anomalous absorption of sound near a second order phase transition point," *Dokl. Akad. Nauk*, vol. 96, pp. 469–472, 1954.

[124] L. Landau, "On the theory of phase transistions," *Zhurnal Eksperimentalnoi i Teoreticheskoi Fiziki*, vol. 7, pp. 19–32, 1937.

[125] V. L. Pokrovsky, "Landau and modern physics," *Physics-Uspekhi*, vol. 52, no. 11, p. 1169, 2009. [Online]. Available: http://stacks.iop.org/1063-7869/52/i=11/a=A10

[126] A. Devonshire, "XCVI. Theory of barium titanate," *The London, Edinburgh, and Dublin Philosophical Magazine and Journal of Science*, vol. 40, no. 309, pp. 1040–1063, 1949. doi: 10.1080/14786444908561372. [Online]. Available: https://doi.org/10.1080/14786444908561372

[127] ——, "CIX. Theory of barium titanate - Part II," *The London, Edinburgh, and Dublin Philosophical Magazine and*

Journal of Science, vol. 42, no. 333, pp. 1065–1079, 1951. doi: 10.1080/14786445108561354. [Online]. Available: https://doi.org/10.1080/14786445108561354

[128] T. Rollo and D. Esseni, "Energy Minimization and Kirchhoff's Laws in Negative Capacitance Ferroelectric Capacitors and MOSFETs," *IEEE Electron Device Letters*, vol. 38, no. 6, pp. 814–817, June 2017. doi: 10.1109/LED.2017.2691002

[129] S. Khandelwal, J. P. Duarte, A. I. Khan, S. Salahuddin, and C. Hu, "Impact of Parasitic Capacitance and Ferroelectric Parameters on Negative Capacitance FinFET Characteristics," *IEEE Electron Device Letters*, vol. 38, no. 1, pp. 142–144, Jan 2017. doi: 10.1109/LED.2016.2628349

[130] T. Dutta, G. Pahwa, A. Agarwal, and Y. S. Chauhan, "Impact of Process Variations on Negative Capacitance FinFET Devices and Circuits," *IEEE Electron Device Letters*, vol. 39, no. 1, pp. 147–150, Jan 2018. doi: 10.1109/LED.2017.2770158

[131] N. Ng, R. Ahluwalia, and D. J. Srolovitz, "Depletion-layer-induced size effects in ferroelectric thin films: A Ginzburg-Landau model study," *Phys. Rev. B*, vol. 86, p. 094104, Sep 2012. doi: 10.1103/PhysRevB.86.094104. [Online]. Available: https://link.aps.org/doi/10.1103/PhysRevB.86.094104

[132] C. Woo and Y. Zheng, "Depolarization in modeling nano-scale ferroelectrics using the Landau free energy functional," *Applied Physics A*, vol. 91, no. 1, pp. 59–63, Apr 2008. doi: 10.1007/s00339-007-4355-4. [Online]. Available: https://doi.org/10.1007/s00339-007-4355-4

[133] M. Hoffmann, M. Pešić, S. Slesazeck, U. Schroeder, and T. Mikolajick, "On the stabilization of ferroelectric negative capacitance in nanoscale devices," *Nanoscale*, vol. 10, pp. 10 891–10 899, 2018. doi: 10.1039/C8NR02752H. [Online]. Available: http://dx.doi.org/10.1039/C8NR02752H

[134] A. Levanyuk, B. Anatolievich Strukov, and A. Cano, "Background dielectric permittivity: Material constant or fitting parameter?" *Ferroelectrics*, vol. 503, pp. 94–103, 10 2016. doi: 10.1080/00150193.2016.1218245

[135] T. Rollo and D. Esseni, "Supersteep retrograde doping in ferroelectric MOSFETs for sub-60mV/dec subthreshold swing," in *2016 46th European Solid-State Device Research Conference (ESSDERC)*, Sept 2016. doi: 10.1109/ESSDERC.2016.7599661 pp. 360–363.

[136] V. Fridkin, M. Kuehn, and H. Kliem, “The Weiss model and the Landau–Khalatnikov model for the switching of ferroelectrics,” *Physica B: Condensed Matter*, vol. 407, no. 12, pp. 2211 – 2214, 2012. doi: https://doi.org/10.1016/j.physb.2012.02.043. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0921452612002311

[137] A. Roelofs, T. Schneller, K. Szot, and R. Waser, “Towards the limit of ferroelectric nanosized grains,” *Nanotechnology*, vol. 14, no. 2, p. 250, 2003. [Online]. Available: http://stacks.iop.org/0957-4484/14/i=2/a=328

[138] P. Chandra and P. B. Littlewood, “A Landau primer for ferroelectrics,” in *Physics of ferroelectrics*. Springer, 2007, pp. 69–116.

[139] P. Lenarczyk and M. Luisier, “Physical modeling of ferroelectric field-effect transistors in the negative capacitance regime,” in *2016 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD)*, Sept 2016. doi: 10.1109/SISPAD.2016.7605209 pp. 311–314.

[140] A. I. Khan, “On the Microscopic Origin of Negative Capacitance in Ferroelectric Materials: A Toy Model,” in *2018 IEEE International Electron Devices Meeting (IEDM)*, Dec 2018. doi: 10.1109/IEDM.2018.8614574. ISSN 2156-017X pp. 9.3.1–9.3.4.

[141] F. Preisach, “Über die magnetische Nachwirkung,” *Zeitschrift fur Physik*, vol. 94, pp. 277–302, May 1935. doi: 10.1007/BF01349418

[142] G. Biorci and D. Pescetti, “Analytical theory of the behaviour of ferromagnetic materials,” *Il Nuovo Cimento (1955-1965)*, vol. 7, no. 6, pp. 829–842, Mar 1958.

[143] J. G. Woodward and E. D. Torre, “Particle interaction in magnetic recording tapes,” *Journal of Applied Physics*, vol. 32, no. 1, pp. 126–127, 1961. doi: 10.1063/1.1735945. [Online]. Available: https://doi.org/10.1063/1.1735945

[144] J. A. Barker, D. E. Schreiber, B. G. Huth, and D. H. Everett, “Magnetic hysteresis and minor loops: models and experiments,” vol. 386, no. 1791, pp. 251–261, 1983. doi: 10.1098/rspa.1983.0035

[145] A. Friedman, “Foundations of modern analysis,” pp. vi, 250 p. ;, 1982, reprint. Originally published: New York : Holt, Rinehart, and Winston, [1970].

[146] J. A. Enderby, “The domain model of hysteresis. part 2.—interacting domains,” *Trans. Faraday Soc.*, vol. 52, pp.

106–120, 1956. doi: 10.1039/TF9565200106. [Online]. Available: http://dx.doi.org/10.1039/TF9565200106

[147] D. H. Everett, "A general approach to hysteresis. part 3.—a formal treatment of the independent domain model of hysteresis," *Trans. Faraday Soc.*, vol. 50, pp. 1077–1096, 1954. doi: 10.1039/TF9545001077. [Online]. Available: http://dx.doi.org/10.1039/TF9545001077

[148] I. Mayergoyz, "Chapter 1 - the classical preisach model of hysteresis," in *Mathematical Models of Hysteresis and Their Applications*, ser. Electromagnetism, I. Mayergoyz, Ed. New York: Elsevier Science, 2003, pp. 1 – 63. ISBN 978-0-12-480873-7. [Online]. Available: http://www.sciencedirect.com/science/article/pii/B9780124808737500025

[149] W. H. Press, S. A. Teukolsky, W. T. Vetterling, and B. P. Flannery, *Numerical Recipes 3rd Edition: The Art of Scientific Computing*, 3rd ed. New York, NY, USA: Cambridge University Press, 2007. ISBN 0521880688, 9780521880688

[150] Z. C. Yuan, S. Rizwan, M. Wong, K. Holland, S. Anderson, T. B. Hook, D. Kienle, S. Gadelrab, P. S. Gudem, and M. Vaidyanathan, "Switching-Speed Limitations of Ferroelectric Negative-Capacitance FETs," *IEEE Transactions on Electron Devices*, vol. 63, no. 10, pp. 4046–4052, Oct 2016. doi: 10.1109/TED.2016.2602209

[151] S. Salahuddin and S. Datta, "Can the subthreshold swing in a classical FET be lowered below 60 mV/decade?" in *2008 IEEE International Electron Devices Meeting*, Dec 2008. doi: 10.1109/IEDM.2008.4796789. ISSN 0163-1918 pp. 1–4.

[152] R. P. Feynman, *The Feynman Lectures on Physics*, new millennium ed. edition (october 4, 2011) - vol. ii ed. Basic Books, 1964. ISBN 978-0465024940

[153] A. Saedi and F. Jazaeri, "Double-Gate Negative-Capacitance MOSFET with PZT gate stack on Ultra-Thin Body SOI : an Experimentally Calibrated Simulation Study of Device Performance," *IEEE Transactions on Electron Devices*, vol. 63, no. 12, pp. 1–7, 2016.

[154] H.-P. Chen and V. Lee, "Modeling and design of ferroelectric MOSFETs," *IEEE Transactions on Electron Devices*, vol. 58, no. 8, pp. 2401–2405, 2011.

[155] K. Majumdar, S. Datta, and S. P. Rao, "Revisiting the Theory of Ferroelectric Negative Capacitance," *IEEE Transactions on*

Electron Devices, vol. 63, no. 5, pp. 2043–2049, May 2016. doi: 10.1109/TED.2016.2544813

[156] D. J. R. Appleby, N. K. Ponon, K. S. K. Kwa, B. Zou, P. K. Petrov, T. Wang, N. M. Alford, and A. O'Neill, "Experimental observation of negative capacitance in ferroelectrics at room temperature," *Nano Letters*, vol. 14, no. 7, pp. 3864–3868, 2014. doi: 10.1021/nl5017255 PMID: 24915057. [Online]. Available: http://dx.doi.org/10.1021/nl5017255

[157] M. Hoffmann, B. Max, T. Mittmann, U. Schroeder, S. Slesazeck, and T. Mikolajick, "Demonstration of High-speed Hysteresis-free Negative Capacitance in Ferroelectric $Hf_{0.5}Zr_{0.5}O_2$," in *2018 IEEE International Electron Devices Meeting (IEDM)*, Dec 2018. doi: 10.1109/IEDM.2018.8614677. ISSN 2156-017X pp. 31.6.1–31.6.4.

[158] M. Hoffmann, M. Pešić, S. Slesazeck, U. Schroeder, and T. Mikolajick, "On the stabilization of ferroelectric negative capacitance in nanoscale devices," *Nanoscale*, vol. 10, pp. 10 891–10 899, 2018. doi: 10.1039/C8NR02752H. [Online]. Available: http://dx.doi.org/10.1039/C8NR02752H

[159] Y. J. Kim, H. Yamada, T. Moon, Y. J. Kwon, C. H. An, H. J. Kim, K. D. Kim, Y. H. Lee, S. D. Hyun, M. H. Park, and C. S. Hwang, "Time-dependent negative capacitance effects in al2o3/batio3 bilayers," *Nano Letters*, vol. 16, no. 7, pp. 4375–4381, 2016. doi: 10.1021/acs.nanolett.6b01480 PMID: 27231754.

[160] W. Shockley and W. T. Read, "Statistics of the recombinations of holes and electrons," *Phys. Rev.*, vol. 87, pp. 835–842, Sep 1952. doi: 10.1103/PhysRev.87.835. [Online]. Available: https://link.aps.org/doi/10.1103/PhysRev.87.835

[161] R. N. Hall, "Electron-hole recombination in germanium," *Phys. Rev.*, vol. 87, pp. 387–387, Jul 1952. doi: 10.1103/PhysRev.87.387. [Online]. Available: https://link.aps.org/doi/10.1103/PhysRev.87.387

[162] M. Rudan, *Physics of Semiconductor Devices*, 1st ed. Springer-Verlag New York, USA, 2015. ISBN 978-1-4939-1151-6

[163] J. M. Luttinger and W. Kohn, "Motion of electrons and holes in perturbed periodic fields," *Phys. Rev.*, vol. 97, pp. 869–883, Feb 1955. doi: 10.1103/PhysRev.97.869. [Online]. Available: https://link.aps.org/doi/10.1103/PhysRev.97.869

[164] A. Rahman, J. Guo, S. Datta, and M. S. Lundstrom, "Theory of ballistic nanotransistors," *IEEE Transactions on Electron Devices*, vol. 50, no. 9, pp. 1853–1864, Sept 2003. doi: 10.1109/TED.2003.815366

[165] M. Lundstrom, "Elementary scattering theory of the Si MOSFET," *IEEE Electron Device Letters*, vol. 18, no. 7, pp. 361–363, July 1997. doi: 10.1109/55.596937

[166] K. Natori, "Ballistic metal-oxide-semiconductor field effect transistor," *Journal of Applied Physics*, vol. 76, no. 8, pp. 4879–4890, 1994. doi: 10.1063/1.357263. [Online]. Available: https://doi.org/10.1063/1.357263

[167] M. Lundstrom and Z. Ren, "Essential physics of carrier transport in nanoscale MOSFETs," *IEEE Transactions on Electron Devices*, vol. 49, no. 1, pp. 133–141, Jan 2002. doi: 10.1109/16.974760

[168] C. Jeong, D. A. Antoniadis, and M. S. Lundstrom, "On Backscattering and Mobility in Nanoscale Silicon MOSFETs," *IEEE Transactions on Electron Devices*, vol. 56, no. 11, pp. 2762–2769, Nov 2009. doi: 10.1109/TED.2009.2030844

[169] M. V. Fischetti, S. Jin, T. . Tang, P. Asbeck, Y. Taur, S. E. Laux, and N. Sano, "caling MOSFETs to 10 nm: Coulomb Effects, Source Starvation, and Virtual Source," in *2009 13th International Workshop on Computational Electronics*, May 2009. doi: 10.1109/IWCE.2009.5091145 pp. 1–4.

[170] T. Rollo and D. Esseni, "Influence of Interface Traps on Ferroelectric NC-FETs," *IEEE Electron Device Letters*, vol. 39, no. 7, pp. 1100–1103, July 2018. doi: 10.1109/LED.2018.2842087

[171] G. Brammertz, K. Martens, S. Sioncke, A. Delabie, M. Caymax, M. Meuris, and M. Heyns, "Characteristic trapping lifetime and capacitance-voltage measurements of GaAs metal-oxide-semiconductor structures," *Applied Physics Letters*, vol. 91, no. 13, p. 133510, 2007. doi: 10.1063/1.2790787. [Online]. Available: https://doi.org/10.1063/1.2790787

[172] M. Jerry, P. Chen, J. Zhang, P. Sharma, K. Ni, S. Yu, and S. Datta, "Ferroelectric FET analog synapse for acceleration of deep neural network training," in *2017 IEEE International Electron Devices Meeting (IEDM)*, Dec 2017. doi: 10.1109/IEDM.2017.8268338. ISSN 2156-017X pp. 6.2.1–6.2.4.

[173] J. Zhou, J. Wu, G. Han, R. Kanyang, Y. Peng, J. Li, H. Wang, Y. Liu, J. Zhang, Q. Sun, D. W. Zhang, and Y. Hao, "Frequency dependence of performance in Ge negative capacitance PFETs achieving sub-30 mV/decade swing and 110 mV hysteresis at MHz," in *2017 IEEE International Electron Devices Meeting (IEDM)*, Dec 2017. doi: 10.1109/IEDM.2017.8268397. ISSN 2156-017X pp. 15.5.1–15.5.4.

[174] A. Saeidi, F. Jazaeri, I. Stolichnov, C. C. Enz, and A. M. Ionescu, "Design Considerations of Ferroelectric Properties for Negative Capacitance MOSFETs," in *2018 IEEE 2nd Electron Devices Technology and Manufacturing Conference (EDTM)*, March 2018. doi: 10.1109/EDTM.2018.8421443 pp. 10–12.

[175] M. Si and P. D. Ye, "Steep slope 2D negative capacitance CMOS devices: MoS2 and WSe2," in *2018 International Symposium on VLSI Technology, Systems and Application (VLSI-TSA)*, April 2018. doi: 10.1109/VLSI-TSA.2018.8403843 pp. 1–2.

[176] J. Li, J. Zhou, G. Han, Y. Liu, Y. Peng, J. Zhang, Q. Sun, D. W. Zhang, and Y. Hao, "Negative Capacitance Ge PFETs for Performance Improvement: Impact of Thickness of $HfZrO_x$," *IEEE Transactions on Electron Devices*, vol. 65, no. 3, pp. 1217–1222, March 2018. doi: 10.1109/TED.2018.2791420

[177] E. Ko, J. W. Lee, and C. Shin, "Negative Capacitance FinFET With Sub-20-mV/decade Subthreshold Slope and Minimal Hysteresis of 0.48 V," *IEEE Electron Device Letters*, vol. 38, no. 4, pp. 418–421, April 2017. doi: 10.1109/LED.2017.2672967

[178] A. Hokazono, H. Itokawa, I. Mizushima, S. Kawanaka, S. Inaba, and Y. Toyoshima, "Steep channel profiles in n/pMOS controlled by boron-doped Si:C layers for continual bulk-CMOS scaling," in *2009 IEEE International Electron Devices Meeting (IEDM)*, Dec 2009. doi: 10.1109/IEDM.2009.5424250. ISSN 0163-1918 pp. 1–4.

[179] N. Damrongplasit, N. Xu, H. Takeuchi, R. J. Stephenson, N. W. Cody, A. Yiptong, X. Huang, M. Hytha, R. J. Mears, and T. K. Liu, "Comparative Study of Uniform Versus Supersteep Retrograde MOSFET Channel Doping and Implications for 6-T SRAM Yield," *IEEE Transactions on Electron Devices*, vol. 60, no. 5, pp. 1790–1793, May 2013. doi: 10.1109/TED.2013.2253105

[180] R. J. Mears, N. Xu, N. Damrongplasit, H. Takeuchi, R. J. Stephenson, N. W. Cody, A. Yiptong, X. Huang, M. Hytha, and T. . King-Liu, "Simultaneous carrier transport enhancement and variability reduction in Si MOSFETs by insertion of partial monolayers of

oxygen," in *2012 IEEE Silicon Nanoelectronics Workshop (SNW)*, June 2012. doi: 10.1109/SNW.2012.6243326. ISSN 2161-4644 pp. 1–2.

[181] S. Lombardo, J. H. Stathis, B. P. Linder, K. L. Pey, F. Palumbo, and C. H. Tung, "Dielectric breakdown mechanisms in gate oxides," *Journal of Applied Physics*, vol. 98, no. 12, p. 121301, 2005. doi: 10.1063/1.2147714. [Online]. Available: https://doi.org/10.1063/1.2147714

[182] S.-T. Fan, J.-Y. Yan, D.-C. Lai, and C. Liu, "The hysteresis-free negative capacitance field effect transistors using non-linear poly capacitance," *Solid-State Electronics*, vol. 122, pp. 13 – 17, 2016. doi: https://doi.org/10.1016/j.sse.2016.04.012

[183] E. H. Nicollian and J. R. Brews, *MOS (metal Oxide Semiconductor) Physics and Technology.* Wiley Interscience, 1982.

[184] S. Chang, U. E. Avci, D. E. Nikonov, and I. A. Young, "Inversion Charge Boost and Transient Steep-Slope Induced by Free-Charge-Polarization Mismatch in a Ferroelectric-Metal–Oxide–Semiconductor Capacitor," *IEEE Journal on Exploratory Solid-State Computational Devices and Circuits*, vol. 4, no. 2, pp. 44–49, Dec 2018. doi: 10.1109/JXCDC.2018.2846202

[185] J. Junquera and P. Ghosez, "Critical thickness for ferroelectricity in perovskite ultrathin films," *Nature*, vol. 442, pp. 506–509, Apr 2003. doi: 10.1038/nature01501

[186] N. A. Spaldin, "Fundamental Size Limits in Ferroelectricity," *Science*, vol. 304, no. 5677, pp. 1606–1607, Jun 2004. doi: 10.1126/science.1099822

[187] B. Yin and S. Qu, "Origin of the vanishing critical thickness for ferroelectricity in free-standing PbTiO3 ultrathin films from first principles," *Journal of Applied Physics*, vol. 114, no. 6, p. 063703, 2013. doi: 10.1063/1.4817503. [Online]. Available: https://doi.org/10.1063/1.4817503

[188] T. Shimizu, K. Katayama, T. Kiguchi, A. Akama, T. J. Konno, O. Sakata, and H. Funakubo, "The demonstration of significant ferroelectricity in epitaxial Y-doped HfO_2 film," *Nature, Scientific Reports*, vol. 6, no. 32931, Sep 2016. doi: 10.1038/srep32931

[189] L. N. Trefethen, *Spectral Methods in MATLAB.* Oxford University, 2000. ISBN 0-89871-465-6

[190] P. J. Davis, *Interpolation and Approximation.* Courier Corporation, 1975. ISBN 9780486624952