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Development of a Soft X-ray CMOS Imager Detector for FEL applications

in co-tutela con ELETTRA Sincrotrone Trieste S.C.p.A.

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Abstract

New generation Synchrotron radiation sources and Free Electron Lasers allow revolutionary science with EUV to X-ray photons; this research calls for innovative photon imaging detectors. Most urgent requirements include high frame rates, very large dynamic range, single-photon counting capability with low probability of false positives, and multi megapixels detectors. The PERCIVAL project is a worldwide collaboration between many facilities targeted at the development of CMOS based detectors compatible with these features. Every stage of the development, from the fabrication technology to the control electronics, requires extraordinary efforts and new technological approaches.

This thesis documents experimental results (Low Noise, High Dynamic Range, Low Energy photon sensitivity, QE) using tests prototypes as well as TCAD simulations to better understand the physic of the single pixel. The development of the system hardware and the characteristics of the final system are provided too. Firsts images of the final system taken with visible light are reported and two different models of the charge collection dynamic in such structures in order to avoid a very time consuming simulations conclude this work.

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Introduction

New generation X-ray sources such as Free Electron Lasers and 3rd-generation synchrotrons have significantly increased the demands for X-ray detection systems for the scientific end stations. One of the most impressive requirements concerns the huge dynamics range which is necessary for a class of experiments: often, especially in diffraction based measurements, up to 10^9 photons can reach the detector in few femtoseconds distributed in such a way that several pixels can receive 10^6 or more photons while other pixels in other part of the sensor receive few photons. Since the experimental information resides in the knowledge of both the intensities, not only high dynamic is required but also single-photon counting capability with a high confidence in rejecting false positives. Moreover, since high area and spatial resolution are required, these detection systems have to acquire Megapixels images with frame rate that can be also of hundreds Hz, making also the data transfer a tremendous challenge.

Several detector based on Charge Coupled Device (CCD) are already present and used in such experiments but they present too major action to fully exploit all the advantages that these light sources provide; in particular the frame rate is too low, although we'll see that few improvements have been recently proposed that improve this aspect. For this reason, the scientific community is looking for other approaches and it seems that CMOS based device are promising candidate for these kind of applications.

Despite nowadays the CMOS fabrication process is very well know and several devices have already been developed for different applications related to radiation detection, generally these concern visible light and do not front the problem of x-ray acquisition (in particular soft xrays, which are typical product of free electron lasers) and the huge dynamics typical of FEL. Moreover, any possible progress in this direction is really difficult, since skills in very different research fields are required, starting from the CMOS development (with x-ray sensitive pixels), ending on test with synchrotron and FEL light, passing through UV compatible electronic design just to mention a few.

For these reasons, in 2012 a collaboration between several different players and research centres began with the precise objective of developing a CMOS detector specialised for soft X-ray (250eV up to 1keV): the **PERCIVAL** ("Pixelated Energy Resolving CMOS Imager, Versatile and Large") Imager detector.

Almost from the beginning of the project I was involved in this research, object of my Master thesis and of this PhD, which engages several important research institutes (DESY, ELETTRA, RAL, STFC, DIAMOND, PAL), each one bringing skills and tools essential for the CMOS development.

Although I was involved in almost all the research and development activities, I mainly focused on three critical points of the project and in this manuscript I will detail them: 1) the study of the single CMOS pixel and its responsivity to soft x-rays 2) the realization of a High Vacuum compatible multilayer electronics, i.e. the power board necessary to power up, in the right (and complex!) way, the detector electronics and 3) the "test phase", performed using several light sources in different synchrotron radiation facilities. Among these research activities, particularly relevant are the TCAD simulations of the pixel photodiode I did in order to better understand its behaviour: during these period I developed an innovative model of charge collection dynamic based on RAMO's theorem and MONTECARLO simulations that includes electrons and holes drift and diffusion contributions allowing, a time efficient numerical evaluation of the photo-current waveforms and estimation of collected charge.

Strictly connected to this research, I followed a four months internship (March 2018 – June 2018) at IMASENIC Advance Imaging S.L. (Barcelona, Spain) where, under the supervision of Dr.Turchetta Renato (CEO) and Dr.Bofill Adriá (CTO), I became familiar with the CA-DENCE/SYNOPSYS design tools of CMOS based devices working directly on the layout of one of their X-Rays Imager Detector design. This experience has been very usefull to understand the very first stages of CMOS device development (design, layout, relations with the foundry, etc...) and some example of the work done will be reported in this thesis.

The proceeding of this thesis is organized as follow:

- Chapter 1 provides an overview of the 3^{rd} and 4^{th} generation light sources. Will focus in particular on ELETTRA Synchrotron and the FERMI Free Electron Laser beamlines where some experiments mentioned before have been performed.
- In Chapter 2 I introduce the basics of standard devices as photodiode that are currently used and implemented in X-ray Imager detector CMOS based.
- In Chapter 3 I present the PERCIVAL project (aims, status, features, etc...).
- In **Chapter 4** the PERCIVAL measurement set-up will be described. In particular a closer look to the POWER BOARD will be given: it is essentially, a multy-layer custom PCB that provides all the bias, voltage and current references allowing the right behaviour of the detector in the high vacuum experimental environment.
- Chapter 5 reports the tests and results of PERCIVAL small prototypes and the 2MPixel system using visible light and experimental light sources in order to verify the features of interest (QE, CCE, noise level, dynamic range).
- **Chapter 6** will show the TCAD simulations of the charge collection dynamic in the pixel photodiode and the proposed model based on RAMO's Theorem and MONTECARLO, that implements charges drift and diffusion dynamic in such structures.
- In Chapter 7 will be dedicated to final considerations and conclusions.
- Appendix A is related on the internship period at IMASENIC. Several examples of layout of the X-ray Imager developed blocks will be reported.
- Appendix B describes the Photon Transfer Curve (PTC) technique used for estimate some parameter of the detector.

Chapter 1

Third and Fourth generation light sources

The aim of this chapter is to give a brief overview of third and fourth generation light sources. The main parts that composed them and how they work will be explained. In the end, some experiments will be presented with particular focus on the features that an imager detector, suitable for these kind operation and fully compatible, must have.

1.1 Third generation light sources

A synchrotron is an extremely powerful source of radiation, ranging from infrared to hard X-rays. It is well known from classical electromagnetic theory that accelerating charges emit radiation. In the case of synchrotron radiation, relativistic electrons are accelerated in a circular orbit (indeed a round-cornered polygon called storage ring) and emit electromagnetic radiation over a broad spectral range as they experience centripetal acceleration due to bending magnet or special insertion devices placed along the linear section of the ring. In typical storage rings several bunches of electrons circulate in vacuum, so that light is not a continuous beam, but is a sequence of pulses separated few ns one from each other, resulting in a very high brightness pulsed radiation. The resulting "light", ten billion times brighter than that supplied by conventional sources, enables a broad spectrum of users from academic institutions and industry to gain access to advanced research capabilities and techniques and conduct state-of-the-art experiments in physics, chemistry, biology, life sciences, environmental science, medicine, forensic science, and cultural heritage. The machine operates day and night, with periodic short and long shut downs for maintenance. The single components are described in fig.1.1.

LINear particle ACcelerator

Here, the electrons for the storage ring are produced in an electron gun, a device similar to the cathode ray tubes found in older televisions or computer screens. These electrons are packed in "bunches" and then accelerated to some millions electron-volts, enough for injection into the booster synchrotron.

Booster

This is a pre-accelerator where the electrons are accelerated to an energy of some billions electron-volts (\simeq GeV) before being injected into the storage ring. The booster synchrotron only works a few times a day for a few minutes, when the storage ring is refilled. Every $\simeq 50$ milliseconds, it can send a bunch of some GeV electrons into the storage ring.



Figure 1.1: Scheme of the principal parts of a Synchrotron: 1. LINAC and Booster; 2. Storage ring; 3. Bending magnet; 4. Injection device; 5. Beamline; 6. Optic hutch; 7. Experimental hutch.

Storage Ring

The storage ring (A section is shown in shown in fig.1.2) is a tube where the electrons circle for hours at relativistic speed. It is formed by straight and curved sections in alternating order. In each curved section, two large bending magnets force the path of the electrons into a racetrack-shaped orbit. In each straight section, several focusing magnets ensure that the electrons remain close to their ideal orbital path. The straight sections also host the undulators, where the intense beams of X-rays are produced. The tube is maintained at very low pressure (around 10^{-9} mbar).

As the electrons travel around the ring, they pass through different types of magnets and in the process produce X-rays. Units called RF cavities restore the lost energy.

Undulator (or Insertion Device)

These magnetic structures, composed by a complex array of small magnets as shown in fig.1.3, force the electrons to follow an undulating, or wavy, trajectory. The radiation emitted at each consecutive bend overlaps and interferes with that from other bends. This generates a much more focused, or brilliant, beam of radiation than that generated by a single magnet. Also, the photons emitted are concentrated at certain energies (called the fundamental and harmonics). The gap between the rows of magnets can be changed to fine-tune the wavelength of the X-rays in the beam.

Bending magnets

The main function of the bending magnets, is to bend the electrons into their racetrack orbit. A simple scheme of the device is reported in fig.1.4. However, as the electrons are deflected from their straight path when passing through these magnets, they emit X-rays tangentially to the trajectory of the electron beam. The synchrotron light from a bending magnet covers a wide and continuous spectrum, from microwaves to hard X-rays, and it is much less focused, or brilliant, than the fine beam of X-rays from an insertion device previously described.



Figure 1.2: Storage Ring and its elements.



Figure 1.3: Undulator structure.

Beamlines

The radiation emitted by the electrons passes through "beamlines" placed tangentially to the storage ring and then reaches the experimental halls. Each beamline is designed for use with a specific technique or for a specific type of research. Experiments run throughout the day and night. An example of ELETTRA's beamline is reported in fig.1.5.

At **ELETTRA** for instance, there are 26 beamlines as shown in fig.1.6. All of the most important techniques in the areas of spectroscopy, spectromicroscopy, diffraction, scattering and lithography are present, together with facilities for infrared microscopy and spectroscopy,



Figure 1.4: Bending magnet structure.



Figure 1.5: The TwinMic beamline experimental chamber at ELETTRA.

ultraviolet inelastic scattering, and band mapping. Versatile experimental stations are maintained at the state-of-the art, offering unique means to carry out outstanding research in diverse fields and disciplines.



Figure 1.6: Beamlines at ELLETRA.

1.2 Fourth generation light sources

Despite the high spectral brightness of the third-generation sources, different techniques of scientific investigation require far more performance in terms of monochromaticity, coherence and duration of impulses, in particular at energies of tens of electron volts or higher. At low energies, the conventional sources as lasers are able to satisfy at least partially such requirements, producing spatially and temporally coherent light with impulses of the femtosecond order.

As already verified in the 70s, it is possible to produce laser light by exploiting particular phenomena that occur in passing of relativistic electrons in the undulators.

A basic scheme of the FEL's operation is shown in figure 1.7.



Figure 1.7: Scheme of a Free Electron Laser.

The basic process is the interaction between the beam of free electrons and the light generated by them, if and only if certain resonance conditions are met. The electrons, travel the length of the undulator in a longer time than that of photons. If such difference corresponds to the wavelength of the emitted radiation, the period of each electron bunch is found in phase with the wave that they produced.

In this case, the exchange of energy between electrons and photons may take place and a radiation amplification mechanism starts. If the electrons were emitting as independent as in normal undulator, the phase of each would be random and the light would not be coherent; however, also thanks to the presence of the optical resonance cavity, the interaction between the radiation present in the undulator and the electrons causes the *micro-bunching*, a strong packaging of electrons at the wavelength of the light itself. Thanks to this phenomenon the electrons tend to displace and emit in phase with the radiation in the cavity, producing a resulting monochromatic and coherent photons beam.

For UV and X-ray radiation, there are no optical elements capable of create resonant cavities similar to those working at low energies; therefore, the diagram of fig.1.7 can not be applied

for these wavelengths. A mechanism that makes laser operation possible even in these spectral regions is the self-amplified spontaneous emission (SASE). This technique is based on the micro-bunching produced by the same radiation generated by the electrons in the undulator. Here, there isn't a reference electromagnetic wave so the process requires considerable lengths ($\simeq 100 \,\mathrm{m}$) because, at the first phase, the micro-bunches can be established and generated.

SASE FEL are able to generate strongly monochromatic pulsed light with considerable spatial coherence; the pulse duration can go down to the scale of femtoseconds with repetition frequencies of $\simeq 10 \div 100 Hz$. These FELs however, suffer from the lack of temporal coherence, due to the aleatory nature of the process that originates the emission.

The problem just described can be solved, in the EUV spectrum, with the introduction of a *seed laser* that acts as a reference radiation for the establishment of micro-bunching and amplification processes. This solution was adopted for istance in the seeded FEL Fermi, also to exploit the reconversion of a linear accelerator (LINAC) that did not have the mileage lengths typically occupied by SASE FEL. At Fermi, the seed laser is generated through a conventional high-harmonic generation (HHG) source. There are no conventional laser sources in the X spectrum and, therefore, it is not possible to apply this scheme; recently, a *self seeded* approach has been tested, in which the laser seed is an X Ray regime emission of the FEL itself.

The impulses generated by the FEL Fermi have a duration of about 100 fs with a repetition frequency of $10 \text{ Hz} \div 50 \text{ Hz}$; the energy per pulse reaches about $100 \,\mu\text{J}$ and the wavelength is tunable between 20 and 100 nm (FERMI-1) corresponding to 62 and 12.4 eV and from 4 to 20 (FERMI-2), corresponding to 62 and 310 eV, respectively.

1.3 Applications

The unprecedented combination of high peak power, femtosecond pulses and penetrating X-ray radiation delivered by X-ray Free Electron Lasers offers researchers an entirely new window into previously unexplored regimes of the time evolution of matter. Capable of producing X-ray pulses ranging in length from less than 10 fs duration to more than 300 fs duration, and with up to 10^{13} monochromatic and spatially coherent X-ray photons per pulse, this new class of high peak power X-ray source is ideally suited for a new generation of time resolved studies.

At the same time new techniques in coherent X-ray imaging have opened up new frontiers in the imaging of condensed matter and biological samples on nanometre to atomic length scales.

The combination of these two developments provide a powerful and unique new set of tools for the study of time evolution of matter on nanometre to atomic length scales, with temporal resolution approaching the time scales of atomic motion. Understanding the dynamic response of materials under extreme conditions of pressure and temperature is a scientific quest that spans nearly a century. Critical to developing this understanding is the ability to probe the spatial and temporal evolution of the material structure and properties at the scale of the relevant physical phenomena.

The effects of high powered X-ray and visible lasers on materials involve such processes as rapid ionisation, coulomb explosion, hydrodynamic expansion, spallation, ablation and nonthermal melting - phenomena that evolve on femtosecond to picosecond timescales and have intrinsic length scales ranging from nanometres to atomic length scales. Meanwhile current molecular dynamics simulations are able to predict the behaviour of materials up to a few microns in size based on the calculated motion and interaction of individual atoms.

Experimental studies of material behaviour on length scales ranging from individual atomic motion to nanometre length scales are essential to bridging the gaps between model-based predictions and experimental reality. In the field of biological imaging, theoretical calculations and numerical simulations predict that ultrashort and extremely bright coherent X-ray pulses will enable the diffraction patterns of large molecules, cells or other nanometre- to micron-sized objects to be measured before the sample explodes and turns into a plasma.

Such predictions depend critically on the rate of sample damage, and careful experiments are required to validate these predictions. The relevant length scales for such investigations once again require simultaneous nanometre to atomic spatial resolution, and femtoseconds to picosecond temporal resolution[1],[2],[3],[4].

In the next sections, some example of typical experiments using FEL light source will be described.

Coherent Diffraction Imaging

X-ray free-electron lasers (X-ray FELs) are expected to permit diffraction imaging at highresolutions of nanometer- to micrometer-sized objects without the need for crystalline periodicity in the sample. High resolution structural studies within this size domain are particularly important in materials science, biology, and medicine. Radiation-induced damage and sample movement prevents the accumulation of high-resolution scattering signals for such samples in conventional experiments. Damage is caused by energy deposited into the sample by the probes used for imaging, e.g. photons, electrons, or neutrons.

At X-ray frequencies, inner shell processes dominate the ionisation of the sample; photoemission is followed by Auger or fluorescence emission and shake excitations. The energies of the ejected photoelectrons, Auger electrons, and shake electrons differ from each other, and these electrons are released at different times, but within about ten femtoseconds, following photoabsorption. Thermalisation of the ejected electrons through collisional electron cascades is completed within 10-100 femtoseconds. Heat transport, diffusion and radical reactions take place over some picoseconds to milliseconds[5].



Figure 1.8: Schematic diagram of the experimental apparatus for lensless coherent diffraction imaging. The image has been taken from [5].



Figure 1.9: Flash X-ray coherent diffraction patterns. Coherent diffraction pattern recorded for a single pulse (top-left), and for the subsequent pulse of similar intensity and duration (top-right), 20s later, showing diffraction from the damage caused by the pulse that formed the diffraction pattern (top-left). The SEM (Scanning Electron Miscroscope) image of the sample (Bottom-left) and its reconstruction (Bottom-right). The image has been taken from [5].

X-ray holography

X-ray Fourier-transform holography (**FTH**) is a robust coherent imaging technique that has found wide spread applications ranging from biology to material science. The technique is particularly suited to imaging magnetic domains and other magnetic samples because holograms generated with circularly polarized X-rays can be used to separate charge scattering from magnetic scattering. X-ray holography has developed into a powerful single measurement technique and has promising applications using X-ray lasers to study structures of radiationsensitive samples and the structural changes of transient phenomena[6].



Figure 1.10: The SEM image of samples (top-left) with the known reference (top right) required for the X-ray Fourier-transform holography technique. The obtained diffraction pattern (bottom-right) and the real image reconstruction (bottom-left). The image has been taken from [6].

Time resolved dynamics of matter through pump-probe experiments

The rapid development of table-top high harmonic generation and free-electron laser (FEL) technologies generating coherent, intense and ultrashort extreme ultraviolet (XUV)/soft X-ray pulses is opening new frontiers of ultrafast science, pushing nonlinear optics into the X-ray domain and providing a basis for a variety of novel time-resolved schemes. Pump-probe techniques, first applied using optical lasers for studying non-equilibrium transient states of matter, have now been extended to high harmonic generation and FEL generated pulses using either X-ray or synchronized optical and X-ray pulses pairs. The great advantage of XUV/X-ray photons is that they can stimulate and probe electronic transitions from core levels, providing chemical selectivity as well. Ultrabright FELs overcome the pulse intensity and wavelength tunability limitations of high harmonic generation sources, allowing experiments not possible a few years ago. Among the numerous exciting opportunities are studies of exotic properties of matter driven into non-equilibrium transient states by ultrabright X-ray pulses; these studies are

K-B focusing а optics Online spectrometer Undulator FEL amplifier Δt b FEL pulses CCD detector Twin seed laser pulses d Ti dispersive 37.1 37.2 37.3 37.4 37.5 grating λ (nm) С 37.0 37.1 37.2 λ (nm) 37.3 37.4 37.5 37.6 500 1,000 -500 0 1,500 2,000 2,500 Delay (fs)

relevant to inertial fusion, planetary interior physics and, more generally, to radiation–matter interactions[7].

Figure 1.11: Generation and characterization of the twin-seeded FEL pulses and experimental set-up. (a) Energetically distinct two ultraviolet laser pulses with an adjustable delay interact with a single electron bunch. (b) Typical spectrum of the twin-FEL pulses. (c) Sequence of FEL spectra obtained during a temporal scan of the seed laser pulse pair with respect to the electron bunch. The zero time is defined as the instant when the first laser pulse interacts with the electron bunch. (d) Experimental layout: the twin FEL pulses with different wavelength, focused by KB (Kirkpatrick-Baez) optics (shown in (a)), impinge on the Ti grating and are diffracted along the horizontal plane. The seventh order diffraction pattern is detected by an Imager detector placed off-axis with respect to the direct beam. The image has been taken from [7].

1.4 Considerations

We presented just few kind of experiments that can be performed in different facilities using FEL light source. Trying to analize how them are performed and which is their particular target, we can notice that all of them required detectors with very performing features in order to achieve all the advantages from this light source.

For instance all the experiments that need to recover an image of a sample from the diffraction pattern or after a pulse and probe pulse sequence need:

- Large area with high pixel density in order to cover all the diffraction pattern (even high harmonic components are detected).
- High Dynamic range with single photon sensitivity because despite the peripheral part of the sensing area collect just few photons, the central part is hit by a huge number of photons almost simultaneously so a system working in integration mode with high dynamic range (pixel saturation condition means data loss) is strongly required.
- Low noise in order to detect photons at very low energies.
- High Frame Rate in order to use all the FEL pulses according with the operational repetition rate of the machine (for example FERMI can operate at 10 Hz but for other FELs (e.g. SLAC, USA) the repetition rate is higher (≈120 Hz)).

The features above mentioned, suggest that in order to correctly collect all the useful experimental data from experiments with FEL light source beamlines require fully compatible imager detector.

The optimal detector must have the following features:

- Large Area with high pixel density
- Wide Energy range
- Low Noise
- Single photon sensitivity
- Uniform QE (Quantum Efficiency along the entire pixels area)
- High Frame rate (>100 Hz)

To meet these requirements, different detection strategies have been suggested and some of them have been implemented recently[8]. Back-thinned, monolithic active pixel sensors (MAPS) based on standard CMOS technology [9],[10] are promising candidates for these applications. In the next chapters the CMOS technology will be presented and in particular the PERCIVAL Imager detector, that aims to achieve all these features listed above[11], will be presented and discussed.

1.5 State-of-art for detectors

In the late 1990s, developments began on dedicated X-ray imaging detectors for synchrotron radiation based on the direct conversion of X-rays within semiconductors. These resulted in experimental methodologies with higher accuracy and higher efficiency, and paved the way for new types of experiment. Today, this type of detector has become a necessity in many fields of synchrotron radiation and laboratory X-ray sources. A strong push for dedicated detector development came with the birth of hard X-ray free-electron laser (XFEL) sources[12].

The current trends in X-ray imaging are based on two detector technologies: **hybrid** and **monolithic** detectors. Both technologies enable the imaging of X-ray patterns with unique capabilities, such as single-photon detection, high dynamic ranges and sharp images.

Moreover, X-ray imaging detectors come in two types with different working principles:

- photon-counting: The signal generated by each absorbed photon is immediately processed and compared with user-defined thresholds in order to decide whether the observed signal corresponds to that expected from a photon with a certain energy. The number of photons passing the threshold criterion during the integration time is stored in a counter inside each pixel of the detector. A great advantage of photon-counting systems is that the processing electronics distinguishes the signal generated by a photon of the desired energy against signals from photons of too high (higher harmonics) or too low (fluorescence) energy, as well as against the electronic background noise. This allows practically zero-noise performance. One example is the well known Pilatus detector[13] developed by the Swiss Light Source (SLS) at the Paul Scherrer Institute (PSI, Villigen, Switzerland) and commercialized by the company DECTRIS. A disadvantage of photon-counting systems is that they cannot handle large instantaneous fluxes.
- **photon-integrating:** The system integrate the total signal, including noise, during a user-selected time interval. The advantage is that these systems can record very large instantaneous fluxes. This is mandatory for XFEL sources, but can also be advantageous for certain storage-ring based experiments. The disadvantage is that, for longer integration times, the noise generated by the dark current can be significant. There is also no discrimination between photons of different energies.

1.5.1 Hybrid detectors

In a hybrid system, the absorption and signal-processing processes are performed by two separate pieces of material which are connected together by high-density interconnects, most often bump-bonding. A description of a generic hybrid detector structure is shown in fig.1.12.

The advantage of this technology is that the absorption and signal processing can be optimized independently, providing greater flexibility. The disadvantage is the need for a fine-pitch or high-density interconnection between the two layers, which is a delicate, time-consuming and often expensive step. This also limits the smallest pixel size obtainable.

Various photon-counting hybrid systems have been introduced at synchrotron sources in recent years, including the Maxipix[14], the XPAD[15] and the well known Pilatus detector. It is difficult to overstate the success and impact of the Pilatus family of detectors on science at storage-ring sources. Nevertheless, the relatively large pixel size of 172μ m and the limited frame rate are now becoming bottlenecks in various experiments.

As a follow-up to the Pilatus detector, the detector group at PSI have developed the EIGER system with a 75μ m pixel size, a reduction in pixel area of a factor of 5.26 [16]. Each pixel contains a 12-bit counter and a 12-bit memory, which makes it possible to have a near dead-timefree readout; by storing the previous image in memory while it is being read out, the



Figure 1.12: A Hybrid detectors general structure is reported. On the left, the top view is shown and the different sections (sensor chip and readout chip) are highlighted. On the right, the cross-section view is reported and in particular, the connection between the sensor chip and readout chip by bump-bonding is shown.

counter can start acquiring the next image almost immediately. Depending on the counter depth used, various frame rates are available, ranging from 8 kHz for a 12-bit counter depth to 23 kHz for 4 bits. The first systems have recently been installed on beamlines at various facilities around the world.

The EIGER system will also be commercialized by DECTRIS and made available to the international community. Similar progress towards smaller pixels and higher frame rates has been achieved by Medipix3-based systems[17]. These have a 55μ m pixel size, which is a reduction in pixel area of a factor of nearly ten compared with the Pilatus detector, and close to a factor of two compared with EIGER systems. The Medipix3 also features two 12-bit counters per pixel, which can be used in a variety of ways: either switching between the counters to give a dead-time free readout, combining the two into a single 24-bit counter, or acquiring two images at different threshold settings simultaneously. With a 12-bit counter, frame rate of 2 kHz is achieved, and 24 kHz is possible for single-bit counter.

One of the most innovative features of the Medipix3 readout chip is its communication between pixels. The principle idea is that, whenever a pixel detects a signal above a pre-set threshold, it "communicates" with the surrounding pixels, and the charge that is spread over multiple pixels is summed together. This charge-summing mode overcomes the charge sharing induced degradation of the energy resolution that is typical for small-pixel hybrid detectors.

Additionally, it is possible to use sensors of 110μ m pixel size and assign the incoming X-ray photons to eight different energy bins, providing coarse energy-resolving capabilities. This is particularly interesting for medical imaging applications, but might also find interesting uses at synchrotron sources. Various larger systems based on Medipix3 readout chips have been and are under construction, notably the Excalibur system at Diamond Light Source (Didcot, UK)[18] and the LAMBDA system at DESY (Hamburg, Germany)[19].

The low-noise performance of photon-counting hybrid systems has proven to be a major advantage over for these devices. However, a disadvantage of these systems is that photons are counted or treated one at a time, limiting the maximum flux that can be handled at storage-ring sources and completely excluding these systems from XFEL applications, where many photons per pixel arrive within a single pulse of less than 100 fs. Several dedicated developments have been initiated to address the formidable challenges imposed by XFELs.

A few hybrid detector development projects will be briefly described here:

- CSPAD and the ePix platform at LCLS: XFEL-specific hybrid system to become operational was the CSPAD (Cornell–Stanford pixel array detector) developed for the Linear Coherent Light Source (LCLS) at the SLAC National Accelerator Laboratory (Stanford, California, USA)[20]. The LCLS delivers ultra-intense ultrashort X-ray pulses with a repetition rate of 120 Hz. Each single pulse is intense enough to produce a complete scattering pattern in the image, ranging from a single or no photons to 10^4 or more photons per pixel. This requires both low-noise performance (in order to distinguish single photons) and a very high peak signal. The CSPAD has a pixel size of $110\mu m$ and, when operated in high-gain (low-noise) mode, an equivalent noise of 1.1 keV. (Note that the magnitude of noise cited in this review is defined as standard deviation.) This mode provides a signal-to-noise ratio of 7 for 8 keV photons, which is sufficient to discriminate between individual photons. In this mode, a maximum of 350 photons can be detected per pixel. The system can also be operated in low-gain (high peak signal) mode, in which case up to 2500 photons of 8 keV can be detected per pixel with a noise floor of 3.5 keV. Since low noise and high-peak signal modes cannot be used simultaneously, the user has to preselect the mode to be used. Various multi-mega pixel systems have been produced and CSPAD detectors are used in most of the experiments performed at the X-ray pump and probe (XPP), coherent X-ray imaging (CXI), X-ray correlation spectroscopy (XCS) and matter in extreme conditions (MEC) stations, producing ground-breaking scientific results. With the experienced gained over the last few years, the science studied at XFELs has evolved rapidly and new experiments are being performed or planned. With that, the demands on the detector have changed, and the current CSPAD does not fulfil all the new requirements. In order to achieve all the features for these new experiments, the detector group at LCLS has started the design of a new generation of readout chips, called the ePix platform[21]. The first member of this new family is the ePix100, with a pixel size of $50\mu m$, equivalent noise of 225 eV and a maximum detection limit of 100 photons per pixel at 8 keV. This system was specifically designed with X-ray photon correlation spectroscopy (XPCS) in mind. The second member under development is the ePix10k system, with $100\mu m$ pixels, a peak signal of up to 10^4 photons at 8 keV and an equivalent noise of 650 eV. A large peak signal with single-photon sensitivity is achieved by dynamic gain switching, which is described in more detail below. In parallel, the Cornell group has developed and is developing new detectors for high-speed imaging at both storage rings and XFEL sources, notably the MMPAD and Keck-PAD systems^[22].
- LPD, DSSC and AGIPD detectors for the European XFEL: The European XFEL currently under construction in Hamburg, Germany, presents an additional challenge for detectors. The European XFEL uses superconducting accelerators, permitting a very high bunch-repetition rate of up to 4.5 MHz during short burst periods of 0.6 ms, creating pulse trains with 2700 X-ray pulses. These bursts are then followed by 99.4 ms without bunches, resulting in a 10 Hz overall repetition rate. Since each pulse produces a complete diffraction pattern, and since 222 ns is too short to read out the million-pixel imaging detectors, the images have to be stored inside the pixels during the pulse trains and read out between pulse trains. In order to meet these challenges, three separate development projects have been funded, each using a different approach. The large-pixel detector (LPD) project uses three parallel gains to cover the high peak signal, and three associated analogue storage memories for storing up to 512 images during the pulse trains[23]. In order to incorporate these three independent detection chains, the pixel size has to be

relatively large at 500μ m. The analogue data are converted to digital by on-chip ADCs (analogue-to-digital converters) and streamed off to the data backend for further processing between pulse trains. The LPD system is optimized for the highest flux experiments like liquid scattering, where spatial resolution is not critical. The DEPFET sensor with signal compression (DSSC) project uses a non-linear DEPFET (depleted p-channel field effect transistor) as the sensor, in order to cover the full range of intensity, and an inpixel ADC plus a digital memory for storing the images.

Since digital memories are much more efficient, up to 800 images can be stored in the hexagonal pixels of approximately 200 μ m. The DSSC system has the lowest noise and is optimized for the lowest-energy experiments at the SASE-3 beamline. The third project is the adaptive gain integrating pixel detector system (AGIPD)[24], which uses a dynamically adapted gain, where each pixel automatically adapts its gain to the incoming number of photons, plus an analogue storage memory. The data are digitized off-chip between pulse trains. The 200 μ m pixel size allows up to 352 images to be stored. The AGIPD system, with an equivalent noise of 1 keV, is optimized for general diffraction and imaging experiments between 5 and 25 keV, where single-photon sensitivity and a large peak signal of more than 10⁴ are required. These performance characteristics are useful not only for FEL experiments but also for storage-ring stations, as shown in the example below. An AGIPD single-chip system with 64×64 pixels was tested on the DESY PETRA III P10 beamline in a small-angle scattering experiment using 500 nm spherical particles and an 8 keV photonbeam.

• Jungfrau and Mönch detectors at PSI: The detector group at PSI, which is one of the partners in the AGIPD project, used the same adaptive gain switching concept in their Jungfrau detector for the SwissFEL[25]. Since the SwissFEL will operate at 100 Hz, there is no need for in-pixel frame storage. A 75 μ m pixel size was chosen, which seems well matched with most of the planned experiments. The lower frame rate compared with the AGIPD system allows for a reduction in the equivalent noise down to 430 eV. Although only a 100 Hz frame is required for the SwissFEL, the Jungfrau system is designed for operation up to 2 kHz, making it also applicable for storage-ring based experiments. The same group at PSI is working on the Mönch system, which is a charge-integrating system with very low noise, 126 eV equivalent, and 25 μ m pixels[26]. These detectors show the potential of hybrid systems in the low energy and small-pixel regimes normally reserved for monolithic systems. One of the most remarkable features will be the imaging of subpixel structures through photon-by-photon analysis of the photo-absorption positions.

1.5.2 Monolithic detectors

There are two pixel types for monolithic detectors, **passive** and **active**. Passive pixels have only a switching function that controls signal charge to flow out of the pixel area of the sensor. The most successful sensor with passive pixels is the CCD. On the other hand, active pixels have transistors for active functions such as amplification and processing. When active pixels are implemented in monolithic sensors, the sensor is sometimes called a monolithic active pixel sensor (MAPS). Several solution have been implemented and others are under study and development. Some examples are reported below:

- Passive-pixel detectors
 - Direct-detection CCD: Direct-detection CCDs offer several unique capabilities, such as low noise and a small pixel size of less than 20μ m[27]. The CCD sensor has a charge-transfer structure on the entire image area. Each pixel has only two, three



or four gates for the charge-transfer function. This simple pixel structure enables a small pixel size. Fig.1.13 reports the general structure of a CCD pixel.

Figure 1.13: General structure of a pixel CCD based device. The structure is based on a MOS capacitor that collects the photo-generated charge. This charge is then transfered by several transfer-gate (Transfer Gate and CCD gates) and converted in a voltage signal at the on-chip amplifier.

The signal charge is transferred across the chip and converted to a voltage signal at the on-chip amplifier, such as a floating-diffusion amplifier. The CCD manufacturing process generally offers low-noise transistors for transmission of the voltage signal with minimum degradation of the noise. The total electronic noise is typically just a few electrons. Such low-noise performance enables not only X-ray intensity imaging, but also X-ray spectroscopic imaging. However, conventional scientific CCDs have several limitations in applications for advanced X-ray imaging. One of the shortcomings is the narrow thickness of the photodiode. Today, several CCD projects, have achieved CCDs with a photodiode thickness greater than 300μ m, which corresponds to a quantum efficiency of 90% at 10 keV. Another weakness is the slow frame rate[27]. In fact, these CCDs can run, at most, at 10 frames per second. The rate is slow because all the pixels are read in a serial fashion by a single or a few on-chip amplifiers.

– pnCCD: The pnCCD developed by the Semiconductor Laboratory of the Max Planck Institute (Munich), with a pixel size of 75μ m[28]. The output voltage waveform is transferred through wire bonding to CAMEX (complementary metal oxide semiconductor analogue multiplexing) signal processors and then to external 14-bit ADCs. The conversion of signal charge to voltage at the on-chip amplifiers proceeds in parallel to increase the frame rate. The system was operated at LCLS, with a maximum frame rate of 120 Hz synchronized to the LCLS pulses. During the first years of operation, the detectors installed in the CAMP chamber yielded important scientific results, such as serial femtosecond crystallography and coherent diffraction imaging [3],[29]. The detector system consists of two imaging planes, one for wider scattering and the other for smaller-angle scattering. Each of the imaging planes consists of two image sensors of 0.5 Mpixels. The low-noise performance of 2.5 electrons when operating at 233K makes single-photon sensitivity possible through post-analysis of the images, even for very soft X-rays. For low-flux images, the photon energy was also resolved to distinguish the different X-ray fluorescence lines. A thick photodiode zone of 500μ m yielded good quantum efficiency, even for harder X-rays.

- MPCCD: A different development direction of CCD technology can be found in multi-port CCDs (MPCCDs) for SACLA experiments[30]. With an emphasis on the peak signal, these workers have optimized MOS CCD technology towards a larger peak signal while keeping the frame rate of 60 Hz, the facility pulse frequency. The resulting pixel has a size of 50μ m, which is larger than typical MOS CCDs. Optimization to 6 keV X-rays resulted in a relaxed noise requirement of the sensor and enabled a higher amplifier readout rate of 5 MHz. A signal-to-noise ratio larger than 7 for 8 keV X-rays (100–250 electrons) was reported at 30 frames per second, matching the pulse frequency of user operations.
- Monolithic active-pixel sensor (MAPS)
 - Femtopix and SOPHIAS based on silicon-on-insulator (SOI) pixel technology: For hard X-ray imaging, a photodiode over 300μ m thick is required to maintain high quantum efficiency. More than a decade of research based on commercially available foundry processes has still not yielded a feasible means of fabricating MAPS with thick photodiodes. KEK, RIKEN and other institutes, mainly in Japan, are developing silicon-on-insulator (SOI) pixel technology as one of the methods enabling a combination of a thick photodiode and advanced CMOS transistors within a single monolithic chip[31]. This is realised by using custom SOI wafers, where the silicon layer for the CMOS, on top of a thin silicon oxide layer, is bonded to the wafer for the photodiode. Additional fabrication steps are carried out to produce the metal pathways (vias) from the photodiode to the CMOS transistors through the thin silicon oxide layer, so that charge generated in the photodiode is transferred to the CMOS layer. The soft X-ray imager FemtoPix was developed by LBNL for femtoslicing experiments at ALS. In-pixel CMOS circuitry within a 17.5 μ m pixel provides a fast gating function. The 192×192 pixel sensor operates at 4000 frames per second.

The SOPHIAS detector for the XFEL facility SACLA uses this feature to control the charge-collection step[32]. Most of the signal charge is transmitted to low-noise charge-collection electrodes. They form a low enough capacitance that a single X-ray photon of 6 keV is converted to a voltage of few mVs. Such a high voltage swing can easily be read out, giving a low noise floor of 0.13 photons at 6 keV, but it will be saturated at 220 photons. The other electrodes collect only a portion of the charge and can measure up to 10^3 photons. The charge-division scheme, together with the in-pixel circuitry optimization, enables a high peak signal within a small pixel size of 30μ m. The first system under development at SACLA will be used for coherent X-ray imaging of micron-scale objects. It consists of two sensors, comprising a total of 3.8 Mpixels at a frame rate of 60Hz.

 PERCIVAL imager for soft X-rays: The PERCIVAL project will be presented in the next chapters.

Page 20 CHAPTER 1. THIRD AND FOURTH GENERATION LIGHT SOURCES

Chapter 2 The Photodiode

In all camera devices based on charge-coupled device (CCD) and CMOS image sensors (CIS) the light sensitive element needs to be integrated in the fabrication process of the sensor.

This chapter introduce the physics basics of the photodiode structure. The P-N and P-I-N junctions will be explain and discussed and their application as photodiode will be presented. At the end integration of the photodiode in the CMOS process will be discussed.

The increasing demand for image acquisition systems pushed for easy-to-manufacture and low-price solutions that eventually converged into the adoption of the well established CMOS fabrication process in order to develop CMOS image sensors on silicon. Light sensing in CMOS technology relies on the generation of *Electron-Hole* (e-h) pairs induced by the incoming photons.

The creation of e-h pairs can occur only if the electron in the valence band acquires enough energy and momentum to jump to the conduction band.

• Energy: The amount of energy that is required depends on the energy bandgap (E_G) of the material. In particular, the energy of the photon must be higher than the bandgap of the material. The generation of e-h pairs at any lower energy than the bandgap must then be assisted by other mechanisms (i.e. energy traps) within the bandgap itself and as a result the generation rate becomes negligible. The energy of a photon is related to its wavelength:

$$E = \frac{hv}{\lambda} = \frac{hc}{n\lambda} \tag{2.1}$$

where v is the velocity of the wave in the medium, n its refractive index and λ is the wavelength. Longer wavelengths convey smaller energies. The formula can be effectively simplified as:

$$E = \frac{1240}{n\lambda[nm]} [eV] \tag{2.2}$$

If the photon energy is much larger than the gap, more e-h pairs can be generated as in the case of X-rays.

• Momentum: Depending on the amount of momentum required to create an e-h pair, we distinguish between direct and indirect bandgap materials. The formers don't require any momentum at all, while the latter ones do. Although photons can provide enough energy to overcome the energy gap, they don't have enough momentum to activate the transitions in indirect bandgap materials. In this case the e-h pair generation must be assisted by the interaction with another particle/wave called phonon that results from

the crystal lattice vibration of the material. As a result, in an indirect bandgap material the probability to absorb a photon and to produce an e-h pair is much lower than in a direct bandgap one. Silicon is an indirect bandgap material.

To account for the general response to light illumination in a medium, the *Absorption* Coefficient (μ) is introduced. The higher the absorption coefficient the higher the probability of producing an e-h pair.

For energies lower than E_G (long wavelengths) the photon travels unscattered through the medium and it starts to be absorbed only for energies higher than E_G . This is to say that long wavelengths have a higher probability to travel through the medium for a long distance, before being absorbed. For energies right above E_G , direct bandgap materials have a sharp absorption transition, while indirect bandgap ones (i.e. silicon) tend to absorb light more gradually as their energy increase.

Since silicon results sensitive to the full visible spectrum and also to deep infrared and UV tails, its affordability and its integration with CMOS fabrication processes easily pays back its being an indirect material bandgap. It should be noted that the absorption coefficient is directly related to the average depth at which the photon is effectively absorbed.

The inverse ratio of the absorption coefficient is the Attenuation Length (λ) .

$$\lambda = \frac{1}{\mu} \tag{2.3}$$

It represents the distance travelled on the medium at which the light intensity experiences a drop of 36% from the incoming original flux. Figure 2.1 shows the Attenuation Length for silicon in the Soft X-ray regime. Because there is a physical limit to the silicon depth, the material sensitivity to longer wavelengths is inevitably cut off.

Figure 2.1: Attenuation Length for Silicon. Data are from [33].

2.1 X-rays interaction with matter

Photons in the X-ray band can be detected and imaged using silicon based devices. In order to better understand the main interaction processes between X-ray and the Silicon lattice, the *Mass Attenuation Coefficient* (σ) is introduced. It is defined as:

$$\sigma = \frac{\mu}{\rho_{Si}} \tag{2.4}$$

where μ is the absorption coefficient (defined above) and ρ_{Si} is the silicon mass density.

The mass attenuation coefficient, characterizes how easily the material can be penetrated by a beam of light, sound, particles, or other energy or matter. The values of these coefficients depend upon the absorption and scattering of the incident radiation caused by several different mechanisms such as:

- Rayleigh scattering (coherent scattering)
- Compton scattering (incoherent scattering)
- Photoelectric absorption
- Pair production: electron-positron production in the fields of the nucleus and atomic electrons.

Figure 2.2 depicts the interaction coefficient σ as a function of photon energy E and it highlights the dominant pair generation processes. Since the typical detection thickness are measured in some tens of μm , silicon can efficiently stop X-rays in the energy range $\simeq 100$ eV to $\simeq 10$ keV, where the photoelectric effect dominates (left part of fig.2.2).

Figure 2.2: Energy dependence of the Mass Attenuation Coefficient with different mechanisms of absorption and scattering of the incident radiation.

At these energies, the photon interacts with core electrons in the silicon lattice and ejects an energetic photoelectron. The excited electron then returns to its ground state through a series of Auger and fluorescence processes, whilst the energetic photo-electron releases energy by ionisation[34].

The whole process results in the creation of an electron-hole cloud around the initial Xray absorption site (a study of the cloud distribution, through GEANT4 simulations, will be reported in chapter 6), with the mean number of free electrons generated equal to $N_e = E/\omega$, where E is the photon energy and ω is the mean energy required to liberate one electron-hole pair. In silicon at room temperature $\omega = 3.65$ eV.
2.2 Basic physics of the PN Junction

Once the e-h pairs have been generated, they must be separated to avoid their recombination. This separation can be performed by means of a strong unidirectional electric field and the silicon PN junction is a suitable electron device for this task. Indeed, the depletion region of a PN junction is enabled by the steep bend in the energy bands due to the alignment of Fermi levels at thermal equilibrium, which gives rise to a strong electric field. This effect is even more remarkable if the junction is driven in reverse bias where on one hand, the depletion region width increases, while on the other one the electric field is stronger.

2.2.1 PN Junction at equilibrium

To build a PN Junction, we begin by considering initially separated *n*-type and *p*-type semiconductor silicon crystals. When these are bought into intimate contact, the large difference in electrons concentrations between the two materials causes an electrons flow from the *n*-type semiconductor into the *p*-type one and an holes flow in the opposite direction. As these mobile carriers move into oppositely doped material, they leave behind uncompensated dopant atoms near the junction, causing an electric field. This field creates a potential barrier between the two types of material. When equilibrium is reached, the magnitude of the field is such that the tendency of electrons to diffuse from the *n*-type region into the *p*-type region is exactly balanced by the tendency of electrons to drift in the opposite direction under the influence of the built-in field. Figure 2.3 shows the charge distribution, the electric field and potential along the structure.

We can analytically study this structure starting from the Poisson equation:

$$\nabla^2 V = -\nabla E = -\frac{\rho}{\epsilon_{Si}} \tag{2.5}$$

Where, according with the step junction approximation as shown in figure 2.3 we obtain:

$$E(x) = -\frac{qN_d}{\epsilon_{Si}}(x_n - x) \qquad 0 < x < x_n \tag{2.6}$$

and

$$E(x) = -\frac{qN_a}{\epsilon_{Si}}(x+x_p) \qquad -xp < x < 0 \tag{2.7}$$

so the maximum field is at x = 0:

$$E_{MAX} = -\frac{qN_a}{\epsilon_{Si}} x_p = \frac{qN_d}{\epsilon_{Si}} x_n \tag{2.8}$$

We see that:

$$N_a x_p = N_d x_n \tag{2.9}$$

Thus, the width of the depletion region on each side of the junction varies inversely with the magnitude of the dopant concentration; the higher the dopant concentration, the narrower the space-charge region.

Following eq. 2.5 in the *n*-type material:

$$\phi(x) = \phi_n - \frac{qN_d}{2\epsilon_{Si}}(x_n - x)^2 \qquad 0 < x < x_n$$
(2.10)

Similarly for the p-type material:

$$\phi(x) = \phi_p + \frac{qN_a}{2\epsilon_{Si}}(x + x_p)^2 \qquad -x_p < x < 0 \tag{2.11}$$



Figure 2.3: PN Junction at equilibrium: The Spatial Charge Region, Charge density, Electric Field, Electric Potential.

where ϕ_n and ϕ_p are the potentials at the neutral edge of the depletion region from:

$$n = n_i e^{\frac{q\phi}{kT}} \rightarrow \begin{cases} \phi_n = \frac{kT}{q} ln \frac{N_d}{n_i} & n\text{-type} \\ \phi_p = -\frac{kT}{q} ln \frac{N_a}{n_i} & p\text{-type} \end{cases}$$
(2.12)

In the end we can express the *built-in* potential from the neutral n-type to the p-type neutral region as:

$$\phi_{i} = \phi_{n} + \phi_{p} = \frac{kT}{q} ln \frac{N_{d}}{ni} + \frac{kT}{q} ln \frac{N_{a}}{ni} = \frac{kT}{q} ln \frac{N_{d}N_{a}}{n_{i}^{2}}$$
(2.13)

Note that the *built-in* potential ϕ_i is positive (that is, the *n*-side is at a higher potential that the *p*-side), which is needed to obtain a balance between drift and diffusion across the junction. The major portion of the potential change occurs in the region with the lower dopant concentration.

CHAPTER 2. THE PHOTODIODE

and the depletion region is wider in the same region. Figure 2.4 shows the band diagram of a pn junction at equilibrium.



Figure 2.4: Band diagram of the pn junction at equilibrium.

The width of the depletion region can be expressed as:

$$W = x_p + x_n = \sqrt{\frac{2\epsilon_{Si}}{q} \left(\frac{1}{N_a} + \frac{1}{N_d}\right)\phi_i}$$
(2.14)

2.2.2 PN Junction under Reverse Bias

If negative voltage is applied to the *p*-region, the barrier against the majority carrier flow increases. The total potential drop can be expressed as $\phi_i - V_a$ except that now V_a is negative and the junction is *reversed biased*. Under reversed bias, majority carriers are pulled away from the edge of the depletion region, which therefore widens and a very little current flows because the bias polarity aids the transfer of electrons from *p*-side to the *n*-side and holes from *n*-side to the *p*-side. Figures 2.5 and 2.6 shows, the charge distribution, electric field, potential and the band diagram along the pn junction under reverse bias.



Figure 2.5: Charge distribution, Electric field and potential along the pn junction under reverse bias condition.



Figure 2.6: Band diagram of the pn junction under reverse bias condition.

Still from eq.2.5 it is easy to evaluate the width of the depletion region for this structure.

$$W = x_p + x_n = \sqrt{\frac{2\epsilon_{Si}}{q} \left(\frac{1}{N_a} + \frac{1}{N_d}\right)(\phi_i - V_a)} = W_0 \sqrt{1 - \frac{V_a}{\phi_i}} \quad with \ V_a < 0$$
(2.15)

The maximum Electric field for x = 0 is:

$$E_{MAX} = \frac{2(\phi_i - V_a)}{W} \tag{2.16}$$

Considerations

When a reverse-biased pn junction is illuminated, the photogenerated carriers greatly increase the reverse current. In the dark, few carriers are present in the depletion region, and the reverse current is very low. When electron-hole pairs are generated by incident light, the number of carriers in the depletion region increases, with a corresponding increase in the reverse current. The ratio of the photocurrent to the dark current in a reverse-biased junction can be several orders of magnitude.

Although carriers are photogenerated throughout the structure of the pn diode if its depletion region is less than or comparable to the absorption length (see figure 2.1) of the light, they are most efficiently collected when they are generated in the depletion region.

The high electric field there separates the photogenerated electron-hole pairs before they can recombine and accelerates the carriers towards the neutral region where they are majority carriers and contribute to the current. The applied bias also enlarges the depletion region, allowing the incident light to generate additional photocurrent.

To increase the efficiency, the depletion region should be made as wide as possible. In specialized photodiode, a lightly doped, nearly intrinsic (i) layer is placed between the heavily doped p- and n-type region to form a p-i-n diode. This i-layer can be readily depleted by a modest reverse bias on the terminals of the diode, so that the region where carrier collection is more efficient gets larger, and so the corresponding photocurrent. Because the carriers are accelerated by the electric field within the depletion region, pin diodes respond rapidly to changes in the light intensity. By contrast, minority carriers generated in neutral regions travel to collecting regions by diffusion, a much slower process.



p-Type

Figure 2.7: p-n diode structure as photodiode.

Figure 2.8: p-i-n diode structure as photo-diode.

Although pin diodes are efficient and fast, adding a lightly doped layer within the diode is not readly compatible with conventional integrated-circuit processing. Consequently, pin are used for specialized applications, while pn diodes are used for photosensing in consumer/low-cost applications because they can be more readily integrated with other functions on an integrated circuit.

2.3 PIN Junction

As discussed before a **p-i-n** junction can be obtained inserting a lightly doped, nearly intrinsic (i) layer between the heavily doped *p*-type and *n*-type region. Figure 2.9 shows the charge distribution, the electric field and the electric potential along the structure.



Figure 2.9: PIN Junction

2.4 Photodiode in the CMOS process

The integrating pn junction photodetector was first introduced by Weckler at Fairchild in 1965[35]. He noted that if a pn junction in an integrated circuit was initially reverse biased and then one terminal left floating by activating a switch, the photocurrent caused the voltage of the photodiode V to discharge according to its capacitance C and the photocurrent I_{ph} flowing into the floating node[9].

The rate of discharge is given by:

$$\frac{dV}{dt} = \frac{I_{ph}}{C(V)} \tag{2.17}$$

Where the photocurrent depends on the wavelength-dependent photon flux $\Phi(\lambda)$ incident on the semiconductor and the wavelength-dependent quantum efficiency $\eta(\lambda)$ which accounts for optical reflection, absorption and carrier collection:

$$I_{ph} = q \int_{\lambda} \Phi(\lambda) \cdot \eta(\lambda) d\lambda$$
(2.18)

The integrating photodiode was the basis for the earliest MOS passive pixel sensors (PPS).

These devices and the further developments that cames out with the first CCDs, presented some limitations. In particular, they presented an high *dark current* (the collected signal in the dark due to thermal generation and diffusion), a low capacitance (high capacitance is required to collected a sensible amount of charge) and the used full frame architecture¹ required a mechanical shutter to allow the correct charge transfer.

Several solutions have been proposed as the interline transfer (ILT) CCD to eliminate the shutter and the associated signal "smearing". This solution implements a n^+p photodetector with a separate and light shielded charge-transfer device composed by shift register. These device were used for years especially in consumer electronics but they still presented several problem:

- High thermal noise.
- When a brightly illuminated pixel is then dimly illuminated, carriers from the brightly illuminated integration period may continue to transfer out of the n+region in subsequent frames. This problem is well know as "Iag image".
- Blue light with a short absorption length in silicon may be absorbed in the n^+ region and the generated holes may recombine before separation by the n^+p junction and be "lost". This leads to reduced quantum efficiency in the blue part of the spectrum.

To solve the ILT lag and the high dark noise problem, a low lag structure was invented. It has been recognized that lag would be eliminated if all the signal carriers could be transferred from the photodiode to the CCD. By creating a buried-diode structure with a p^+cap layer (p^+np vertical structure) the n layer could be fully depleted with application of sufficient transfer-gate voltage. Since it is a buried photodiode, dark current was also strongly reduced. In 1984, the structure received the name "**pinned photodiode**" (a.k.a. PPD) in a paper published by Burkey et al. at Kodak [9],[36].

¹The early CCDs used a full-frame architecture, meaning that the CCD cell serves both as the photodetector (while the CCD clocking signals are "frozen" during signal integration) and as a charge-transfer device through which signals from other pixels pass while the clocking signals are active, and where a pixel is the unit cell of the image sensor[9].

2.4.1 Pinned Photodiode



Figure 2.10: Example of a pinned photodiode implemented in a CMOS image sensor showing doping concentrations (dimensional units are microns). The image has been taken from [9].

Fig.2.10 reports a particular photodiode structure. It is a buried channel photodiode, formed by a double p^+np junction, where the p^+ implant, also referred to as *pinning-implant*, pins the surface at the substrate potential. That is the reason why we are talking about **Pinned Photodiode (PPD)**. This configuration forms a buried N-well region within the semiconductor as we can see in fig. 2.10. Dopings levels and widths are engineered such that when Fermi levels of the three regions are aligned (thermal equilibrium) a QNR exists within the N-Well. The band diagram along the vertical cut of the PPD is shown in fig. 2.11.



Figure 2.11: Energy band diagram of the PPD at equilibrium.

Under normal operation, the imaging cycle starts with the PPD n-region fully depleted by prior charge transfer. The potential in the PPD has a maximum in the n-region with a value called the pinning potential Ψ_{bi}^+ . Between the PPD and the floating contact there is a minimum



Figure 2.12: Ideal potential well diagram for a PPD. Turning on the transfer gate TG we can observe how the barrier decrese and the charge transfer to the FD is allowed. The image has been taken from [9].

potential or barrier potential Ψ_{bi}^{-} controlled primarily by TG. Signal carriers are collected and integrated in the Storage Well (SW) prior to readout. The SW is isolated from FD by a low voltage on TG. To achieve correlated double sampling² (CDS) of the signal carriers, FD is reset by the reset transistor (RST) as the first step in the readout cycle and then left floating. The floating potential of FD is sampled by the readout signal chain using source-follower SF. TG is then pulsed high to transfer signal carriers from SW to under TG and on to FD. The TG pulse voltage, the doping profile under TG, and the FD potential must cause a monotonic increase in potential from the SW to FD to allow complete transfer of all signal carriers from SW to FD. The change in potential ΔV_{on} FD is determined by the capacitance C of the FD node and the photogenerated charge Q_{ph} transferred from SW to FD[9].

Here, we introduce several important figures-of-merit of a pixel.

Full-well

A very important parameter to evaluate the performance of a PPD is the **Full-well capacity**. It defines the amount of charge an individual pixel can hold before saturating.

The nominal full-well capacity of the SW is evident from fig2.12:

$$N_{FW} = \frac{1}{q} C_{PPD} (V_p - V_b)$$
 (2.19)

where C_{PPD} is the average capacitance of the PPD.

²When used in imagers, correlated double sampling is a noise reduction technique in which the Reference Voltage of the pixel (i.e., the pixel's voltage after its reset) is removed from the signal voltage of the pixel (i.e., the pixel's voltage at the end of integration).

The primary challenge in fabricating the PPD is achieving a high full-well value even allowing the correct charge transfer. The challenge increases with reduced operating voltages and smaller pixel size. Secondary challenges include reducing leakage and dark current from the transfer gate, and decreasing charge transfer times.

Fill Factor

The ratio between the PD area and the pixel area is called **Fill Factor (FF)**. The fill factor depends on the amount of electronic circuitry included within the pixel. A lot of performance parameters depend on the PD area and thus the comparison between two pixels with different dimensions should always take into account the PD area (or equivalently the fill factor and the pixel area). Some performance parameters also depend on the perimeter of the PD, but this information is rare to be included within the design specification of a pixel.

A typical fill factor for the PPD is around $\simeq 25 - 35\%$ and due to the CMOS process design it is a big challenge increase this parameter and this result in a lower overall sensitivity[37].

2.4.2 Partially Pinned Photodiode

The partially pinned photodiode (PPPD) is an useful configuration of PPD that allows to increase several intrinsic features like the fill factor of the standard PPD keeping the good features of the standard configuration[37].

This pixel comprises a photodiode with a *pinned region* and an *un-pinned region*, and a transistor to reset the photodiode. Figure 2.15 shows the cross section of the structure. The name "partially pinned photodiode" means that only part of the diode has a pinned surface potential. Since an appreciable portion of the photo-sensitive region has a pinned surface potential, this pixel retains the advantages of the pinned photodiode pixels as the low dark current and in addition less lag images³ and shorter reset time can be achieved.

In addition, this pixel architecture has a higher fill factor due to the elimination of the transfer gate and floating diffusion regions. Whereas a pinned photodiode pixel has a fill factor of approximately 25%-35%, given the same design rules used to layout the pinned photodiode pixel, the partially pinned photodiode has a fill factor of approximately 50%-60%. Figures 2.13 and 2.14 compare the different layouts of a PPD and a PPPD.



Figure 2.13: Schematic example of layout of a PPD. The blue part rapresent the pinned photodiode (PPD). The Transfer Gate (TG) connects the PPD with the Floating Diffusion (FD) which is share with the source of the Reset MOSFET. It is activated by the Reset Gate (RG). Bias is provided by metal layer (dark gray) connections to the drain of the reset MOS (RD). The image has been rearranged from [37].

It should be noted that some of the increase in fill factor is due to less metal interconnect required in the partially pinned photodiode pixel[37].

³Image lag is a phenomenon that exists within many conventional CMOS imagers that can result in ghost image artifacts. Image lag results from the inability to completely reset a photodiode in the short amount of time due to the large capacitance associated within the photodiode and reset by sub-threshold current. This causes photoelectrons to be left within the photodiode and inadvertently be read as Signal electrons corresponding to the next frame in the image Sequence, causing ghost images[37].



Figure 2.14: Schematic example of layout of a PPPD. The blue part represents the photodiode (PD) where a part is "Pinned" and another portion is left "Un-Pinned". In this structure the Floating Diffusion (FD) is the "Un-Pinned" region where even the source diffusion of the Reset MOSFET is connected. RESET is activated by the Reset Gate (RG). In this configuration, bias is directly connected to the drain of the reset MOS (RD). The image has been rearranged from [37].



Figure 2.15: A cross section of the PPPD along the AA cut line in fig.2.14. The image has been rearranged from [37].

2.5 CMOS Image Sensor Technology

The Pinned photodiode (as well as the Partially Pinned photodiode or others...) is a single small base unit for catching all the informations coming from the absorption of photons and transfer them to the outside world. This unit is called **PIXEL**.

In 1993, a CMOS active pixel image sensor (APS) with intra-pixel charge transfer circuitry was proposed by Fossum et al. at JPL[9].

A CMOS APS pixel with a PPD is shown schematically in fig.2.16.



Figure 2.16: Schematic of CMOS APS pixel with PPD. The image was taken from [9].

Signal charge collected by the pixel photodetector is transferred to a floating diffusion (FD) (activating the transfer gate if the photodiode is a PPD or directly if a PPPD is used) whose potential is monitored by a source-follower (SF) within the pixel. The FD is reset by transistor reset signal (RST) prior to transfer and the source-follower is connected to the column bus line (COL BUS) using a row-select transistor (SEL). Usually the closest transistor to the photodiode (Transfer MOS for PPD or Reset MOS for PPPD) has a fixed position established by the foundry in their pixels layout. The other transistors can be integrated in the interpixel region suitable for the matrix configuration architecture. An example of layout is shown in the left part of fig.2.17.

In order to build an imager sensor we need to have a large sensitive area composed by millions of these pixels physically organized in a matrix as shown in the right part of fig.2.17.



Figure 2.17: Example of a pixel layout for the structure reported in fig.2.16 and its final arrangement in a matrix to form the image sensor sensitive area.

Features

Some pixel physical key definitions can be now introduced:

- Sensor Area: The area covered by the image sensor is a primary design driver and it obviously depends on the application that the sensor is aimed at.
- Number of pixels: The number of pixels counted on a sensor is given by the product between the number of rows and the number of columns. They determine the degree of detail that it is possible to cover with the image sensor.
- **Pixel Area and Pixel Pitch:** The ratio between the image sensor area and the number of pixels gives the pixel area. This is not a measure of the area covered by the PD but it rather includes the whole architecture. The horizontal and vertical dimensions of the pixel are called horizontal and vertical pitch, as in the leftmost sketch of fig.2.17. Considered that usually the pixel is square-shaped the squared pixel pitch is usually a measure of the pixel area.
- Quantum efficiency (QE): Is the proficiency of a pixel to sense electrons, given an certain amount of impinging photons. It is a function of the energy of the photon. We can define an EXTERNAL QE or an INTERNAL QE. They are define as:

$$EQE = \frac{generated \ electrons}{incident \ photons}$$
(2.20)

$$IQE = \frac{generated \ electrons}{absorbed \ photons} = \frac{EQE}{1 - Reflection}$$
(2.21)

In general QE for a real pixel is affected by several additional losses. These can be conceptually divided in:

- Optical losses: The amount of photons that impinges on top of the CMOS stack suffers a severe optical degradation before reaching the silicon. The incident light beam is indeed affected by reflection losses on every encountered interface.
- Electrical Losses: Even if the creation of an e-h pair occurs, its final collection from the PD and its successive sensing is not totally guaranteed because of electrical losses (i.e. SRH recombination, leakage).
- Quantum Detection Efficiency (QDE): As seen in the first section, in X-ray regime, only a certain fraction of incoming photons are absorbed and then detected by the device. This ratio is defined as:

$$QDE(E) = \frac{absorbed \ photons}{incident \ photons} = 1 - e^{-\frac{d}{\alpha(E)}}$$
(2.22)

where $\alpha(E)$ is the attenuation coefficient of the material (defined above) as function of the energy of the incoming photons and d is the thickness of the substrate of the device.

Chapter 3 The PERCIVAL Imager

In this chapter a general overview of the PERCIVAL (Pixelated Energy Resolving CMOS Versatile And Large) project and imager will be given. The project objective, the detector general structure including the sensor, the front-end electronic, the data receiving system and the operating principle will be explained and discussed.

As discussed in the previous chapter, over the last decade, synchrotron radiation sources have seen a significant increase in brilliance, and the advent of free electron lasers has made entire new research fields accessible to investigations with X-rays. These advances in light source capabilities have resulted not only in a host of scientific advances and discoveries, but also in the need for a new generation of X-ray imaging detectors that can match the sources capabilities in terms of frame rate and image dynamic range while recording image information with fine granularity over a large, preferably uninterrupted, (multi)Megapixel area with single-photon sensitivity. In particular, the high intensity beams provided by Free Electron Lasers (FELs) often result in large numbers of diffracted photons (up to 10^5 per pixel per pulse and more), which make the use of photon counting devices impossible. Simultaneously, single-photon detection capability with high confidence in false positive rejection is needed. Therefore, high dynamic range and low noise are mandatory and simultaneous requirements. Moreover, at FELs, handling repetition rates of up to 120 Hz while imaging individually the diffraction pattern of each photon is mandatory. Also, large and uninterrupted imaging areas combined with small pixel sizes and a high quantum efficiency (QE) over a large photon energy range is commonly required. Developing such next-generation imagers is both costly and timeconsuming, and the requirements at many facilities working with photon sources are similar enough to require a collaborative effort [8].

PERCIVAL is a monolithic active pixel sensor (MAPS), based on silicon CMOS technology. It is being developed by a large international collaboration consisting of DESY (a), ELETTRA (b), STFC-RAL (c), DLS (d), and PAL (e), to address the detection challenges at high brilliance Light Sources as discussed above and in the previous chapter. The list of the partners and their LOGO are reported in figure 3.1.

3.1 The system

For the above listed needs, CMOS sensors offer several advantages compared to other available technologies: they can be faster than CCDs since their architecture naturally enables massive parallelization[38]; the use of smaller pixels is less problematic than in hybrid[38] systems because it does not push the limits of bump bonding technology and finally, smaller photo-



Figure 3.1: The collaboration partners LOGOS.

diode capacitances can be achieved in CMOS compared to hybrid pixel sensors allowing lower noise levels.

The PERCIVAL Imager consists of a CMOS sensor developed by RAL/STFC (or an array of these two-side buttable devices), control and readout front-end electronics developed by DESY and ELETTRA, and a data back-end developed by Diamond. An overview of the system structure is reported in figure 3.2.



Figure 3.2: Scheme of the PERCIVAL system. The image has been taken from [39].

The sensor, which will be cooled down to -40°C, is mounted on a Low Temperature Cofired Ceramic (LTCC) Board and the assembly is accommodated in a vacuum chamber. A Power Board to supply the chip with the currents and voltages and which also includes the safety control, will be situated as well in vacuum, close to the chip. The PERCIVAL sensor is wire-bonded on two sides only, which opens the possibility to arrange up to four detectors in a cloverleaf configuration to still increase the detection areas shown in figure 3.3.

LVDS lines are connected via a vacuum chamber feed-through flange to a Carrier Board that



Figure 3.3: A scheme of a four detector system in a cloverleaf configuration.

hosts a Mezzanine Board for data acquisition, a Plug-in Board to interface with the beamline control, a Marker Board to extract timing info from the facility and a dedicated FPGA for communication between the boards and chip control/monitoring/readout.

Percival is suited at direct X-ray detection in the 250-1000eV energy range (extended desirable range from ≤ 100 eV up to 3keV).

Its core is a Monolithic Active Pixel Sensor (MAPS) array, manufactured in a commercial 180 nm CMOS technology on a high-resistivity epitaxial layer. In its soft-x-ray version, the MAPS is back-thinned (using the δ -doping process to achieve high Quantum Efficiency (QE) for the soft X-ray range, e.g. at 250 eV with 50 nm 25% of photons are lost) and Back-Side-Illuminated (BSI). In this way the back-side entrance window is minimized and even photons a very low energy can be detected.

In-pixel circuitry is used to extend dynamic range, modulating the pixel gain according to the impinging photon flux (lateral overflow). The signal collected is digitized on-chip to 12(+3) bits and streamed out up to 300 frame/s. The MAPS is wire-bonded to a ceramic (LTCC) board; bias, monitoring and (reconfigurable) addressing are provided by ad-hoc developed boards.

To cope with the high data rate (~ 20 Gbit/sec for the 2 Mpixels version), its outputs are passed to a data-concentrator board and streamed out through parallel 10Gb Ethernet links to multiple nodes, through a buffer switch. A HDF5 Virtual Dataset architecture has been decided for the data storage, to access images as a single data archive.

Some of the most important features are here summarised:

- Energy Range, Primary: 250 to 1000 eV, Extended: 100 to 3000 eV
- QE over Primary Energy Range: >85% uniform over sensing area
- Frame Rate up to 120 [Hz]
- Pixel Size: 27 μm
- Sensor Size:

- P2M version: 1408×1484 pixels, 4×4 cm²
- P13M version: 3520 \times 3710 pixels, 10 \times 10 cm^2
- Noise RMS $<15~e^-$
- Full Well > $10^7 e^-$
- Resulting Dynamic Range: 10^5 photons (at 250 eV)
- Sensor Output: Digital, LVDS
- Buttability: 2 side (adjacent edges), allowing cloverleaf configuration as reported in fig. 3.3.
- Exposure Modes, FEL: all photons in < 300 fs, Synchrotron: quasi-continuous

In chapter 5 the achievements of these features through tests with synchrotron and FEL radiations will be introduced and discussed.

3.2 The sensor

The PERCIVAL sensor has been designed by RAL/STFC[8]. Figure 3.4 illustrates the pixel architecture[39], where the photodiode structure is based on a **partially pinned photodi-ode**[10] that it has been discussed in chapter 2.



Figure 3.4: The basic 3T APS with lateral overflow capacitors. As discussed in chapter 2, the implemented photodiode is a PPPD (Partially Pinned Photodiode).

The basic 3T structure (source follower, reset, and select transistors) is enhanced by the addition of a series of switches (SW0-1, AB) and capacitors (C0-C1). During charge integration, the gates of the SW transistors connecting the capacitors are biased moderately at around 0.7V.

Under low-flux conditions, the photodiode voltage is not lowered much from its reset voltage, no current can flow through the transistors to the capacitors, and the system behaves like an ordinary 3-Transistor Active Pixel Sensor.

At higher photon fluxes, the photodiode voltage is lowered significantly, to the point where its voltage becomes comparable to the threshold voltage of source follower transistor. At this point, sub-threshold current will start flowing, starting charging the (first) additional capacitor C0, while the voltage on the diode will stay roughly constant: the system has switched to its first-highest gain mode by combining the capacitance of the diode and the C0 capacitor. When C0 is charged and the associated voltage reach the sub-threshold level, the exceed charge will start flowing and charging the (second) additional capacitor C1. At this point the system has switched to its second-highest gain mode by combining the capacitance of the diode and the C0 and C1 capacitors. The charge integration phase is described in fig.3.5.



Figure 3.5: Pixel charge distribution during the integration phase using the lateral overflow. The SWs are kept in sub-threshold. During the integration time the charge is collected by the photodiode (a), (b). Once the sub-threshold level is reached (red line)(c), the exceeded charge (light blue) flows towards the overflow capacitors and starts to charge them(d), (e).

During readout, the switches SW0-1 are sequentially opened (resulting in ever increasing effective pixel capacitance). This phase is explained in fig.3.6. The resulting source-follower voltages are compared to a threshold in the sampling stage to identify which of the two overall capacitances (and thus gains) is best suited to the charge recorded within the particular pixel

and image. In normal operation, only this "best" voltage is passed on to the ADC for conversion (and the gain information is stored). For moderate charge deposits, SW0 remains effectively open and the circuit behaves like a regular 3T pixel.



Figure 3.6: Pixel readout phases. After the integration phase, all SWs are opened (plot at the top) in order to confine the charge (light blue) in the corresponding capacitors. Then, they are sequentially closed in order to allow the read of the charge stored in the photodiode (D), C0 and then C1 by the source-follower transistor.

The ADC consists of a coarse and fine stage with two different current ramps, allowing for a total of 12-bit (plus one bit of over range) conversion. Together with the 2-bit information encoding the gain (defined by the lateral overflow capacitor used), 15 bits per pixel and reading must be transmitted to the readout. The sensor is designed to allow for digital correlated double sampling (CDS), i.e. recording the baseline voltage in each pixel before charge integration, and this information, although useful only for the highest gain based on diode capacitance only, is also converted into the same 15 bits.

In order to achieve readout rates of 120Hz over 3710 rows, 7 ADCs per column operating at 7ms conversion time are used. Data from 32 columns is multiplexed into one LVDS data output line running at \sim 460MHz data rate. In total, 111 LVDS lines output the data from 24864 ADCs, resulting in 50Gbit/s (including CDS) image data from a single sensor running at 120Hz.

3.3 Front-End Electronics

In order to operate the sensor, about 100 control signals plus several voltage supplies as well as biases are required, and a raw data rate of 50 Gbit/s has to be transported away from the sensor.

In order to optimize the noise performance, sensor voltages and biases are generated close to the chip (i.e. in vacuum).

The sensor is wire-bonded to a passive LTCC (Low Temperature Co-fired Ceramic) board, as shown in figure 3.7, which route the control signals and output data lines as well as the required voltages and currents to the CMOS sensor chip.



Figure 3.7: The sensor chip wire bonded to the LTCC.

The required voltage biases, voltage references with corresponding monitoring, current sources, ADCs, current monitor and temperature sensing circuitry are located on ad hoc custom PCB named **Power Board**, developed by ELETTRA as part of this PhD and reported in figure 3.8, which is connected through different high-density connectors to the LTCC with the control and data LVDS lines. This very complex board will be discussed in chapter 4. The ~ 200 data lines are connected to control and data processing electronics boards outside the vacuum vessel. The **Carrier Board**, developed by ELETTRA and reported in figure 3.9, interfaces to these LVDS lines, as well as to the "outside world" in terms of a control, timing, and monitoring interface. An FPGA on the Carrier board is responsible for providing the Finite State Machine signals for the CMOS sensor, and for controlling and reading out the supply, bias, and monitoring components on the Power Boards. The firmware architecture is based on a parameter lookup table; this enables easy on-the-fly changes of control parameters for the CMOS sensor operation, from timing adjustments to bias voltage changes.

The data lines from the Sensor are passed from the Carrier board to a **Mezzanine board** shown in figure 3.10 sitting on the Carrier board. These multi-purpose data handling board it has been developed at DESY and currently used for other project like LAMBDA and AGIPD. They combine a Virtex5 with several GB RAM, Flash memory, and 4×10 GBit Ethernet links.



Figure 3.8: The detector HEAD consisting of by the sensor, LTCC board, copper cooling block and many holders.



Figure 3.9: The carrier board with empty slots for the mezzanine board, the plug-in board and the marker board.

3.4 Data Receiving System

A single PERCIVAL sensor running at 120 Hz will produce a data stream of 50 Gbit/s. The image fragments transmitted on each of the sensor's 111 LVDS output links need to be assembled back into full frames, combined with auxiliary information including e.g. frame numbers, and calibrated and CDS-subtracted before any meaningful scientific analysis can be performed. The



Figure 3.10: The mezzanine board with a Virtex-5 XILINX FPGA and four GBit Ethernet sockets for the data connection.

sorting and reassembling of data will start in the Mezzanine board' FPGA, and be completed by the time the images are written on disk. In addition, by this point several on-the-fly data processing steps can be completed, such as ADC correction and CDS subtraction of the data for storage of a "meaningful floating point image" rather than raw ADC counts per pixel. These same on-the-fly processing steps will of course enable real-time display of science data. The data receiving system, from the 10GbE outputs of the Mezzanine board onwards to where calibrated, CDS-subtracted full images are written to disk at full frame rate, is being developed by Diamond.

3.5 Mechanics and Thermal Management

The low photon energy requires vacuum operation, and the sensor performs best at operating temperatures of the order of -40°C, requiring significant cooling efforts. Moreover, several scientific applications need the sensors to be movable within the chamber: all these constraints entail significant mechanical and thermal engineering efforts which partially will be supported by DESY and in part are left to each beamline that will use the detector, since the requirements in terms of vacuum, volumes, movements can be quite different.

Chapter 4

The PowerBoard

As presented in the previous chapter, the PERCIVAL Imager detector is a very complex device. In order to start using this system properly, a development of a very versatile **diagnostic device** is mandatory in this first preliminary phase because all we know about the detector comes from simulations and theoretical predictions.

Other information comes from tests of several scaled prototypes (test results on these intermediate chips will be shown in the next chapter) and CADENCE simulations performed by the designers, so in this initial stage we need to start operating with the sensor in a very carefully way having the possibility of real time fine tuning (accuracy of μA and mV) and monitoring of all the signals that we feed to the chip.

The **POWER BOARD**, object of this chapter, is the diagnostic devices developed for this purpose; it needs to implement all the aforementioned features becoming in many respects very similar to a waveform generator that has to work under very difficult conditions:

- Size constraints: The board has to fit behind the detector and has to work in a very limited space inside the experimental chamber.
- Design cooling oriented: The device is directly attached to the chip that it will be cooled down to \simeq -40°C, which is too low and not compatible with most of the components working conditions, so a proper low-temperature oriented design is mandatory.
- Vacuum compatibility: The device has to operate inside a high vacuum experimental chamber, which means that a sophisticated cooling system is necessary and particular care about components degassing is mandatory.

All these points will be presented in the following of this chapter showing the implemented solutions.

4.1 General overview

Looking at the experimental set-up, as shown in figure 4.1, the part that will be placed inside the experimental chamber is the detector HEAD composed by sensor, LTCC board, copper cooling block and many holders, cables that bring the control signals to the chip and the POWERBOARD suitable to provide all the biases that the sensor requires with the opportunity to adjust them very finely in order to find the best configuration for each part of the experiment.

All these parts meet a very hostile environment with **high vacuum** ($\simeq 10^{-6}$ mbar) and **cryogenic temperature** ($\simeq -40$ °C). The "CARRIER BOARD" instead, with a FPGA on board that control the entire system, will be placed outside together with external supplies and data storage system.



Figure 4.1: Scheme of the PERCIVAL system. The image has been taken from [39].

The detector HEAD has been designed in order to allow the direct connection of the POWER BOARD to the chip through the LTCC board.

Figure 4.2 shows the detector HEAD and the place where the POWERBOARD is connected and while figure 4.3 shows a picture of the board itself.



Figure 4.2: The detector HEAD consisting of by the sensor, LTCC board, copper cooling block and many holders.



Figure 4.3: The POWERBOARD.

4.2 Features

While the sensor is working (cooled down at $\simeq -40^{\circ}$ C and at $\simeq 10^{-6}$ mbar), it requires several control signals (clocks, settings, etc...), adjustable supplies and references in order to be setted in the optimal configuration[8]. Everything is controlled by the FPGA on the carrier board that, with specific signals and communication protocols, drives the sensor and sets all the required parameters.

In particular, the FPGA provides several dedicated I^2C lines for the control and monitoring of all the voltage and current sources available on the POWERBOARD.

All these sources can be summarize as:

• Voltage biases: Analog and digital general biases for turning ON and OFF the sensor.

In general they need to provide a bias with an associated high current.

- Voltage references: references for the internal circuitry. Low current consumptions are expected.
- Current biases: biases for the internal circuitry of the sensor. They need to be very precise and a very fine control (accuracy of $1\mu A$) is mandatory.

Considering the complexity of the system and its architecture, the board needs to provide to the chip:

- Nr. 11 adjustable voltage biases.
- Nr. 6 adjustable voltage references.
- Nr. 19 adjustable current biases with very fine control (accuracy of $1\mu A$).

In addition, for safety reasons, other features need to be implemented as:

- All the sources implemented need to be adjustable. This is mandatory in order to allow a turn ON or OFF following a right sequence and for calibrating the entire system.
- Monitoring of all the supply inputs that are given to the chip:
 - Monitoring of all the voltage biases and references generated.
 - Monitoring of all the currents generated.
- Monitoring of the external biases of the POWERBOARD circuitry.
- Temperature monitoring of the chip in real time.
- Temperature monitoring of the POWERBOARD in real time.
- Temperature monitoring of the vacuum chamber in real time.
- Each source can be by-passed by an external one in case there is a fault.
- At least two spare reserve sources for each kind of signal have to be provide on board.

The design and development this of fundamental device took more than one year of work to obtain a first working prototype.

4.3 The design

As mentioned, the design has been very challenging in order to satisfy all the requirements. It has been developed using the CAD Altium Designer[40] at Instrumentation and Detector Laboratories at ELETTRA.

The development required some steps and iterations, since the first requirement was to find the correct components and layouting solutions for each section of the final board. Once the results of each section met the requirements, these circuits have been integrated in the final design. An example of these prototypes is shown in fig. 4.4.

A screen-shots of the final project and the 3D view of the PCB are reported in fig.4.5 and in fig.4.6.



Figure 4.4: An example of a prototype built at ELETTRA laboratories in order to test a sub-circuitry (here, a current source is reported) before its implementation in the final design.



Figure 4.5: Design of the POWERBOARD using Altium Design tool.

In the following sections, a general description of all the different kind of sources is reported.



Figure 4.6: A 3D view of the POWERBOARD using Altium Design tool.

4.3.1 Voltage supplies

Voltages supplies are required to activate the analog and digital circuits of the chip. As mentioned, they need to be adjustable and capable to provide an high current at the output in order to supply the entire chip.

Figure 4.7 reports a scheme of the chosen circuitry.



Figure 4.7: Voltage bias circuitry.

The circuit is composed by a linear regulator and a 8-bit digital potentiometer controlled by the FPGA through the I^2C communication protocol. At the pin V_{ref} there is a fixed current (for instance $10\mu A$) provided by the regulator and the output V_{out} is set according with the relation:

$$V_{out} = V_{ref} = R_{digi_pot} I_{ref} \tag{4.1}$$

It is evident from the schematic that the output is controlled by the value of the resistance of the digital potentiometer that has been chosen in order to be compliant with the specifications of the chip.

For example, if the maximum value of the supply needs to be 2V, from eq. 4.1 we see that the maximum value of the resistance of the digital potentiometer will be $200K\Omega$.

Figure 4.8 shows the behaviour of the circuit while changing the value of the digital potentiometer. Each output of these voltage supplies, is connected both to the chip and to an ADC (Analog to Digital Converter) in order to provide a real time monitoring of the measured output fed to the chip. In fig. 4.8 the red line reports the value of the monitored voltage.



Figure 4.8: Measured and monitored (internal ADC) output of the voltage bias circuitry. The 8-bit digital potentiometer that set the output value is controlled by the FPGA by a I^2C lines.

4.3.2 Voltage references



Figure 4.9: Schematic of the voltage reference circuit.

In order to provide a **voltage reference** (suitable for setting particular threshold levels, etc...), a unity gain buffer amplifier has been chosen. It is realized by applying a full series negative feedback to an op-amp simply by connecting its output to its inverting input, and connecting the signal source to the non-inverting input. The circuitry scheme is shown in fig. 4.9.

In this configuration, the entire output voltage is fed back into the inverting input. The difference between the non-inverting input voltage and the inverting input voltage is amplified

by the op-amp. This connection forces the op-amp to adjust its output voltage equal to the input voltage (V_{out} follows V_{in} so the circuit is named "op-amp voltage follower").

$$V_{out} = V_{in} \tag{4.2}$$

The input V_{in} is provide by a 16-DAC (Digital to Analog Converter) controlled by the FPGA through I^2C communication protocol.



Figure 4.10: Output of the voltage reference circuitry. The input V_{in} is provide by a DAC controlled by the FPGA by a I^2C lines.

Figure 4.10 shows the behaviour of the circuit following a scan of the input voltage through the DAC from the lowest to the highest possible value. Even in this case, each output is connected both to the chip and to an on board ADC (Analog to Digital Converter). The monitored value is shown with the red line in fig.4.10. As we can see, for high values, there is a discrepancy between measurements which is due to the ADC input channel saturation that allows a maximum value of 4V.

Since expected values required by the chip are around $1.5 \simeq 2V$ the implemented circuit and the corresponding monitoring work fine and in accordance with the chip specification.

4.3.3 Current Sources

Several current sources are required to provide references or to supply some circuitries inside the chip. Figure 4.11 reports a scheme of the designed source that is know as "Improved Howland Current Pump" [41], [42].



Figure 4.11: Schematic of the Current source. The input V_{in} is provided by a 16-bit DAC controlled by the FPGA through the I^2C lines.

The input V_{in} is provided by a 16bit-DAC (Digital to Analog Converter) controlled by the FPGA through I^2C communication. From [41] the relation between the output current and the input voltage is:

$$I_{out} = \frac{V_{in}}{R_3} \tag{4.3}$$

The proof of this relation is reported below:

- The Norton theorem can be applied to the circuit shown in fig.4.11 so the output node (between R_2 and R_3) is considered to be grounded.
- The current flowing in R_1 is $I_1 = \frac{V_{in}}{R_1 + R_2}$
- V_a is the potential at the + input of the opamp and V_b is the potential at the input. Under the assumption of virtual short $V_a = V_b$ and therefore $V_{out} = 2 \cdot V_a$.
- The current of R_3 is $I_2 = \frac{V_{out}}{R_3}$
- $I_{out} = I_1 + I_2 = \frac{V_{in}}{R_1 + R_2} + \frac{V_{out}}{R_3}$
- A way of expressing V_{out} is $V_{out} = 2 \cdot V_a = 2 \cdot I_1 \cdot R_2$
- The output current becomes $I_{out} = \frac{V_{in}}{R_1 + R_2} + \frac{2 \cdot V_{in} \cdot R_2}{R_1 + R_2}$
- Factoring out $\frac{V_{in}}{R_1+R_2}$ we get $I_{out} = \frac{V_{in}}{R_1+R_2} \cdot \left(1 + \frac{2 \cdot R_2}{R_3}\right)$
- Assuming $R_1 = R_2 + R_3$ we can simplify the expression as $I_{out} = \frac{V_{in}}{R_3}$
- Since the equivalent resistor at the output of the circuit is relatively high ($\simeq 10$ s of K Ω) and the equivalent resistor of the chip is very low ($\simeq 300 \ \Omega$, data provided by the designer), the load does not influence the behaviour of the source.

Figure 4.12 show the relation between the digital input provide by a 16bit-DAC I^2C controlled and the output current of the designed source.


Figure 4.12: Measured output of the current source circuitry. The input V_{in} is provide by a DAC controlled by the FPGA by a I^2C lines.

4.4 Vacuum Test

After demonstrating the right behaviour of the device from the electrical point of view, a vacuum test has been performed in order to confirm the compatibility of POWERBOARD with experimental environment. These tests were conducted at ELETTRA laboratories thanks to the support of the vacuum group.

Tests were performed using an experimental chamber equipped with a mass spectrometer in order to detect the possible leakage of material due to the degassing of the tested device.

Before measurements, the board was cleaned with no-aggressive solvents in order to remove all the dirt layers presented on the surface without damaging it and then the device has been placed inside the chamber. Figure 4.13 shows the test set-up before start pumping the vacuum and figure 4.14 shows the entire apparatus during the test.



Figure 4.13: The test vacuum chamber with the POWERBOARD.

Test showed (with the red line) that after three hours of pumping the the chamber reached a pressure around $\simeq 5 \times 10^{-6}$ mbar, then the sample was treated with bake-out at 80°C for 24h. The final measured pressure was around $\simeq 2 \times 10^{-7}$ mbar demonstrating the fully compatibility of the POWERBOARD with typical levels of vacuum which are present in the PERCIVAL experimental chamber.



Figure 4.14: The test chamber during the vacuum test.



Figure 4.15: Materials quantities detected due to the degassing of the POWERBOARD during the vacuum test.

Figure 4.15 shows the data collected by the mass spectrometer during the vacuum test (red line) and the background of the chamber (blue line). Material quantities come from the residual presence of dirt layers. They can been removed with a more aggressive cleaning. Without bakeout we observed the same species in the chamber with different quantities.

4.5 Considerations

The design took more than one year of development. The first release of this board was available in February 2017 and all the measurements and verifications showed that:

- There aren't PCB errors as shorts, wrong connection, etc...
- All the sources implemented works properly.
- All the required performances are reached.

After a period of evaluation where the POWERBOARD and each source on it have been fully characterized in order to define the best work set-points, in September 2017 the first POWER UP of the 2Mpixel PERCIVAL chip (P2M) has been correctly performed, first at DESY and then at ELETTRA with a second available device. The results and the preliminary images will be presented in the next chapter.

Chapter 5

Results of the test-beams

In this chapter, we present tests on scaled prototypes of the PERCIVAL detector, a monolithic CMOS Imager for detection of soft x-rays in Synchrotron Rings and Free Electron Lasers. We describe in which way the imager achieves low noise and high dynamic range by means of an adaptive-gain in-pixel circuitry. We also demonstrate low energy photons sensitivity and measurements of CCE (charge collection efficiency). Furthermore, at the end of the chapter, the firsts images with the 2Mega Pixels final system will be presented.

5.1 PERCIVAL test chips

Before designing and fabricating a full $4 \times 4 \ cm^2$ chip, smaller test sensors were produced to evaluate the performance of various pixel architectures, gain decision logic, and of the ADC and to verify the fast digital output circuitry. These chips were fabricated in a commercial 180 nm CMOS technology. Test sensors with $210 \times 160 \ 25\mu m$ pixels each, allow comparison of a total of 12 different pixel designs (70×80 pixels each), with identical periphery; of these, half use an annular partially pinned photodiode[10], half are based on a more conventional n-well diode design. These sensors use slower CMOS output lines and slightly less efficient data formatting, but enable testing of the pixel and ADC performance at full readout and conversion speeds.

Preliminary tests have shown the correct functioning of the test chips, so wafers on 18 μ m epi-layer were forwarded to NASA's Jet Propulsion Laboratory (JPL) for back-thinning in order to achieve the direct detection of photons under X-rays regime[8].

The chips are wire-bonded to a carrier board (Chip on Board, or CoB) which interfaces to both the custom readout systems. Figure 5.1 shows the test system and figure 5.2 reports the system placed in the experimental chamber.



Figure 5.1: The test setup on a benchtop. From right to left, CoB with test chip, interposer board, periphery board. The latter connects to the horizontal SD board (note the vacuum barrier flange already in place), on which in turn the Mezzanine board is placed. The image has been taken from [8].



Figure 5.2: The PERCIVAL test chamber. Copper plates thermally tied to the chamber surround the Periphery board and provide cooling paths to hot active components, tied to the chamber walls. The cryo-cooler sits in the chamber extension to the right, resistors on the cold finger provide counter-heating. The image has been taken from [8].

5.2 Demonstration of low-noise operation

Noise sets the fundamental limit on image sensor performances under low illumination.

Before the measurements, the Photon Transfer Curve (PTC) technique[43] has been used to calibrate the system and find the conversion factor between the measured ADU level at the output of the system and the corresponding equivalent e⁻ r.m.s level. An overview of the PTC technique is reported in appendix B.

The r.m.s. of the output signal (reported to an equivalent input charge) has been used as a measure of its noise. In general, 5000 dark images have been averaged for a 8.33 ms of integration time and thanks to the conversion factor (calculated through the PTC) it has been possible to evaluate the corresponding equivalent noise (e^-) of the system[39].

The low value ($\simeq 15 \text{ e}^-$) measured on cooled ($\simeq -40^{\circ}\text{C}$) system confirms that the detector is suitable for single-photon discrimination in the 250-1000eV energy range. The system performance has been confirmed on a wide range of readout speeds, from 10 frame/s up to 120 frame/s (Fig. 5.3), thus confirming the compatibility of PERCIVAL with most of the Free Electron laser facilities (built or under construction)[44].



Figure 5.3: Noise measurements performed in dark conditions, using frame rates compatible with several Free Electron Laser Facilities. The image has been taken from [44].

When the in-pixel lateral overflow (reported in chapter 3) circuit changes the pixel gain (because it is exposed to a high flux), the additional capacitors introduced in the circuit increase the system noise. The noise introduced, however, has been measured to remain far below the Poisson limit (i.e. the intrinsic uncertainty of the photo-generation process). This means that the system noise remains shot-noise limited, also under high-flux conditions (fig. 5.4). In addition to this, some degree of reconfigurability has been implemented in the system, by means of a Programmable Gain Amplifier (PGA) in the circuit chain, that can be tuned to find



Figure 5.4: Noise measurements performed under high-flux conditions. The circuit contribution to the system noise (blue line) is always below the poissonian uncertainty (red line, calculated with the corresponding generated charge by 250 eV incident photons). The charge values where the noise switches between different levels are defined by the lateral overflow gain switching points; they can be configured by the PGA stage. The image has been taken from [44].

the best trade-off between the noise level and the overflow-gain switching points[44]. Other findings on these measurements can be found in [39].

5.3 Dynamic Range

The adaptive gain modulation induced by the lateral overflow mechanism has been verified on reduced-sized prototypes, measuring the system response to a increasingly large charge integration[39]. Results reported in fig. 5.5 show that the system is able to span through several orders of magnitudes still keeping a linear behaviour. It is to be observed that, because of the lateral overflow mechanism, the sensor response to an increasing integrated charge deviates from a straight line, and is instead divided in three lines having increasingly gentler slopes, each one characteristic of one of the detector "gain" stages. A 3-level signal (encoded with 2 bits) is provided by each pixel to identify its "gain" stage in that image (thus allowing to reconstruct the collected charge).

The pixel response was measured to saturate at an integrated-charge-level exceeding 3.5 million electrons, corresponding to 50000 x-ray photons at an energy of 250eV. The bits encoding the lateral-overflow information were also verified to correctly report the pixel gain stage [44],[39].



Figure 5.5: Dynamic range characterization of the PERCIVAL system, spanning several order of magnitudes. The top plot shows the output of the system while the different stages of the lateral overflow is activated. The bottom plot shows the associated gain level (encoded with 3 bits). The underline green box shows a magnification of the system response to low flux. The plots are taken taken from [44].

5.4 Low-energy-photon detection

In order to verify that the back-side post processing produces a surface compatible with lowenergy-photon detection, tests were performed on prototypes at several FEL and Synchrotron Rings.

As an example, tests were performed at the BL2 beamline of the FLASH FEL (DESY, Hamburg, Germany) illuminating the detector with 13.5nm (nominal energy 91.84eV) photons, to verify that the detector response was compatible with the signal expected from such photons, rather than being dominated by the higher harmonics components of the beam (which would be more likely to pass through an eventual entrance window of inert material)[44].

A pinhole of known diameter was inserted between the beam and the detector (at $\simeq 40$ cm distance), and the detector was used to record diffraction patterns. The diffraction pattern through a circular aperture consists of concentric circular rings, having a distribution of minima and maxima depending on the wavelength of incoming photons according with:

$$x \simeq D \frac{m\lambda}{d} \tag{5.1}$$

where D is the distance of the pinhole from the imager, d is the circular aperture and λ is the wavelength of the incident photons.

Fig. 5.6 shows the comparison between experimental data along a cut-line (blue circles) and the analytic prediction of the diffracted image shape (green line): the good agreement confirms that, due to the thin entrance window, the detector response is dominated by the beam main harmonic ($\simeq 92 \text{eV}$), and that the contribution of higher harmonics is negligible[44].



Figure 5.6: Diffraction through a 20μ m-pinhole: comparison between data (blue circles) and analytical prediction (green line) according with equation 5.1. The image has been taken from [44].

Capability to work in Single-shot operation mode has been verified too: Figure 5.7 shows the

comparison between a single-pulse image (taken at the same FEL beamline) and an integrated multi-pulses average. The images show the diffraction rings used for the previous evaluation[44].



Figure 5.7: Comparison between a single-pulse image (left) and an integrated multi-pulses average (right). The image has been taken from [44].

5.5 Charge Collection Efficiency

Charge Collection Efficiency (CCE) can be used to estimate a lower limit of the QE of the system[43]. It basically accounts for the number of electrons measured under a particular illumination situation, per time unit. This figure of merit can be define as[38]:

$$CCE = \frac{N_{e^-}}{N_{ph}} \tag{5.2}$$

where N_{e^-} is the number of carriers measured with the sensor and N_{ph} is the number of carriers produced by an impinging photon flux, ϕ_{ph} . In Silicon, an average of 3.6eV[45] is required to create a electron-hole pair in the most probable interaction.

A well defined ϕ_{ph} is crucial in order to have a correct estimation of the CCE[38], so it was measured with a calibrated photodiode placed in front of the sensitive area of the detector before the measurements. The measured number of electrons is then compared with the number of expected pairs to be created under the same flux condition. Since no quantum yields correction are applied, the QE is essentially lower-bounded by the CCE[46]. In figure 5.8 several measurements are reported.

For the primary energy range, the CCE measured at 400 eV was $85 \pm 3.64\%$. Measurements at 400 eV and higher energy photons are slightly lower (between 65% and 80%) but still compatible with the target of 85% QE(LINK al capitolo). These experiments were performed with two different post-processed instances of test chip; therefore, differences between them could help to explain the observed variation. Also, a significant dip below our target of 85% is observed in the range between 275 and 375 eV. A pronounced reduction of the CCE to $\simeq 40\%$ at 325 eV was found too.

A more detailed description of these measurements and further investigations to fully understand the results can be found in [46].



Figure 5.8: CCE measured for two different test chips as a function of the photon energy, for a total of 3 measurement campaigns. Note the relatively high CCE ($51.83\pm4.35\%$) obtained at 125 eV, below the primary energy range (250 eV-1 keV). A lower than expected CCE was found for energies within the primary energy range. Specifically, between 325 eV and 375 eV the CCE shows values between 40% and 60%. Error bars in this range are lower than $\pm 3\%$. The image has been taken from [46].

5.6 The P2M system

The Full 2M-pixel system in its Front-Side-Illuminated version has been manufactured and assembled, and it is at the present under test (in air, at room temperature): preliminary electrical and optical tests show the expected behaviour, and the first images to demonstrate the pixel-array functionality (using visible light and a shadow mask between the detector and the light source as shown in figure 5.9) have been taken at several frame rates (from 10 to 100 frame/s).

Fig. 5.10 shows as an example a comparison of images taken at different frame rates: when a longer integration time is used, the signal amplitude progressively increases, and, if high enough, the lateral-overflow mechanism is triggered (which lowers the signal amplitude, and reduces the charge-to-voltage transfer function), thus expanding the dynamic range of the pixels that would otherwise saturate. Such pixels can be recognized by their lateral overflow "gain" stage being higher than the baseline[44].

At the same time, the Front-Side-Illuminated (FSI) system is used to test appropriate calibration and data-analysis procedures (on the basis of the algorithms that were developed for use in the prototype chips).

Currently, the full calibration of the FSI sensors is ongoing. Fine-tuning the sensor operation parameters is largely independent of FSI vs Back Side Illuminated (BSI) operation of the sensors. In parallel, wafers are being post-processed for BSI operation.

Moreover an example of readout using the present "full-speed" mode (the full image is attached) has been tested. Figure 5.11 shows a reverted ELETTRA logo, plus some traces of glue present in the mask surface.

Most importantly, the image is part of a set of 10 consecutive frames taken at about 150 Hz frame rate, using the ODIN-based DAQ software without packet loss.

We expect a first mounted BSI sensor ready for tests in next year. For a first assessment of performance parameters such as noise, cooled operations in vacuum are necessary and will be possible on a similar timescale.



Figure 5.9: Detector set-up with a shadow mask horseman shaped representing the PERCIVAL logo. The image has been taken from [44].



Figure 5.10: Comparison on the P2M system response to visible light, for different integration times. For the higher integration time (the bottom one), some pixels extend their dynamic range by means of the lateral overflow mechanism. The left column shows the gain bits introduced by the lateral overflow. The right column shows the MSBs of the image. No correction and no proper calibration was applied to the images. The image has been taken from [44].



Figure 5.11: Image of the ELETTRA logo (inverted) (the mask used on the right) has been taken in "full speed mode". The image is part of a set of 10 consecutive frames taken at about **150 Hz** frame rate without packet loss. Only the most significant bits (MSBs) are shown and no correction and no proper calibration was applied to the images.

Chapter 6

TCAD simulations and modeling

To meet the requirements that have been presented in the previous chapters, different detection strategies have been suggested and some of them have been implemented recently. Backthinned, monolithic active pixel sensors (MAPS) based on standard CMOS technology [9],[10] are promising candidates for these applications and in particular, the PERCIVAL CMOS based imager detector has been presented. In some architectures, due to the substrate thickness and to the low bias voltages that are typical of CMOS based devices, regions of the pixel structure are not entirely depleted, thus diffusion has relevant effects on the charge collection mechanism of photo-generated electrons (e) and holes (h).

It is therefore fundamental to understand if such structures in which carrier diffusion is dominant are suited to fulfill all the aforementioned requirements for X-ray imagers by means of extensive simulations and design optimizations. Moreover, since TCAD simulation can be very time consuming on such structures, a development of a model that implements the main processes of the charge dynamic collection (drift and diffusion) is needed.

In this chapter we will present the result of TCAD simulations of the charge collection dynamic on these structures and two possible modeling approaches to simplify such evaluations.

6.1 Simplified structure

To exemplify the difficulties of the modeling, in this chapter we firstly analyze a generic CMOS back-thinned pinned photodiode for X-ray detection in the low energy range (from 250eV to 1keV)[47] using the commercial TCAD tool Sentaurus [48]. A 2D cross-section of such device, which has been inspired by the pinned photodiode presented in [10], is sketched in Fig. 6.1.

As we will see in Sect.6.2, because of the low applied bias (the pixel is intended to be part of a matrix build in standard CMOS technology operating at standard CMOS supply voltages) and to the silicon thickness, some regions within the substrate of the pixel are not fully depleted. This means that carriers generated deep inside the substrate will reach - if at all - the contacts mainly by diffusion. The analysis of such diffusion dominated charge collection process requires CPU time consuming 3D simulations in the time domain.

We thus propose in Sect.6.3 a model based on RAMO's theorem extended by including diffusion processes to analyze the time response of the sensor, which can be simulated using the results of a much less computationally demanding stationary TCAD simulation as input instead of time-dependent TCAD simulation. This model is firstly verified against a TCAD simulation of a simple p-i-n diode (Sect.6.4.1), and then applied to investigate the 3D generic CMOS sensor (Sect.6.4.2).



Figure 6.1: Sketch of the 3D (a) and 2D cross-section (b) of the CMOS pinned photodiode considered in this work. The n^+ region is a ring contacted in a point as shown in chapter 2. V_{bias} is applied to the n^+ contact, p^+ contacts are grounded. The backside is not contacted. These images have been taken from [49].

6.2 TCAD simulations

To start with, an analysis of the pixel of fig.6.1 has been carried out using the TCAD tool Sentaurus [48]. The simulator solves the coupled Poisson and drift-diffusion equations for electrons and holes in the time domain. Unless otherwise stated, simulations include SRH (Shockley-Read-Hall) generation/recombination with parameters $\tau_n = 100\mu s$ and $\tau_p = 10\mu s$ typical of high quality substrates needed to reduce the dark current. The current transient response due to e-h pairs generated at different positions is reported in the right-hand graph of Fig.6.2. We can see that if e-h pairs generation occurs outside the depletion region (points 2-5) the current pulses are broader than when pairs are generated inside the depletion region (point 1), consistently with the diffusive nature of transport.

To simplify the simulations, a DC bias was applied to the n^+ contact with respect to the grounded p^+ diffusions. It is noteworthy that in a real CMOS pixel this is the case just during the short reset phase of the pixel, while during the charge collection phase the terminal is left floating (as seen in chapter 2). We are thus assuming that the photo-generated charges do not alter significantly the electrostatic potential profile inside the structure; in fact simple estimates of the device capacitance point out that 100 e-h pairs modify the bias of the diode by a few 10s of μ V. Also, in the right plot of Fig.6.2, we are showing current waveforms to display



Figure 6.2: Right: simulated current waveforms assuming a photo induced charge of 100 e-h pairs corresponding to a single photon with energy of 365 eV with Dirac- δ spatial distribution at the locations shown in the left graph. $V_{bias} = 1.8V$; T = 273K. This image has been taken from [49].



Figure 6.3: Color map of the electrostatic potential in a 2D cross-section of the pixel at $V_{bias} = 1.8V$ (left) and the corresponding field lines (right). This image has been taken from [49].

the build-up of charge in the n^+ region, charge that is then extracted from photodiode by the transistors embedded in the pixel: the current waveform itself cannot be measured in the real pixel matrix. The waveform is thus an indication of how much charge can be collected over a certain amount of time.

The electrostatic potential profile for a 2D cross-section extracted from the results of the DC simulation of the CMOS pinned photodiode is reported in Fig.6.3 (left plot). A critical region can be identified in the center of the pixel (i. e. point 2 in Fig.6.2), since here the electrostatic potential is essentially constant and the electric field tends to zero (right plot). In the absence of an external drift field, diffusion mechanisms are dominant and cannot be neglected.

The simulation took about 50 hours of computation time for each of the curves in Fig.6.2 on a HP workstation with Intel Xeon E7 processor (40 cores) and 200 GB of RAM. Because of such large computational burden, Ramo's theorem is often used to estimate the induced current pulses due to a given charge from stationary solutions of the Poisson equation in the semiconductor [50, 51].

As known from the Haynes-Shockley experiment [52] both drift and diffusion contribute to shaping the induced current pulses but previous numerical implementations of Ramo's theorem neglected diffusion effects. We show in the next section how diffusion processes can be included in an efficient numerical implementation of Ramo's theorem.

6.3 PROPOSED MODEL

In order to derive a physically based realistic model of the system overcoming the limitations of existing models accounting only for carrier drift, we start from TCAD simulations of a generic p-i-n diode with a $0.6\mu m$ long intrinsic region (see Fig.6.4) and we simulate the time evolution of the electron and hole concentration profiles, after a single e-h pair is generated at a position near to the center of the pixel. To highlight the effect of transport, we have turned off generation-recombination mechanisms in these simulations. Not surprisingly, diffusion gives rise to concentration profiles with a Gaussian distribution (Fig.6.4). The drift of the carriers is proven by the drift of the pulse peak and centroid in time towards the p⁺ and n⁺ regions for holes and electrons, respectively. The width of the charge distribution increases according to the Einstein-Smoluchowski relation[53], as a result of diffusion in the longitudinal direction. This is consistent with the Haynes-Shockley theory[52].



Figure 6.4: Charge density dynamics after the generation of one electron (red) - hole (blue) pair in the middle of a 1D P-I-N diode with an intrinsic region of $600\mu m$ at T = 300K and $V_{bias} = 5V$. This image has been taken from [49].

Fig.6.5 (left) shows the evolution of the position of the concentration peak versus time for electrons and holes. They exhibit a linear trend. The slope yields the carrier drift velocity $v_e \simeq 1 \cdot 10^7 cm/s$ and $v_h \simeq 6.7 \cdot 10^6 cm/s$. Since the electric field inside the intrinsic region, as extrapolated from the TCAD, is approximately 97000 V/cm, the corresponding carrier mobility for electrons and holes are $\mu_e = \frac{v_e}{F} = 102 cm^2/V \cdot s$ and $\mu_h = \frac{v_h}{F} = 69 cm^2/V \cdot s$. As expected these values are very close to the value of the high field mobility (defined as the ratio between the velocity and the field absolute values) computed by the TCAD according to the Caughey-Thomas expression [54]: $\mu_e = 104 cm^2/V \cdot s$ and $\mu_h = 78 cm^2/V \cdot s$.

The right plot of Fig.6.5 shows the standard deviation of the Gaussian functions that bestfit the profiles in Fig.6.4. The linear trend is again consistent with the Haynes-Shockley theory that predicts $\sigma^2 = 2 \cdot D \cdot t$. The slope of the curves in Fig.6.5 (right) gives $D_e = 2.62cm^2/s$ and $D_h = 1.76cm^2/s$ which are in good agreement with the mobilities extracted from the slopes in Fig.6.5 (left) once multiplied by KT/q.



Figure 6.5: Left: position of the centroid of the charge density cloud for electrons and holes after the generation of an electron-hole in the middle of the device as in Fig.6.4. Right: standard deviation of the electron's and hole's charge density profiles as extracted from the data in Fig.6.4. These images have been taken from [49].

In fact:

$$D_e = \mu_e \frac{KT}{q} = 102 \cdot 0.0259 = 2.64 cm^2/s$$

$$D_h = \mu_h \frac{KT}{q} = 69 \cdot 0.0259 = 1.78 cm^2/s$$

The results in Fig.6.4 and 6.5 can be used to derive a model for the induced current as follows. First of all, the peaks of the Gaussian distributions move according to pure drift, i.e. the position at a time $t + \Delta t$ can be obtained from the one at time t as:

$$\begin{bmatrix} X_p \\ Y_p \\ Z_p \end{bmatrix} (t + \Delta t) = \begin{bmatrix} X_p \\ Y_p \\ Z_p \end{bmatrix} (t) + \Delta t \cdot \begin{bmatrix} v_x(t) \\ v_y(t) \\ v_z(t) \end{bmatrix},$$
(6.1)

where the velocity vector is again computed according the Caughey-Thomas expression[54], as commonly used in TCAD, namely:

$$\begin{bmatrix} v_x(t) \\ v_y(t) \\ v_z(t) \end{bmatrix} = -\mu_0 \frac{\begin{pmatrix} F_x(t) \\ F_y(t) \\ F_z(t) \end{pmatrix}}{\sqrt[\beta]{1 + \left(\frac{\mu_0 |F(t)|}{v_{sat}}\right)^\beta}},$$
(6.2)

The electric field profile \vec{F} is obtained from a TCAD stationary (not transient) simulations. The low-field mobility μ_0 , the saturation velocity v_{sat} and the coefficient β are the same used by the TCAD and all quantities are evaluated at the concentration peak position at time t.

In the absence of diffusion, the induced current will thus be given by:

$$i_{DRIFT}(t) = q \cdot \left\{ \begin{bmatrix} v_x(t) \\ v_y(t) \\ v_z(t) \end{bmatrix} \cdot \nabla \left(\frac{\Delta \Psi(X_p(t), Y_p(t), Z_p(t))}{\Delta V_{bias}} \right) \right\},$$
(6.3)

where $\Delta \Psi$ is the potential variation due to a small difference in the applied voltage ΔV_{bias} computed at the particle position at time t. The gradient of $\Delta \Psi / \Delta V_{bias}$ is the weighted field

of the generalized RAMO's theorem presented in [55],[56]. $\vec{v}(t)$ is the velocity of the concentration peak at the position corresponding to time t, see Eq.6.1. Eq.6.3 has to be evaluated for electrons and holes separately and then the two currents are summed together. This expression is consistent with similar implementations of Ramo's theorem[50],[51].

In order to include the effect of diffusion, we consider one carrier type at once and we start assuming that generation is perfectly localized, so that $\sigma^2(t=0) = 0$. Then, according to Fig.6.5 (right) and to the Haynes-Shockley theory, if Δt is short enough:

$$\sigma^2(t + \Delta t) = \sigma^2(t) + 2 \cdot \Delta t \cdot D(t) , \qquad (6.4)$$

where D(t) is an apparent diffusion coefficient obtained from the high field mobility[57] using Einstein's relation:

$$D(t) = \frac{KT}{q} \frac{\mu_0}{\sqrt[\beta]{1 + \left(\frac{\mu_0 |F(t)|}{v_{sat}}\right)^\beta}},$$
(6.5)

where F(t) is the electric field seen by the carrier at the position $(X_p(t), Y_p(t), Z_p(t))$.

At this stage one could use Ramo's theorem to compute the current induced by the Gaussian concentration profile whose peak position and width evolve during time according to Eqs.6.1 and 6.4. However, when applied to a 3D structure, this procedure would require the calculation of integrals in three dimensions at each time step, definitely a heavy computational burden. For this reason, we transform the spatial Gaussian profile into a Gaussian function in the time domain with a variance:

$$\sigma_{time}^2(t) = \frac{\sigma^2(t)}{|v(t)|^2} , \qquad (6.6)$$

where v(t) is the velocity of the particle at time t, i.e. evaluated with the field at $(X_p(t), Y_p(t), Z_p(t))$.

We then convolve this function with the current computed considering transport of the carriers by drift (Eq.6.3):

$$i_{DRIFT+DIFF}(t) = \int_0^\infty i_{DRIFT}(t_1) \cdot \frac{1}{\sigma_{time}(t)\sqrt{2\pi}} \cdot e^{-\frac{(t-t_1)^2}{2\sigma_{time}^2(t)}} \cdot dt_1 , \qquad (6.7)$$

Eq.6.7 has to be evaluated for electrons and holes separately and the two contributions are then summed to yield the total current.

6.4 MODELING RESULTS

6.4.1 SIMPLE 1D P-I-N DIODE

We have applied Eq.6.3 (Ramo's theorem with carrier drift only) and Eq.6.7 (new model including diffusion) to simple 1D p-i-n diodes. Results are reported in Fig.6.6 (diode with an intrinsic region of 600nm) and Fig.6.7 (300nm). Once again generation-recombination mechanisms have been turned off to highlight the role of drift and diffusion only.

Since the electric field is fairly constant inside the intrinsic region, in absence of diffusion the photo-current consists of two rectangular pulses corresponding to the contributions of electrons moving toward the n⁺ region and the holes moving toward the p⁺ region (curves *RAMO* (*Drift only*)). The inclusion of diffusion (curves *RAMO* (*Drift only*), Eq.6.7) makes the transitions smooth and provides a very good agreement with the time-dependent TCAD simulations, demonstrating the accuracy of the model in this simple reference case.



Figure 6.6: Current pulse due to the generation of electron-hole pairs in different regions of a p-i-n diode with an intrinsic region of 600nm at T = 300K: a) 50nm from the edge of the p⁺ region, b) in the middle of the intrinsic region, c) 50nm from the edge of the n⁺ doping region. These images have been taken from [49].



Figure 6.7: Current pulse due to the generation of electron-hole pairs in different regions of a p-i-n diode with an intrinsic region of 300nm at T = 300K: a) 50nm from the edge of the p⁺ doping region, b)50nm from the edge of the n⁺ doping region. These images have been taken from [49].

6.4.2 3D PINNED PHOTODIODE

We now apply Eq.6.7 to the template pinned photodiode of Fig.6.1 biased at $V_{bias} = 1.8V$. The temperature is T = 273K. For e-h pairs generated in regions with negligible electric field, the velocity at time t = 0 is set as $v_e = v_h = 10^6 cm/s$ with random direction at each step in order to emulate the motion of the charge cloud inside the device structure.



Figure 6.8: Trajectory of the centroid of the electron and hole charge clouds in a cross-section of the pinned photodiode of Fig.6.1. Left and right plots correspond to generation points 5 and 1 in Fig.6.2, respectively. These images have been taken from [49].

Fig.6.8 shows the trajectories of the centroid of the electron and hole clouds for generation at different positions as obtained by solving Eq.6.1. Electrons always move toward the n^+ region, while holes may be collected by the p^+ contacts on top or accumulate at the bottom of the pixel until they recombine.

Fig.6.9 reports the normalized Ramo potential $\Delta \Psi / \Delta V_{bias}$ (with $\Delta V_{bias}=0.1$ V) which varies between 1 at the n⁺ contacts and 0 at the p⁺ contacts. We see that the e-h pairs induce a significant current (Eq.6.3) only when the transport moves them next to the n⁺ regions, namely within the depletion layer.



Figure 6.9: Normalized Ramo's potential $\Delta \Psi / \Delta V_{bias}$ on a 2D cross-section of the pixel with a bias of 1.8V at T = 237K. This image has been taken from [49].

Fig.6.10 compares the current pulses obtained with Sentaurus to the ones from Eq.6.7. Sentaurus simulations have been run with and without SRH generation-recombination, showing that in the high quality substrates considered in this work ($\tau_n = 100\mu s$, $\tau_p = 10\mu s$) this mechanism has a minor impact on the result and can be neglected in the simplified model. We also see that the main features of the current pulses are captured by the model described in Sec.6.3, at least in terms of pulse duration. In contrast, the application of Ramo's theorem (without diffusion) yields current pulses very different from the Sentaurs results, see Fig.6.11. In such case, pulses are remarkably shorter in time, since the model fails to capture the slow tail of carriers that diffuse in opposite direction with respect to the drift direction. The shape of the waveforms in Fig.6.11 are consistent with the normalized Ramo's potential of Fig.6.9:



Figure 6.10: Comparison of the current pulses from Sentaurus and from Eq.6.7 in the 3D pixel considering generation at the positions 5 (left) and position 1 (right) of Fig.6.2. These images have been taken from [49].

significant current is induced only when the electrons get closer to the n⁺ regions.



Figure 6.11: Calculations without including diffusion (i.e. by using Eq.6.3 instead of Eq.6.7) for the same device and generation points of Fig.6.10, the left plot corresponds to generation in point 5 of Fig.6.2, while the right plot corresponds to point 1. These images have been taken from [49].

The convolution of the curves in Fig.6.11 with the Gaussian function described in Eq.6.7 yields a much better agreement with Sentaurus results, as seen in Fig.6.10. We verified that the residual discrepancy is partly due to the coarse sampling of the discretization mesh (a finer mesh would require an enormous amount of memory and time).

Comparison between Fig.6.10 and Fig.6.11 shows that diffusion plays a dominant role in shaping the pulse in the template pinned photodiode considered here. The simple model developed in Sec.6.3 provides an efficient and accurate way to estimate the collection time (about 15 minutes for each curve).

It is worth mentioning that our model, consistently with the TCAD, assumes that Einstein's relation holds also at high electric fields (see Eq.6.5). Recent results suggest that this is not true and that the diffusion coefficient at high electric field is indeed larger than what predicted by Einstein's relation [57]. In our model it is possible to set mobility and diffusion coefficient independently. Fig.6.12 shows that implementing the correction proposed in [57] for the electron

diffusion coefficient at high fields has a small effect on the results mainly because the electric field is not too large inside the structure.



Figure 6.12: Comparison of current pulses from Eq.6.7 in the 3D pixel considering generation at the positions 5 (left) and position 1 (right) of Fig.6.2. In this figure, the model consider different high-field behaviour for the mobility and the diffusion coefficient for electrons according to [57]. These images have been taken from [49].

Another reasonable assumption is the almost point-like generation since one could set $\sigma(0)$ as the size of the e-h packet generated by the X-ray photon [58].

The last section of this chapter will focus on the evaluation of the size of the e-h photogenerated packet through GEANT4 simulations.

6.5 MONTECARLO approach

The implemented diffusion model, where there is a temporal convolution with a gaussian shape diffusion of the RAMO associated current pulse, helps to better fit the charge pulse waveform with the one from the Sentaurus. Anyway it presents some limitations. A more realistic model, in order to obtain a better match between the two waveforms, is needed. A MONTECARLO approach has been considered.

This algorithm implements a real diffusion model where *scattering events* take place during the particle dynamic and modify the direction and velocity of the particles. Moreover, the analysis of more particles in parallel gives a more precise estimation of the diffusion contribution to the global dynamic behaviour of the charge collection.

6.5.1 Algorithm

The implemented algorithm in its 1D version is reported in fig. 6.13.

```
for p = (1:Np)
1
        for tn = (2:Nt)
2
             t = 0:
3
             x(p, tn) = x(p, tn-1);
4
             vx(p,tn) = vx(p,tn-1);
\mathbf{5}
             while (t <= dt)
6
                  rtau=-tau*log(rand(1,1)*0.9999); %duration of next FF
7
                  t=t+rtau; %next scattering event
8
                  if (t<=dt) %Diffusion section
9
                       x(p,tn) = x(p,tn) + vx(p,tn) * rtau + q * rtau^2 * F/2 / meff;
10
                       vx(p,tn) = sqrt(K*T/meff)*randn(1,1);
11
                  else %Drift section
12
                       tleft=rtau-(t-dt); %time to the end of the time step
13
                       x(p,tn) = x(p,tn) + vx(p,tn) * t left + q * t left ^2 * F/2 / meff;
14
                       vx(p,tn) = vx(p,tn) + q * F * t left / meff;
15
                  end
16
             end
17
        end
18
  end
19
```

Figure 6.13: MATLAB sub-routine implemented to emulate the drift and diffusion contributions.

The algorithm analyzes N_p particles in parallel for a number of steps N_t each of them of duration dt. At each step the *free flight time* of the particle is continuously and randomly calculated from τ for each particle until the time step has been covered. τ is expressed as:

$$\tau = \frac{\mu \cdot m_{eff}}{q} \tag{6.8}$$

where m_{eff} is the effective mass and the nominal value that have been used for electrons and hole are: $m_{eff,e} = 0.98 \cdot m_0$ and $m_{eff,h} = 0.48 \cdot m_0$ with $m_0 = 9.10938356 \cdot 10^{-31}$ kg.

In order to emulate the diffusion, after each *free flight time* a scattering event occurs so the particle changes its direction randomly and moves at thermal velocity in the new position. At the last iteration before the end of the time step duration (where several scattering event occurred) the particle moved by drift according with the field F present in that position. Electrons

and holes start to move from the same initial point and then they are treated separately. At each step the velocity and the weighted field are recorder for each particle in order to obtained the associated current through eq. 6.3.

The drift and diffusion of carriers in the random motion of the MC (MONTECARLO) algorithm have been analysed in details.

Figure 6.14 reports the comparison between the implemented drift part and the theoretical prediction accordingly with the Caughey-Thomas relation (Eq. 6.2).



Figure 6.14: Comparison between the drift component of the MC transport and the theoretical prediction accordingly with the Caughey-Thomas relation for electrons with different numbers of iterations.

Figure 6.15 compares the obtained standard deviation of the space and the linear trend consistent with the Haynes-Shockley theory.

Figure 6.16 compares the final charge space distribution with the expected theoretical gaussian distribution where the variance is predicted by the Haynes-Shockley theory.

Figures 6.17 and 6.18 show respectively the velocity of electrons and holes as function of the electric field F and compared with the expected velocity from the Drift-Diffusion model. Moreover, different effective masses have been used in order to verify their influence on the diffusion section of the algorithm. Instead, figure 6.19 and 6.20 compare the diffusion coefficient as a function of the field.



Figure 6.15: Comparison between the extracted standard deviation of the space and the linear trend consistent with the Haynes-Shockley theory for electrons with different numbers of iterations.



Figure 6.16: Comparison of the final charge space distribution with the expected theoretical gaussian distribution for electrons with different numbers of iterations.



Figure 6.17: MC (Np = 1000) obtained electrons velocity compared with the Drift-Diffusion Model with $m_{nom} = 0.98 \cdot m_0$.



Figure 6.18: MC (Np = 1000) obtained holes velocity compared with the Drift-Diffusion Model with $m_{nom} = 0.48 \cdot m_0$.



Figure 6.19: MC (Np = 1000) obtained electrons diffusion coefficient compared with the Drift-Diffusion Model with $m_{nom} = 0.98 \cdot m_0$.



Figure 6.20: MC (Np = 1000) obtained holes diffusion coefficient compared with the Drift-Diffusion Model with $m_{nom} = 0.48 \cdot m_0$.

6.5.2 Diode P-I-N 1D

The algorithm has been tested on a simple one dimensional P-I-N diode under reverse biased condition (N-type region is polarized at 5V and P-type region is set to 0V). Carriers have been generated in different points along the structure. The geometry of the structure and the different generation points are reported in fig.6.21. The corresponding outputs are reported in figures 6.22, 6.23, 6.24 and they are in good agreement with the Sentaurus TCAD. In terms of time performance, since the structure is very simple, the algorithm takes less than a minute of computation against the $\simeq 15$ minutes of the Sentaurus TCAD.



Figure 6.21: Simple P-I-N diode 1D structure The yellow stars show the different generation points. The diode is reverse biased with $V_{bias}=5V$ at 0°C.



Figure 6.22: Comparison between MC and Sentaurus waveform outputs of the device in figure 6.21. Generation point near the P-layer (Nr. 1).



Figure 6.23: Comparison between MC and Sentaurus waveform outputs of the device in figure 6.21. Generation point in the middle of the i-layer (Nr. 2).



Figure 6.24: Comparison between MC and Sentaurus waveform outputs of the device in figure 6.21. Generation point close the N-layer (Nr. 3).

6.5.3 2D Structure

Since the algorithm works fine in the 1D case, it has been tested on a more complex 2D device. This geometry, reported in fig.6.25, emulates a back-thinned pinned photo-diode with δ -doping with a N-type buried channel (N_{well}) on a p-type silicon epi-layer (Si_{epi}) with size of 12 × 5 μ m. In order to create the depletion region, the diode needs to be reverse biased so the N_{well} in polarized with 1.8V (typical value for a CMOS technology) from the top, while the p⁺-layer at the bottom is connected to 0V. The MC simulations have been performed at T = 0°C. The corresponding outputs are reported in figures 6.26, 6.27, 6.28 and they are in good agreement with the Sentaurus TCAD.







Figure 6.26: Comparison of the current waveforms between the Sentaurus and the MC model with Np=3000 when one e-h pair is generated in point 1 in the device of figure 6.25.



Figure 6.27: Comparison of the current waveforms between the Sentaurus and the MC model with Np=3000 when one e-h pair is generated in point 2 in the device of figure 6.25.



Figure 6.28: Comparison of the current waveforms between the Sentaurus and the MC model with Np=3000 when one e-h pair is generated in point 3 in the device of figure 6.25.

Since the structure is more complex, a bigger number of iteration is required to achieve a good result. In terms of time performance, the algorithm takes few minutes of computation
against almost two hours of the Sentaurus TCAD.

6.6 GEANT4 simulations

In order to evaluate the initial distribution of photo-generated e-h pairs, GEANT4[59] simulations have been performed. This simulator is based on a Monte Carlo track-structure toolkit designed for the simulation of particle transport through matter. The aim of this analysis is to evaluate the photo-generated spatial charge distribution after the absorption of the incoming photons. The entire set-up is based on the extended example TestEm5 which allows the study of the transmission, absorption and reflection of particles through a single, thin or thick, layer.

Figure 6.29 shows the simulation set-up where, inside a generic volume (blue box) with constant parameter (T=273K at 10^{-6} mbar), an incident photon beam (in green) with photons at different energies, orthogonally hits a silicon layer, which emulate the sensitive area of the detector (orange square) with $15\mu m$ of thickness.



Figure 6.29: GEANT4 simulation environment.

The *ad hoc* created subroutines allow to see and track the "primary" generated photoelectrons and observe their simulated path inside the material. While they are travelling through the silicon, they lose their energy generating all the "secondary" electrons that will compose the charge cloud. Figure 6.30 shows the photo electron generation inside the silicon layer at each iteration of the tool.

The evaluation has been done with 10000 iterations (MONTECARLO approach).

The final position of the electrons has been recorded. From this, we evaluate the distance between it and the photon beam position.

Figures 6.31, 6.32 and 6.33 show the spatial particles pattern collected at energies of 500eV, 1KeV and 1.5KeV. Fig. 6.34 compares the three collected patterns.

The results of the mean distance from the beam and its standard deviation for each energies and for the different physic libraries are reported in tables 6.1, 6.2, 6.3.



Figure 6.30: Track of the photogenerated primary electrons after the photon absorption in the silicon layer.



Figure 6.31: Spatial distribution of the primary electrons generated by incoming photons at $500 \,\mathrm{eV}$.



Figure 6.32: Spatial distribution of the primary electrons generated by incoming photons at 1 KeV.



Figure 6.33: Spatial distribution of the primary electrons generated by incoming photons at $1.5\,{\rm KeV}.$



Figure 6.34: Spatial distribution of the primary electrons generated by incoming photons at $500 \,\mathrm{eV}$, $1 \,\mathrm{KeV}$, $1.5 \,\mathrm{KeV}$.

PHYSICS	Average [nm]	Standard Deviation [nm]
Standard	2.15	0.35
Penelope	2.5	0.62
Livermore	2.3	0.45
LowEnergy	1	0.6

Table 6.1: Average and standard deviation of the electron cloud at 500eV using different physics libraries.

PHYSICS	Average [nm]	Standard Deviation [nm]
Standard	7	1.16
Penelope	7.1	1.30
Livermore	7	1.33
LowEnergy	3	1

Table 6.2: Average and standard deviation of the electron cloud at 1KeV using different physics libraries.

PHYSICS	Average [nm]	Standard Deviation [nm]
Standard	13.8	2.4
Penelope	14	2.7
Livermore	13.8	2.6
LowEnergy	5.64	2

Table 6.3: Average and standard deviation of the electron cloud at 1.5KeV using different physics libraries.

The results show that even at relative high energies (e.g. 1.5KeV) the initial spatial distribution of electrons is negligible compared with pixel size($\simeq 25\mu m$). We then can assume that a point like generation implemented in our models is in good agreement with these simulations.

Chapter 7

Conclusions

This work started with a description of the main requirements that new generation detectors have to satisfy in order to meet the challenge of biomedical and advanced material research exploiting most advanced light sources potentials.

In particular we described the tremendous challenges, in terms of frame rate, dynamic range, quantum efficiency and single photon counting capability, that detectors have to front when installed on Free Electron Lasers (FEL) machines, where the photon energy is in the range between few hundreds eV and some keV and the radiation is distributed in very intense periodic pulses.

To meet these requirements, different detection strategies have been suggested and some of them have been implemented recently. In particular, back-thinned, monolithic active pixel sensors (MAPS) based on standard CMOS technology [10],[9] are promising candidates for these applications and the main topic described in this thesis is the PERCIVAL CMOS based imager detector which adopts state of the art of this approach.

After an overview of the main stages of the PERCIVAL detector and the scientific reasons that started this international project, we focused on some of the main sections of this device. A detailed description of the pixel CMOS technology, commonly used in these kind of detector, has been given and discussed.

The development of a fundamental diagnostic device for the early stage of testing of the PERCIVAL detector, referred as **POWERBOARD**, has been reported showing the main results that this board allowed to get. In particular this device has been employed for the evaluation of the 2Mpixels sensor allowing for a very fine tuning and monitoring of all the bias and reference signals that the chip requires during tests and experimental operations.

The first complete power-up in air of the system has been performed on September 2017 at DESY and then at ELETTRA with a second identical device available in January 2018 and in this work we described the main results of these first measurements.

The expected performance of the detector have been tested on several scaled prototypes $(210 \times 160 \text{ pixels})$ and more recently on the P2M Front Side Illuminated sensor. These tests showed the achievement of the chip of all the aforementioned features as:

- Low Noise: It has been demonstrated that the system operate with a noise lower than $15e^-$ under low flux condition keeping the noise contribution of the device shot noise limited.
- **High Dynamic Range**: Thanks to the adaptive gain modulation induced by the lateral overflow mechanism, the system is able to span through several orders of magnitudes of collected charge, generated by incoming photons, still keeping a linear behaviour.
- Low Energy Sensitivity: It has been demonstrated with an experiment of a diffraction pattern from a pinhole where, thanks the thin entrance window produced by the back-

thinned process, the detector response is dominated by the beam main harmonic down to $\simeq 92 \text{eV}$ and the contribution of higher harmonics is negligible.

- High QE: Several measurements have been performed in order to evaluate the Charge Collection Efficiency (CCE, lower bound of the QE) and despite some problems of contamination of the entrance window and non-uniformity of the back thinned process, the target of a QE≥ 85% seems still compatible with the obtained results.
- High Frame Rate: The capability of the multy-Mega pixels system to acquire images has been demonstrated in air with visible light. In particular, in October 2018 at ELETTRA, with the P2M system, we were able to acquire a set of ten images at a frame rate of 150 Hz.

Among these experimental activities (hardware development and testing) where I was mainly involved, we have been able to perform several TCAD simulations on the pixel photodiode structure in order to better understand its features especially regarding the charge collection dynamic. Since time-dependent simulations on such complex structure are very time consuming, we mainly focused on an implementation of an innovative model based on RAMO's theorem and MONTECARLO that describes the particles dynamic in the substrate taking in account the drift and diffusion contributions allowing the evaluation of the photo-current waveform and the estimation of the collected charge.

This model has been applied first on very simple structure as an 1D P-I-N diode in order to evaluate its behavior and then on more complex 2D and 3D structures (representing real devices). The reported results, compared with the TCAD simulator, despite some approximations, are very promising and allow for a more time efficient numerical evaluations of the photo-current waveform and the estimation of the collected charge.

In addition some experience on CMOS based detector design and layout has been acquired during the internship at IMASENIC (Barcellona, Spain) working on a multi-Mega pixels detector suitable for X-rays medical applications. Some example of layouts developed during this period have been reported. All of them passed the DRCs (Design Rules Checks) performed by the foundry and the chip production is on going.

In conclusion, in this PhD, in addition to the obtained results and considering the entire path of a detector development, both the pure technical skills (from the design to the testing of prototypes in different facilities, simulations, etc) and the soft skills (working in an international collaborations, be part of a team and present your own work clearly), have been acquired, making this three years formative course very complete in CMOS detector development field.

Future developments

At the moment, the Front-Side-Illuminated (FSI) system is used both to test appropriate calibration and data-analysis procedures (on the basis of the algorithms that were developed for use in the prototypes). The first test with a synchrotron beam is planned at the end of year accordingly with availability of the beamline at DESY.

The Full 2Mpixel system in its Back-Side-Illuminated (BSI) version is at the moment in its post-processing phase, and is estimated to be ready for test at the begin of 2019.

When the P2M will be fully characterized and all the operational procedures will be established, a more compact review of the POWERBOARD will be developed in order to engineer the entire system and making it a commercial product.

The developed model of the charge collection dynamic still need some evaluations on more complex structures. At moment the results look promising and it could be applied for prelimi-

nary analysis of the evaluation of the photo-current waveform and estimation of the collected charge more effectively than employing commercial TCAD.

Appendix A

In 1990s, complementary metal-oxide semiconductor (**CMOS**) image sensor, where a single chip integrates the readout electronics and the sensing element in a single piece of silicon, was invented. A few years after their invention, CMOS image sensors were proposed for the detection of charged particles and are now routinely used for transmission electron microscopy and are starting to be used in particle physics as well.

Driven by the support of an increasing market, research has therefore constantly proposed novel CMOS sensor architecture that ended up increasing the performance of this emerging technology above the well radicalized CCD technology. The key feature of CMOS imagers, compared with CCDs, is the ability to integrate in the fabrication of light detector within the standard well know CMOS fabrication process.

Beside the drastic reduction of cost and time to market, this has allowed the integration of localized electronic circuitry within the sensor in what is referred as the CMOS pixel. These devices offer several advantages compared to other available technologies: they can be faster than CCDs since their architecture naturally enables massive parallelisation, the use of smaller pixels is less problematic than in hybrid systems because it does not push the limits of bump bonding technology and finally, smaller photo-diode capacitances can be achieved in CMOS compared to hybrid pixel sensors allowing lower noise levels.

The design of such devices require the use of very specific tools as CADENCE design suite, SYNOPSYS or others.

The flowchart reported in figure A.1 explains the different stages of a chip, design using these tools, starting from the desired specifications. Once the schematic circuitries have been created and tested, through several circuit numerical simulation, the layout design of the main blocks can start. After its implementation, several checks need to be validated. The first is the **Design Rules Check (DRC)**, which verifies that the physical parameter as track width, distances between tracks, vias size, metal coverage density and others are compatible with the chosen industrial process and with the constraints provided by the foundry itself. The next step is the **Layout Versus Schematic (LVS)**. This phase checks that the realized layout corresponds to the schematic circuit. In this case all the connections are verified and compared with the circuit schematic.

Once the layout has been validated, all the resulting physical parameter are required in order to re-simulate the circuit adding the parasitic variables introduced by the layout. This phase is called "Extraction" and Extracted Simulation are performed in order to verify the right behaviour of the circuit with its layout.

If all these checks pass without problems (usually several iterations are required before reach this point) the layout can be implemented in the final design and then it will be sent to the foundry for the chip realisation.



Figure A.1: Flow chart of the design process.

During the internship at IMASENIC Advance Imaging S.L. there was the opportunity to work on the layout of a 2Mpixel imager suitable for digital radiography.

A simplified scheme of the sensor is reported if fig. A.2. The chip is organized in stitching blocks which allow to scale the chip in a bigger (in terms of sensitive area) versions keeping the same layout configuration.



Figure A.2: Stitching block simplified organization of the sensor.

Some of the layout that have been created during this period are:

- Serializer: The *Output stage* block is composed by different circuits as the ADCs, LVDS transmitter and others. One of them is the serializer that is responsible to collect all the data coming from the ADCs output and organized them in the right-format (from parallel to series). After this phase, the data are ready to be sent out of the chip thorough the LVDS transmitter. The developed layout is reported in fig. A.3, A.4.
- **SPI counter**: This logic circuit is part of the *Configuration block* and it generates all the control signals fo different blocks. The developed layout is reported in fig.A.5.
- **RowDriver**: This block is responsible of generate all the signals that the pixels require to work properly accordingly with the circuit logic that is present on the *Configuration Block*. The developed layout is reported in fig. A.6.

The layout of the entire chip has been submitted to the foundry and the chip realization is on going.



Figure A.3: SERIALIZER layout.



Figure A.4: Zoom of the SERIALIZER layout.



Figure A.5: SPI COUNTER layout.



Figure A.6: ROW DRIVER layout.

Appendix B - Photon Transfer Curve (PTC)

Photon transfer was developed at JPL during the early 1970s when CCDs were first being developed by JPL where Jim Janesick, Tom Elliott and others applied it to analyzing and optimizing imagers.

The great advantage of this measuring method is the fact that no absolute measurements of any light input is needed.

The baseline Photon Transfer Curve plots noise versus signal and from the graph you can learn: Read Noise, Full Well capacity, ADC Gain, Photoresponse Non Uniformity and Dark Signal Non Uniformity[43].

In the PERCIVAL system, two main parameters are extracted from this technique. These parameters are the **ADC Gain** (or conversion gain), which is the ratio of the number of electrons to the ADU value, and the **Full Well Capacity** per pixel.

One way to obtain a PTC curve is uniformly exposed to light the sensor , while varying the exposure time. For every exposure time applied, several images are grabbed, the average value of the obtained images as well as the temporal noise on pixel level are calculated.



Figure B.1: Example of PTC on a PERCIVAL test chip at ELETTRA in December 2016.

The measured signal of the sensor can be written as :

$$S_{tot} = kN_0 + S_{off} \tag{B.1}$$

While the measured temporal noise on pixel level can be written as :

$$s_{tot}^2 = k^2 s_R^2 + s_o^2 \tag{B.2}$$

with:

- S_{tot} is the measured output signal expressed with a digital number (DN),
- k is the conversion gain (DN/e^{-}) ,
- N_0 is the number of optically generated electrons,
- S_{off} is the offset signal (DN),
- s_{tot} is the total temporal noise measured (DN),
- s_R is temporal noise associated with the readout channel e^- , also the noise floor in dark at 0 s exposure time,
- s_0 is the photo shot noise (e^-) .

Considering that the noise s0 is a shot type:

$$s_0^2 = N_0 = (S_{tot} - S_{off})/k \tag{B.3}$$

the total noise reported in Eq.B.2 can be written as :

$$s_{tot}^2 = k^2 s_R^2 + k(S_{tot} - S_{off})$$
(B.4)

The signal-to-noise ratio of the system under these assumption can be written as :

$$\frac{S_{tot}}{s_{tot}} = \frac{(S_{tot} - S_{off})}{\sqrt{k^2 s_R^2 + k(S_{tot} - S_{off})}}$$
(B.5)

The obtained measurement data can be used to create standard deviation versus average effective signal, both on a log-scale ("Mean-Standard Deviation"), as reported in fig.B.1.

In fact, in this plot we can identify two different regions:

• Just before the saturation, a linear trend with slope $\simeq 0.5$ can be recognized. In this region, the photon shot noise is the dominant noise source, and based on Eq.B.5, the signal-to-noise ratio can be simplified to:

$$\frac{S_{tot}}{s_{tot}} = \sqrt{(S_{tot} - S_{off})/k} \tag{B.6}$$

At the intersection of the linear fit with the horizontal axis, Eq. B.6 can be simplified as:

$$k = (S_{tot} - S_{off}) \quad at \quad \frac{S_{tot}}{s_{tot}} = 1 \tag{B.7}$$

where k is the **conversion gain** factor.

• At the saturation, in the right part of the plot, the signal-to-noise ratio becomes extremely large, due to the fact that the temporal noise of the sensor is reduced to almost zero by saturation of the pixels. This corresponding point in the horizontal axis define the **Full Well Capacity**.

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