Investigation of Hot Carrier Stress and Constant Voltage Stress in High-κ Si-Based TFETs

Investigation of hot carrier stress and constant voltage stress in high-κ Si-based TFETs

Lili Ding, Elena Gnani, Simone Gerardin, Marta Bagatin, Francesco Driussi, Pierpaolo Palestri, Luca Selmi, Cyrille Le Royer, and Alessandro Paccagnella

***Abstract*—This paper reports the experimental investigation of hot carrier stress (HCS) and constant voltage stress (CVS) in high-κ Si-based Tunnel FETs. For the devices in this study, due to the large injection of cold carriers and to the presence of traps in the gate dielectric, the degradation of the transfer characteristics under CVS is much more severe than under HCS. The experimental results show that the sub-threshold swing (SS) remains stable under both HCS and CVS conditions, and it is not influenced by the stress-induced increase of the interface trap density.**

***Index Terms*—Tunnel FET; Hot carrier stress; Constant voltage stress; High-κ dielectric**

I. Introduction

Tunnel field effect transistors (TFET) have attracted much attention due to their possibility to offer a sub-60 mV/dec sub-threshold swing (SS) [1], [2]. Many investigations have been carried out to improve the characteristics of TFET by modifying the device structure, introducing new materials, or improving the fabrication technology [3], [4], [5], [6], [7]. Limited attention has been paid so far to the reliability of TFETs.

Initial studies on TFET reliability were based on n-type transistors with SiO_2 gate dielectric [8], where the degradation of I-V characteristics was more severe under hot-carrier stress (HCS) than under constant voltage stress (CVS). In TFETs, HCS is due to the injection of hot carriers at the source/channel junction resulting from the strong electric field, while in conventional MOSFETs, the hot carrier injection occurs near the drain end [9]. Referring to the existing studies on MOSFETs, after replacing the gate stacks with high-κ dielectrics, the hot-carrier reliability of nMOS transistors worsens, because the oxide barrier is much lower and the trap density is higher [10]. Significant cold-carrier trapping in high-κ gate dielectric during HCS has been reported as well [11], [12].

It is thus important to study the bias stress effects on high-κ TFET devices due to both hot-carrier damage and cold-carrier trapping. In [13], bias stress measurements of high-κ TFET were performed under CVS and substantial degradation could be observed, although no comparison with the HCS condition was reported.

In this paper, the performance degradation of Si-based TFETs with high-κ dielectrics under HCS and CVS is investigated. Compared to advanced TFETs featuring e.g., source dopant pocket [14] or small band-gap materials [3], [4], the all-silicon TFETs presented here exhibit modest performance in terms of on-current and sub-threshold swing. However, for the purpose of studying the reliability appraisal of HCS and CVS of TFETs with high-κ dielectrics, the comparative degradation in all-silicon TFETs can provide us new insights on the cold carrier trapping and hot carrier injection, which can be useful to understand TFETs with different structures or materials as well.

This paper is organized as follows. Section II presents the device structure and the measurement setup. Charge pumping tests are performed to evaluate the density of interface states (N_{it}). In addition, pulsed I-V measurements which can suppress trap-assisted tunneling (TAT) are carried out to evaluate the influence of stress on band-to-band tunneling (BTBT) [15], [16]. The degradation of Si-based TFETs under HCS and CVS are investigated and discussed in Section III. Conclusions are drawn in Section IV.

II. Device and experiment description

Si-based TFETs were fabricated by CEA/LETI, France, using a 100 nm fully depleted SOI-CMOS compatible process flow (see Fig. 1(a)). The gate dielectric is a 3 nm HfO_2 layer. Additional details of the device processing can be found in [4]. We have applied stress with time ranging from 10 to 10,000 s, performing either HCS (V_g=V_d=2.5 V, V_s=0 V) or CVS (V_g=2.5 V, V_d=V_s=0 V) (see the energy bands in Fig. 1(b)). Alternated to stress, both DC and pulsed I-V measurements have been performed at room temperature to study the influence of stress on the I-V characteristics.

In fact, although the working principle of TFETs is based on BTBT, TAT will inevitably contribute to the total drain-source current. As illustrated in Fig. 1(c), TAT is activated by the traps with energy levels located in the forbidden Si bandgap, and consists of the electrons coming from the valence band in the source that get trapped in the forbidden bandgap and then are re-emitted to the conduction band of the channel [17]. With V_d=1 V and source grounded, the gate was pulsed at 10 kHz and 500 kHz with a 100 ns edge time and a 50% pulse duty cycle. The base voltage of the gate pulse was 0 V, whereas

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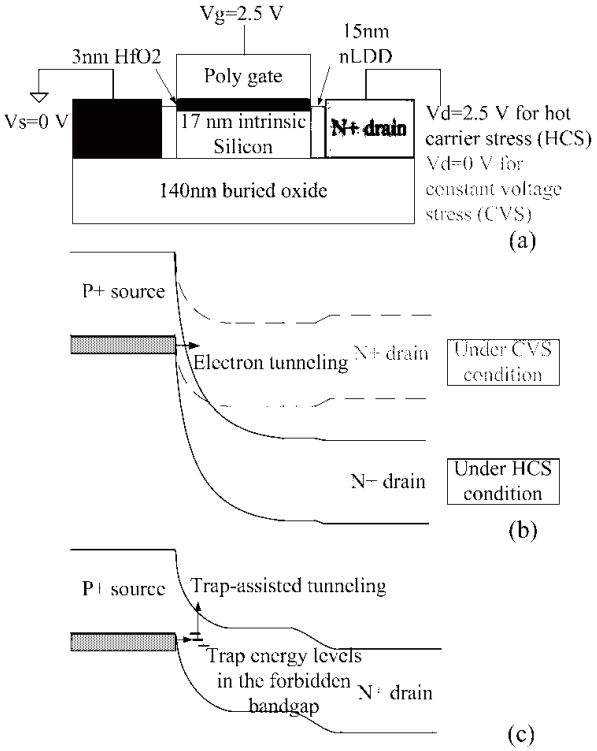

Fig. 1. (a) Schematic device structure of n-type TFETs and bias setups for HCS and CVS; (b) Schematic energy bands corresponding to HCS (black solid lines) and CVS (red dashed lines) conditions. Under HCS, high BTBT generation takes place; (c) Schematic representation of trap-assisted tunneling processes at low V_{gs}.

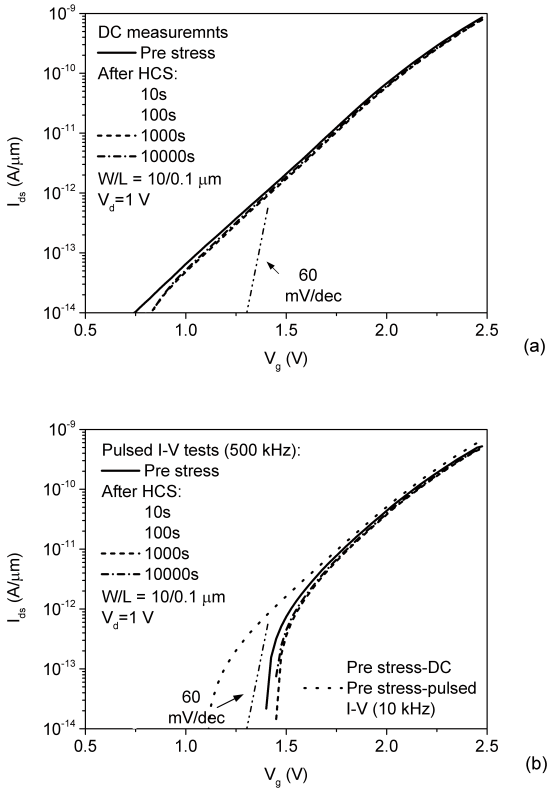

Fig. 2. Transfer characteristics of a 10/0.1 μm TFET before and after HCS: (a) DC; (b) 500 kHz pulsed I-V measurements and transfer curves of fresh TFET corresponding to DC and 10 kHz pulsed I-V.

the amplitude voltage was swept from 0 to 2.5 V. At every data point, the measurements were repeated 5 times to output an average value. The whole process is expected to take more than 1 μs [18]. TAT is expected to be substantially suppressed at high pulse frequency and BTBT can be better detected since it is no longer masked by TAT [15], [16].

The TFETs are floating-body SOI devices in this study, so the feasibility of performing change pumping measurements should be evaluated first [19]. When pulsing the gate with a squared waveform of constant base level and amplitude, the drain and source were maintained at the same potential that was swept across a suitably chosen range from 0 to 1.5 V, in order to activate the generation-recombination process at the Si/gate dielectrics interface. The current measured at the P+ source contact was found to be proportional to the frequency of the gate pulses, proving the correctness of the charge pumping setup [20], [21]. Thus, even in the absence of the body contact in our SOI-based TFETs, since the source and drain feature opposite doping type, we could still perform charge pumping measurements to evaluate N_{it}. For the charge pumping results presented below, the gate was driven with a 500 kHz square waveform with the edge time of 100 ns, the amplitude of 1.5 V, the base level of 0 V and a pulse duty cycle of 50%.

In this study, TFETs with different geometries have been characterized and consistent trends and similar absolute values of the degradation have been observed. Thus, in the following discussions, only the results of a few typical TFETs are presented.

III. Results and Discussion

A. Hot carrier stress

The transfer characteristics of a 10/0.1 μm TFET before and after different time steps of HCS are shown in Fig. 2. In this study, two V_{gs} at different drain currents are chosen as the indicators to illustrate the characteristics shift during stress, they are $V_{th,1}$ (V_{gs} at I_{ds}=2 pA/μm) and $V_{th,2}$ (V_{gs} at I_{ds}=0.2 nA/μm). Fig. 2(a) shows the results from DC measurements, where only a small shift of the characteristics within 40 mV can be observed. Fig. 2(b) shows the results of the 500 kHz pulsed I-V tests. The comparison between the transfer characteristics of the fresh TFET with DC and 10 kHz pulsed I-V tests are presented, too. It can be seen that TAT is substantially suppressed at 500 kHz: the sub-threshold characteristics are much steeper than in DC. Indeed, the actual BTBT current is no longer masked by the TAT-induced leakage current. The values of $\Delta V_{th,1}$ and $\Delta V_{th,2}$ obtained from the DC and the pulsed I-V tests are extracted and shown in Fig. 3. The shifts of the pulsed I-V curves are similar to the DC case. Fig. 2 also shows that the shifts of characteristics increase at the first stage, but then decrease at longer stress time (>100 s), where the trend can be observed also at other samples under HCS stress. In [22], similar trend was reported in nMOSFETs due to HCS which was called

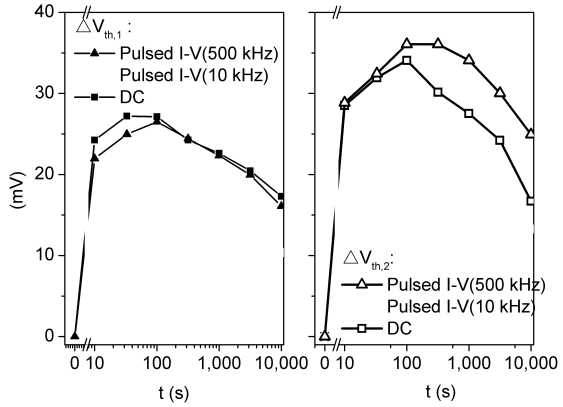

Fig. 3. Experimental values of $\Delta V_{th,1}$ and $\Delta V_{th,2}$ after HCS extracted from DC, 10 kHz, and 500 kHz pulsed I-V characteristics (see Fig. 2).

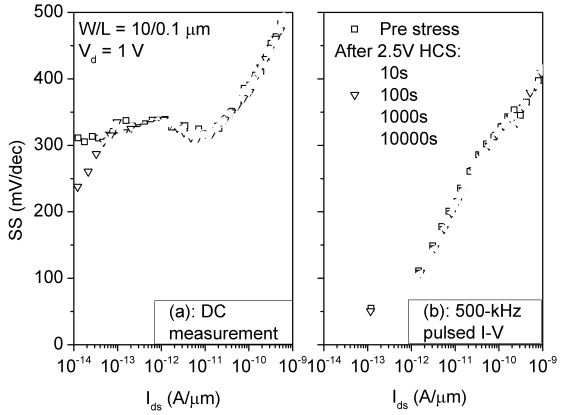

Fig. 4. Subthreshold swing of the TFET before and after HCS, as a function of I_{ds}: (a) DC; (b) 500 kHz pulsed I-V measurements.

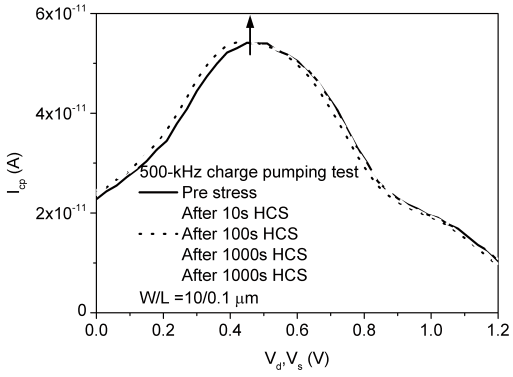

Fig. 5. Charge pumping current as a function of the drain and source voltages (V_d=V_s) before and after HCS up to 10000 s.

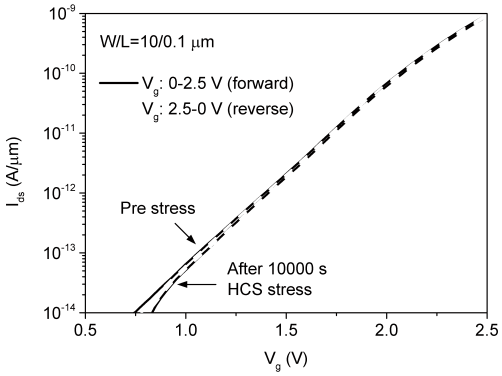

Fig. 6. Transfer characteristics of the TFET before and after 10000 s HCS stress using forward and reverse sweeps: negligible hysteresis can be observed.

"threshold voltage turn-around effect" and attributed to the secondary holes generated by impact ionization due to hot electrons. In this study, the research object is TFET instead of MOSFET, but the impact ionization is even more highlighted [8]. Thus, the induce of secondary carriers and the following buildup of the localized interface traps are also reasonable. The secondary holes-induced localized interface traps have opposite impacts on the characteristics with electrons-induced oxide charge, which is the possible explanation of the shifts evolution during stress.

The corresponding SS as a function of the drain current is shown in Fig. 4. The SS values extracted from DC are much larger than the 60 mV/dec for both fresh and stressed TFET (see Fig. 4(a)). After HCS, a slight improvement in SS was observed in the very low drain current region ($I_{ds} < 10^{-13}$ A/μm). On the other hand, SS in 500 kHz pulsed curves is smaller than 60 mV/dec at low drain current (see Fig. 4(b)), consistently with the findings in [16] where the SS from pulsed measurements is lower than from DC measurements. From the characteristics in Fig. 2(b), we can observe the small improvement in SS from the 500 kHz I-V curves. However, due to the steepness and the limited data points at the low current region from 500 kHz I-V test, this small improvement is not visible from Fig. 4(b) where SS is reported as a function of I_{ds}.

Therefore, based on the discussions above, the small improvement of SS in the DC curves appears to be due to the impact of HCS on TAT, not on BTBT. Generally speaking, in this study, the TFET SS is robust to HCS and this may be due to the limited hot electrons density under HCS (I_{ds} is about 1 nA/μm).

During the HCS, the peak value of charge pumping current $I_{cp,max}$ increased progressively, suggesting an increase in N_{it} (see Fig. 5), which is estimated as:

$$N_{it} = I_{cp,max}/(f \cdot q \cdot A_g) \quad (1)$$

where f is the pulse frequency, q is the unit charge, and A_g is the gate area [23].

After 10000 s HCS, N_{it} increases from 6.8×10^{10} cm^{-2} to 7.2×10^{10} cm^{-2}. It's worth noting that this is the average value of N_{it} instead of the the peak density for the localized interface traps. Correspondingly, Fig. 6 shows the transfer characteristics for both forward and reverse quasi-static sweeps. For the V_g swept from 0 V to 2.5 V, the electron filling factor of interface traps is inclined to be lower than for V_g swept from

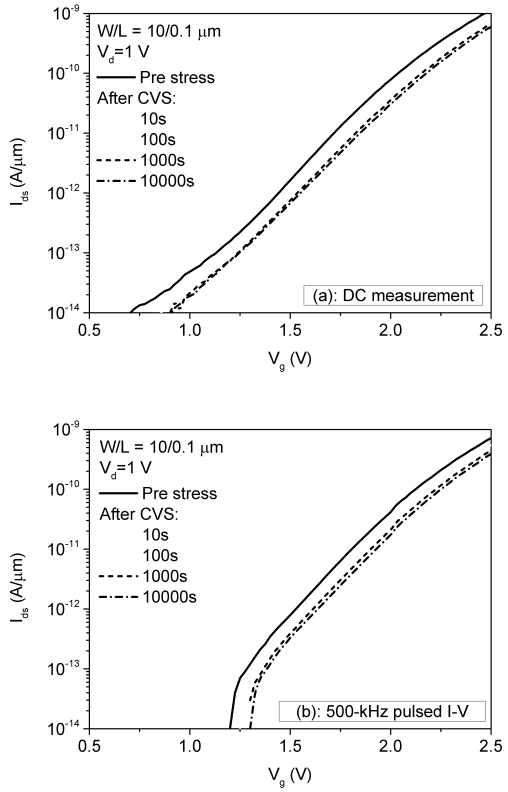

Fig. 7. Transfer characteristics of a 10/0.1 μm TFET before and after CVS: (a) DC; (b) 500 kHz pulsed I-V measurements.

2.5 V to 0 V [8], which makes hysteresis an indicator for interface traps. The negligible hysteresis after 10000 s HCS suggests that the influence of the interface trap, even after they increase due to stress, is very limited.

B. Constant voltage stress

The transfer characteristics of a TFET before and after CVS are reported in Fig. 7. The shifts of the curves are quite visible. From Fig. 8, the increases in $V_{th,1}$ and $V_{th,2}$ extracted from DC, 10 kHz, and 500 kHz pulsed I-V are similar, suggesting that the degradation in the transfer characteristics is mainly due to the oxide trapped charge and/or increase in N_{it}. The increase in both $V_{th,1}$ and $V_{th,2}$ are more evident than under HCS.

Concerning N_{it}, the charge pumping currents before and after CVS are presented in Fig. 9. Under CVS, there is a significant voltage shift between the I_{cp} curves related to the fresh and stressed device. By considering the increases of $V_{th,1}$ and $V_{th,2}$ due to CVS, and by shifting the I_{cp} curves after stress by the same $\triangle V_1$, the stressed curve almost overlap with the fresh one. N_{it} increases by 6×10^9 cm^{-2} (from 4.0×10^{10} cm^{-2} to 4.6×10^{10} cm^{-2}), a value comparable with that found after HCS. Fig. 10 presents the transfer characteristics before and after 10000 s CVS using forward and reverse sweeps, where negligible hysteresis can be observed, suggesting again the limited contribution of interface traps.

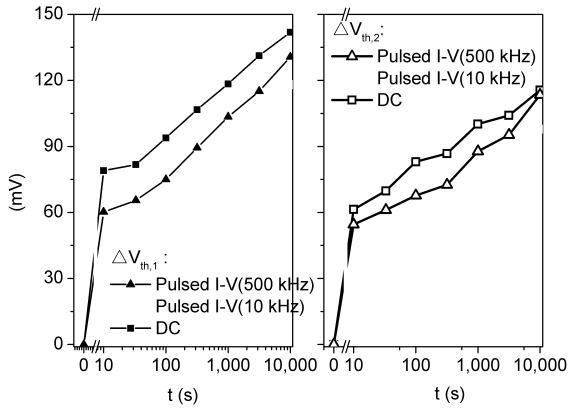

Fig. 8. Experimental values of $\Delta V_{th,1}$ and $\Delta V_{th,2}$ after 2.5 V CVS extracted from DC, 10 kHz, and 500 kHz pulsed I-V measurements.

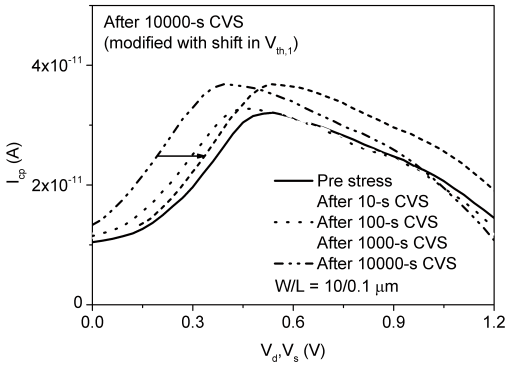

Fig. 9. Charge pumping current as a function of the drain and source voltages (V_d=V_s) before and after 2.5 V CVS up to 10000 s. The purple short-dash curve is the 10000 s CVS curve (purple dash-dot-dot curve) shifted by the $\triangle V_{th}$ obtained from the DC measurements.

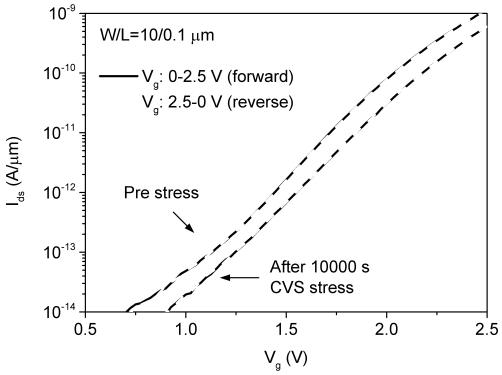

Fig. 10. Transfer characteristics of the TFET before and after 10000 s CVS stress using forward and reverse sweeps: negligible hysteresis can be observed.

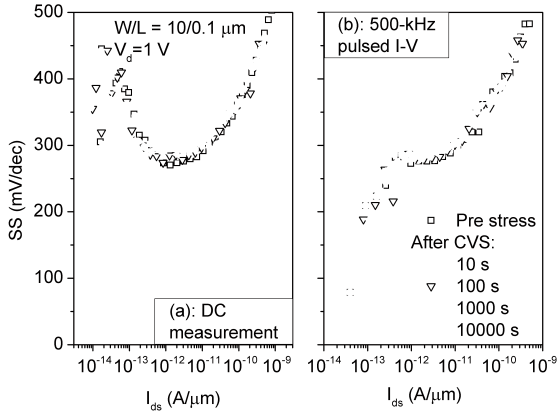

Fig. 11. SS of the TFET before and after CVS, as a function of I_{ds}: (a) from DC; (b) from 500 kHz pulsed I-V measurements.

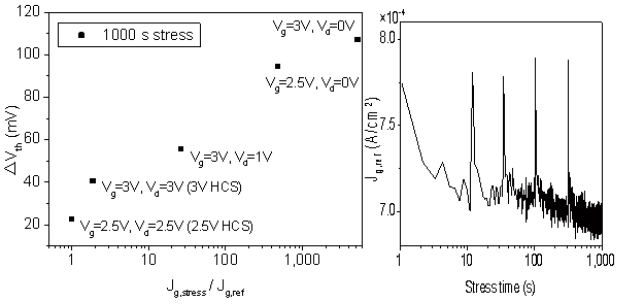

Fig. 12. Left: Threshold voltage shift as a function of the normalized gate current density during stress ($J_{g,stress}/J_{g,ref}$), where $J_{g,ref}$ corresponds to 2.5 V HCS; Right: Gate leakage density during HCS stress test (2.5 V).

Therefore, $\triangle V_{th}$ should be attributed to the negative trapped charge in the gate oxide, deriving from the trapping of hot and/or cold electrons. The electric field near the source/channel junction is stronger under HCS than under CVS (see Fig. 1(b)). Hence, hot electrons trapping more likely occurs under HCS.

Fig. 11 presents SS as a function of the drain current. After including the influence of statistical errors, we do not see any clear dependence of SS on the stress time, for both DC and pulsed I-V measurements.

C. Discussion

From the results above, the degradation in the transfer characteristics is more severe under CVS than under HCS. Referring to [24], under HCS, the hot electrons are accelerated by the longitudinal field component parallel to the channel direction and injected close to the source/channel junction. However, under CVS, the degradation is mainly due to the cold electron injection determined by the vertical field component perpendicular to the channel surface. The V_{th} increase in both DC and pulsed I-V measurements indicates the buildup of negative charge in the oxide, and the trapping of cold electrons plays an important part in the stress effects of the high-κ Si-based TFET.

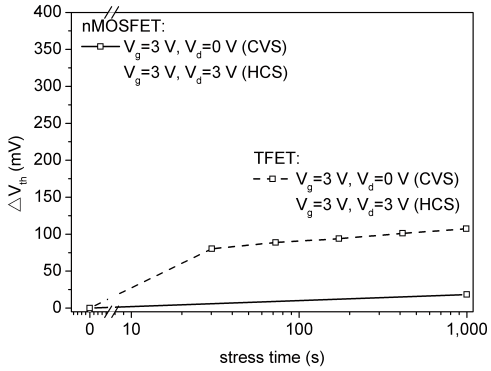

Fig. 13. Comparison of the threshold voltage shift (ΔV_{th}) for the TFET and the nMOSFET, measured as a function of the stress time under 3 V CVS and 3 V HCS conditions.

To understand the relationship between the stress-induced degradation and cold electrons injection, several different bias conditions during stress were chosen for comparison. Fig. 12 presents ΔV_{th} after 1000 s stress as a function of the normalized gate current density during stress ($J_{g,stress}/J_{g,ref}$), where $J_{g,ref}$ corresponds to 2.5 V HCS. The gate current is fairly constant during the stress experiments (see Fig. 12). It can be seen clearly that more gate leakage during stress induces a stronger degradation, proving that the main factor of inducing the shifts in characteristics should be the trapping of cold electrons. No direct evidence of hot carriers injection can be observed in the results of degradation under 2.5 V HCS. Although the degradation under 3 V HCS is stronger than that under 2.5 V HCS, since the cold electrons injection becomes larger, it is hard to attribute that to the hot carrier injection.

Since it was not possible to further increase the voltage during HCS without possible breakdown, nMOS transistors fabricated with the same process were analyzed in this study, to help evaluating the damage due to hot carriers injection.

Fig. 13 reports ΔV_{th} as a function of the stress time for both TFETs and MOSFETs. Under 3 V CVS, a smaller ΔV_{th} could be observed for the nMOSFET due to a weaker cold electrons injection, which is proved by the fact that $J_{g,stress}$ of the nMOSFET was half that of the TFET under 3 V CVS. For nMOSFETs, ΔV_{th} under 3 V HCS is larger than that under 3 V CVS, suggesting a big contribution of hot carriers injection. Furthermore, under 3 V HCS, ΔV_{th} of the nMOSFET is much larger than the value of the TFET (370 mV and 40 mV respectively, after a stress of 1000 s). This difference suggests a much stronger hot carriers injection for the nMOSFET.

In this study, the on-state current of TFET is very small (about 1 nA/μm). TFETs with larger on-state current per unit width, hence larger hot carrier fluxes, may actually exhibit more prominent hot carrier degradation.

Since SS is a very important performance indicator of TFET, the evolution of SS under stress tests should be further investigated. In this study, the increases in interface trap density are not very large under both HCS and CVS. To investigate the influence of larger $\triangle N_{it}$ on SS, the degradation of a 10/0.2 μm p-type TFET under negative CVS (V_g=-2.5 V,

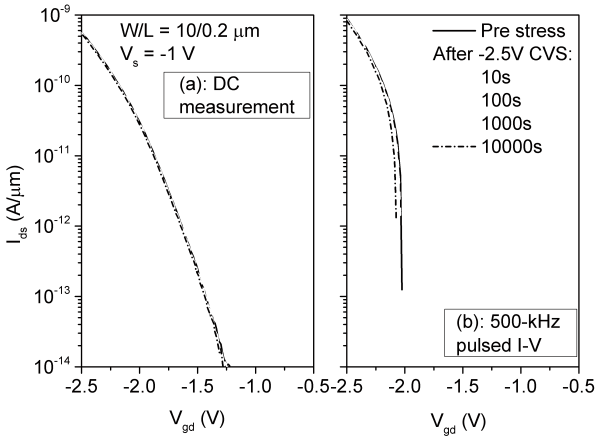

Fig. 14. Transfer characteristics of the p-type TFET before and after -2.5 V CVS: (a) from DC; (b) from 500 kHz pulsed I-V measurements.

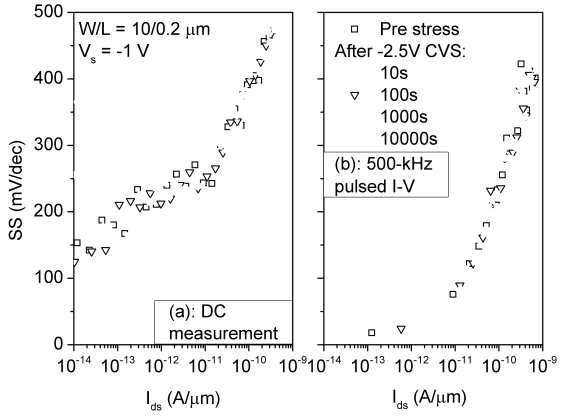

Fig. 15. SS of the p-type TFET before and after -2.5 V CVS, as a function of I_{ds}: (a) from DC; (b) from 500 kHz pulsed I-V measurements.

V_d=V_s=0 V) was investigated. The value of N_{it} increased from 1.0×10^{11} cm^{-2} to 1.3×10^{11} cm^{-2} ($\triangle N_{it}=3\times10^{10}$ cm^{-2}, whereas $\triangle N_{it}=4\times10^{9}$ cm^{-2} for the n-type TFET under HCS condition). Although the increase in N_{it} was larger, there was no visible degradation in the transfer characteristics (see Fig. 14) and no change in the SS-I_{ds} characteristics (see Fig. 15). However, in our previous study, radiation effects of TFETs exposed to 10-keV X-ray have been investigated, and an SS increase could be observed at $\triangle N_{it}=2\times10^{11}$ cm^{-2} [25]. These findings suggest that N_{it} increase may change TFET SS region, but the electrical stress-induced limited N_{it} increase is too small to induce visible changes.

IV. Conclusion

The effects of HCS and CVS on high-κ Si-based TFETs have been investigated. The bias stress effects in TFETs with high-κ gate dielectrics are different from conventional MOSFETs and TFETs with SiO_2 gate dielectrics.

In this study, the degradation of the TFET transfer characteristics under CVS is much more severe than under HCS, due to the strong injection of cold carriers overwhelming the hot carriers injection. This conclusion is different from that in [4], where more severe degradation was observed under HCS for TFETs with SiO_2 gate dielectrics, suggesting more traps existing in high-κ dielectrics. Meanwhile, this is also due to the small on-state current of the TFET in this study. If the on-state current would be significantly increased, a strong degradation of TFET might be observed under HCS.

No increase in SS has been observed under both HCS and CVS, meaning that the SS behavior is not appreciably influenced by the limited stress-induced increase in N_{it}.

V. Acknowledgement

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References

[1] A. M. Ionescu and H. Riel, "Tunnel filed-effect transistors as energy-efficient electronic switches," *Nature*, vol. 479, pp. 329–337, 2011.

[2] H. Lu and A. Seabaugh, "Tunnel field-effect transistors: State-of-the-art," *IEEE Journal of the Electron Devices Society*, vol. 2, no. 4, pp. 44–49, 2014.

[3] E. H. Toh, G. H. Wang, L. Chan, G. Samudra, and Y. Yeo, "Device physics and guiding principles for the design of double-gate tunneling field effect transistor with silicon-germanium source heterojunction," *Applied Physics Letters*, vol. 91, pp. 243 505–243 505–3, 2007.

[4] F. Mayer, C. L. Royer, J. Damlencourt, K. Romanjek, F. Andrieu, C. Tabone, B. Previtali, and S. Deleonibus, "Impact of SOI, Si1-xGexOI and GeOI substrates on CMOS compatible Tunnel FET performance," in *International Electrons Devices meeting*, San Francisco, CA, 2008, pp. 4.4.1–4.4.4.

[5] A. Villalon, C. L. Royer, M. Casse, D. Cooper, B. Previtali, C. Tabone, J. Hartmann, P. Perreau, P. Rivallin, J. Damlencourt, F. Allain, F. Andrieu, O. Weber, O. Faynot, and T. Poiroux, "Strained tunnel FETs with record ION: first demonstration of ETSOI TFETs with SiGe channel and RSD," pp. 49–50, 2012.

[6] G. Dewey, B. Chu-Kung, J. Boardman, J. M. Fastenau, J. Kavalieros, R. Kotlyar, W. K. Liu, D. Lubyshev, M. Metz, N. Mukherjee, P. Oakey, R. Pillarisetty, M. Radosavljevic, H. W. Then, and R. Chau, "Fabrication, characterization, and physics of IIICV heterojunction tunneling field effect transistors (H-TFET) for steep sub-threshold swing," pp. 33.6.1–33.6.4, 2011.

[7] D. K. Mohata, R. Bijesh, S. Mujumdar, C. Eaton, R. Engel-Herbert, T. Mayer, V. Narayanan, J. M. Fastenau, D. Loubychev, A. K. Liu, and S. Datta, "Demonstration of MOSFET-like on-current performance in arsenide/antimonide tunnel FETs with staggered hetero-junctions for 300mV logic applications," pp. 33.5.1–33.5.4, 2011.

[8] X. Y. Huang, G. F. Jiao, W. Cao, H. Y. Yu, Z. X. Chen, N. Singh, G. Q. Lo, D. L. Kwong, and M. F. Li, "Effect of interface traps and oxide charge on drain current degradation in Tunneling Field-Effect transistors," *IEEE Electron Device Letters*, vol. 31, no. 8, pp. 779–781, 2010.

[9] D. Vuillaume, A. Bravaix, and D. Goguenheim, "Hot-carrier injections in SiO2," *Microelectronics Reliability*, vol. 38, no. 1, pp. 7–22, 1998.

[10] H. Park, R. Choi, B. H. Lee, S. C. Song, M. Chang, C. D. Young, G. Bersuker, J. C. Lee, and H. Hwang, "Decoupling of cold-carriers effects in hot-carrrier reliablity assessment of HfO2 gated nmosfets," *IEEE Electron Device Letters*, vol. 27, no. 8, pp. 662–664, 2006.

[11] M. Takayanagi, T. Watanabe, R. Iijima, K. Ishimaru, and Y. Tsunashima, "Investigation of hot carrier effects in n-MISFETs with HfSiON gate dielectric," in *IEEE International Reliability Physics Symposium*, Phoenix, USA, 2004, pp. 13–17.

[12] J. H. Sim, B. H. Lee, S. C. Song, C. D. Young, R. Choi, H. R. Harris, and G. Bersuker, "Comparison of hot carrier stress and constant voltage stress in Hf-silicate NMOS transistors with Poly and TiN gate stack," in *IEEE International Reliability Physics Symposium*, San Jose, USA, 2005, pp. 638–639.

[13] A. M. Walke, A. Vandooren, B. Kaczer, A. S. Verhulst, R. Rooyackers, E. Simoen, M. M. Heyns, V. R. Rao, G. Groeseneken, N. Collaert, and A. V. Thean, "Part II: Investigation of subthreshold swing in line Tunnel FETs using bias stress measurements," *IEEE Transactions on Electron Devices*, vol. 60, no. 12, pp. 4065–4072, 2013.

[14] H. Chang, B. Adams, P. Chien, J. Li, and J. C. S. Woo, "Improved subthreshold and output characteristics of source-pocket Si Tunnel FET by the application of laser annealing," *IEEE Transactions on Electron Devices*, vol. 60, no. 1, pp. 92–96, 2013.

[15] A. Vandooren, D. Leonelli, R. Rooyackers, A. Hikavyy, K. Devriendt, M. Demand, R. Loo, G. Groeseneken, and C. Huyghebaert, "Analysis of trap-assisted tunneling in vertical Si homo-junction and SiGe hetero-junction Tunnel-FETs," *Solid-State Electronics*, vol. 83, pp. 50–55, 2013.

[16] L. Knoll, Q. T. Zhao, A. Nichau, S. Richter, G. V. Luong, S. Trellenkamp, A. Schafer, L. Selmi, K. K. Bourdelle, and S. Mantl, "Demonstration of improved transient response of inverters with steep slope strained Si NW TFETs by reduction of TAT with pulsed I-V and NV scaling," in *International Electrons Devices meeting*, Washington DC, USA, 2013, pp. 4.4.1–4.4.4.

[17] M. Baudrit and C. Algora, "Tunnel diode modeling, including nonlocal trap-assisted tunneling: a focus on iii-v multijunction solar cell simulation," *IEEE Transactions on Electron Devices*, vol. 57, no. 10, pp. 2564–2571, 2010.

[18] A. Gehring, *Simulation of Tunneling in Semiconductor Devices*. Technical University of Vienna: Ph. D's dissertation, 2003.

[19] E. X. Zhang, D. M. Fleetwood, S. A. Francis, C. X. Zhang, F. E. Mamouni, and R. D. Schrimpf, "Charge pumping and DCIV currents in SOI FinFETs," *Solid-State Electronics*, vol. 78, pp. 75–79, 2012.

[20] B. Tang, W. Zhang, M. Toledano-Luque, J. F. Zhang, R. Degraeve, Z. Ji, A. Arreghini, G. V. D. Bosch, and J. V. Houdt, "Experimental evidence toward understanding charge pumping signals in 3-D devices with Poly-Si channel," *IEEE Transactions on Electron Devices*, vol. 61, no. 5, pp. 1501–1507, 2004.

[21] C. Dou, T. Shoji, K. Nakajima, K. Kakushima, P. Ahmet, Y. Kataoka, A. Nishiyama, N. Sugii, H. Wakabayashi, K. Tsutsui, K. Natori, and H. Iwai, "Characterization of interface state density of three-dimensional Si nanostructure by charge pumping measurement," *Microelectronics Reliability*, vol. 54, pp. 725–729, 2014.

[22] I. Starkov, H. Enichlmair, S. Tyaginov, and T. Grasser, "Analysis of the threshold voltage turn-around effect in high-voltage n-MOSFETs due to hot-carrier stress," pp. XT.7.1–XT.7.6, 2012.

[23] K. Martens, B. Kaczer, T. Grasser, B. D. Jaeger, M. Meuris, H. E. Maes, and G. Groeseneken, "Applicability of charge pumping on germanium MOSFETs," *IEEE Transactions on Electron Devices*, vol. 29, no. 12, pp. 1364–1366, 2008.

[24] G. F. Jiao, Z. X. Chen, H. Y. Yu, X. Y. Huang, D. M. Huang, N. Singh, G. Q. Lo, D. L. Kwong, and M. F. Li, "New degradation mechanisms and reliability performance in Tunneling Field Effect Transistors," pp. 741–744, 2009.

[25] L. Ding, E. Gnani, S. Gerardin, M. Bagatin, P. Palestri, F. Driussi, L. Selmi, C. L. Royer, and A. Paccagnella, "Total ionizing dose effects in Si-based Tunnel FETs," in *IEEE Nuclear and Space Radiation Effects Conference*, Paris, France, 2014.