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Ferroelectric based FETs and synaptic devices for highly energy efficient computational technologies

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I. ABSTRACT

The technological exploitation of ferroelectricity in CMOS electron devices offers new design opportunities, but also significant challenges from an integration, optimization and modelling perspective. We here revisit the working principle and the modelling of some novel ferroelectric based devices, with an emphasis on energy efficiency and on applications to new computational paradigms.

Keywords: Negative Capacitance, Ferroelectric Tunneling Junctions, Ferroelectric FETs, Neuromorphic Computing.

II. INTRODUCTION

The slowing down of the CMOS geometrical scaling has steered the research in electron devices for computing applications to new functionalities for innovative computational paradigms and to the energy efficiency. The energy dissipation in CMOS digital circuits can be improved by an aggressive V_{DD} scaling that, however, is hampered by the requirement of a large ratio $[I_{on}/I_{off}]$. This led to the quest for transistors featuring a room temperature subthreshold swing below 60mV/dec [1]–[5], and thus capable of improving $[I_{on}/I_{off}]$ in near-threshold or sub-threshold circuits. At the same time, the rise of artificial intelligence has emphasized the need for hardware platforms conceived for new computational paradigms, such as crossbar arrays for artificial deep neural networks [6], and new hybrid memristive-CMOS circuits for spike-based neuromorphic processors [7], [8].

The discovery of a robust ferroelectricity in hafnium oxides opened exciting perspectives for a exploitation of ferroelectric materials in CMOS technologies [9], [10], with prospective applications including negative capacitance transistors, non volatile memories and memristors [11], [12].

In this paper we review a few selected topics from this exciting research field.

III. CORRELATED DOMAIN DYNAMICS AND NEGATIVE CAPACITANCE OPERATION

The negative capacitance (NC) operation of ferroelectric materials and devices has been originally proposed based on a homogeneous Landau theory [1], and for a Metal-Ferroelectric-Insulator-Metal (MFIM) capacitor sketched in Fig.1(a). In such a single domain picture a NC stabilization condition can be derived as $(C_D + C_F) < 1/(2|\alpha|t_F)$ [13], [15], where α is the anisotropy constant of the polarization (P) term in the ferroelectric dynamic equations, and $C_D = \epsilon_0 \epsilon_D / t_D$, $C_F = \epsilon_0 \epsilon_F / t_F$,

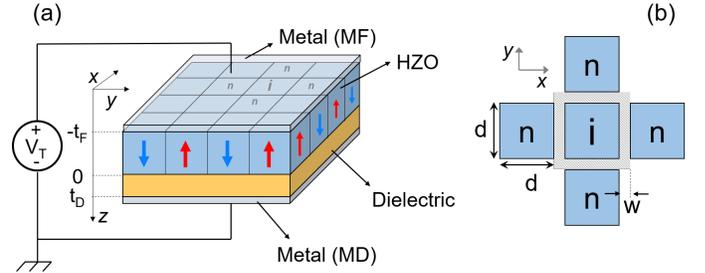


Fig. 1: (a) Sketch of a MFIM capacitor used as template device for simulations of both NC operation in Sec.III, and FTJs in Sec.IV. MF , MD are the electrodes contacting respectively the ferroelectric and the dielectric, and t_F , t_D are the ferroelectric and dielectric thickness. (b) Sketch of the ferroelectric domains, where d and w are respectively the side of the square domains and the width of the domain-wall region entering the LGD equations [15]. In this work we used $d=5$ nm and $w/d=0.1$.

with t_D , ϵ_D , t_F , ϵ_F being the thickness and relative permittivity of the dielectric and ferroelectric materials, respectively.

A more thorough investigation based on the multi-domain Landau, Ginzburg, Devonshire (LGD) theory has recently pointed out that the coupling constant k of the domain wall energy has an important influence on the NC stabilization [13], [14] (see Fig.1), and a k dependent stability condition was derived in [15], [16].

From an experimental standpoint, NC observations have been first reported for ferroelectric films connected in series to an external resistance [17], [18], then discussed for steep slope FETs [19]–[21], and more recently assessed in Metal-Ferroelectric-Insulator-Metal (MFIM) capacitors [22], [23].

From the standpoint of the multi-domain LGD equations, the NC behaviour corresponds to a strongly correlated domain dynamics as illustrated by the simulations reported in Fig.2 and obtained with the modelling approach discussed in [15], [16]. For a relatively large domain wall coupling constant $k=2 \cdot 10^{-9}$ m³/F, the trajectories for all domains are tightly correlated, whereas for a smaller k we see that the switching occurs via a domain nucleation process.

Figure 3 reports the domain averaged voltage drop, $V_{D,AV}$, for the k values used in Fig.2. The correlated switching process results in a hysteresis free NC behavior and, during the V_T ramp, $V_{D,AV}$ increase faster than V_T itself, thus leading to a larger than one voltage gain $[\partial V_{D,AV} / \partial V_T]$, which is the original idea behind the NC exploitation in nanoscale FETs [1].

The possible advantages of a ferroelectric NC operation have been investigated up to a full-chip level and in a high

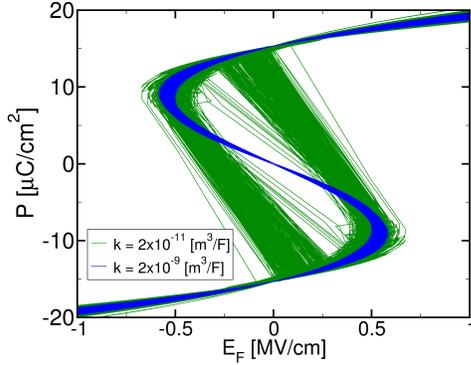


Fig. 2: Simulated spontaneous polarization versus ferroelectric field of each individual domain in an $\text{Hf}_{0.5}\text{Zr}_{0.5}\text{O}_2\text{-Ta}_2\text{O}_5$ MFIM structure. Simulation parameters are $\epsilon_F = 33$, $\epsilon_D = 23.5$, $t_F = 11.6 \text{ nm}$, $t_D = 13.5 \text{ nm}$, $\alpha = -4.6 \cdot 10^8 \text{ m/F}$, $\beta = 9.8 \cdot 10^9 \text{ m}^5/\text{C}^2/\text{F}$ and $\gamma = 0$, that provide good agreement with experiments of [23]. The simulated device has $n_D = 20 \times 20$ domains.

quality industrial technology [24]. While the benefits of the NC operation on the sub-threshold characteristics of actual transistors seem only modest, design studies for NC transistors are still being actively reported [25]–[27].

IV. POLARIZATION DEPENDENT TUNELLING IN FTJs

Ferroelectric Tunneling Junctions (FTJs) are promising candidates as highly energy efficient memristors, in fact the polarization switching is an ultra low energy mechanism to enable the potentiation and depression and, moreover, the readout impedance is very large. The originally proposed FTJ relies on a metal-ferroelectric-metal (MFM) junction [28], whose band diagram is sketched in Fig.4(a). The metal electrodes must have different screening lengths, λ_1 and λ_2 , to obtain a polarization dependent tunnelling.

The MFIM architecture sketched in Fig.4(b), instead, separates the switching element and the tunnelling oxide, and an experimental demonstration of a Back-End-Of-Line (BEOL), four level FTJ memristor has been recently reported in [29].

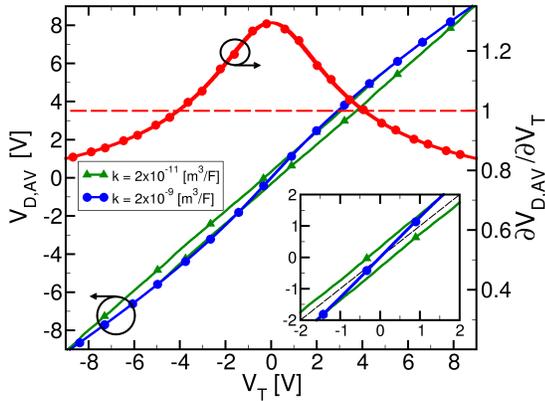


Fig. 3: Voltage enhancement across the thin insulator in NC condition (blue line), compared to the hysteretic one (green line), versus applied external voltage (same simulations reported also in Fig.2). The NC condition allows a voltage gain (red line) greater than 1 across the central V_T region, between -4V and 4V .

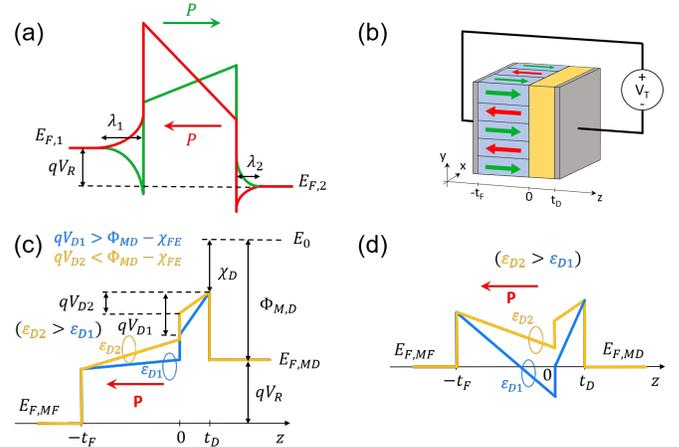


Fig. 4: (a) Band diagram for an MFM based FTJ, where λ_1 and λ_2 (with $\lambda_1 > \lambda_2$) are the screening lengths in the metal electrodes. (b) Cross-section of a MFIM based FTJ (see also Fig.1(a)) used for simulations in Sec.IV. (c) Band diagram across a MFIM based FTJ during reading $V_T = V_R$. qV_D should be larger than the ferroelectric tunnelling barrier $[\Phi_{M,D} - \chi_F]$, so that the ferroelectric conduction band profile can drop below $E_{f,MD}$. The band diagram is shown for two different dielectric constants $\epsilon_{D2} > \epsilon_{D1}$ of the tunnelling oxide. (d) Same as in (c) but for the retention condition at $V_T = 0$. The depolarization field $E_{DEP} \approx P_r [\epsilon_F (C_D / C_F + 1)]^{-1}$, where P_r is the remanent polarization, should be minimized, and it larger the smaller is ϵ_D . E_0 and $\Phi_{M,D}$ are respectively the vacuum level and the work function of the MD electrodes. χ_F , χ_D are the electron affinity of the ferroelectric and dielectric. $E_{f,MD}$, $E_{f,MF}$ are the Fermi levels of the MD and MF electrode (see also Fig.1(a)).

A robust operation of an MFIM based FTJ requires that during reading the oxide voltage drop V_D is large enough to have $qV_D > [\Phi_{M,D} - \chi_F]$ (see Fig.4(c)), so that tunnelling is limited by the thin dielectric layer. This can be achieved for a small enough $C_D = \epsilon_D / t_D$ which, however, enhances the depolarization field E_{DEP} destabilizing the polarization state during retention (see Fig.4(d)). It is evident that device design entails quite delicate tradeoffs that demands a sound modelling support. In this respect, Fig.5 shows the simulated read current characteristics for an HZO/ Al_2O_3 FTJ. A four level operation is observed and the simulated read currents are in fairly good agreement with experiments in [29].

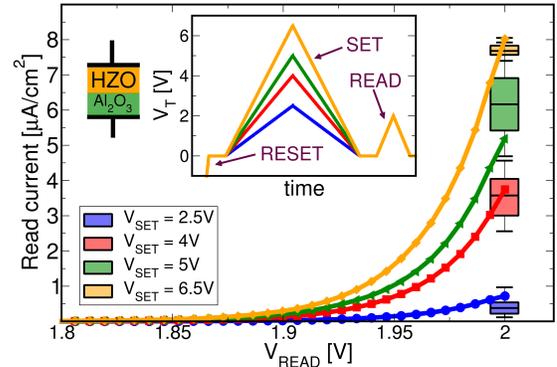


Fig. 5: Simulations for the read current of an HZO/ Al_2O_3 FTJ ($t_F = 12\text{nm}$, $t_D = 2\text{nm}$) versus read voltage V_R . The box plots for experiments were inferred from the cycle to cycle variations reported Fig.3(d) of [29] (device area $\approx 3.14 \cdot 10^{-4} \text{ cm}^2$). The inset shows the signal waveforms for the write and read operation. The reset voltage is -8V .

V. POLARIZATION DEPENDENT I_{DS} IN FEFETs

Ferroelectric FETs (FeFETs) represent an alternative device concept for neuromorphic and in-memory computing systems. Several BEOL-compatible HfO based ferroelectric capacitors [30], [31], as well as ferroelectric memristors have already been demonstrated [32]–[34].

Figure 6 shows a 2D-FeFET with an n -type polysilicon active region and, as such, compatible with a BEOL integration. Simulation results are obtained using Sentaurus TCAD and are reported in Fig.7 for very different values of channel doping concentrations. Because the ferroelectric layer is placed between a metal electrode and a semiconductor channel material, the semiconductor depletion can set serious limitations to the ferroelectric switching to a negative polarization (i.e. a polarization pointing to the metal contact, see Fig.6).

In this respect, a high channel doping concentration can avoid the complete depletion of the thin polysilicon layer during the switching to negative polarization. While this is a desirable behavior from a polarization switching perspective, high doping concentrations reduce the conductance modulation induced by the ferroelectric switching, as it is shown in Fig.7. On the other hand doping concentrations lower than about 10^{19} cm^{-3} can enlarge the difference in the read current for positive and negative polarization (see Fig.7), however during the switching to negative polarization the polysilicon gets fully depleted and a minority carrier inversion is needed. In this case the physical mechanisms for the supply of minority carriers become crucial.

For an SRH generation of minority carriers we need small carrier lifetimes, in which case the polysilicon channel can help because the defects at the grain boundaries largely enhance the generation rates compared to mono-crystal silicon [35]. An alternative design option may be give by mid-gap Schottky contacts able to supply both electrons and holes, but at the cost of a larger contact resistance.

VI. OUTLOOK AND CONCLUSIONS

The ferroelectricity has introduced substantial innovation in the design of electron devices. The support of modelling and simulation is important to unleash the potentials of these materials, particularly in new applications such as hybrid memristive-CMOS neuromorphic processing systems.

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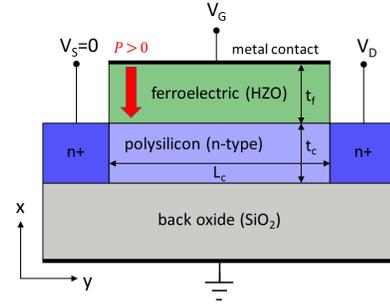


Fig. 6: Cross-sectional view of the simulated FeFET. The polysilicon channel is n -type with donor doping varying between $N_D = 5 \cdot 10^{18} \text{ cm}^{-3}$ and $N_D = 1 \cdot 10^{20} \text{ cm}^{-3}$ with a thickness $t_c = 20 \text{ nm}$ and length $L_c = 500 \text{ nm}$. Source and drain regions are n -type doped ($N_D = 5 \cdot 10^{20} \text{ cm}^{-3}$). Ferroelectric thickness is $t_f = 20 \text{ nm}$ and Landau coefficients are reported in the caption of Fig.2. The polarization is positive when it points to the polysilicon channel.

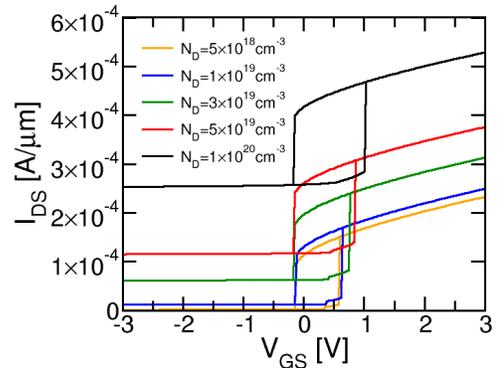


Fig. 7: Quasi static I_{DS} - V_{GS} transcharacteristic for different channel dopings for a $V_{DS} = 0.05 \text{ V}$. Results obtained by using a constant mobility of $100 \text{ cm}^2/\text{Vs}$.

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