Going ballistic: Graphene hot electron transistors

Going Ballistic: Graphene Hot Electron Transistors

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Abstract

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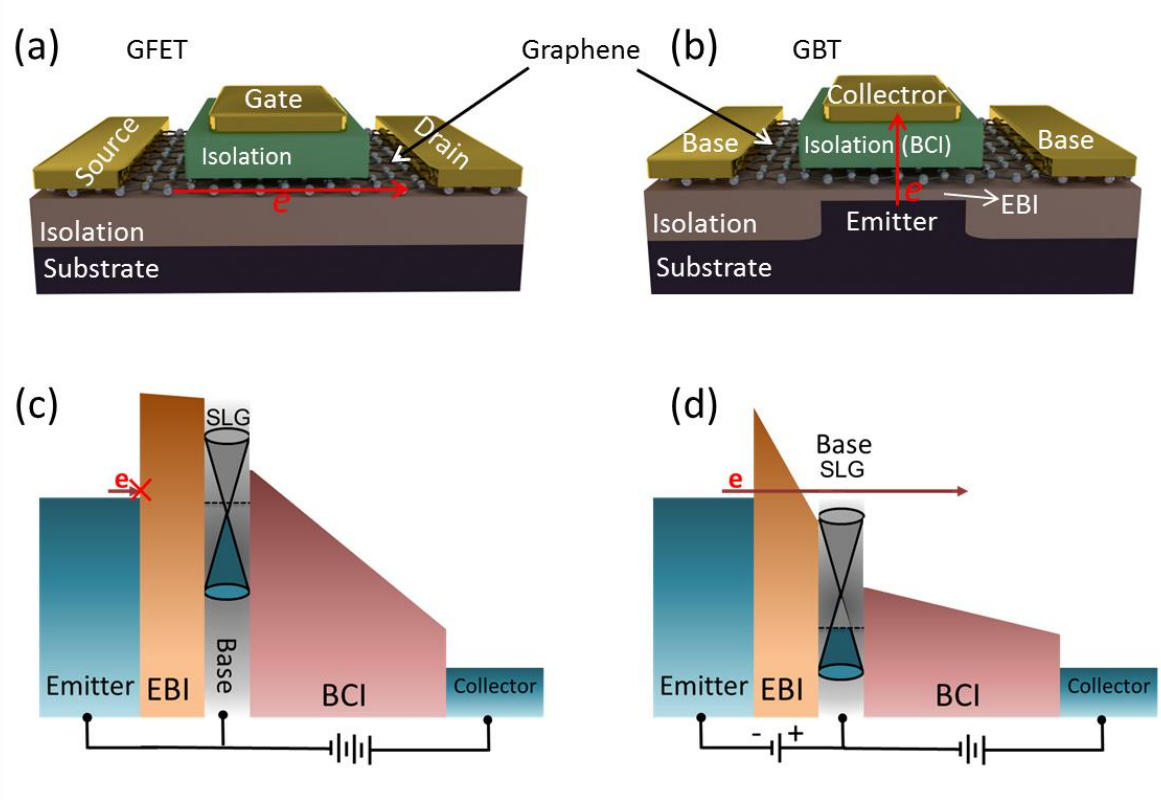
Introduction

The experimental realization of graphene [1] and, subsequently, other graphene-like materials [2] has opened new opportunities for pushing the limits of the state-of-the-art electronics [3], [4] and photonics [5], [6]. This has been motivated by graphene's excellent properties which surpass conventional 3D, 1D, and 0D materials. However, in spite of its promising properties, like high carrier mobility [7] and high saturation velocity [8], graphene has struggled to outperform conventional MOSFETs when it acts as the channel material in graphene field effect transistors (GFETs) [9], [10]. One of the main challenges originates from the zero band gap characteristics of graphene. This characteristic leads to high off-state current and low on/off ratios, which degrade the performance of GFETs in logic applications. Another consequence of having no band gap is band to band tunneling which reduces the output current saturation and the voltage gain limiting the RF performance of the GFETs [11], [12]. Therefore, novel device concepts, such as graphene-based vertical devices [13]–[19], have been introduced as alternative approaches to overcome this intrinsic limitation. One of these novel device concepts, proposed by Mehr et al. in 2012, is vertical graphene base transistor (GBT) [13]. The concept of the GBT is based on metal base hot-electron transistors (HETs) introduced by Mead in 1961 [20]. HETs utilize high energy tunneling injected electrons (hot electrons) to reach high speed functionality [21]. The first HET was comprised of a metal emitter, a metal base, and a metal collector which were isolated from each other by thin oxide layers. One of the main challenges for HETs as well as heterojunction bipolar transistors (HBTs) is that the cutoff frequency is limited by base transit time. While thinning down the base mitigates this issue, it dramatically increases the base resistance resulting in high RC delay and self-bias crowding. On the other hand, the GBT exploits high conductivity and ultra-thinness of graphene as the base material in conventional HETs to minimize the base transit time and achieve high cutoff frequencies. Here, note that the operational principle of GBTs is different from vertical graphene field effect tunneling transistors introduced by Britnell et al. [16]. While the former operates based on emitter-base barrier modulation analogous to the bipolar technology, the latter functions due to the limited

density of states in SLG and electrostatic gate control of the carrier transport between two isolated single layer graphene (SLG) sheets. This article reviews the progress on the GBTs and related devices.

Working principles of the GBT

The difference between the GBT and the GFET is shown in Fig. 1. In the GFET, carriers transport in the graphene plane between the source and the drain with a V_{ds} bias while the gate electrostatically controls the conductivity of the graphene channel (Fig. 1a). In contrast, in the GBT, carriers move perpendicular to the graphene plane. The graphene base is isolated from metal/doped semiconductor emitter and collector by emitter-base isolator (EBI) and base-collector isolator (BCI). Fig. 1c and 1d illustrate the simplified band diagram of a GBT in the off-state and on-state, respectively. By applying an appropriate emitter-collector voltage, the collector current can be modulated by the emitter-base voltage (common emitter configuration). As shown in Fig. 1c, when the emitter-base voltage is insufficient, electrons cannot be injected and the device is in the off-state. However, using an EBI with appropriate electron barrier height and thickness, and applying a high enough emitter-base bias, the effective barrier thickness is reduced allowing the electrons to be injected to the graphene base utilizing Fowler-Nordheim tunneling (Fig. 1d). Alternatively, EBIs with small enough barrier height can facilitate the injection of electrons by thermionic emission (not shown) as a result of effectice barrier height lowering. The electrons injected to the base with energy comparable to the emitter Fermi level are considered as hot electrons. Consequently, due to the 2D nature of graphene base, electron motion through the atomically thin graphene could approach ideal ballistic transport – resulting in “zero” base transit time. Finally, by applying a low BCI barrier to suppress or minimize quantum mechanical backscattering phenomena at the base-collector interface, the injected hot electrons contribute to the collector on-current, approaching the current gain of 1.



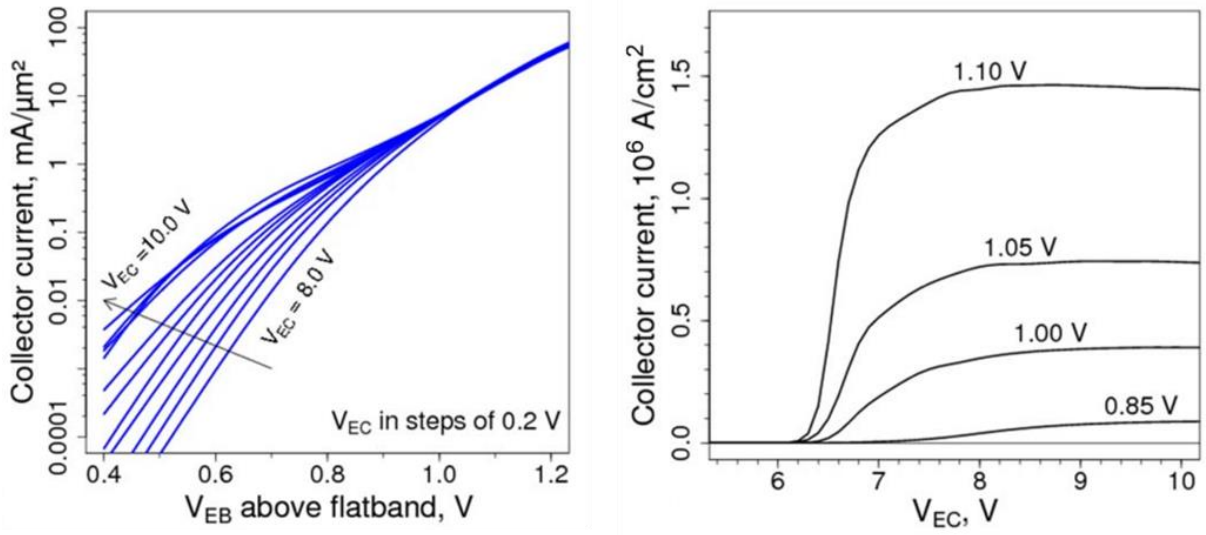
Figur 1 Schematics of (a) GFET and (b) GBT. The red arrow shows the direction of electron transport in the on-state of these devices. (c,d)Simplified band diagram of the GBT in the (c) off-state and (d) on-state in the common-emitter configuration. We note that, in (c) and (d) the energy difference between Fermi level and Dirac potential in graphene represents graphene's quantum capacitance effect.

The performance of the GBT strongly depends on the design parameters to maximize the current and minimize the loss mechanisms. Thanks to the one-atom thick graphene, the scattering of hot electrons in the base is already minimized. However, EBI parameters need to be accurately chosen to guarantee high injection current. Simultaneously, EBI needs to prevent the emission of cold electrons, with energy comparable to the base Fermi energy, via defect mediated electron transport or direct tunneling. These cold electrons are not able to surpass base-collector barrier leading to the unfavorable base current limiting the common-base current gain or current transfer ratio α. Furthermore, BCI needs to act as an electron filter which allows the passage of hot electrons and blocks the cold electron emission from

base to collector. This requires a low barrier to minimize the quantum mechanical backscattering of hot electrons at the BCI barrier, and, simultaneously, suppress thermionic, tunneling, and defect mediated electron transport from base to collector. As a result, modeling of the GBT and defining the window of the optimized design parameters for high performance operation are essential.

Device modeling/simulation and performance projection

Based on simulation, the first proposal of the GBT predicted several orders of magnitude on/off ratio in the transfer characteristics, current saturation of the output characteristics, and THz cutoff frequencies [13]. Figure 2a shows simulated common-emitter transfer characteristics for.. . Figure 2b shows the output characteristics for various emitter-base voltages for the same device..



Further, new modeling implementations have confirmed the functionality of the GBT and explored the design space of the device [F. Driussi et al., *Microelectronic Engineering* 109 (2013) 338–341]. Venica et al. have proposed a model that calculates the GBT electrostatics self-consistently with the charge stored in the graphene and the electrons tunneling through the

EBI and BCI [S.Venica et al., IEEE TED 61 (7) (2014) 2570–2576]. In this way, the model accounts for the electrostatic impact of the charge traveling along the GBT. As a result, space charge effects at high current levels (that usually reduce the maximum f_T in bipolar transistors) are considered. Since the physical origin of the base current is still unclear and debated [Zeng et al., Nano Letters, vol. 13, no. 4, pp. 1435–1439, 2013], the model assumes a priori a negligible base current and the collector current density (J_C) is thus due to the electrons injected from the emitter.

The model calculates the I-V characteristics and it has been verified through comparison with available experiments (see Fig. 3a). In addition, it estimates f_T by means a quasi-static approach and the unity power gain frequency (f_{max}), by considering as base resistance (R_B) the sum of the intrinsic graphene resistance (R_{INT}) and the contact resistance between the graphene layer and the base contact (R_{CONT}) [S.Venica et al., IEEE TED 61 (7) (2014) 2570–2576].

The model confirmed the possibility of GBT's THz operation within a fairly large design space. In particular, Fig. UD1(a) reports the f_T vs. J_C curves of an optimized GBT with Si emitter, Ta_2O_5 EBI and SiCOH BCI [S. Venica et al., Proc. of MEET, pp. 39-44, 2014]. By comparing symbols and dashed lines in Fig. UD1(a), we note that space charge effects are present also in GBTs, but are less important than in bipolar transistors, and the THz operation is feasible. Furthermore, by an appropriate optimization of the GBT geometry, it is possible to limit the detrimental effect of the contact resistance between the metal and the graphene and to obtain large f_{max} values (see Fig. UD1(b)).

Concerning other RF figures of merit, Fig. UD2(a) shows the output characteristics of the GBT of Fig. UD1. The curves show quite good saturation, confirming that GBTs can overcome the GFET limitations concerning the output conductance (g_d). As a result, the intrinsic gain g_m/g_d reaches values up to 50, as shown in Fig. UD2(b).

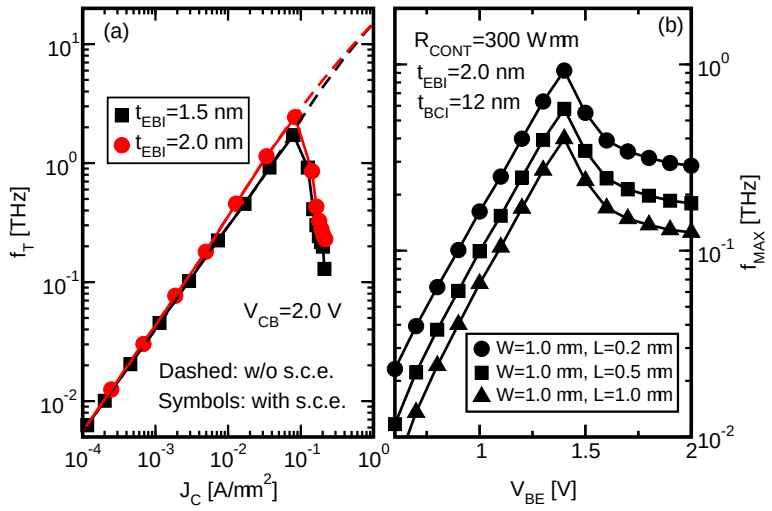


Figure UD1 (a) Cutoff frequency versus collector current for an optimized GBT exploiting Si emitter, Ta_2O_5 EBI and SiCOH BCI [S. Venica et al., Proc. of MEET, pp. 39-44, 2014]. Although space charge effects (s.c.e.) in BCI limit f_T at high current (compare symbols with dashed lines), THz operation is still feasible. (b) f_{max} versus V_{BE} for different GBT geometries. We assumed R_{CONT}=300 Ωμm. The device is contacted at both sides. Optimization of dimensions allows f_{max} around THz.

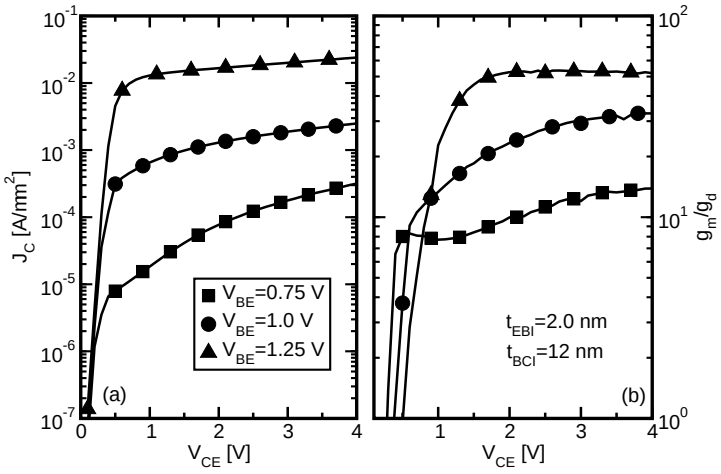


Figure UD2 (a) J_C vs. V_{CE} of the GBT of Fig UD1 showing the quite good saturation of the output characteristics. (b) The good intrinsic gain of the GBT.

Furthermore, Di Lecce et al. have performed a simulation study of GBTs with semiconducting EBI and BCI layers utilizing a quantum transport model and Poisson's equation. They

showed that voltage gain of 10 and simultaneously cutoff frequencies of 1-3 THz can be achieved.

Proof-of-concept and experimental realization of the GBT

In 2013, Vaziri et al. demonstrated the first proof of concept GBT[14]. The device comprised of an n-doped silicon emitter, a 5 nm-thick silicon dioxide (SiO2) EBI tunneling barrier, a graphene base, a 15-25 nm-thick atomic layer deposited (ALD) aluminum oxide (Al_2O_3) BCI, and a metal (titanium/gold) collector. The fabrication was done on 8-inch wafers and the GBTs were isolated by 400 nm SiO_2 shallow trench isolation (STI) making the fabrication scheme potentially CMOS compatible[22]. The reported DC functionality of this device confirmed the working principles of the GBT. Figure xa illustrates the transfer characteristics of a GBT at V_{BC} of 2 V. The device is in its off-state before the onset of the collector current at emitter-base voltage of roughly 4.5 V (threshold voltage). Moreover, thanks to the good isolation characteristics of 20 nm Al_2O_3 BCI, the device shows a very low off-state current and more than four orders of magnitude on/off ratio. Fig. xb shows temperature dependent I-V characteristics of the emitter-base tunneling diode. Clearly, the dependence of the current to the temperature diminishes for higher voltages. This fact together with the excellent linear fit of the I-V characteristics to the Fowler-nordheim model (the inset of Fig. xb) confirm that the transport mechanism is dominated by tunneling. In addition, in Fig. xb the threshold of the emitter-base tunneling current is well matched to the threshold voltage of the collector current in Fig. xa.

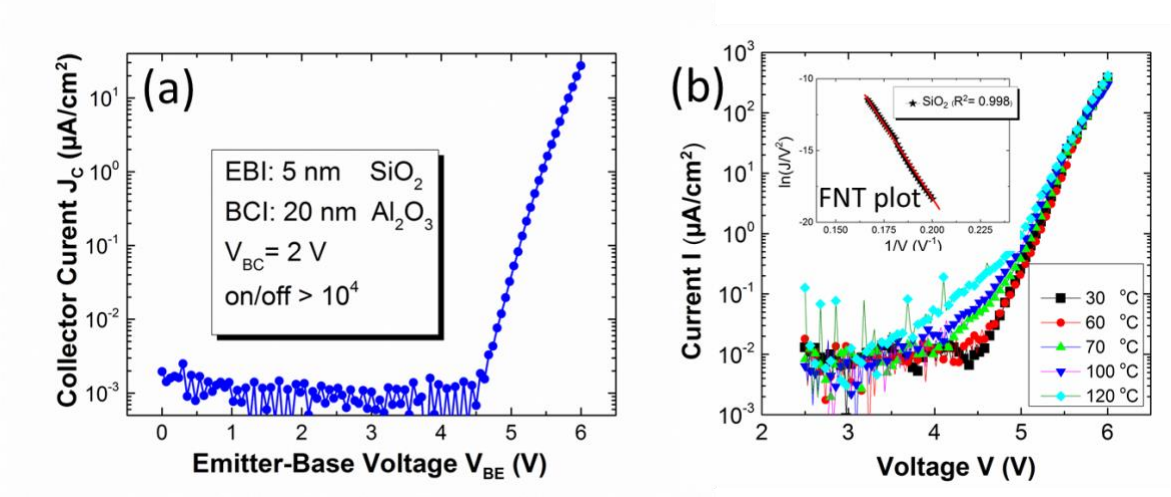


Figure 2 (a) Transfer characteristics of a GBT with 5 nm thick SiO_2 and 20 nm thick Al_2O_3 as the EBI and the BCI, respectively. The transfer characteristics shows an on/off ratio exceeding 10_4. (b) Temperature dependence I-V for the injection tunnel diode with 5 nm SiO_2 as the tunnel barrier. The inset FN plot shows and an excellent linear fit.

While the proof of concept device confirmed the DC functionality of the GBT, the performance of this device didn't reach to the projected one due to the non-optimized design parameters. Specifically, this device had low collector current density and limited current transfer ratio α (or common-base current gain) of 6.5% preventing efficient high frequency performance. These problems originate from the characteristics of 5 nm SiO_2 tunneling barrier and Al_2O_3 BCI. While these materials were chosen for the proof concept device demonstration, their characteristics are far from the criteria needed for a high performance GBT. Considering the exponential dependence of the tunneling current on barrier height and thickness, a 5 nm SiO_2 EBI having a 3.1 eV barrier height with respect to the conduction band of silicon dramatically limits the injected emitter current. On the other hand, Al_2O_3 forms a 3.3 eV barrier height with respect to the graphene Fermi level reducing the collector current and the current transfer ratio due to the large quantum mechanical backscattering. As a consequence, it is expected that optimized tunneling and filtering barrier heights and

thicknesses would dramatically improve the device performance. Moreover, efficient transfer of high quality pinhole-free graphene layer, low metal-graphene contact resistance, and high quality EBI and BCI materials with good interfaces are critical to achieve the high performance GBT.

Zeng et al. later reported functional GBTs with clear saturation behavior of the output characteristics and improved current transfer ratio α [15]. The article covered GBTs with four different sets of material parameters showing how the transfer ratio can be affected by these design parameters. For example, in two devices with the same EBI of 25 nm SiO_2, four times improvement in the current transfer ratio was reported using 21 nm HfO_2 BCI in comparison to Al_2O_3 BCI with the same thickness. This can be attributed to 1.3 eV lower band offset using HfO_2 instead of Al_2O_3. While the maximum current transfer ratio α was about 5%, the effective α (normalized to the effective collector area) was about 40%. However, beside of the very low currents, the devices with higher α values exhibited lower on/off ratios in comparison to the previous report. This again emphasizes the importance of the device layout and material parameters in GBT device performance.

EBI and BCI technology

EBI

High frequency performance of the GBT requires high on-state collector current I_C. On the other hand, in an ideal device with α=1, I_C is equal to the emitter current I_E which consists of a beam of injected hot electrons. Hence, the EBI should be a low and thin enough barrier to provide high current of hot electrons, yet blocking cold electron emission. In Fig. xa, replacing the SiO_2 EBI with 6 nm thick ALD HfO_2 resulted in an improved threshold voltage and the higher emitter current. One should note that this 6 nm thick insulator includes less than 0.5 nm interfacial SiO_2 layer. However, the choice of dielectric materials to form a low band offset is limited to the high-k dielectrics which are known for lower quality and worse interface in compare with SiO_2 or even higher band gap dielectrics. This means, for thin

tunneling layers, the defect mediated carrier transport or unfavorable direct tunneling would become the dominant transport mechanisms. One possible solution could be utilizing bilayer dielectric tunnel barriers. In the bilayer structure, the first layer in contact with emitter provides a good interface and higher material quality. This layer, together with the thicker layer 2 dielectric, minimizes any trap mediated carrier transport (Fig. xb). This approach facilitates the application of low band gap (high electron affinity) dielectrics to improve the emitter current by promoting FNT or step tunneling[23] (Fig. xb). Fig. xa shows dramatic improvement in the emitter current by applying our novel $TmSiO/TiO_2$ (1 nm/5 nm) bilayer tunnel barrier. Recently, we reported that electron injection through this dielectric stack is dominated by tunneling (submitted).

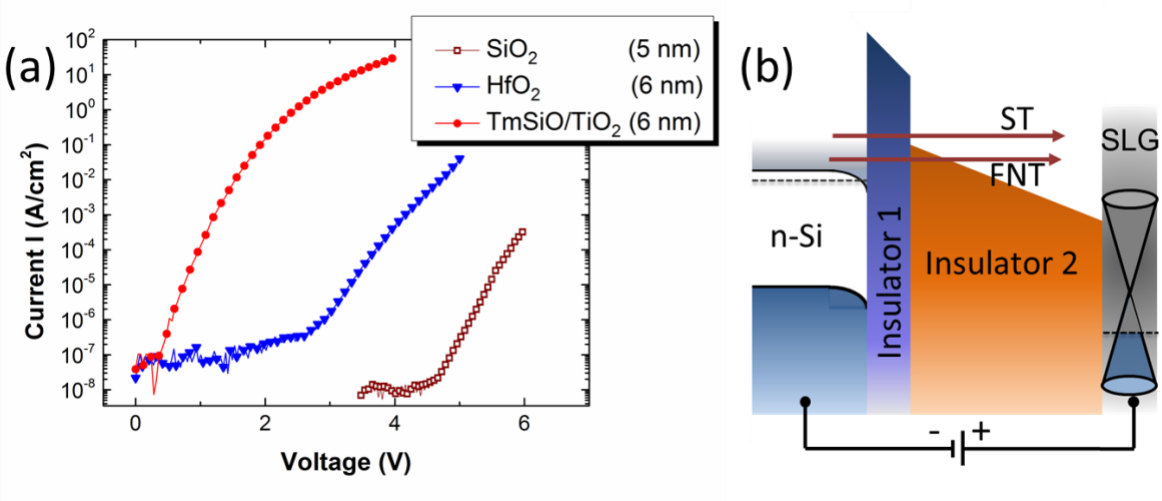


Figure 3 (a) I-V characteristics of Si-insulator-graphene tunnel diodes with SiO_2, HfO_2, and $TmSiO/TiO_2$ tunnel barriers. The HfO_2 tunnel barrier with lower band offset with respect to Si conduction band shows improved I-V characteristics (blue triangulars) in comparison to SiO_2 (brown squares). Superior I-V characteristics have been achieved using $TmSiO/TiO_2$ bilayer tunnel barrier (red circles). The tunneling transport mechanisms in the bilayer tunnel barriers is shown in the (b) simplified band diagram.

Other structures to improve the emitter injected current have been also proposed. Recently, the carrier transport in graphene on GaN/AlGaN heterostructure has been studied for both

potential applications in graphene vertical tunneling field effect transistors and GBTs[24], [25]. This heterostructure provides a 2DEG at the GaN/AlGaN junction as the emitter and a low barrier with crystalline quality which ensures high thermionic electron emission. Alternative structures utilizing 2D crystalline materials and bulk semiconductor heterojunctions have been also proposed[18], [19]. These structures will be briefly discussed in the following sections.

BCI

So far in this paper, our devices were based on the formation of EBI on the substrate prior to the graphene transfer onto the EBI. This is due to the graphene's inert surface which makes it very challenging to deposit high quality thin dielectric/semiconductor layers on top of graphene. On the other hand, the BCI could be much thicker than EBI making it more reasonable to be formed on top the graphene instead of EBI.

In the previous reports, the formation of BCI on graphene has been accomplished by applying a 2-3 nm thick evaporated Al seed layer and consequent ALD of Al_2O_3 or HfO_2. There are several main concerns in this technology. First, uncompleted oxidation of the seed layer can introduce charge trap sites and fixed charges to the graphene-dielectric interface. Moreover, this layer may dramatically affect the effective barrier height of the BCI. Another issue is that BCI materials utilized as BCIs, Al_2O_3 and HfO_2, form rather large barrier height with respect to the graphene Fermi level. On the other hand, it is not straight forward to experimentally realize defect-free/low defect thin isolation layers of low band gap dielectrics like TiO_2 and Ta_2O_5.

One promising approach could be the deposition of semiconductor materials on graphene as the BCI. Graphene-semiconductor junction forms a Schottky barrier. A low enough schottky

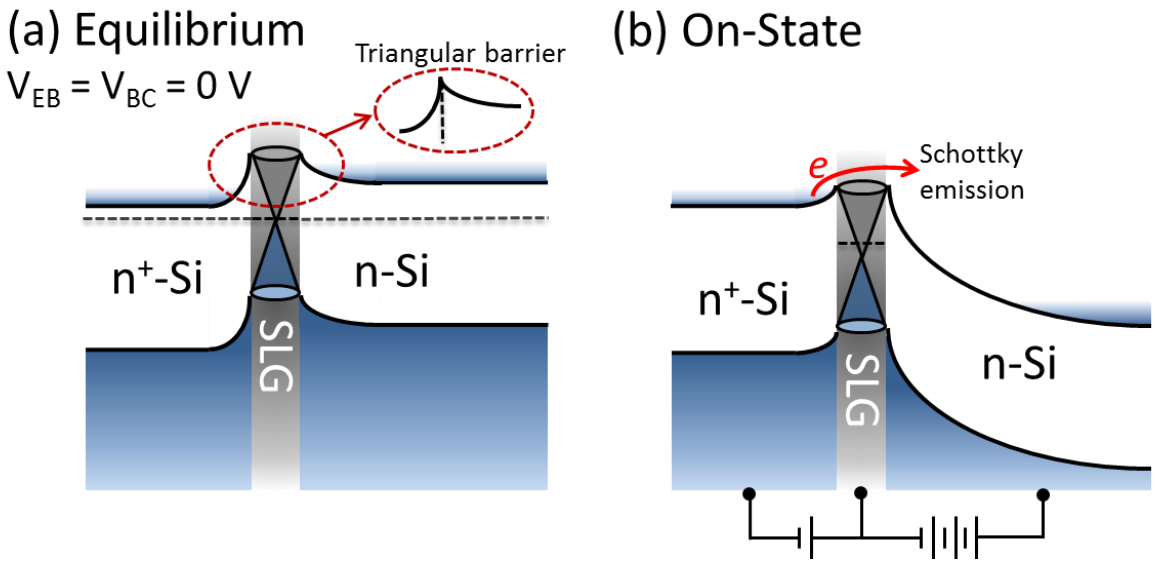
barrier could be an ideal BCI barrier by minimizing the reflection of hot electrons at the base-collector interface.

Wafer-scale integration of vertical graphene base transistors

Theoretical limits and potential

The Graphene-Base Heterojunction Transistor (GBHT) proposed by Lecce et al. is a promising adaptation of the GBT concept. In this device, graphene base is sandwiched between an n_+-Si layer (emitter) and an n-Si layer (collector). Utilizing this structure, the carrier transport mechanism is dominated by thermionic emission over the emitter-base Schottky barrier. As a result, the GBHT is envisioned to overcome part of the GBT's engineering issue regarding obtaining high current and cutoff frequency. Fig.x shows the simplified band diagram of the GBHT. At zero bias condision, the work function difference between semiconducting emitter/collector and graphene forms depletion regions and band-bending in the both emitter and collector. This band-bending results in a triangular potential energy barrier between the emitter and the collector. In the off-state, in spite of applying a reasonable positive collector-emitter voltage, the triangular barrier blocks the current. However, in the on-state, the height and shape of this barrier can be modulated by the emitter-base voltage. When the height of the barrier is small enough for electrons to overcome (in the on-state), electrons are injected to the base, passing through graphene and will be accelerated by the electric field in the collector region. Based on simulation, this

device is capable of having on/off ratios on the order of four and cut-off frequencies higher than 1 THz. The GBHT has the processing advantage of eliminating the need for ultra-thin tunnel barriers. However, the formation of a high quality crystalline semiconductor layer on top of graphene remains a processing challenge.



Figur 4 Band diagram of the GBHT at (a) equilibrium and in the (b) on-state.

Alternatively, Kong et al. reported a simulation study on GBTs based on 2D crystal heterostructures. The authors suggest using 2D crystal materials with appropriate band gap as the EBI tunneling barrier to exploit their ultimate thickness control and lateral uniformity to prevent current crowding and device to device variability. For instance, hexagonal boron nitride and MoS_2 were considered as good candidates as the EBI tunneling barrier. At the collector side, an n-type semiconductor was suggested to form a low Schottky barrier in contact with graphene. This device has been predicted to operate with cutoff frequencies well above 1 THz.

Conclusions

To be written after completion of the main body.

Acknowledgements

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References

[1] K. S. Novoselov, A. K. Geim, S. V. Morozov, D. Jiang, Y. Zhang, S. V. Dubonos, I. V. Grigorieva, and A. A. Firsov, “Electric Field Effect in Atomically Thin Carbon Films,” *Science*, vol. 306, no. 5696, pp. 666–669, 2004.

[2] K. S. Novoselov, D. Jiang, F. Schedin, T. J. Booth, V. V. Khotkevich, S. V. Morozov, and A. K. Geim, “Two-dimensional atomic crystals,” *Proc. Natl. Acad. Sci. U. S. A.*, vol. 102, no. 30, pp. 10451–10453, 2005.

[3] G. Fiori, F. Bonaccorso, G. Iannaccone, T. Palacios, D. Neumaier, A. Seabaugh, S. K. Banerjee, and L. Colombo, “Electronics based on two-dimensional materials,” *Nat. Nanotechnol.*, vol. 9, no. 10, pp. 768–779, 2014.

[4] M. C. Lemme, L.-J. Li, T. Palacios, and F. Schwierz, “Two-dimensional materials for electronic applications,” *MRS Bull.*, vol. 39, no. 08, pp. 711–718, 2014.

[5] F. N. Xia, H. Wang, D. Xiao, M. Dubey, and A. Ramasubramaniam, “Two-dimensional material nanophotonics,” *Nat. Photonics*, vol. 8, no. 12, pp. 899–907, 2014.

[6] K. S. Novoselov, V. I. Fal, L. Colombo, P. R. Gellert, M. G. Schwab, K. Kim, and others, “A roadmap for graphene,” *Nature*, vol. 490, no. 7419, pp. 192–200, 2012.

[7] K. I. Bolotin, K. J. Sikes, Z. Jiang, M. Klima, G. Fudenberg, J. Hone, P. Kim, and H. L. Stormer, “Ultrahigh electron mobility in suspended graphene,” *Solid State Commun.*, vol. 146, no. 9–10, pp. 351–355, 2008.

[8] V. E. Dorgan, M. H. Bae, and E. Pop, “Mobility and saturation velocity in graphene on SiO2,” *Appl. Phys. Lett.*, vol. 97, no. 8, 2010.

[9] M. C. Lemme, T. J. Echtermeyer, M. Baus, and H. Kurz, “A Graphene Field-Effect Device,” *IEEE Electron Device Lett.*, vol. 28, pp. 282–284, 2007.

[10] F. Schwierz, “Graphene transistors,” *Nat. Nanotechnol.*, vol. 5, no. 7, pp. 487–496, 2010.

[11] I. Meric, N. Baklitskaya, P. Kim, and K. L. Shepard, “RF performance of top-gated, zero-bandgap graphene field-effect transistors,” in *Electron Devices Meeting, 2008. IEDM 2008. IEEE International*, pp. 1–4.

[12] S. Das and J. Appenzeller, “On the importance of bandgap formation in graphene for analog device applications,” *IEEE Trans. Nanotechnol.*, vol. 10, no. 5, pp. 1093–1098, 2011.

[13] W. Mehr, J. Dabrowski, J. C. Scheytt, G. Lippert, Y.-H. Xie, M. C. Lemme, M. Ostling, and G. Lupina, “Vertical Graphene Base Transistor,” *IEEE Electron Device Lett.*, vol. 33, pp. 691–693, 2012.

[14] S. Vaziri, G. Lupina, C. Henkel, A. D. Smith, M. Östling, J. Dabrowski, G. Lippert, W. Mehr, and M. C. Lemme, “A graphene-based hot electron transistor,” *Nano Lett.*, vol. 13, no. 4, pp. 1435–1439, 2013.

[15] C. Zeng, E. B. Song, M. Wang, S. Lee, C. M. Torres Jr, J. Tang, B. H. Weiller, and K. L. Wang, “Vertical graphene-base hot-electron transistor,” *Nano Lett.*, vol. 13, no. 6, pp. 2370–2375, 2013.

[16] L. Britnell, R. V. Gorbachev, R. Jalil, B. D. Belle, F. Schedin, A. Mishchenko, T. Georgiou, M. I. Katsnelson, L. Eaves, S. V. Morozov, N. M. R. Peres, J. Leist, A. K. Geim, K. S. Novoselov, and L. A. Ponomarenko, “Field-Effect Tunneling Transistor Based on Vertical Graphene Heterostructures,” *Science*, vol. 335, no. 6071, pp. 947–950, 2012.

[17] H. Yang, J. Heo, S. Park, H. J. Song, D. H. Seo, K.-E. Byun, P. Kim, I. Yoo, H.-J. Chung, and K. Kim, “Graphene barristor, a triode device with a gate-controlled Schottky barrier,” *Science*, vol. 336, no. 6085, pp. 1140–1143, 2012.

[18] B. D. Kong, Z. Jin, and K. W. Kim, “Hot-Electron Transistors for Terahertz Operation Based on Two-Dimensional Crystal Heterostructures,” *Phys. Rev. Appl.*, vol. 2, no. 5, p. 054006, 2014.

[19] V. Di Lecce, R. Grassi, A. Gnudi, E. Gnani, S. Reggiani, and G. Baccarani, “Graphene-base heterojunction transistor: An attractive device for terahertz operation,” *Electron Devices IEEE Trans. On*, vol. 60, no. 12, pp. 4263–4268, 2013.

[20] C. A. Mead, “Operation of Tunnel-Emission Devices,” *J. Appl. Phys.*, vol. 32, no. 4, pp. 646–652, 1961.
[21] M. Heiblum, “hot-electron transistors,” in *Proc. IEEE Conf. High-speed Semicon, ductor Devices*, 1984.
[22] S. Vaziri, G. Lupina, A. Paussa, A. D. Smith, C. Henkel, G. Lippert, J. Dabrowski, W. Mehr, M. Östling, and M. C. Lemme, “A manufacturable process integration approach for graphene devices,” *Solid-State Electron.*, vol. 84, pp. 185–190, 2013.
[23] N. Alimardani and J. F. Conley Jr, “Step tunneling enhanced asymmetry in asymmetric electrode metal-insulator-insulator-metal tunnel diodes,” *Appl. Phys. Lett.*, vol. 102, no. 14, p. 143501, 2013.
[24] G. Fisichella, G. Greco, F. Roccaforte, and F. Giannazzo, “Current transport in graphene/AlGaN/GaN vertical heterostructures probed at nanoscale,” *Nanoscale*, vol. 6, no. 15, pp. 8671–8680, 2014.
[25] A. Zubair, O. Saadat, Y. Song, J. Kong, M. Dresselhaus, and T. Palacios, “Vertical Graphene-base transistor on GaN substrate,” *Bull. Am. Phys. Soc.*, vol. 59, 2014.