Benchmarking of 3-D MOSFET Architectures: Focus on the Impact of Surface Roughness and Self-Heating

Benchmarking of 3D MOSFET architectures: Focus on the impact of surface roughness and self-heating

O. Badami, D. Lizzit, F. Driussi, P. Palestri, L. Selmi and D. Esseni

***Abstract*—Tremendous improvements in the fabrication technology has allowed us to scale the physical dimensions of the transistors and also to develop different promising 3D architectures that may allow us to continue the Moore's law. In this work we perform a comparative delay analysis of different architectures and study the impact of surface roughness and self-heating on on-current using a comprehensive in-house simulation framework comprising of Schrödinger, Poisson and Boltzmann transport equations solvers along with relevant scattering mechanisms and self-heating. Our results highlight that the parasitic capacitance can alter the relative ranking of the architectures from delay point of view. We demonstrate that the surface roughness can cause architecture and material dependent degradation and hence it is necessary to account for it in simulations benchmarking different architectures.**

***Index Terms*—FinFETs, nanowire FETs, stacked-nanowire FETs, surface roughness scattering, self-heating.**

I. Introduction

The semiconductor industry has been constantly scaling the physical dimensions of the MOSFETs to enable better transistors with every CMOS generation and also obtain economic advantages [1], [2]. This scaling has been possible due to the tremendous improvements in the fabrication methods which have enabled us to move from bulk planar transistors, to 3D multigate architectures, and then stacks of 3D multigate architectures [3], [4], [5], [6], [7]. Hence the industry and academia are looking for the optimum architecture and material combinations [8], [9]. The simulation-based studies allow us to compare different architectures and materials at much lower cost and time as compared to experiments. Moreover, the simulations enable us to study different physical phenomena in isolation and thus obtain a good physical insight.

The simulations of transistors have been carried out with different transport formulations ranging from moments of Boltzmann transport equation to full quantum transport analysis [10], [11]. Even though the drift-diffusion and energy balance formulations have much lower computational burden, they need a larger number of fitting parameters, and a number of studies have shown that in decananometric devices several assumptions in these models are violated [12], [13]. Nevertheless most of the simulation studies benchmarking the stacked nanowires against more conventional architectures like FinFET and gate-all-around nanowires have been carried out using quantum corrected drift-diffusion based models [10], [14].

Moreover, we emphasize that for modern 3D technologies it is important to account for self-heating because of the reduced dimension of the fin area, which causes a significant reduction in the thermal conductivity. Self-heating has been thoroughly studied for planar SOI structures [15]. Recently it has been demonstrated that the self-heating can cause significant degradation in the on-current for cylindrical gate-all-around nanowires, whereas a comparative study of the impact of self-heating on different possible 3D architectures is missing to the best of our knowledge [16]. In this context surface roughness can also play an important role by further reducing the thermal conductivity and thus increasing the self-heating effects [17], [18], [19].

In this work, we have used Boltzmann transport equation to model the carrier transport along with the Schrödinger-Poisson solver to model the electrostatics to benchmark different FET architectures for future CMOS technology node having channel length of 14 nm. We systematically study and compare performance parameters for different architectures based on strained silicon and $In_{0.53}Ga_{0.47}As$. We provide comparative analysis of the impact of the surface roughness when it is varied over a practical range and provide physical insight into the architecture and material dependent degradation. We also study and discuss the impact of self-heating in different architectures based on strained silicon.

This paper is organized as follows. In section II we discuss several theoretical and implementation aspects of the simulation framework. Then we discuss the simulation results in section III, wherein we first discuss the impact of parasitic capacitance on the delay analysis, followed by study of influence of surface roughness and self-heating on the on-current. Finally, in section IV we report our concluding remarks.

II. Simulation framework

It has been recently shown by Grillet *et al.* in [20] that for gate-all-around nanowire-based devices the source to drain tunneling current component is less than 10% of the total off-current in strained silicon (sSi) and InAs based devices having a channel length of 14 nm. This justifies our choice to use semi-classical transport formulation (Boltzmann transport equation) in analyzing different FET architectures having channel lengths greater than or equal to 14 nm.

A. Schrödinger-Poisson-BTE solver

In this work, we solve a 2D effective mass Schrödinger equation in the device cross-sections, while the Poisson equation is solved in the entire 3D domain. The 2D effective mass Schrödinger equation reads [21]

$$\left[-\frac{\hbar^2}{2}\nabla\cdot(\mathrm{W}_{yz}\nabla)+U(y,z)\right]\xi_n(y,z)=\varepsilon_n^{(p)}\xi_n(y,z) \tag{1}$$

(Email addresses.)

where W_{yz} is the 2×2 inverse effective mass tensor in the device coordinate system [21], $U(y,z)$ is the total potential energy, $\xi_n(y,z)$ is the envelope wavefunction corresponding to the n^{th} parabolic eigen energy $\varepsilon_n^{(p)}$, which is then corrected for the non-parabolicity in the dispersion relation as discussed in [22]. Both $\mathbf{k}\cdot\mathbf{p}$ and empirical pseudopotential methods have been used to validate the effective masses and non-parabolic coefficients used in this work [23]. Throughout the work we have accounted for the wavefunction penetration into the oxide, which is also necessary for our formulation of surface roughness scattering [24], [25]. The wavefunction continuity at the oxide-semicoductor interface (continuity of $\xi_n(y,z)$ and $W_{yz}\nabla\xi_n(y,z)$) is naturally satisfied in the Discrete Geometric Approach (DGA) [26]. Schrödinger and Poisson equations are solved with the DGA because it has the flexibility of the Finite Element method in accounting for arbitrary cross-section, but with the remarkable advantage that the discretized Schrödinger equation also reduces to standard eigenvalue problem unlike the Finite Element method which leads to a generalized eigenvalue problem [27], [26].

The Boltzmann transport equation for a 1D electron gas can be written as

$$v_{g,n}(x,k_x)\frac{\partial f_n(x,k_x)}{\partial x} - \frac{\partial f_n(x,k_x)}{\partial k_x}\left(\frac{1}{\hbar}\frac{\partial E_n}{\partial x}\right) = S_n^{in}(k_x) - S_n^{out}(k_x) \quad (2)$$

where $f_n(x,k_x)$ is the occupation function for an electron in the n^{th} subband, $v_{g,n}(x,k_x)$ is the group velocity of the electron, S_n^{in} and S_n^{out} are the in and out scattering rates from the state indexed by (n,k_x) respectively. By changing the variables from (x,k_x) to (x,E_n), the eq.2 can be separated for carriers having either positive or negative k_x [28]

$$+|v_{g,n}(x,E_n)|\frac{df_n^+(x,E_n)}{dx} = S_n^{in,+} - S_n^{out,+}, \quad \text{for } k_x > 0 \quad (3a)$$

$$-|v_{g,n}(x,E_n)|\frac{df_n^-(x,E_n)}{dx} = S_n^{in,-} - S_n^{out,-}, \quad \text{for } k_x < 0 \quad (3b)$$

where $f_n^+(x,E_n)$ and $f_n^-(x,E_n)$ are the occupation functions for the electrons having respectively positive and negative momentum.

The Schrödinger, Poisson and Boltzmann Transport equation are self-consistently solved in a Gummel iterative fashion. In the Boltzmann Transport equation all the relevant scattering mechanisms are included without resorting to any simplification like relaxation time approximation. The surface roughness scattering has been modeled with the recently developed non-linear model, which allows us to use realistic values of the surface roughness parameters [24], [25].

B. Self-heating formulation

Self-heating has been modeled in the literature by using a very comprehensive formulations including full quantum electron phonon treatment [29], and moments for phonon Boltzmann Transport equation [15]. However in this work we have used a simple and yet physically transparent formulation that is discussed in [19]. This methodology is also numerically efficient (as we have to solve a linear 1D differential equation), and it can be seamlessly integrated into the simulation framework discussed in II-A.

In this formulation the lattice temperature along the transport direction is calculated by solving the 1D Fourier heat transport equation

$$-A\kappa_{sc}\frac{d^2}{dx^2}T(x) + \frac{\kappa_{BOX}}{h_{BOX}}\left[T(x) - T_0\right]W = H_{1D}(x) \quad (4)$$

where A is the semiconductor cross-section area, $T(x)$ is the lattice temperature, T_0 is the lattice temperature at the bottom of the buried oxide (taken to be 300 K in this work), $H_{1D}(x)$ is the heat power generated in the cross-section of the device, h_{BOX} is the thickness of buried oxide and κ_{sc} and κ_{BOX} are the thermal conductivities of the semiconductor and buried oxide, respectively. The second term on the left-hand-side describes the heat flow through the buried oxide in a phenomenological way. Eq.4 is solved assuming that the temperature at the source and drain edges is 300 K (Dirichlet boundary condition). While the use of such a simple boundary condition may be questionable, a study of the influence of different boundary conditions is beyond the scope of this work.

The heat generated in the device is due to optical phonon scattering of the carriers and consequently very intrinsically linked with the carrier transport. Heat power generated at x_i is given by

$$H_{1D}(x_i)dx = \int_{-\infty}^{+\infty} dE\frac{E}{-e}\left[\mathcal{I}_{i\to i+1}(E) + \mathcal{I}_{i\to i-1}(E)\right] \quad (5)$$

where dx is distance between two successive nodes along the transport direction, E is the energy, e is the electron charge, $\mathcal{I}_{i\to i+1}(E)$ and $\mathcal{I}_{i\to i-1}(E)$ are the spectral current density from node i to $i\pm1$. The term in the square bracket is spectral imbalance in the current. This imbalance occurs only in the presence of the optical phonon scattering, hence the overall term represents the energy exchanged between the carrier and the lattice.

C. Iteration Scheme

The main advantage of the Drift-Diffusion (or moments of Boltzmann Transport equation in general) method over more accurate transport formulations (like non-equilibrium Green's function) is its lower computational burden. In our work, the computational load is very high because we use a Boltzmann transport equation along with the non-linear surface roughness scattering model and also account for the polar optical phonon (for III-V architectures). Hence, in order to perform comparative analysis with comprehensive simulation structure discussed earlier we have developed a new iteration scheme.

Fig.1 shows the developed iteration scheme, which differs from conventional schemes where all the scattering mechanisms are turned-on from the first iteration. In the new method, the initial guess is generated from the equilibrium statistics and then, instead of starting all the scattering mechanisms, we perform only ballistic simulations until the difference

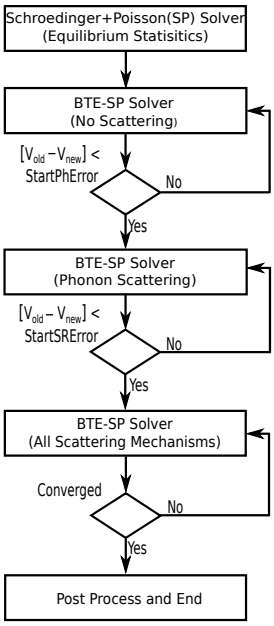

Fig. 1: Novel iteration scheme used to reduce the computational burden. By appropriately choosing the values of StartPhhError and StartSRhError we can reduce the simulation time significantly.

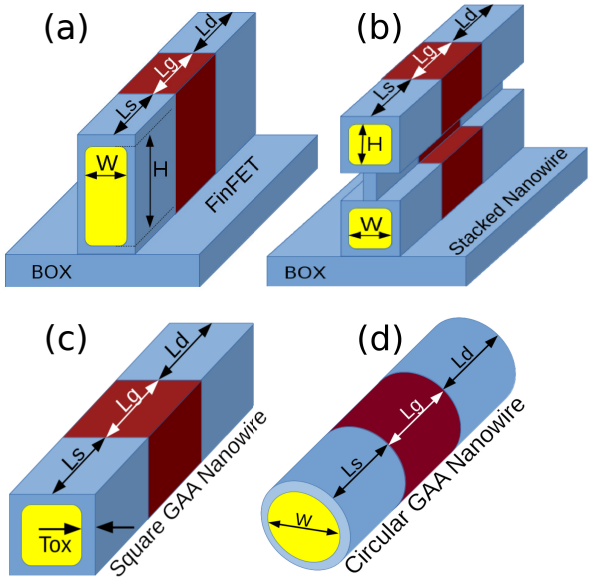

Fig. 2: Schematics of the (a) FinFET with an aspect ratio of 2:1 (H:W) (b) Stacked nanowires (c) Square and (d) Circular gate-all-around nanowires. The source (drain) length, Ls (Ld), was set to 25 nm while the channel length, Lg, was set to 14 nm. The thickness of HfO_2 based gate oxide was taken to be 2.8 nm (EOT=0.5 nm).

in the potential between two successive iterations (error) is below a certain tolerance ("StartPhError"). After this, phonon scattering is turned-on and the simulation is continued until the error is reduced further (below "StartSRhError"), and only then the surface roughness scattering is turned-on, which is the computationally heaviest scattering mechanism. In this way, by progressively enabling the computationally heavier mechanisms we generate better initial starting points for the simulation and the computationally heaviest calculations are performed only in the last few iterations. The values of StartPhError and StartSRError must be chosen on the basis of experience.

III. Simulation Results and Physical Insights

A. Simulation Setup

Schematics of different device architectures that we have simulated in this work are shown in Fig.2. The channel length of all the architectures was set to 14 nm. The other geometrical parameters like the width, W, and oxide thickness, Tox, were varied so that the FinFET device has subthreshold slope around 75 mV/dec as required by ITRS [30]. The width and oxide thickness was kept the same for all the architectures so that they have the same foot print (area on chip i.e. W×(Ls+Lc+Ld)) for a fair comparison. In addition, the stacked nanowire and FinFET were taken to have same semiconductor cross-section area. The devices based on silicon were assumed to be strained (with 2 GPa tensile stress). The transport direction for strained silicon based devices was taken along [110] crystal direction, while $In_{0.53}Ga_{0.47}As$ FETs were taken to be oriented along [100] direction. The $In_{0.53}Ga_{0.47}As$ based devices were taken to be unstrained, as it has been demonstrated by both experiments and simulations that the strain is an ineffective performance booster for III-V based FETs [31], [32]. The supply voltage, V_{DD}, was set to 0.7 V. The off-current was set to 100 nA/μm and the on-current is defined at V_{GS}=V_{DS}=V_{DD} as required by the ITRS specifications. The source and drain series resistance value was taken to be 202 $\Omega \cdot \mu$m (converted to Ω by using the gate perimeter) consistent with 14 nm channel length devices [30]. The material and phonon scattering parameters are same as stated in [21], [33], [34]. It is important to account for all relevant scattering mechanisms because the scattering strongly influences the transport even in devices having channel length of 14 nm [35]. The surface roughness root mean square (Δ_{rms}) was taken to be 0.21 nm and the correlation length was set to 1.4 nm unless specified otherwise.

B. Delay analysis

Delay is one of the most important performance metric for CMOS integrated circuits and it is also strongly affected by the factors that are extrinsic to the device like the parasitic capacitance due to the interconnects [36]. Hence it is necessary to introduce an estimate for the external capacitances while calculating the delay of individual FET architecture as well as performing comparative analysis of different architectures. Fig.3 plots the total delay as a function of the external parasitic capacitance which is taken to be a parameter. The total delay, D_T, was calculated as

$$D_T = \frac{Q_{on} - Q_{off}}{I_{on}} + \frac{Q_{frng}}{I_{on}} + \frac{Q_{FO3}}{I_{on}} + \frac{C_{par} V_{DD}}{I_{on}} \quad (6)$$

where Q_{on} and Q_{off} are the total on-state charge calculated at V_{DS}=0,V_{GS}=V_{DD} and off-state charge calculated at V_{DS}=V_{DD}, V_{GS}=0, Q_{frng} is the charge due to the fringe capacitance which is taken to be 1.2 times the intrinsic charge, $Q_{on} - Q_{off}$ [37], and C_{par} is the parasitic capacitance. The

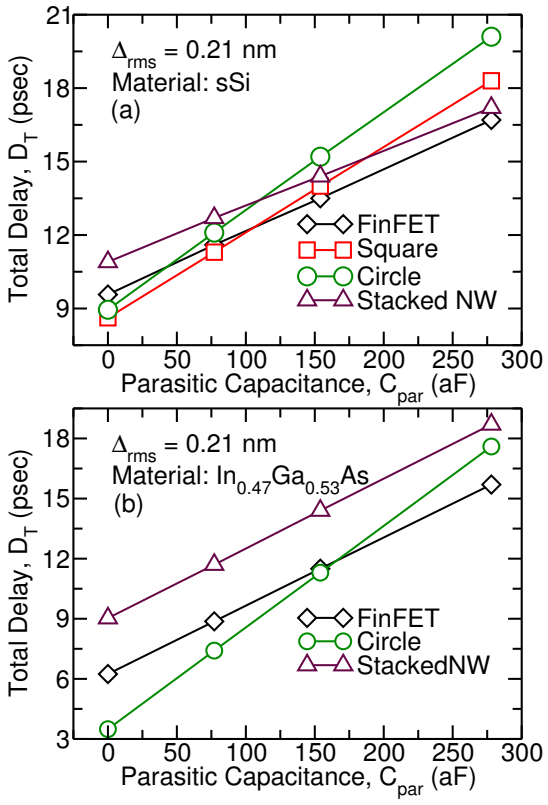

Fig. 3: (a) Total delay as a function of parasitic capacitance for different architectures based on strained silicon (b) Same as (a) but for $In_{0.53}Ga_{0.47}As$ based FETs.

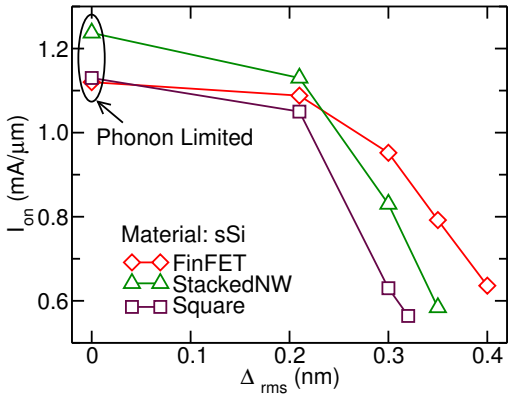

Fig. 4: Impact of surface roughness on the on-current for stacked nanowire, FinFET and square-GAA nanowire architectures based on strained silicon. The surface roughness shows an architecture dependent degradation. The normalization of the current is done by the gate perimeter.

third term on the right accounts for the FO3 load capacitance. Q_{FO3} is taken to be $3\times2(Q_{on}\text{-}Q_{off}+Q_{frng})$.

An important outcome of the delay analysis reported in Fig.3(a) and (b) is that even though the gate-all-around architectures have a lower delay for smaller values of the parasitic capacitance as compared to the FinFET and stacked nanowire architecture, this advantage is eclipsed with the increase in the parasitic capacitance. The reason for the reversal of the trend is that FinFET and stacked nanowires have a larger on-current per unit footprint as compared to the gate-all-around architecture which helps these architectures counter the parasitic capacitance better [35].

C. Influence of surface roughness

In the device performance analyses we have until now, assumed a very good interface quality by setting Δ_{rms}=0.21 nm. Such a small value of surface roughness has been mainly observed in mature technologies that employ Si-SiO_2 interface, and only in some recent studies similarly small surface roughness values have been extracted from simulation for III-V based FETs [25], [38], [39], [40], [41], [42]. This warrants a study of on-current dependence on surface roughness for different architectures and materials.

Fig.4 shows the impact of the surface roughness for different architectures based on strained silicon. It can be seen that at lower values of Δ_{rms} ($\Delta_{rms} = 0$ nm corresponds to the scattering due to phonons only) the stacked nanowire gives a larger on-current as compared to the FinFET. However, the degradation of the on-current with the increase in the surface roughness in stacked nanowires is much more than it is in FinFET and consequently FinFET has better performance than the stacked nanowires for larger values of Δ_{rms}. Similar behaviour is observed in the $In_{0.53}Ga_{0.47}As$ based architectures as well (not shown here).

To get a physical insight into this architecture dependent degradation we note that the matrix element, $M(\Delta(s))$, lies at the core of the surface roughness scattering mechanism [25], and it can be written as

$$M_{nn'}(s) = \int_{\eta_{min}}^{\eta_{max}} \xi_n(s,\eta)^{\dagger} \Phi_B \xi_{n'}(s,\eta) d\eta \qquad (7)$$

where s is the coordinate along the oxide-semiconductor interface, η is the abscissa in the direction normal to the interface and $\xi_n(s,\eta)$ is the envelope wavefunction for the n^{th} subband in the curvilinear coordinate system formed by (s,η).

Fig.5 plots the matrix elements, $M_{nn'}(s)$, for strained silicon based stacked nanowire and FinFET versus the normalized perimeter. The integration in the direction normal to the interface is carried over the range $-3\Delta_{rms}$ to $+3\Delta_{rms}$. It can be seen that the matrix element for stacked nanowire is larger than that of the FinFET and thus, with the increase in the surface roughness, the on-current of stacked nanowire degrades more than the FinFET. Since stacked nanowire has stronger physical confinement (smaller cross-section area), the wavefunction at the oxide-semiconductor interface calculated accounting for the penetration in the oxide is larger, which results in the greater matrix element.

Fig.6 compares the on-current degradation due to increase in surface roughness for strained silicon and $In_{0.53}Ga_{0.47}As$ based FinFET. It can be seen that at smaller values of Δ_{rms} strained silicon based FinFET gives better on-current than the one based on $In_{0.53}Ga_{0.47}As$ because of the larger density-of-states (DoS) in the former material, as already discussed earlier. However, with the increase in the Δ_{rms} there is a cross-over in the on-current and $In_{0.53}Ga_{0.47}As$ based FinFET delivers a higher on-current. This cross-over can be explained by the fact that the intersubband scattering in the strained silicon is much more than $In_{0.53}Ga_{0.47}As$ based FinFET. At this

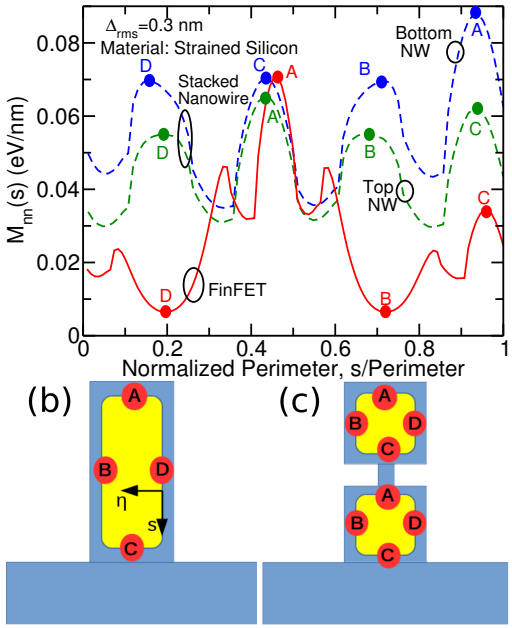

Fig. 5: (a)Plot of matrix element (as defined in eq.7) versus the normalized abscissa along the oxide-semiconductor interface for stacked nanowire and FinFET architectures is shown on the left. The larger value of the matrix element in the stacked nanowires results in stronger degradation of the on-current as observed in Fig.4. (b) and (c) show the position of the peaks or minima of the matrix elements on the perimeter of FinFET and stacked nanowire respectively.

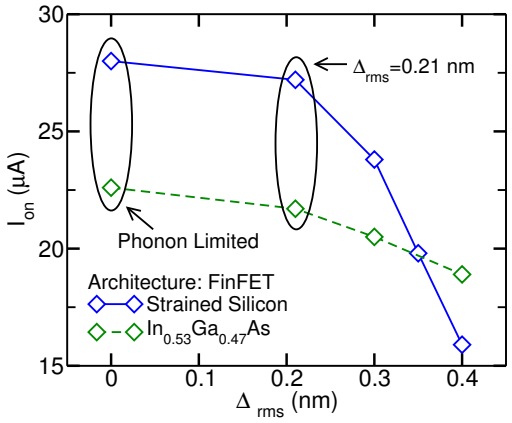

Fig. 6: Impact of surface roughness on the on-current for FinFET based on strained silicon and $In_{0.53}Ga_{0.47}As$. The results show that the impact of the surface roughness depends on the semiconductor material.

regard, in fact, Fig.7(a) plots density of states versus the energy for FinFET based on strained silicon and $In_{0.53}Ga_{0.47}As$. It can be seen that the number of subbands that lie below the Fermi level, E_F, in the strained silicon based devices is much larger than the $In_{0.53}Ga_{0.47}As$ because of the larger electron effective mass in silicon. The larger number of subbands result in more possible transitions from lower to higher subbands that lead to a reduction of the electron velocity (because the potential energy of the carrier increases) and their momentum decreases, hence in a reduced drive current. To get a measure of the impact of intersubband scattering, in Fig.7(b) we report also the on-current with and without intersubband scattering for surface roughness. It can be seen that when intersubband scattering is turned on the degradation in the on-current with

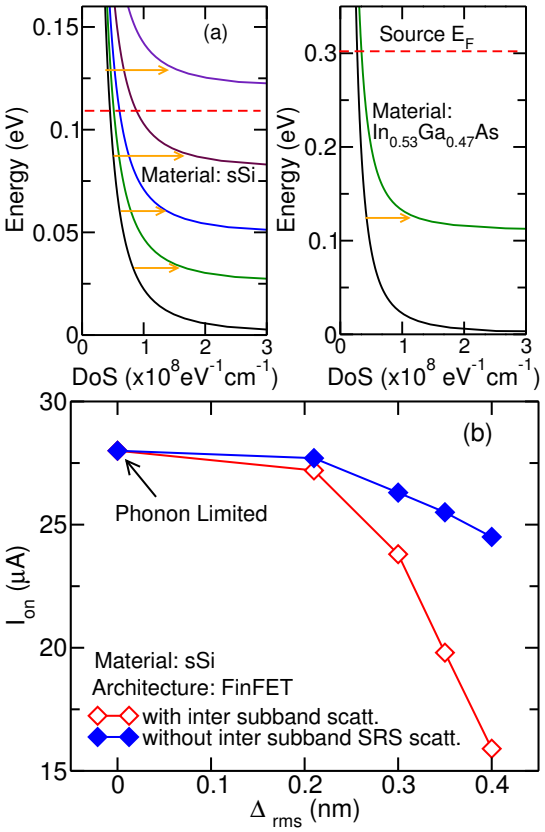

Fig. 7: (a) Plot of energy versus DoS for FinFET based on strained silicon and $In_{0.53}Ga_{0.47}As$. The lowest subband minima is taken as a reference in both the cases. (b) Plot of on-current versus surface roughness with and without intersubband surface roughness scattering.

the increase of the roughness is much steeper as compared to the case where the intersubband scattering is not considered.

D. Influence of self-heating

It is has been demonstrated both experimentally and with simulations that spatial confinement has a strong negative impact on the thermal conductivity. For example the thermal conductivity of the bulk silicon is 148 $Wm^{-1}K^{-1}$ but for a nanowire with a diameter of 22 nm a value of about $\sim$7 $Wm^{-1}K^{-1}$ has been reported corresponding to a reduction of 21x [43]. Furthermore surface roughness tends to degrade the thermal conductivity. Thus the thermal conductivity is doubly, affected and consequently the impact of self-heating as well. However, due to various approximations generally made in simulations, the thermal conductivity obtained from calculations is larger than the experimentally measured value [18], [19]. In addition the thermal conductivity also depends on the fabrication method [44]. Due to these uncertainties, we have considered thermal conductivity as a parameter that was varied so as to cover the range of experimentally reported values.

Fig.8 shows the temperature profiles for stacked nanowire architecture for different values of the thermal conductivity of the semiconductor. The temperature at the source and drain edges is 300 K due to the Dirichlet boundary condition used in this work. As expected with the reduction in the thermal

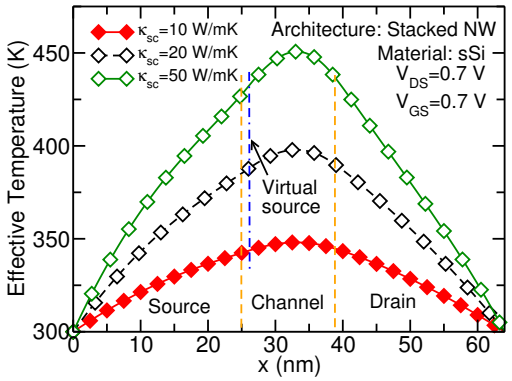

Fig. 8: Plot of effective temperature along the transport direction for different values of the thermal conductivity. The temperature in the device increases with the reduction in the thermal conductivity.

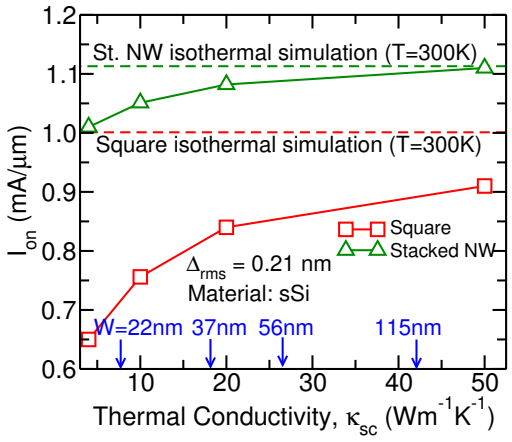

Fig. 9: Plots the impact of the reduction in thermal conductivity on normalized on-current (by the gate perimeter). The simulation results highlight that the current reduces with the reduction in the thermal conductivity (i.e. increase in device temperature see Fig.8). The experimental values of the thermal conductivity for different diameters are shown by vertical arrows.

conductivity the thermal resistance of the device increases, thus leading to increase in the temperature in the device.

Fig.9 shows the impact of the thermal conductivity on the on-current in different architectures. It can be seen that there is a reduction in the on-current when self-heating is taken into account, even though the thermal velocity (the upper limit on the carrier velocity) is expected to increase with the reduction in the thermal conductivity (i.e. increase in temperature). In addition, the simulation results suggest that the degradation in the on-current is architecture dependent.

In order to understand the physical mechanism causing the degradation we plot the carrier velocity and concentration at the virtual source versus thermal conductivity in Fig.10 for a square GAA nanowire. It can be seen that with the reduction in the thermal conductivity the carrier concentration increases slightly but, at the same time, we observe significant reduction in the carrier velocity. The overall effect results in the reduction of the on-current. The reduction in the carrier velocity highlights that the increase in temperature enhances phonon scattering to such an extent that there is reduction in the on-current.

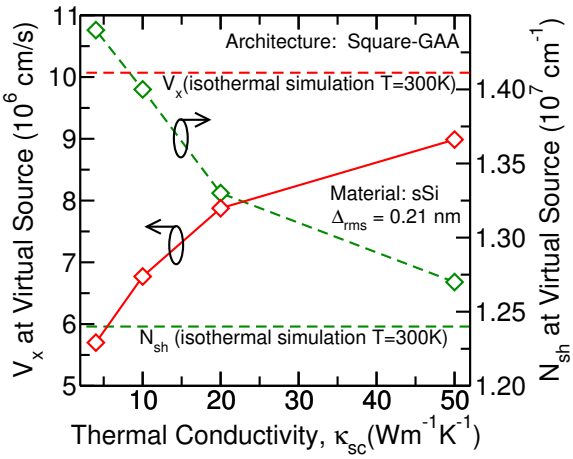

Fig. 10: Dependence of the carrier velocity and concentration at the virtual source versus the thermal conductivity is shown. The results shown that the reduction in the carrier velocity is the cause for the reduction of the current that is seen in the Fig.9. The isothermal limits of the carrier concentration and velocity are indicated by the dashed lines.

IV. Conclusion

We have developed a comprehensive simulation framework equipped with relevant scattering mechanisms, self-heating and series resistance. The simulator was streamlined with a novel iteration scheme to reduce the time needed for simulations. Our simulation results highlight that in performing delay analysis it is necessary to account for parasitic capacitances as they can alter the relative ranking of the architectures. Our analysis of the on-current degradation due to surface roughness suggests that the degradation in the on-current is both device architecture and material dependent. The simulation results highlight that the interface quality is vital in order to harness the supposed superiority of stacked nanowire over FinFETs in terms of on-current. We also point out that with the increase in the device temperature the degradation of the on-current is due to the increase in phonon scattering, which reduces the carrier velocity.

Acknowledgments

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